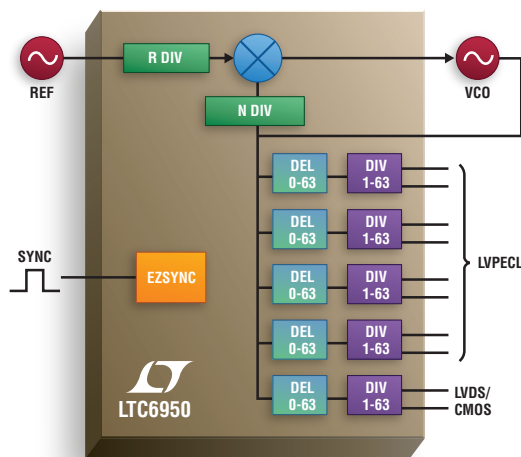


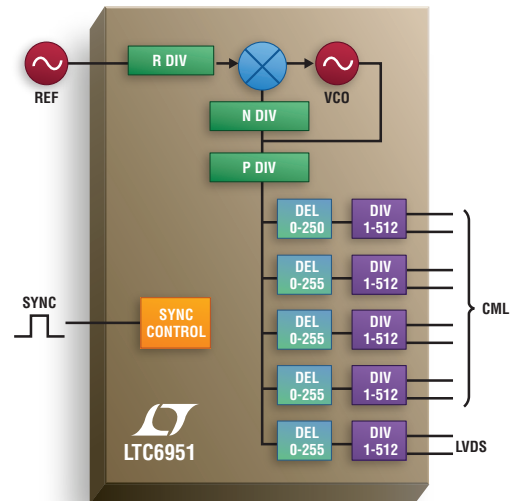
Ultralow Jitter Clock Generators and Distributors Maximize Data Converter SNR

Linear Technology clock generators and distributors are ideal for producing the ultralow jitter clocks essential to clocking data converters with high signal-to-noise ratio (SNR). Maintaining low jitter on the data converter clock is fundamental to achieving outstanding SNR levels when digitizing or synthesizing direct RF or high analog frequencies. Our clocking solutions achieve the best data converter SNR yet are simple to synchronize. The simulation and design are streamlined by free, user friendly software tools that enable effortless design and accurately predict behavior.

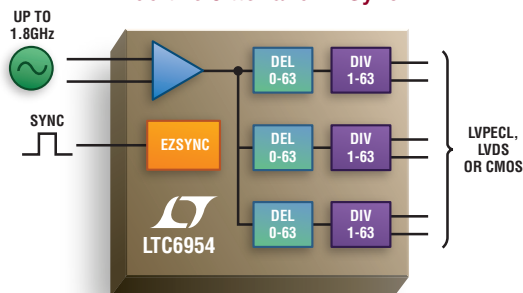
**1.4GHz Clocking Solution with 18fs_{RMS}
Additive Jitter and EZSync**



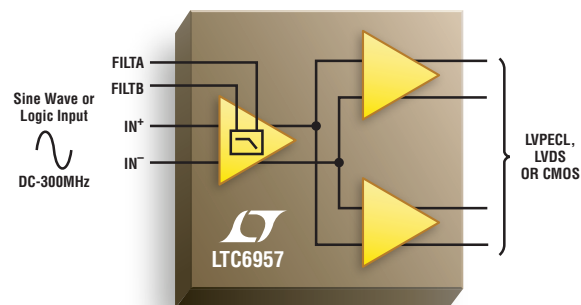
**2.7GHz Multi-Output Clock Synthesizer with
Integrated VCO and Sync Functions**



**Clock Distribution Solution with <20fs_{RMS}
Additive Jitter and EZSync**



**Low Phase Noise Reference Buffer
and Logic Converter**



Clock Generator and Distributor Selection Guide

Part Number	Integrated PLL	Integrated VCO	Max Output Frequency (MHz)	# of Outputs	Max Output Divide Ratio	EZSync™	ParallelSync™	JESD204B Subclass 1 Compatible	Design, Simulation and Demo Board Control Tool
LTC®6950	✓		1400	5	63	✓			ClockWizard™
LTC6951	✓	✓	2700	5	2048	✓	✓	✓	LTC6951Wizard™
LTC6954			1800	3	63	✓			LTC6954_GUI
LTC6957			300	2	1				



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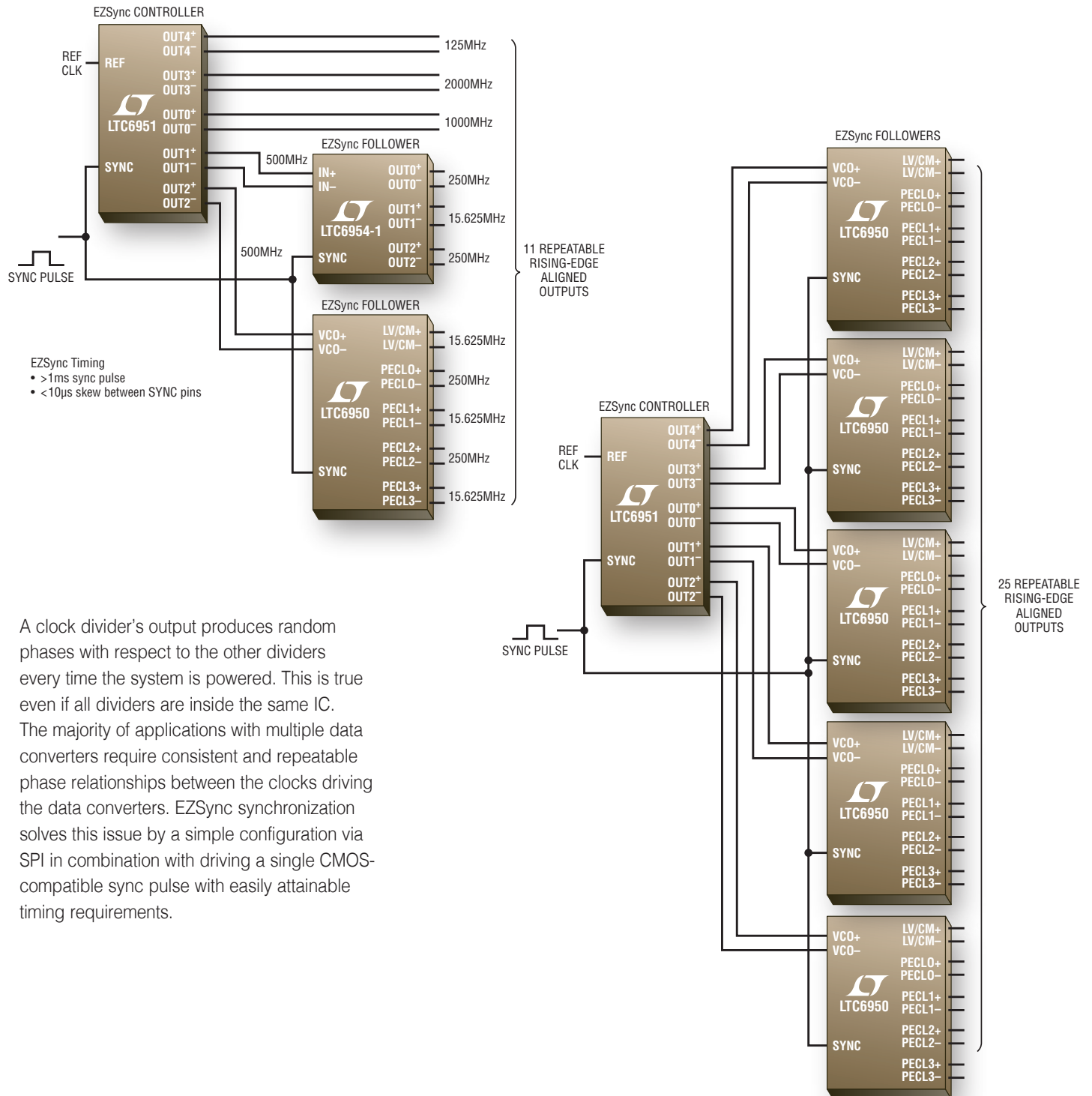
Synchronization and the Generation of Large Clock Trees

Many data converter applications require the generation of a large number of synchronized clocks. The LTC695x family of devices simplifies clock expansion and the creation of clock trees in systems with multiple daughter cards or with a large number of data converters.

EZSync

Linear Technology's proprietary EZSync output synchronization method guarantees repeatable and deterministic phase relationships between all clock divider outputs on all EZSync supporting devices.

EZSync synchronization is ideal for aligning the outputs of parallel and series (cascaded) connected devices. This scheme is useful when creating large clock distribution trees or when producing JESD204B compliant clocks.

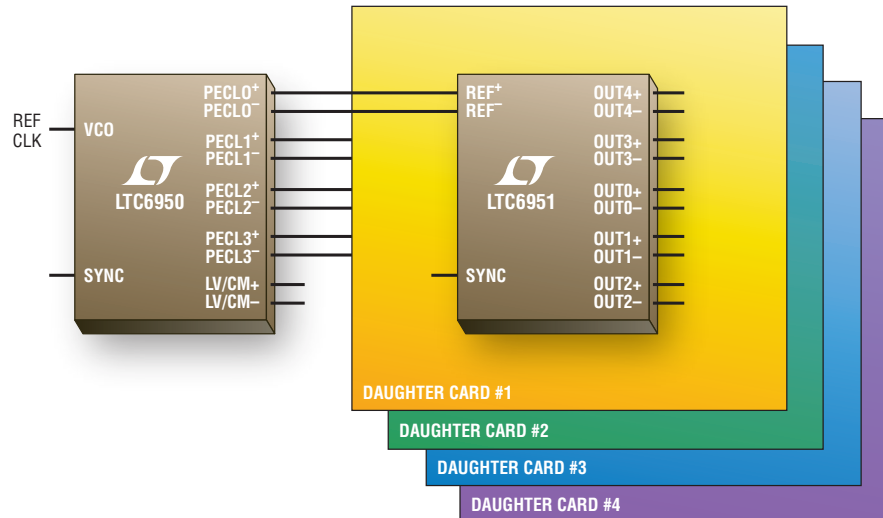


A clock divider's output produces random phases with respect to the other dividers every time the system is powered. This is true even if all dividers are inside the same IC. The majority of applications with multiple data converters require consistent and repeatable phase relationships between the clocks driving the data converters. EZSync synchronization solves this issue by a simple configuration via SPI in combination with driving a single CMOS-compatible sync pulse with easily attainable timing requirements.

ParallelSync

The ParallelSync multichip parallel synchronization feature allows the outputs of multiple LTC6951 ICs to be retimed to the common reference clock. This permits reference-aligned synchronization in the reference clock domain with easy-to-meet nanosecond range setup and hold time requirements.

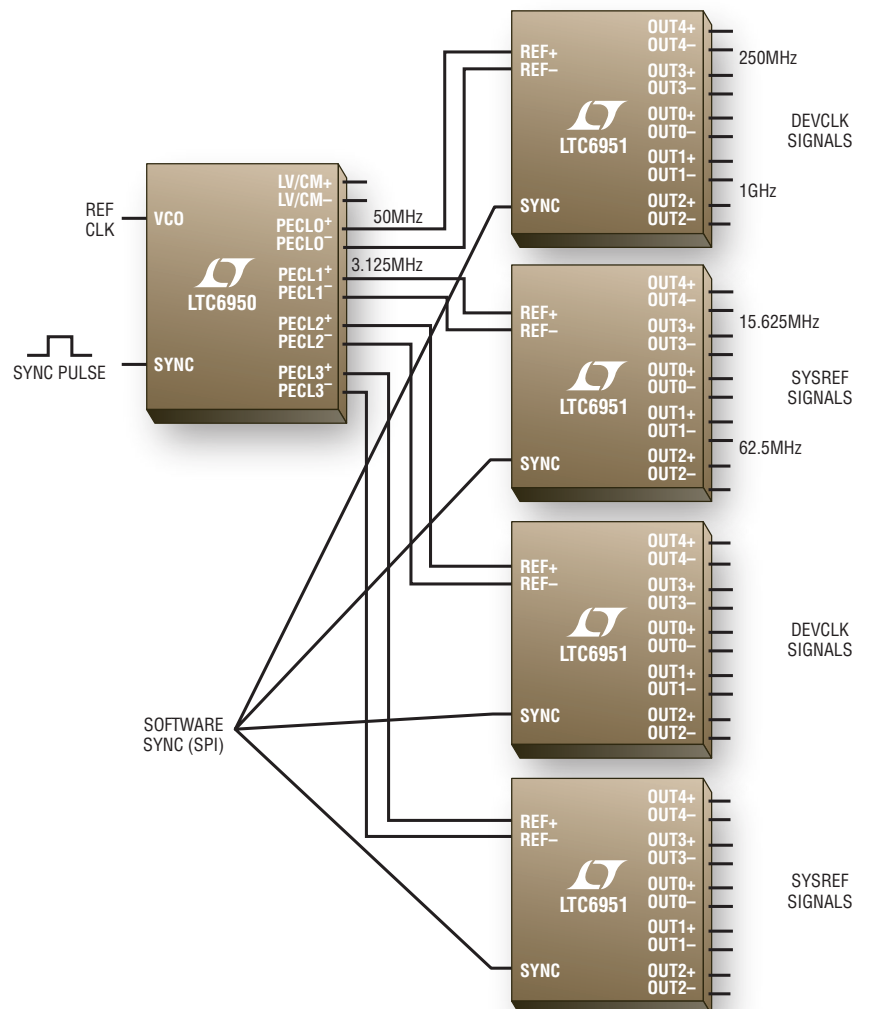
This reference distribution parallel synchronization example makes use of the LTC6950 to distribute the reference clock with minimal additive jitter, and delivers the world class jitter performance of the LTC6951 on each of the daughter cards. All LTC6951 outputs on all daughter cards are retimed to the reference clock, making them all reliably synchronized with each other.



JESD204B Subclass 1 Support

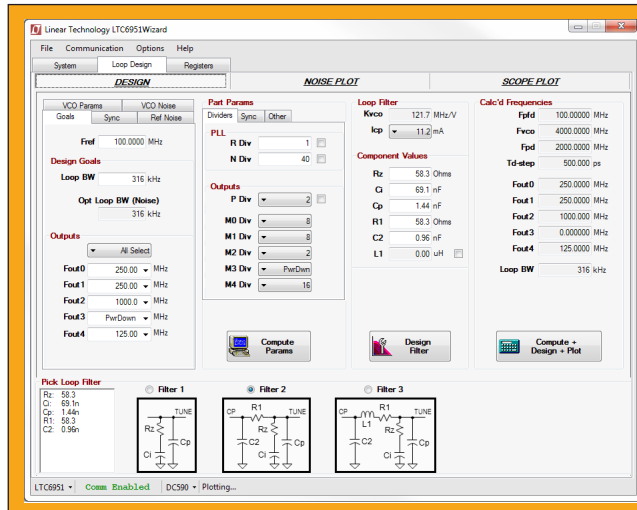
The EZ204Sync™ JESD204B subclass 1 compatible synchronization method builds on the previous two synchronization approaches. It enables the generation of the SYSREF and DEVCLK signals essential to this JEDEC standard across multiple parallel connected LTC6951 ICs along with any other EZSync compatible clock devices.

The LTC6950 distributes the reference clock while appropriately dividing it down to optimize the phase noise performance of the following PLLs. The LTC6951 ParallelSync output retiming to the reference is enabled through the SPI port on all LTC6951 devices to ensure the DEVCLK and SYSREF signals are all synchronized. The SYSREF generating devices can be optionally powered down after JESD204B initialization to save power.

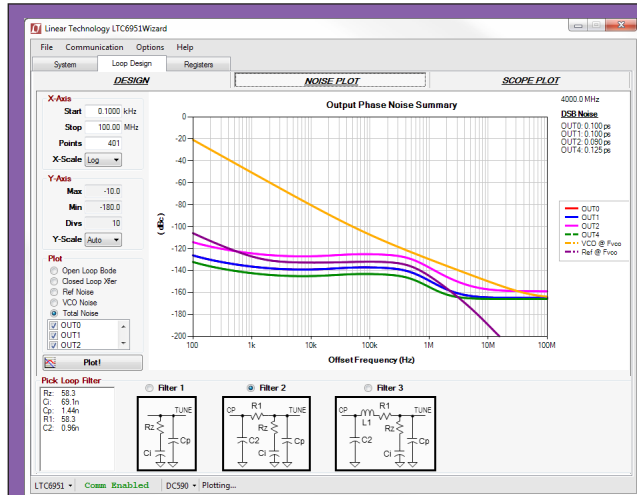


Control, Design, Simulate and Visualize with a Click of the Button

The free GUIs offered by Linear Technology have the ability to design the loop filter components for the integrated PLL, predict the resulting phase noise and jitter performance, and plot the clock outputs in the time domain to illustrate the phase relationships between the outputs. These tools save time and help the system designer make optimal decisions. These tools also offer the means to control the demo board systems and simplify the evaluation process of the clock generator and distributor ICs.

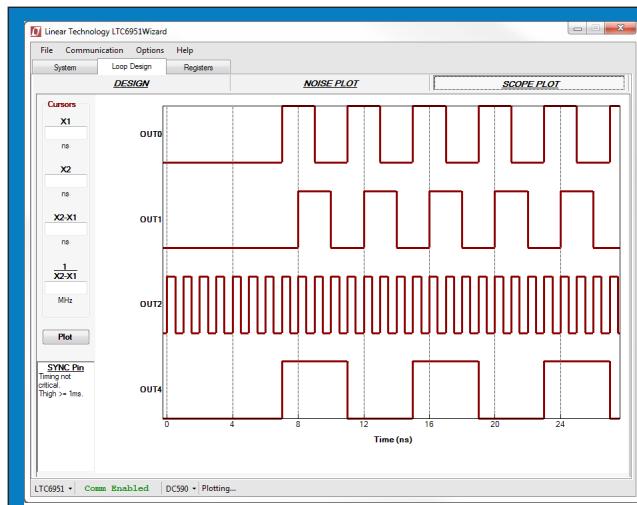


Set your frequency goals and find the loop filter component values of the PLL. This saves hours of design time and ensures the correct PLL parameters are chosen.



Accurately simulate the expected phase noise to better predict the system behavior. Import and export phase noise graphs to simplify the simulation process of the complete system.

Integrate the phase noise over a given bandwidth to arrive at the double sideband jitter value necessary to predict the data converter behavior.



Plot the output clocks in the time domain to visualize the phase relationships based on the synchronization and delay settings. This ability immensely helps the system designer better understand the available synchronization methods and saves time during the hardware debug phase.