1.95 GHz to 3.4 GHz, Tunable Band-Pass Filter

Data Sheet **HMC891ALP5E**

FEATURES

- **Amplitude settling time: 200 ns**
- **Re-entry rejection (wideband rejection): ≥30 dB**
- **Single-chip replacement for mechanically tuned designs**
- **RoHs compliant, 32-lead, 5 mm x 5 mm LFCSP package**

APPLICATIONS

- **Testing and measurement equipment**
- **Military radar and electronic warfare/electronic counter measure (ECM)**
- **Satellite communication and space**
- **Industrial and medical equipment**

FUNCTIONAL BLOCK DIAGRAM

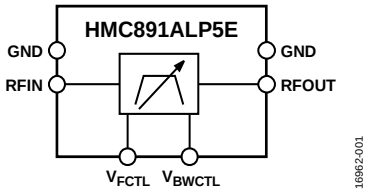


Figure 1.

GENERAL DESCRIPTION

The HMC891ALP5E is a monolithic microwave integrated circuit (MMIC) band-pass filter that features a user-selectable pass band frequency. The 3 dB filter bandwidth is approximately 9% and the 20 dB filter bandwidth is approximately 23%. The center frequency (f_{CENTER}) can be varied between 1.95 GHz and 3.4 GHz by applying an analog tune voltage between 0 V and 14 V.

This tunable filter can be used as a smaller alternative to physically large switched filter banks and cavity tuned filters.

The HMC891ALP5E has excellent microphonics due to the monolithic design, and provides a dynamically adjustable solution in advanced communications applications.

Rev. 0 **Document Feedback**

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REVISION HISTORY

9/2018—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, center frequency control voltage (V_{FCTL}) = bandwidth control voltage (V_{BWCTL}), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE					
Center Frequency (f_{CENTER})	1.95		3.4	GHz	
BANDWIDTH					
3 dB		9		%	
3 dB Bandwidth Control (V_{BWCTL})		±3		%	Percent change of bandwidth over f_{CENTER} as voltage changes
REJECTION					
Low-Side		0.89 × f_{CENTER}			≥20 dB
High-Side		1.13 × f_{CENTER}			≥20 dB
Re-entry		6.40 × f_{CENTER}			≤30 dB
LOSS					
Insertion Loss		8		dB	
Return Loss		10		dB	
DYNAMIC PERFORMANCE					
Max Input Power for Linear Operation			10	dBm	
Input Third-Order Intercept (Input IP3)		32		dBm	Input power (P_{IN}) = 20 dBm, two tone
Group Delay		3		ns	
Phase Sensitivity		3.6		Rad/V	
Amplitude Settling		200		ns	Time to settle to minimum insertion loss, within ≤0.5 dB of static insertion loss
Drift Rate		0.6		MHz/°C	
RESIDUAL PHASE NOISE					
1 MHz Offset		−165		dBc/Hz	
TUNING					
Voltages (V_{FCTL}, V_{BWCTL})	0		14	V	Each pin can be driven independently
Current					
Center Frequency Control Current (I_{FCTL})			±1	µA	Rated current for each pin
Bandwidth Control Current (I_{BWCTL})			±1	µA	Rated current for each pin

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Tuning	
Voltage (V_{FCTL}, V_{BWCTL})	−0.5 V to +15 V
Current (I_{FCTL}, I_{BWCTL})	±1 mA
RF Input Power	27 dBm
Temperature	
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature for 1 Million Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (Electronic Pad Temperature, T_{EPAD} = +85°C, P_{IN} = 10 dBm)	90°C
Electrostatic Discharge (ESD) Rating	
Human Body Model (HBM)	1500 V
Field Induced Charge Device Model (FICDM)	1250 V
Moisture Sensitivity Level (MSL) Rating	MSL3

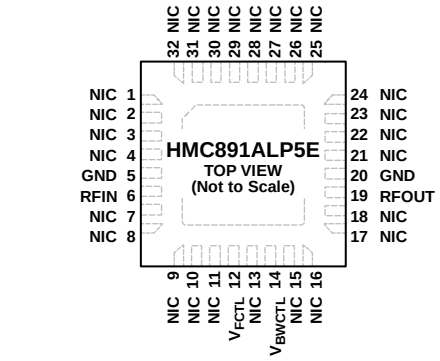
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. ALL DATA SHOWN HEREIN WAS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE PACKAGE BOTTOM HAS AN EXPOSED PAD THAT MUST BE CONNECTED TO RF/DC GROUND.

16962-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4, 7 to 11, 13, 15 to 18, 21 to 32	NIC	Not Internally Connected. These pins are not connected internally. All data shown herein was measured with these pins externally connected to RF/dc ground.
5, 20	GND	Ground. Connect these pins to RF/dc ground.
6	RFIN	Radio Frequency Input. This pin is dc-coupled and matched to 50 Ω. Do not apply an external voltage to this pin.
12	V_{FCTL}	Center Frequency Control Voltage. This pin controls the f_{CENTER} of the device.
14	V_{BWCTL}	Bandwidth Control Voltage. This pin controls the bandwidth of the device.
19	RFOUT	Radio Frequency Output. This pin is dc-coupled and matched at 50 Ω. Do not apply an external voltage to this pin.
	EPAD	Exposed Pad. The package bottom has an exposed metal pad that must be connected to RF/dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

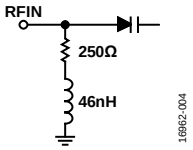


Figure 4. RFIN Interface Schematic

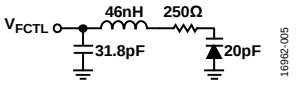


Figure 5. V_{FCTL} Interface Schematic

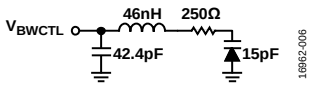


Figure 6. V_{BWCTL} Interface Schematic

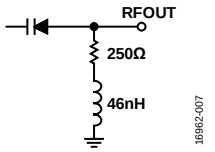


Figure 7. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

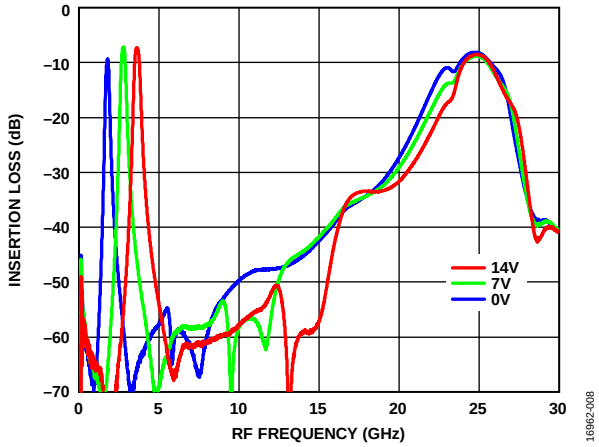


Figure 8. Insertion Loss vs. Broadband RF Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

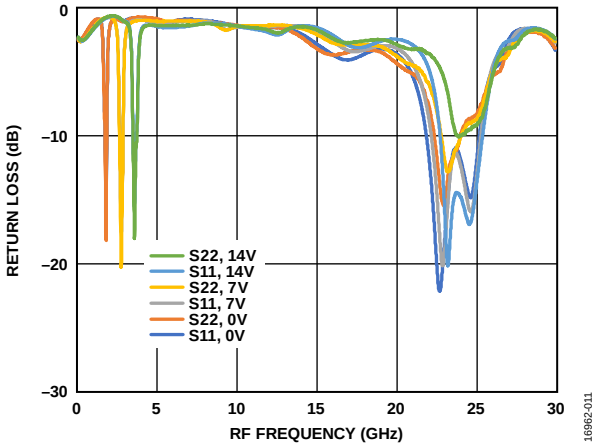


Figure 11. Return Loss vs. Broadband RF Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

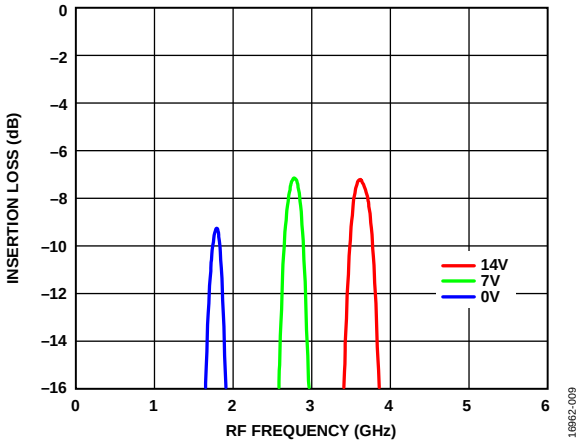


Figure 9. Insertion Loss vs. RF Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

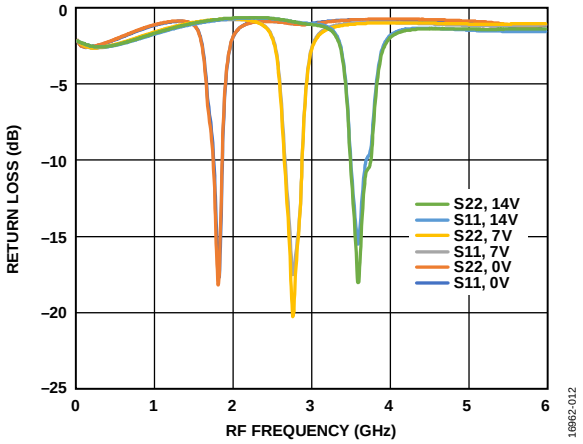


Figure 12. Return Loss vs. RF Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

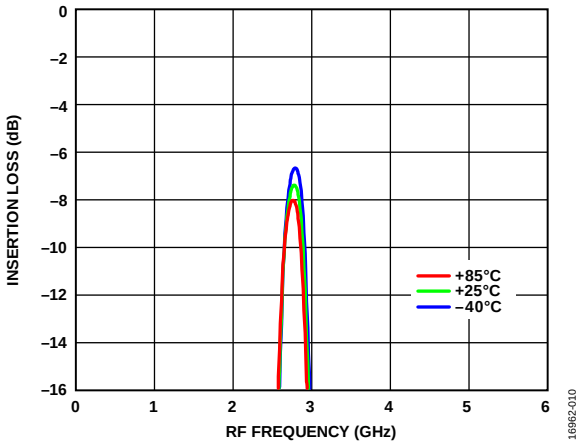


Figure 10. Insertion Loss vs. RF Frequency at Various Temperatures, $V_{FCTL} = V_{BWCTL} = 7$ V

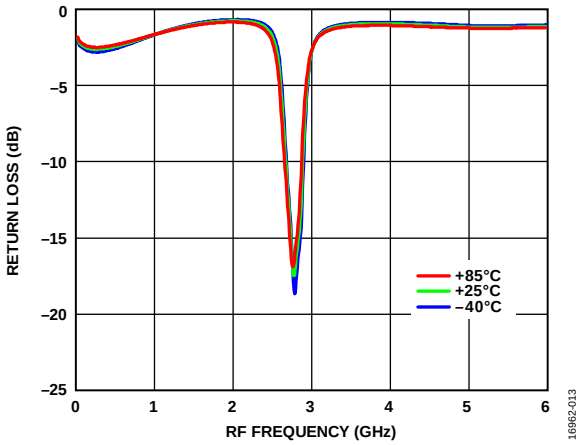


Figure 13. Return Loss vs. RF Frequency at Various Temperatures, $V_{FCTL} = V_{BWCTL} = 7$ V

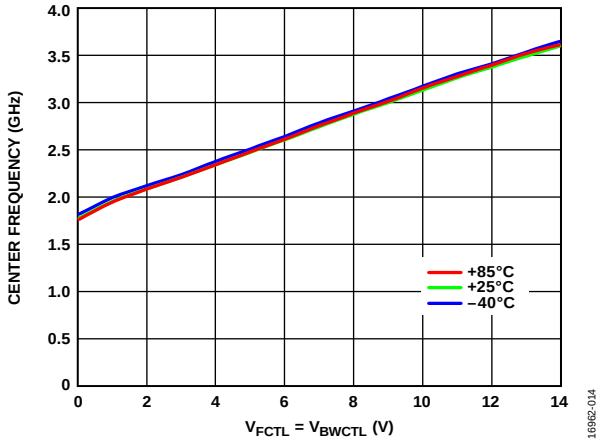


Figure 14. Center Frequency (f_{CENTER}) vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

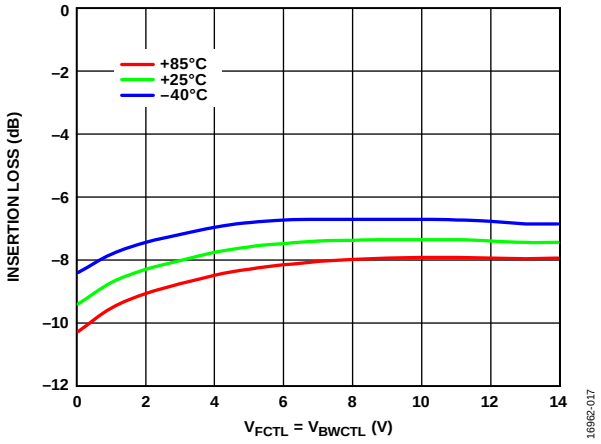


Figure 17. Insertion Loss vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

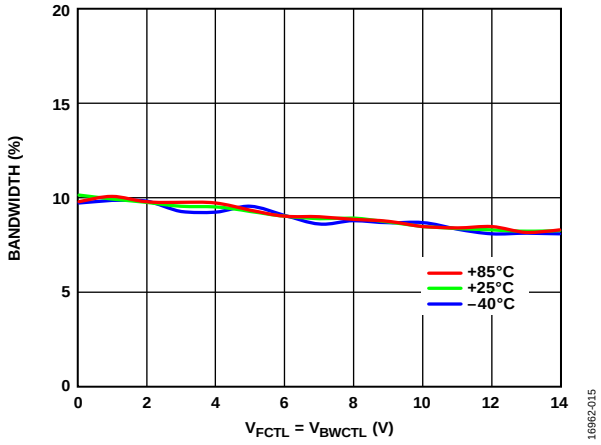


Figure 15. 3 dB Bandwidth vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

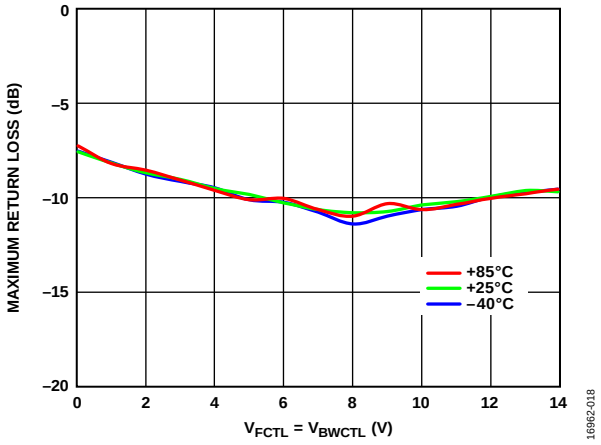


Figure 18. Maximum Return Loss in a 2 dB Bandwidth vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

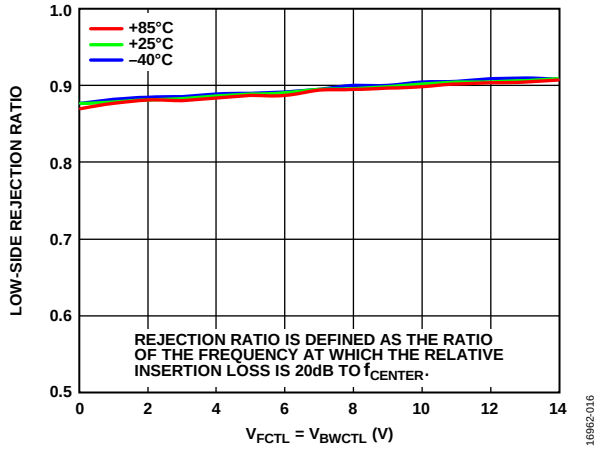


Figure 16. Low-Side Rejection Ratio vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

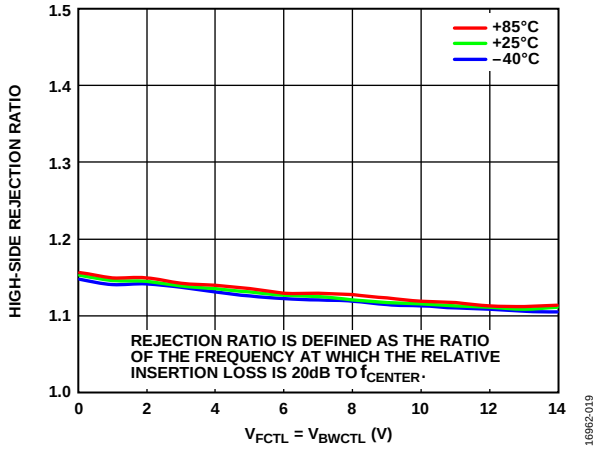


Figure 19. High-Side Rejection Ratio vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

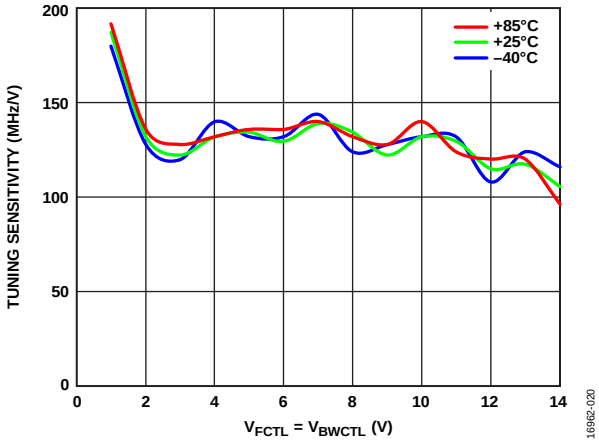


Figure 20. Tuning Sensitivity vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures

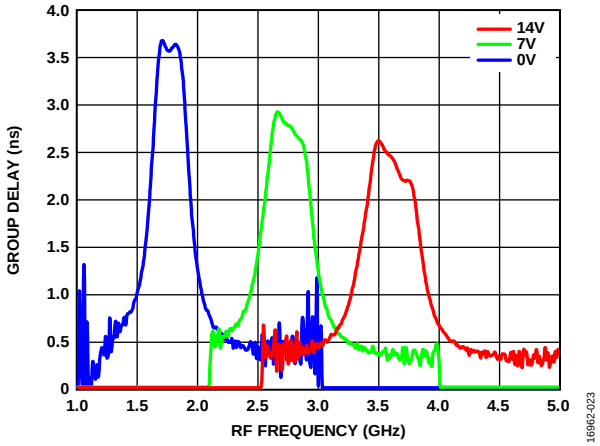


Figure 23. Group Delay vs. RF Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

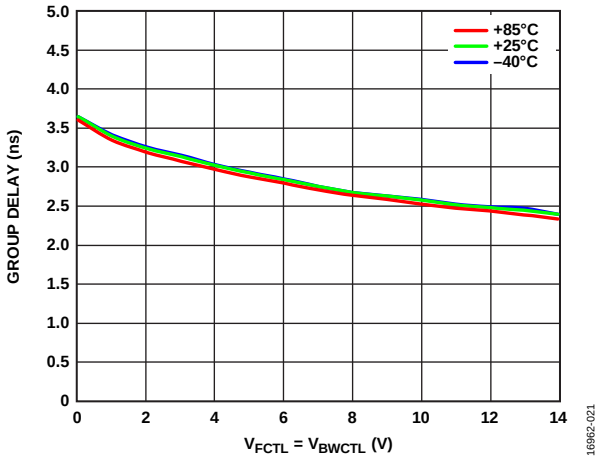


Figure 21. Group Delay vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperature

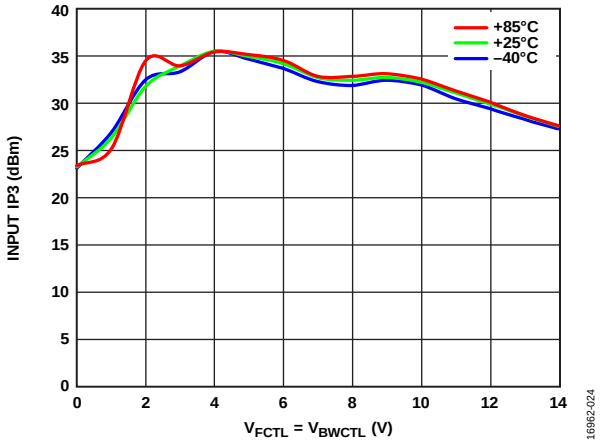


Figure 24. Input IP3 vs. $V_{FCTL} = V_{BWCTL}$ at Various Temperatures, Input Power (P_{IN}) = 20 dBm

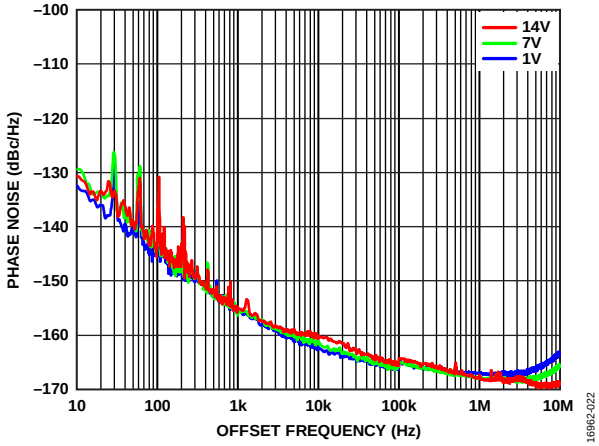


Figure 22. Residual Phase Noise vs. Offset Frequency at Various $V_{FCTL} = V_{BWCTL}$ Voltages

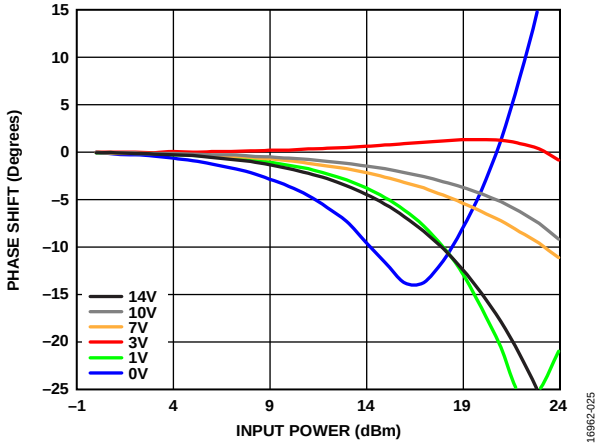


Figure 25. Phase Shift vs. Input Power (P_{IN}), at Various $V_{FCTL} = V_{BWCTL}$ Voltages

THEORY OF OPERATION

The HMC891ALP5E is a MMIC band-pass filter that features a user-selectable pass band frequency. Varying the applied analog tuning voltage between 0 V and 14 V at V_{FCTL} varies the f_{CENTER} frequency between 1.95 GHz and 3.4 GHz. The bandwidth of the filter is adjustable by using the V_{BWCTL} control voltage, which can vary from 0 V to 14 V. Typical operation is to tie the V_{FCTL} and V_{BWCTL} control voltages together.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 26 shows the typical application circuit for the HMC891ALP5E. The RFIN and RFOUT pins are dc-coupled and require external, 100 pF series capacitors (C1 and C2).

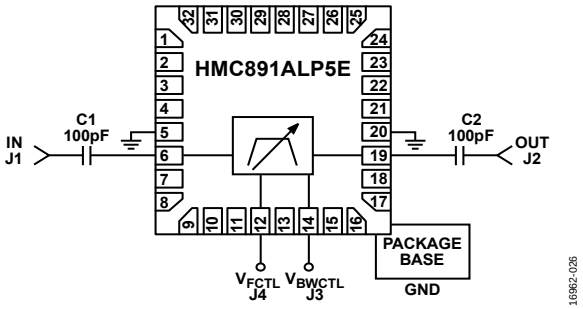


Figure 26. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD (PCB)

All RF traces are routed on Layer 1 (primary side) and the remaining three layers are ground planes that provide a solid ground for RF transmission lines, as shown in Figure 27. The top dielectric material is Rogers 4350, which offers low loss performance. The prepreg material in Layer 2 attaches the Isola 370HR core layer with copper traces layers above and below the core layer. The prepreg material and the Isola 370HR core layer are used to achieve the required board finish thickness.

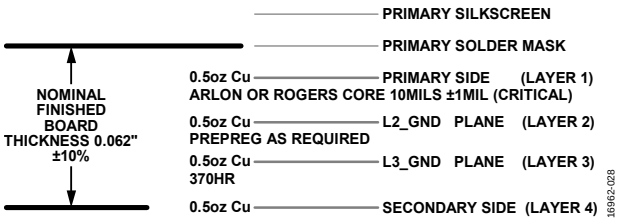


Figure 27. Cross Sectional View of the EV1HMC891ALP5 PCB Layers

The circuit board in this application uses RF circuit design techniques. Signal lines must have an impedance of 50 Ω, and the package ground leads and exposed pad must be connected directly to the ground plane (see Figure 27). Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 28 is available from Analog Devices, Inc. upon request.

Table 4. Bill of Materials for the EV1HMC891ALP5

Item	Description
J1, J2	PCB mount, Subminiature Version A (SMA) connector, SRI
J3, J4	PCB mount SMA connector, Johnson
C1, C2	Capacitor, 100 pF, 0402
U1	HMC891ALP5E
PCB	08-049598[2] evaluation PCB

[1] Circuit board material is Arlon 25FR or Rogers 25FR.
[2] 08-049598 is the raw, bare PCB identifier. Reference the EV1HMC891ALP5 when ordering the complete evaluation PCB.

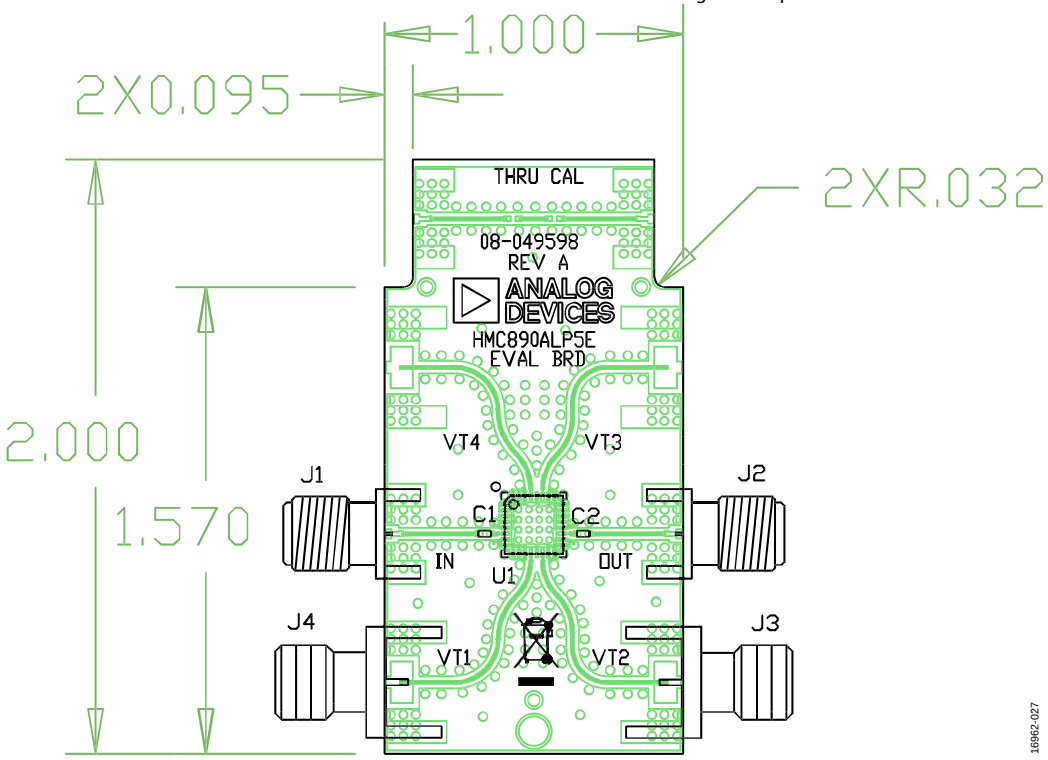
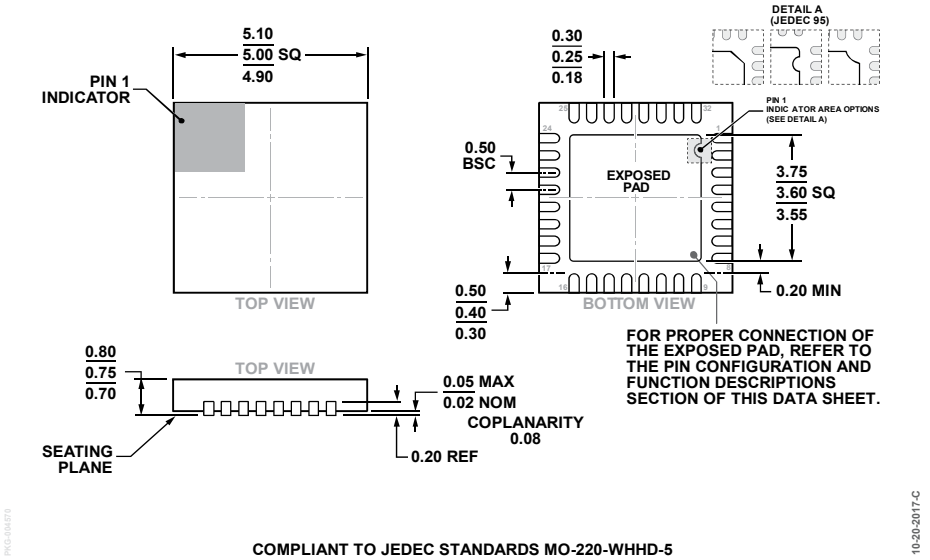


Figure 28. Evaluation PCB, Top Layer Outline Dimensions

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5

Figure 29. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC891ALP5E	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
HMC891ALP5ETR	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
EV1HMC891ALP5		Evaluation PCB	

[1] All models are RoHS-Compliant Parts.

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