DRV201A Voice Coil Motor Driver for Camera Auto Focus

1 Features

- Configurable for Linear or PWM Mode VCM Current Generation
- High Efficiency PWM Current Control for VCM
- Advanced Ringing Compensation
- Integrated 10-bit D/A Converter for VCM Current Control
- Protection
  - Open and Short-Circuit Detection
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown
  - Internal Current Limit for VCM Driver
  - 4-kV ESD-HBM
- I^2C Interface
- Improved PWM-to-Linear Mode Setting Time vs. DRV201
- Improved EMC Performance vs. DRV201
- Improved PWM-to-Linear Mode Settling Time vs. DRV201
- Improved EMC Performance vs. DRV201
- Operating Temperature Range: -40ºC to 85ºC
- 6-Ball WCSP Package With 0.4-mm Pitch
- Max Die Size: 0.806 mm × 1.49 mm
- Max Package Height: 0.3 mm

2 Applications

- Cell Phone Auto Focus
- Digital Still Camera Auto Focus
- Iris and Exposure Controls
- Security Cameras
- Web and PC Cameras
- Actuator Controls

3 Description

The DRV201A is an advanced voice coil motor driver for camera auto focus. It has an integrated D/A converter for setting the VCM current. VCM current is controlled with a fixed frequency PWM controller or a linear mode driver. Current generation can be selected via I^2C register. The DRV201A has an integrated sense resistor for current regulation and the current can be controlled through I^2C.

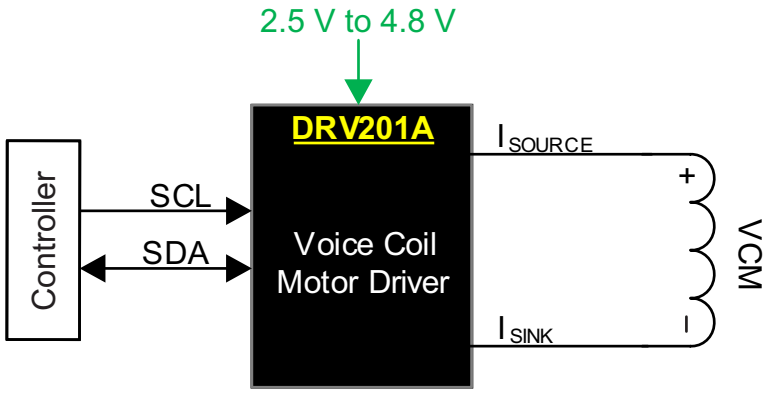
When changing the current in the VCM, the lens ringing is compensated with an advanced ringing compensation function. Ringing compensation reduces the needed time for auto focus significantly. The device also has VCM short and open protection functions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV201A	PicoStar (6)	0.80 mm × 1.48 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2013) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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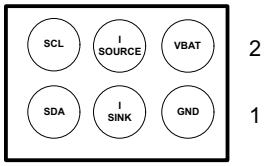
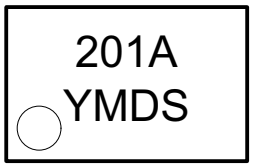
5 Pin Configuration and Functions

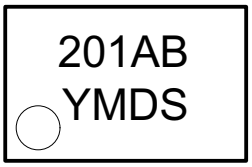
YMB Package
6-Pin PicoStar
Bottom View



YMB Package
6-Pin PicoStar
Top View



YMB Package
6-Pin PicoStar
Top View



The coated package option has a backside polymer coating that is 40µm thick. The final package heights of both the packages are the same for both options. This coating helps minimize edge chipping or die cracking during assembly and manufacturing.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VBAT	2A	—	Power
GND	1A	—	Ground
I_SOURCE	2B	—	Voice coil positive terminal
I_SINK	1B	—	Voice coil negative terminal
SCL	2C	I	I^2C serial interface clock input
SDA	1C	I/O	I^2C serial interface data input/output (open drain)

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	VBAT, ISOURCE, ISOURCE pin voltage(2)	–0.3	5.5	V
	Voltage at SDA, SCL	–0.3	3.6	V
	Continuous total power dissipation	Internally limited		
$R_{\theta JA}$	Junction-to-ambient thermal resistance(3)		130	°C/W
T_J	Operating junction temperature	–40	125	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) This thermal data is measured with high-K board (4-layer board).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VBAT - Supply voltage	2.5	3.7	4.8	V
Voltage Range - SDA and SCL	–0.1	3.3	3.6	V
T_J - Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRV201A YMB (PICOSTAR) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{BAT}	Input supply voltage		2.5	3.7	4.8	V
V_{UVLO}	Undervoltage lockout threshold	V_{BAT} rising			2.2	V
		V_{BAT} falling	2			
V_{HYS}	Undervoltage lockout hysteresis		50	100	250	mV
INPUT CURRENT						
$I_{SHUTDOWN}$	Input supply current shutdown, includes switch leakage currents	MAX: V_{BAT} = 4.4 V		0.15	1	µA
$I_{STANDBY}$	Input supply current standby, includes switch leakage currents	MAX: V_{BAT} = 4.4 V		120	200	µA
STARTUP, MODE TRANSITIONS, AND SHUTDOWN						
t_1	Shutdown to standby				100	µs
t_2	Standby to active				100	µs
t_3	Active to standby				100	µs
t_4	Shutdown time	Active or standby to shutdown	0.5		1	ms
VCM DRIVER STAGE						
I_{RES}	Resolution			10		bits
	Relative accuracy		-10		10	LSB
	Differential nonlinearity		-1		1	
	Zero code error			0		mA
	Offset error	At code 32			3	mA
	Gain error			±3		% of FSR
	Gain error drift			0.3	0.4	%/°C
	Offset error drift			0.3	0.5	%/°C
I_{MAX}	Maximum output current			102.3		mA
I_{LIMIT}	Average VCM current limit	See (1)	110	160	240	mA
$I_{DETCODE}$	Minimum VCM code for OPEN and SHORT detection	See (2)	256			mA
f_{SW}	Switching frequency	Selectable through CONTROL register	0.5		4	MHz
V_{DRP}	Internal dropout	See (3)			0.4	V
L_{VCM}	VCM inductance		30		150	µH
R_{VCM}	VCM resistance		11		22	Ω
LENS MOVEMENT CONTROL						
t_{set1}	Lens settling time	±10% error band		$2/f_{VCM}$		ms
t_{set2}	Lens settling time	±10% error band		$1/f_{VCM}$		ms
f_{VCM}	VCM resonance frequency		50		150	Hz
	VCM resonance frequency tolerance	When $1/f_{VCM}$ compensation is used	-10%		10%	
		When $2/f_{VCM}$ compensation is used	-30%		30%	

(1) During short circuit condition driver current limit comparator will trip and short is detected and driver goes into STANDBY and short flag is set high in the status register.
(2) When testing VCM open or short this is the recommended minimum VCM code (in dec) to be used.
(3) This is the voltage that is needed for the feedback resistor and high side driver. It should be noted that the maximum VCM resistance is limited by this voltage and supply voltage. E.g. 3-V supply maximum VCM resistance is: $R_{VCM} = (V_{BAT} – V_{DRP})/I_{VCM}$ = (3 V - 0.4 V)/102.3 mA = 25.4 Ω.

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Electrical Characteristics (continued)

Over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC I/Os (SDA AND SCL)						
I_{IN}	Input leakage current	V = 1.8 V, SCL	-4.25		4.25	µA
		V = 1.8 V, SDA	-1		1	
R_{PullUp}	I^2C pull-up resistors	SDA and SCL pins		4.7		kΩ
V_{IH}	Input high level	See (4)	1.17		3.6	V
V_{IL}	Input low level	See (5)	0		0.63	V
$t_{TIMEOUT}$	SCL timeout for shutdown detection		0.5		1	ms
R_{PD}	Pull down resistor at SCL line			500		kΩ
f_{SCL}	I^2C clock frequency				400	kHz
INTERNAL OSCILLATOR						
f_{OSC}	Internal oscillator	20°C ≤ T_A ≤ 70°C	-3%		3%	
	Frequency accuracy	-40°C ≤ T_A ≤ 85°C	-5%		5%	
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shutdown trip point			140		°C

(4) During shutdown to standby transition V_{IH} low limit is 1.28 V.
(5) During shutdown to standby transition V_{IL} high limit is 0.51 V.

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6.6 Data Transmission Timing Requirements

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Serial clock frequency		100		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{SP}	Tolerable spike width on bus	SCL = 100 KHz			50	ns
		SCL = 400 KHz				
t_{LOW}	SCL low time	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{HIGH}	SCL high time	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{S(DAT)}$	SDA → SCL setup time	SCL = 100 KHz	250			ns
		SCL = 400 KHz	100			
$t_{S(STA)}$	Start condition setup time	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	600			ns
$t_{S(STO)}$	Stop condition setup time	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{H(DAT)}$	SDA → SCL hold time	SCL = 100 KHz	0		3.45	µs
		SCL = 400 KHz	0		0.9	
$t_{H(STA)}$	Start condition hold time	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{r(SCL)}$	Rise time of SCL Signal	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
$t_{f(SCL)}$	Fall time of SCL Signal	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	
$t_{r(SDA)}$	Rise time of SDA Signal	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
$t_{f(SDA)}$	Rise time of SDA Signal	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	

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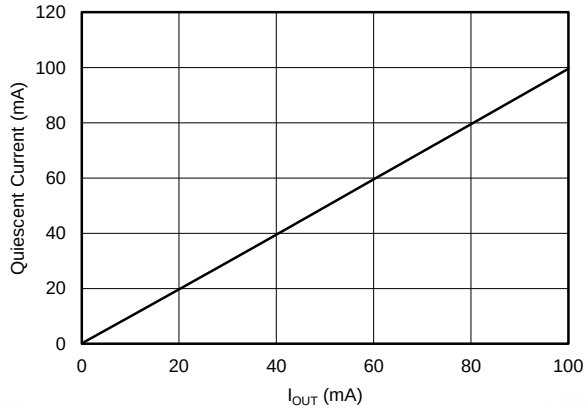
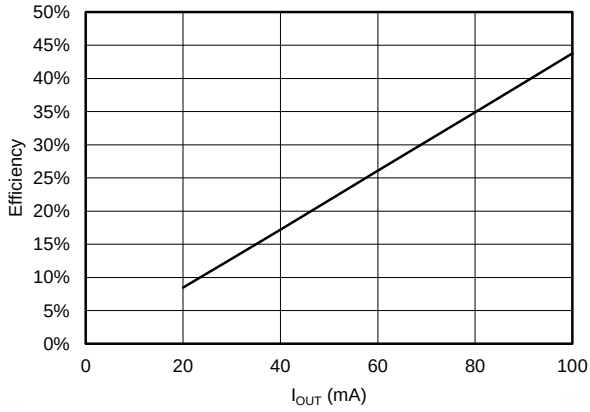
6.7 Typical Characteristics



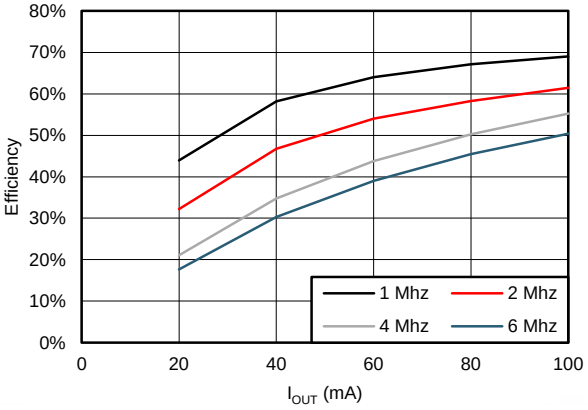
VBAT = 3.7 V

Figure 1. Linear Mode: Supply Current vs Output Current



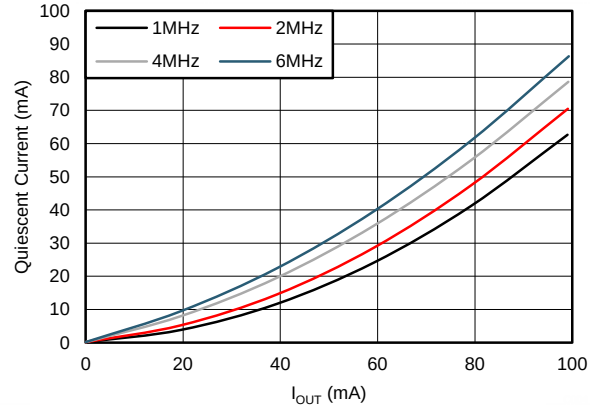
VBAT = 3.7 V

Figure 2. Linear Mode: Efficiency vs Output Current



VBAT = 3.7 V

Figure 3. PWM Mode: Efficiency vs Output Current



VBAT = 3.7 V

Figure 4. PWM Mode: Supply Current vs Output Current

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7 Detailed Description

7.1 Overview

The DRV201A is intended for high performance autofocus in camera modules. It is used to control the current in the voice coil motor (VCM). The current in the VCM generates a magnetic field which forces the lens stack connected to a spring to move. The VCM current and thus the lens position can be controlled via the I^2C interface and an auto focus function can be implemented.

The DRV201A offers a higher level of performance than the DRV201 in two areas. First, the transition between PWM and linear modes is free of any resonance. This allows faster image capture after achieving focus in the PWM mode. The other performance enhancement is in the area of EMC performance. When operating in PWM mode, transitions were significantly slowed down resulting in lower conducted and radiated noise versus the DRV201.

The device connects to a video processor or image sensor through a standard I^2C interface which supports up to 400-kbit/s data rate. The digital interface supports IO levels from 1.8 V to 3.3 V. All pins have 4-kV HBM ESD rating.

When SCL is low for at least 0.5 ms, the device enters SHUTDOWN mode. If SCL goes from low to high the driver enters STANDBY mode in less than 100 µs and default register values are set as shown in Figure 5. ACTIVE mode is entered whenever the VCM_CURRENT register is set to something else than zero.

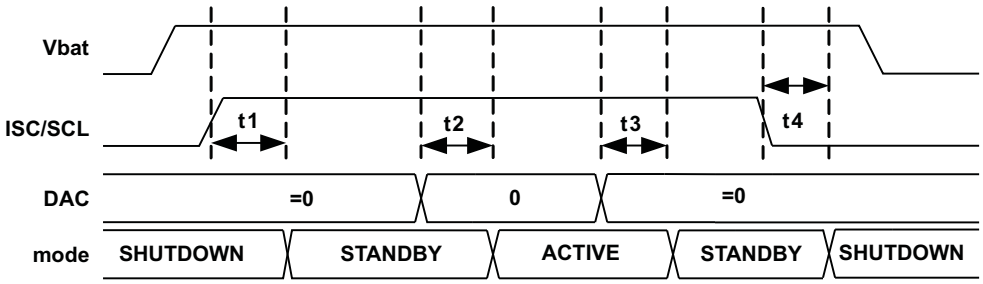

Figure 5. Power Up and Down Sequence

VCM current can be controlled via an I^2C interface and VCM_CURRENT registers. Lens stack is connected to a spring which causes a dampened ringing in the lens position when current is changed. This mechanical ringing is compensated internally by generating an optimized ramp whenever the current value in the VCM_CURRENT register is changed. This enables a fast autofocus algorithm and pleasant user experience.

Current in the VCM can be generated with a linear or PWM control. In linear mode the high side PMOS is configured as a current source and current is set by the VCM_CURRENT control register. In PWM control the VCM is driven with a half bridge driver. With PWM control the VCM current is increased by connecting the VCM between V_{BAT} and GND through the high side PMOS and then released to a 'freewheeling' mode through the sense resistor and low side NMOS. PWM mode switching frequency can be selected from 0.5 MHz up to 4 MHz through a CONTROL register. PWM or linear mode can be selected with the PWM/LIN bit in the MODE register.

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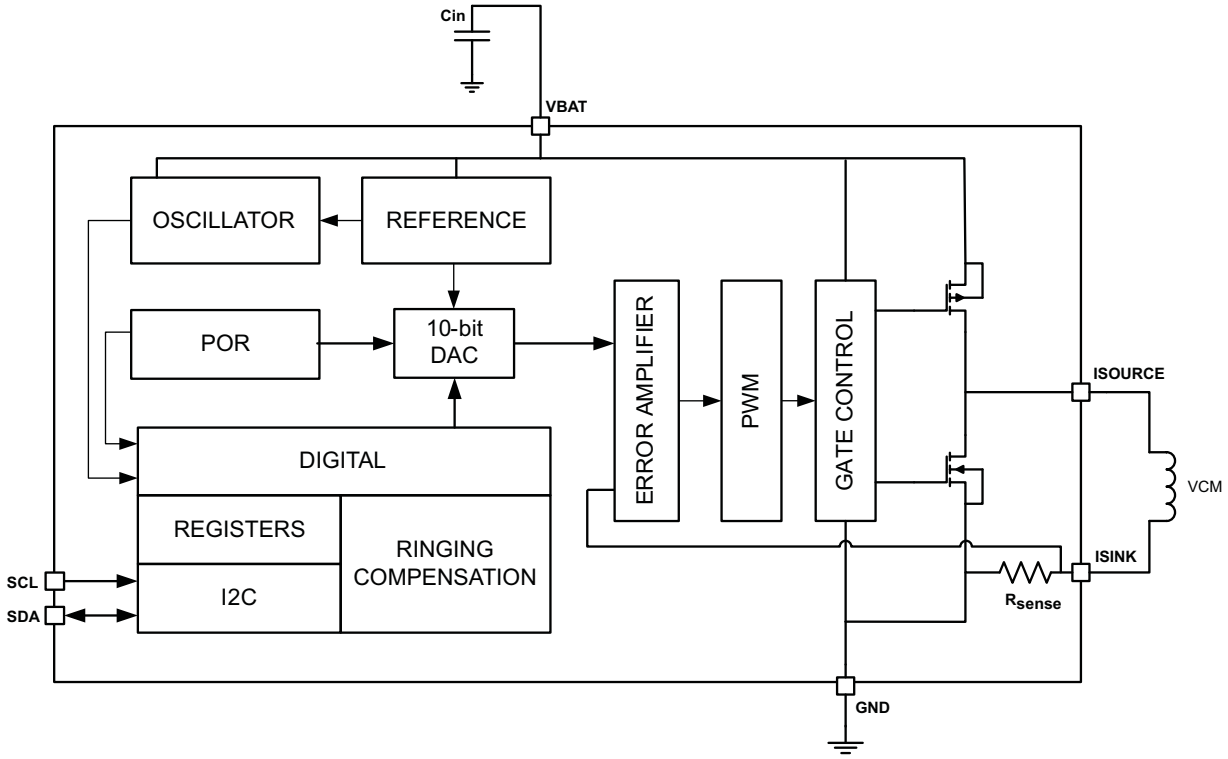
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCM Driver Output Stage Operation

Current in the VCM can be controlled with a linear or PWM mode output stage. Output stage is enabled in ACTIVE mode which can be controlled through VCM_CURRENT control register and the output stage mode is selected from MODE register bit PWM/LIN.

In linear mode the output PMOS is configured to a high side current source and current can be controlled from a VCM_CURRENT registers.

In PWM control the VCM is driven with a half bridge driver. With PWM control the VCM current is increased by connecting the VCM between V_{BAT} and GND through the high side PMOS and then released to a 'freewheeling' mode through the sense resistor and low side NMOS. Current in the VCM is sensed with a 1-Ω sense resistor which is connected into an error amplifier input where the other input is controlled by the 10-bit DAC output. PWM mode switching frequency can be selected from 0.5 MHz up to 4 MHz through a CONTROL register. PWM or linear mode can be selected with the PWM/LIN bit in the MODE register.

7.3.2 Ringing Compensation

VCM current can be controlled via an I^2C interface and VCM_CURRENT registers. Lens stack is connected to a spring which causes a dampened ringing in the lens position when current is changed. This mechanical ringing is compensated internally by generating an optimized ramp whenever the current value in the VCM_CURRENT register is changed. This enables a fast auto focus algorithm and pleasant user experience.

Ringing compensation is dependent on the VCM resonance frequency and this can be controlled via VCM_FREQ register (07h) from 50 Hz up 150 Hz. Table 1 shows the VCM_FREQ register setting for each resonance frequency in 1-Hz steps. If more accurate resonance frequency is available, the control value can be calculated with Equation 1.

Ringing compensation is designed in a way that it can tolerate ±30% frequency variation in the VCM resonance frequency when $2/f_{VCM}$ compensation is used and ±10% variation with $1/f_{VCM}$ so only statistical data from the VCM is needed in production.

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Feature Description (continued)

Table 1. VCM Resonance Frequency Control Register (07h) Table

VCM Resonance Frequency [Hz]	VCM_FREQ[7:0] (07h)		VCM Resonance Frequency [Hz]	VCM_FREQ[7:0] (07h)		VCM Resonance Frequency [Hz]	VCM_FREQ[7:0] (07h)	
	DEC	BIN		DEC	BIN		DEC	BIN
50	0	0	84	154	10011010	118	220	11011100
51	7	111	85	157	10011101	119	222	11011110
52	14	1110	86	160	10100000	120	223	11011111
53	21	10101	87	162	10100010	121	224	11100000
54	27	11011	88	165	10100101	122	226	11100010
55	34	100010	89	167	10100111	123	227	11100011
56	40	101000	90	170	10101010	124	228	11100100
57	46	101110	91	172	10101100	125	229	11100101
58	52	110100	92	174	10101110	126	231	11100111
59	58	111010	93	177	10110001	127	232	11101000
60	63	111111	94	179	10110011	128	233	11101001
61	68	1000100	95	181	10110101	129	234	11101010
62	73	1001001	96	183	10110111	130	235	11101011
63	78	1001110	97	185	10111001	131	236	11101100
64	83	1010011	98	187	10111011	132	238	11101110
65	88	1011000	99	189	10111101	133	239	11101111
66	92	1011100	100	191	10111111	134	240	11110000
67	96	1100000	101	193	11000001	135	241	11110001
68	101	1100101	102	195	11000011	136	242	11110010
69	105	1101001	103	197	11000101	137	243	11110011
70	109	1101101	104	198	11000110	138	244	11110100
71	113	1110001	105	200	11001000	139	245	11110101
72	116	1110100	106	202	11001010	140	246	11110110
73	120	1111000	107	204	11001100	141	247	11110111
74	124	1111100	108	205	11001101	142	248	11111000
75	127	1111111	109	207	11001111	143	249	11111001
76	130	10000010	110	208	11010000	144	250	11111010
77	134	10000110	111	210	11010010	145	251	11111011
78	137	10001001	112	212	11010100	146	251	11111011
79	140	10001100	113	213	11010101	147	252	11111100
80	143	10001111	114	215	11010111	148	253	11111101
81	146	10010010	115	216	11011000	149	254	11111110
82	149	10010101	116	217	11011001	150	255	11111111
83	152	10011000	117	219	11011011	-	-	-

7.4 Device Functional Modes

7.4.1 Modes of Operation

SHUTDOWN If the driver detects SCL has a DC level below 0.63 V for duration of at least 0.5 ms, the driver will enter shutdown mode. This is the lowest power mode of operation. The driver will remain in shutdown for as long as SCL pin remain low.

STANDBY If SCL goes from low to high the driver enters STANDBY mode and sets the default register values. In this mode registers can be written to through the I^2C interface. Device will be in STANDBY mode when VCM_CURRENT register is set to zero. From ACTIVE mode the device will enter STANDBY if the SW_RST bit of the CONTROL register is set. In this case all registers will be reset to default values.

STANDBY mode is entered from ACTIVE mode if any of the following faults occur: Over temperature protection fault (OTPF), VCM short (VCMS), or VCM open (VCMO). When

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Device Functional Modes (continued)

STANDBY mode is entered due to a fault condition current register is cleared.

ACTIVE The device is in ACTIVE mode whenever the VCM_CURRENT control is set to something else than zero through the I^2C interface. In ACTIVE mode VCM driver output stage is enabled all the time resulting in higher power consumption. The device remains in active mode until the SW_RST bit in the CONTROL register is set, SCL is pulled low for duration of 0.5 ms, VCM_CURRENT control is set to zero, or any of the following faults occur: Over temperature protection fault (OTPF), VCM short (VCMS), or VCM open (VCMO). If active mode is entered after fault the status register is automatically cleared.

7.5 Programming

7.5.1 I^2C Bus Operation

The I^2C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The DRV201A hosts a slave I^2C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I^2C standard 3.0.

DRV201A supports four different read and two different write operations; single read from a defined location, single read from a current location, sequential read starting from a defined location, sequential read from current location, single write to a defined location, sequential write starting from a defined location. All different read and write operations are described below.

7.5.1.1 Single Write to a Defined Location

Figure 6 shows the format of a single write to a defined register. First, the master issues a start condition followed by a seven-bit I2C address. Next, the master writes a zero to conduct a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, DRV201A sets the I^2C register to a defined value and the master writes the eight-bit data value across the bus. Upon receiving a third acknowledge, DRV201A auto increments the internal I^2C register number by one and the master issues a stop condition. This action concludes the register write.

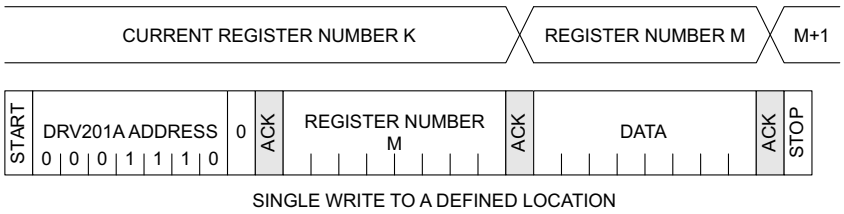

Figure 6. Single Write

7.5.1.2 Single Read from a Defined Location and Current Location

Figure 7 shows the format of a single read from a defined location. First, the master issues a start condition followed by a seven-bit I^2C address. Next, the master writes a zero to conduct a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, DRV201A sets the internal I^2C register number to a defined value. Then the master issues a repeat start condition and a seven-bit I^2C address followed by a one to conduct a read operation. Upon receiving a third acknowledge, the master releases the bus to the DRV201A. The DRV201A then writes the eight-bit data value from the register across the bus. The master acknowledges receiving this byte and issues a stop condition. This action concludes the register read.

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Programming (continued)

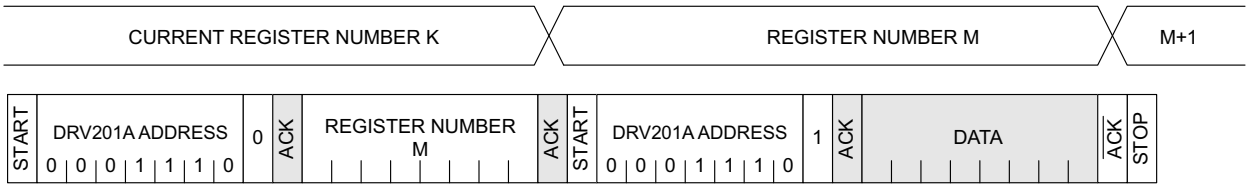

Figure 7. Single Read From A Defined Location

Figure 8 shows the single read from the current location. If the read command is issued without defining the register number first, DRV201A writes out the data from the current register from the device memory.

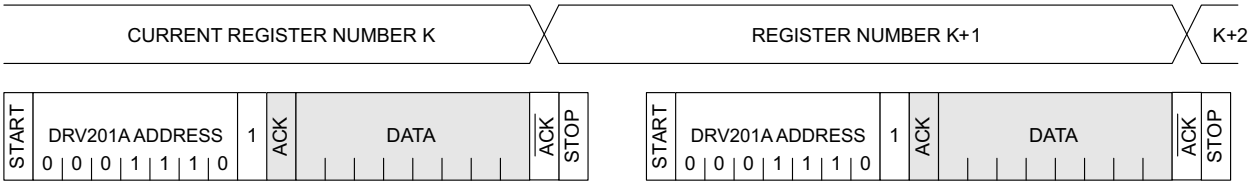

Figure 8. Single Read From The Current Location

7.5.1.3 Sequential Read and Write

Sequential read and write allows simple and fast access to DRV201A registers. Figure 9 shows sequential read from a defined location. If the master doesn't issue a stop condition after giving ACK, DRV201A auto increments the register number and writes the data from the next register.

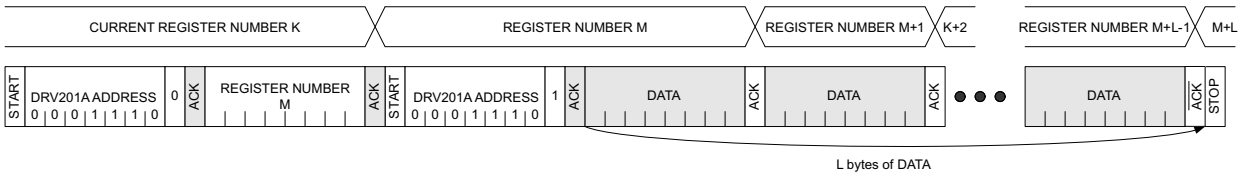

Figure 9. Sequential Read From A Defined Location

Figure 10 shows the sequential write. If the master doesn't issue a stop condition after giving ACK, DRV201A auto increments it's register by one and the master can write to the next register.

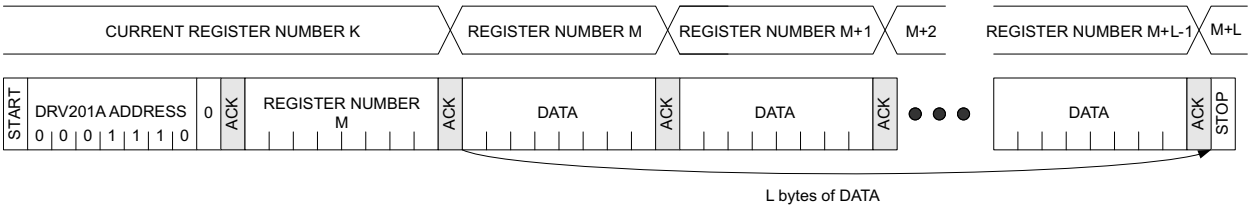

Figure 10. Sequential Write

If read is started without writing the register value first, DRV201A writes out data from the current location. If the master doesn't issue a stop condition after giving ACK, DRV201A auto increments the I^2C register and writes out the data. This continues until the master issues a stop condition. This is shown in Figure 11.

Programming (continued)

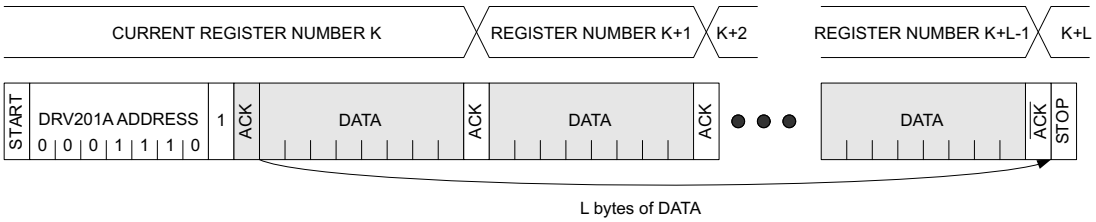

Figure 11. Sequential Read Starting From A Current Location

7.5.1.4 I²C Device Address, Start and Stop Condition

Data transmission is initiated with a start bit from the controller as shown in Figure 12. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. SDA data is latched by DRV201A on the rising edge of the SCL line. If the appropriate device address bits are set for the device, DRV201A issues the ACK by pulling the SDA line low on the next falling edge after 8th bit is latched. SDA is kept low until the next falling edge of the SCL line.

Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. Reference Figure 13.

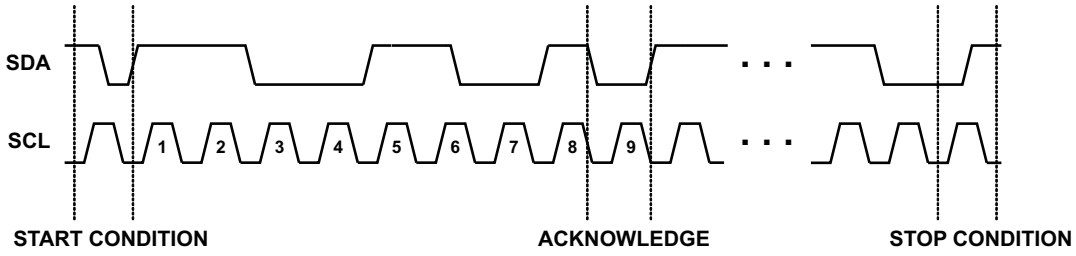

Figure 12. I²C Start/Stop/Acknowledge Protocol

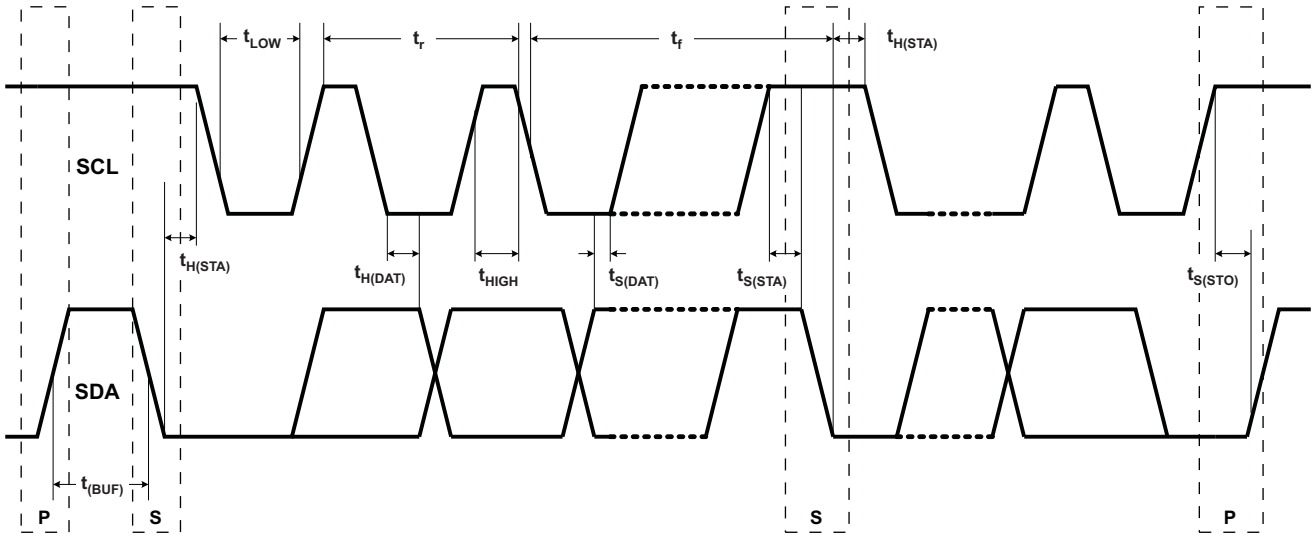

Figure 13. I²C Data Transmission Protocol

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7.6 Register Maps

Table 2. Register Maps

REGISTER	ADDRESS (HEX)	NAME	DEFAULT VALUE	DESCRIPTION
1	01	not used		
2	02	CONTROL	0000 0010	Control register
3	03	VCM_CURRENT_MSB	0000 0000	Voice coil motor MSB current control
4	04	VCM_CURRENT_LSB	0000 0000	Voice coil motor LSB current control
5	05	STATUS	0000 0000	Status register
6	06	MODE	0000 0000	Mode register
7	07	VCM_FREQ	1000 0011	VCM resonance frequency

7.6.1 Control Register (Address – 0x02h)

Table 3. Control Register Address – 0x02h Description

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	not used	EN_RING	RESET
READ/WRITE	R	R	R	R	R	R	R/W	R/W
RESET VALUE	0	0	0	0	0	0	1	0

Table 4. Control Register Address Field Definitions

FIELD NAME	BIT DEFINITION
RESET	Forced software reset (reset all registers to default values) and device goes into STANDBY. RESET bit is automatically cleared when written high. 0 – inactive 1 – device goes to STANDBY
EN_RING	Enables ringing compensation. 0 – disabled 1 – enabled

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7.6.2 VCM MSB Current Control Register (VCM_Current_MSB) Address – 0x03h

Table 5. VCM MSB Current Control Register (VCM_Current_MSB) Address – 0x03h Description

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	not used	VCM_CURRENT[9:8]	
READ/WRITE	R	R	R	R	R	R	R/W	
RESET VALUE	0	0	0	0	0	0	0	0

Table 6. VCM MSB Current Control Register Field Definitions

FIELD NAME	BIT DEFINITION
VCM_CURRENT[9:8]	VCM current control 00 0000 0000b – 0 mA 00 0000 0001b – 0.1 mA 00 0000 0010b – 0.2 mA … 11 1111 1110b – 102.2 mA 11 1111 1111b – 102.3 mA **NOTE** When setting the current in DRV201A both VCM_CURRENT_MSB and VCM_CURRENT_LSB registers have to be updated. DRV201A starts updates the current after LSB register write is completed.

7.6.3 VCM LSB Current Control Register (VCM_Current_ISB) Address – 0x04h

Table 7. VCM LSB Current Control Register (VCM_Current_ISB) Address – 0x04hDescription

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VCM_CURRENT[7:0]							
READ/WRITE	R/W							
RESET VALUE	0	0	0	0	0	0	0	0

Table 8. VCM LSB Current Control Register Field Definitions

FIELD NAME	BIT DEFINITION
VCM_CURRENT[7:0]	VCM current control 00 0000 0000b – 0 mA 00 0000 0001b – 0.1 mA 00 0000 0010b – 0.2 mA … 11 1111 1110b – 102.2 mA 11 1111 1111b – 102.3 mA **NOTE** When setting the current in DRV201A both VCM_CURRENT_MSB and VCM_CURRENT_LSB registers have to be updated. DRV201A starts updates the current after LSB register write is completed.

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7.6.4 Status Register (Status) Address – 0x05h(1)

Table 9. Status Register (Status) Address – 0x05h Description

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	TSD	VCMS	VCMO	UVLO	OVC
READ/WRITE	R	R/WR	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

(1) Status bits are cleared when device changes it's state from standby to active. If TSD was tripped the device goes into Standby and will not allow the transition into Active until the device cools down and TSD is cleared.

Table 10. Status Register Address Field Descriptions

FIELD NAME	BIT DEFINITION
OVC	Over current detection
UVLO	Undervoltage Lockout
VCMO	Voice coil motor open detected
VCMS	Voice coil motor short detected
TSD	Thermal shutdown detected

7.6.5 Mode Register (Mode) Address – 0x06h

Table 11. Mode Register (Mode) Address – 0x06h Description

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	PWM_FREQ[2:0]			PWM/LIN	RING_MODE
READ/WRITE	R	R	R	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

Table 12. Mode Register (Mode) Address Field Definitions

FIELD NAME	BIT DEFINITION
RING_MODE	Ringing compensation settling time 0 – 2x(1/f_{VCM}) 1 – 1x(1/f_{VCM})
PWM/LIN	Driver output stage in linear or PWM mode 0 – PWM mode 1 – Linear mode
PWM_FREQ[2:0]	Output stage PWM switching frequency 000 – 0.5 MHz 001 – 1 MHz 010 – N/A 011 – 2 MHz 100 – N/A 101 – 4.8 MHz 110 – 6.0 MHz 111 – 4 MHz

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7.6.6 VCM Resonance Frequency Register (VCM_FREQ) Address – 0x07h

Table 13. VCM Resonance Frequency Register (VCM_FREQ) Address – 0x07h Description

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VCM_FREQ[7:0]							
READ/WRITE	R/W							
RESET VALUE	1	0	0	0	0	0	1	1

Table 14. VCM Resonance Frequency Register Field Definitions

FIELD NAME	BIT DEFINITION
VCM_FREQ[7:0]	VCM mechanical ringing frequency for the ringing compensation can be selected with the below formula. The formula gives the VCM_FREQ[7:0] register value in decimal which should be rounded to the nearest integer. $VCM_FREQ = 383 - \frac{19200}{F_{res}}$ (1) Default VCM mechanical ringing frequency is 76.4 Hz. $VCM_FREQ = 383 - \frac{19200}{76.4} = 131.69 \Rightarrow 132 \Rightarrow '1000\ 0011'$ (2)

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV201A device is a voice coil motor driver designed for camera auto focus control. The device allows for a highly efficient PWM current control for VCM, while reducing lens ringing in order to significantly lower the time needed for the lens to auto focus. The following design is a common application of the DRV201A device.

8.1.1 VCM Mechanical Ringing Frequency

Ringing compensation is dependent on the VCM resonance frequency, and this can be controlled through the VCM_FREQ register (07h) from 50 Hz up to 150 Hz. VCM mechanical ringing frequency for the ringing compensation can be selected using Equation 3. The formula gives the VCM_FREQ[7:0] register value in decimal which should be rounded to the nearest integer.

$$VCM_FREQ = 383 - \frac{19200}{F_{res}} \tag{3}$$

Default VCM mechanical ringing frequency is 76.4 Hz.

$$VCM_FREQ = 383 - \frac{19200}{76.4} = 131.69 \Rightarrow 132 \Rightarrow '1000\ 0011' \tag{4}$$

8.2 Typical Application

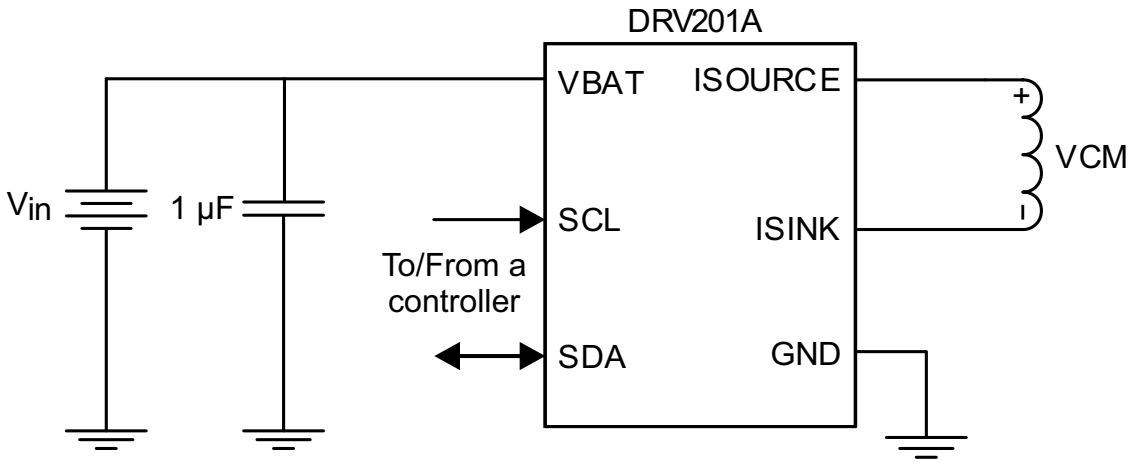

Figure 14. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 15 lists the design parameters.

Table 15. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	Vin	3.7
Motor Winding Resistance	RL	15 Ω
Motor Winding Inductance	IL	100 µH
Actuator Size		8.5 x 8.5 x 3.4 (mm)
Lens in the VCM		M6 (Pitch: 0.35)
Weight of VCM		75 mg
TTL		4.2 mm
FB		1.1 mm

8.2.2 Detailed Design Procedure

List of components:

- C_{in} - Panasonic ECJ0EB1A105M
- VCM - Mitsumi VCM KAF-V85S60
- Actuator size: 8.5 × 8.5 × 3.4 (mm)
- Lens in the VCM: M6 (Pitch: 0.35)
- Weight: 75 mg
- TTL: 4.2 mm
- FB: 1.1 mm

8.2.2.1 User Example 1

In Figure 15, lens settling time and settling window shows how lens control is defined. Below is an example case how the lens is controlled and what settling time is achieved:

Measured VCM resonance frequency = 100 Hz

- According to Table 1, VCM_FREQ[7:0] = ‘10111111’ (reg 0x07h)

VCM resonance frequency, f_{VCM}, variation is within ±10% (min 90 Hz … max 110 Hz)

- $1/f_{VCM}$ ringing compensation is used : RING_MODE = ‘1’ (reg 0x06h)

Stepping the lens by 50 µm

- The lens is settled into a ±5-µm window within 10 ms ($1/f_{VCM}$)

8.2.2.2 User Example 2

If the case is otherwise exactly the same, but VCM resonance frequency cannot be guaranteed to stay at more than ±30% variation, slower ringing compensation should be used:

Measured VCM resonance frequency = 100 Hz

- According to Table 1, VCM_FREQ[7:0] = ‘10111111’ (reg 0x07h)

VCM resonance frequency, f_{VCM}, variation is within ±30% (min 70 Hz … max 130 Hz)

- $2/f_{VCM}$ ringing compensation is used : RING_MODE = ‘0’ (reg 0x06h)

Stepping the lens by 50 µm

- The lens is settled into a ±5-µm window within 20 ms ($2/f_{VCM}$)

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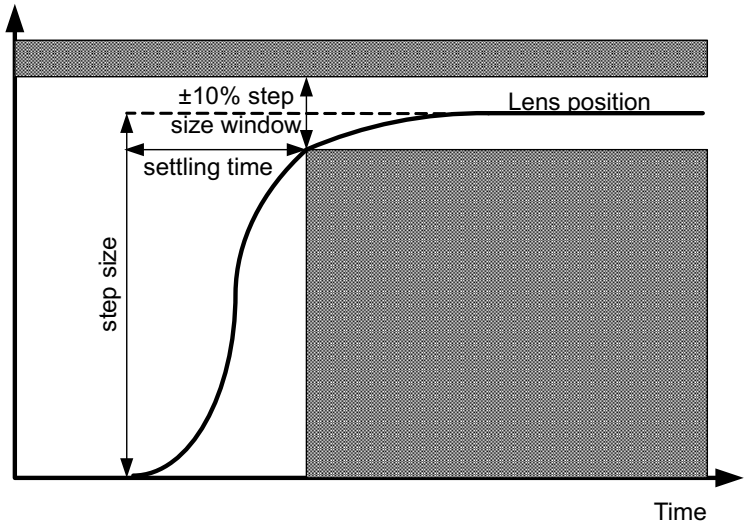

Figure 15. Lens Settling Time and Settling Window

8.2.3 Application Curves

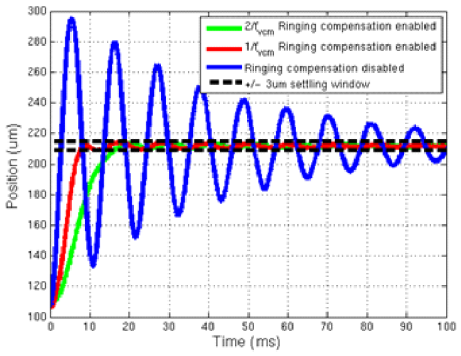

Figure 16. Lens Positions With and Without Ringing Compensation With 100-µm Step on the Lens Position

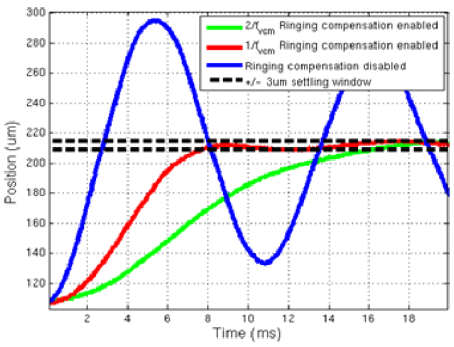

Figure 17. Lens Positions With and Without Ringing Compensation With 100-µm Step on the Lens Position, Zoomed In

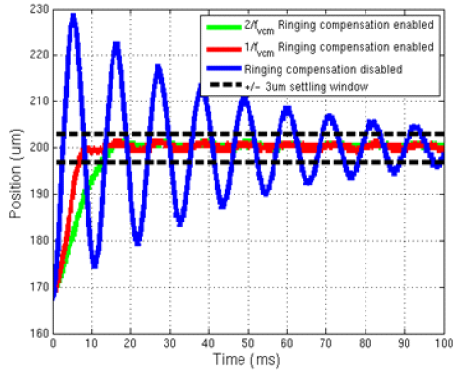

Figure 18. Lens Positions With and Without Ringing Compensation With 30-µm Step on the Lens Position

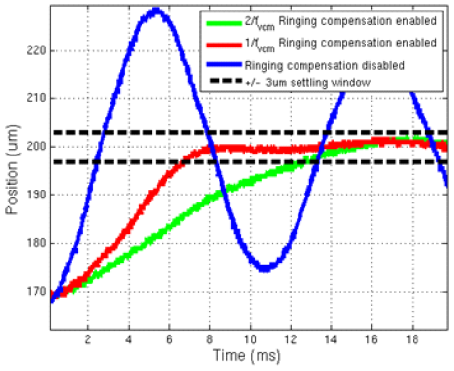

Figure 19. Lens Positions With and Without Ringing Compensation With 30-µm Step on the Lens Position, Zoomed In

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9 Power Supply Recommendations

The DRV201A device is designed to operate from an input voltage supply, VBAT, range between 2.5 and 4.8 V. The user must place at least a 1-uF ceramic bypass capacitor rated for a minimum of 6.3 V as close as possible to VBAT and GND pin.

10 Layout

10.1 Layout Guidelines

The VBAT pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of at least 1-µF rated for a minimum of 6.3 V. Place this capacitor as close to the VBAT and GND pins as possible with a thick trace or ground plane connection to the device GND pin.

10.2 Layout Example

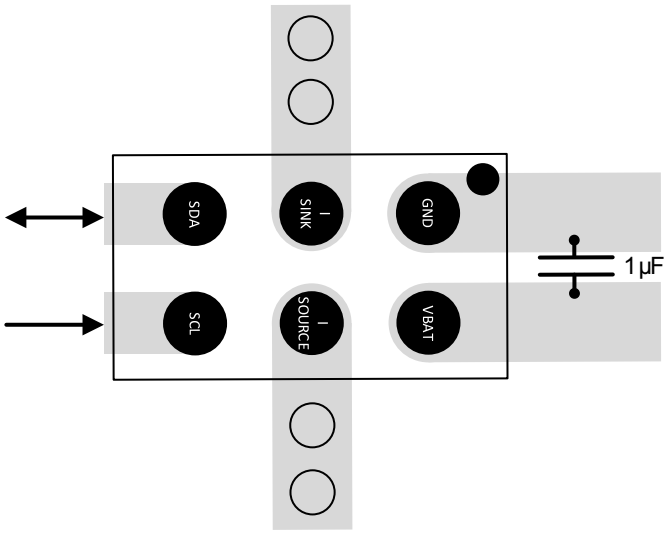

Figure 20. Recommended Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

YMB package markings (see pinouts in *Pin Configuration and Functions*):

- YM = YEAR / MONTH DATE CODE
- D = DAY OF LASER MARK
- S = ASSEMBLY SITE CODE
- O = PinA1 (Filled Solid)

Table 16. YMB Package Dimensions

DIMENSION	MIN	TYP	MAX	UNIT
Length			1.49	mm
Width			0.806	mm
Height(1)	0.278	0.289	0.3	mm
Ball pitch	0.39	0.4	0.41	mm
Ball height	4.8	6	7.2	µm
Coating thickness(2)	0.39	0.4	0.41	mm

(1) Height tolerances valid for both coated and non-coated packages.
(2) Coating thickness only applies to DRV201AYMBRB (coated) package option.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV201AYMBR	ACTIVE	PICOSTAR	YMB	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	201A	Samples
DRV201AYMBRB	ACTIVE	PICOSTAR	YMB	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	201AB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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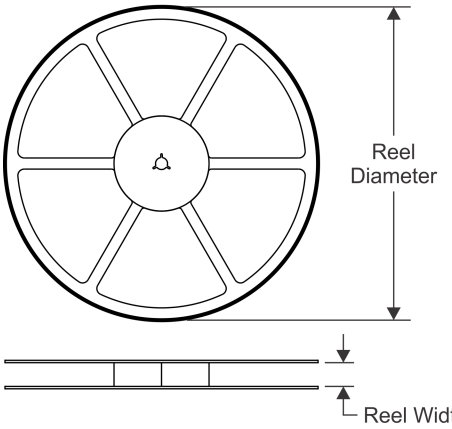
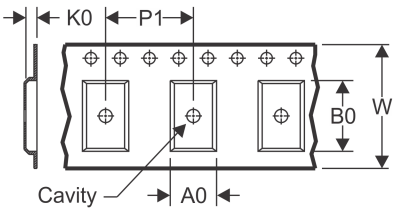
TAPE AND REEL INFORMATION

REEL DIMENSIONS

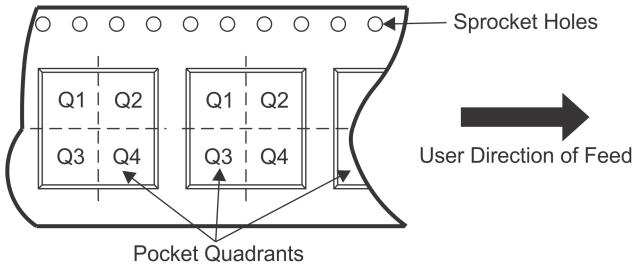


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

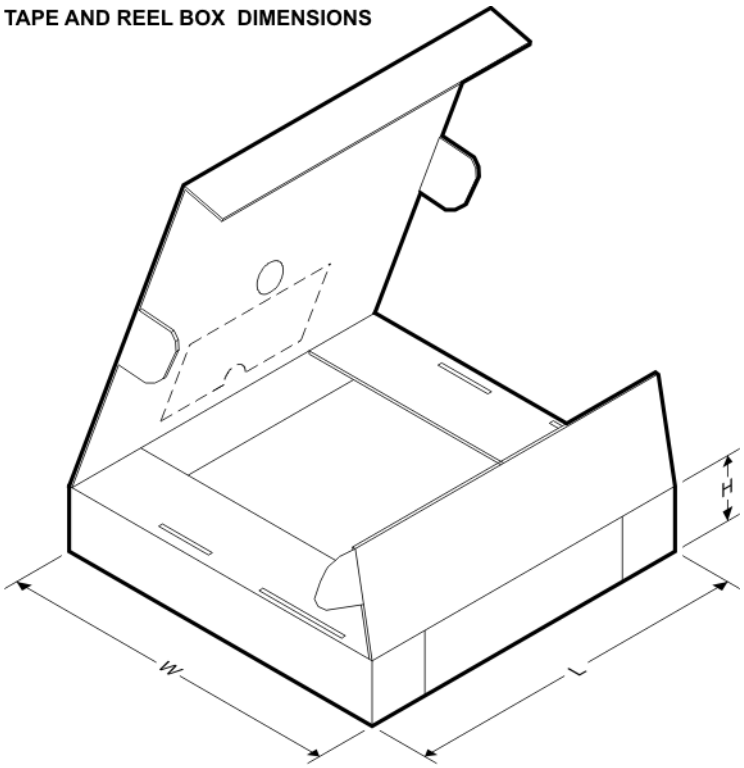
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV201AYMBR	PICOSTAR	YMB	6	3000	180.0	8.4	0.91	1.59	0.36	4.0	8.0	Q1
DRV201AYMBRB	PICOSTAR	YMB	6	3000	180.0	8.4	0.91	1.59	0.36	4.0	8.0	Q1

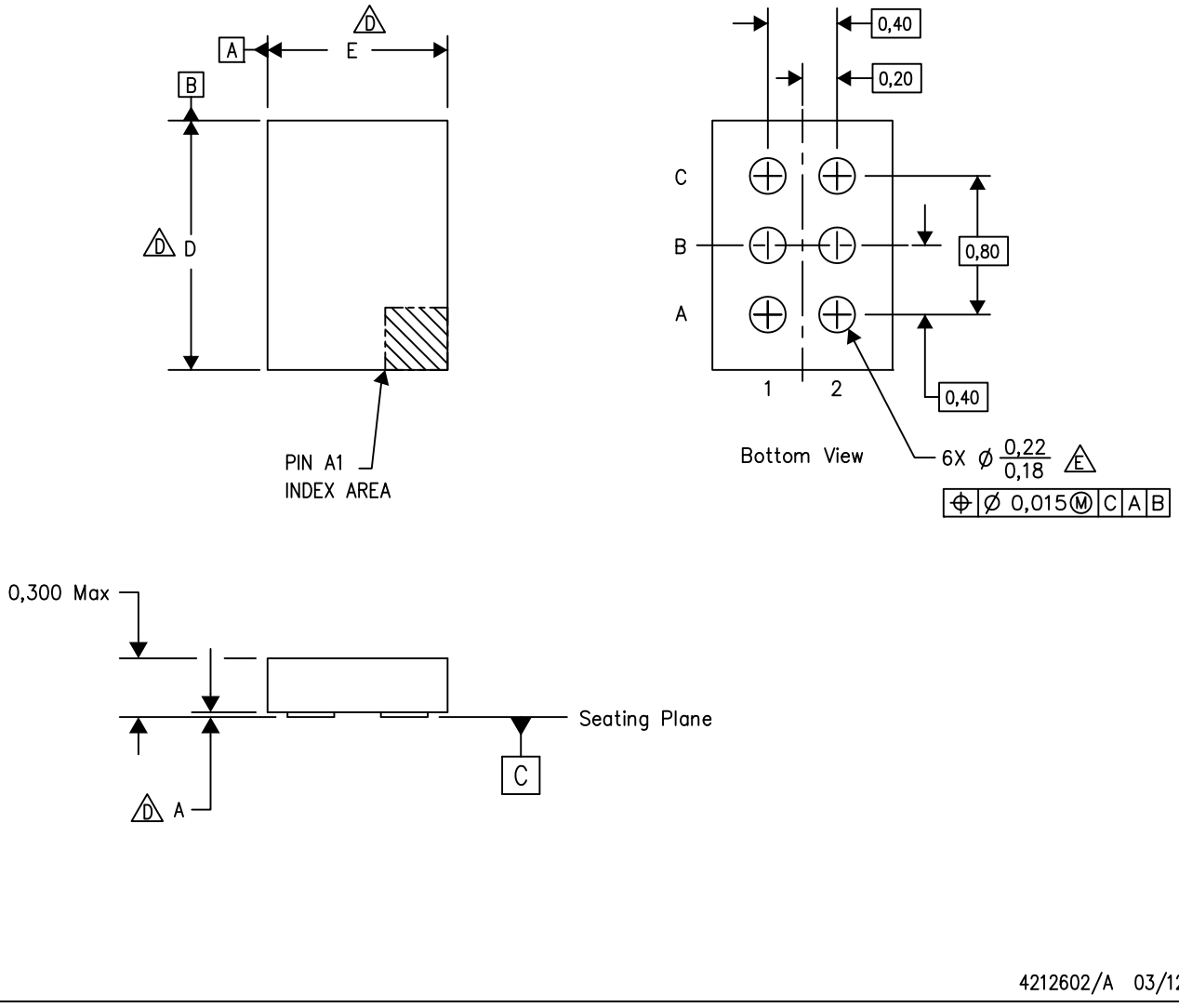
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV201AYMBR	PICOSTAR	YMB	6	3000	182.0	182.0	20.0
DRV201AYMBRB	PICOSTAR	YMB	6	3000	182.0	182.0	20.0

YMB (R–pSTAR–N6) PicoStar™



4212602/A 03/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. PicoStar™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 3 matrix pattern is shown for illustration only.
F. This package is a Pb–free solder land design.

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