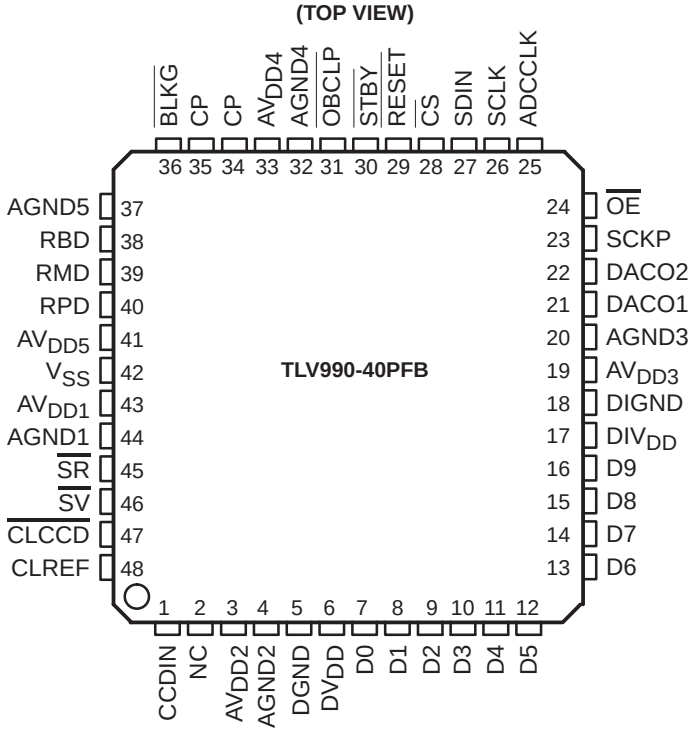
## features

- **Single-Chip CCD Analog Front-End**
- **10-Bit, 40-MSPS†, A/D-Converter Single 3-V Supply Operation**
- **Very Low Power: 200 mW Typical, 2-mW Power-Down Mode**
- **Differential Nonlinearity Error: < ±0.6 LSB Typical**
- **Integral Nonlinearity Error: < ±1.75 LSB Typical**
- **Programmable Gain Amplifier (PGA) With 0-dB to 36-dB Gain Range (0.045 dB/Step)**
- **Automatic or Programmable Optical Black Level and Offset Calibration With Digital Filter and Bad Pixel Limits**
- **Additional DACs for External Analog Setting**
- **Serial Interface for Register Configuration**
- **Internal-Reference Voltages**
- **48-Pin TQFP Package**

## application

- **Digital Still Camera**
- **Video Camcorder**

**PFB PACKAGE**
**(TOP VIEW)**




## description

The TLV990-40 is a complete CCD and video signal processor/digitizer designed for digital still camera and video camcorder applications. The TLV990-40 performs all the analog-processing functions necessary to maximize the dynamic range, corrects various errors associated with the CCD sensor, and then digitizes the results with an on-chip high-speed analog-to-digital converter (ADC).

The key components of the TLV990-40 include: an input clamp circuit for CCD and analog video signals, a correlated double sampler (CDS), a programmable-gain amplifier (PGA) with 0 to 36-dB gain range, two internal digital-to-analog converters (DAC) for automatic or programmable optical black level and offset calibration, a 10-bit, 40-MSPS pipeline ADC, a parallel data port for easy microprocessor interface, a serial port for configuring internal control registers, two additional DACs for external system control, and internal reference voltages.

Designed in advanced CMOS process, the TLV990-40 operates from a single 3-V power supply with a normal power consumption of 200 mW at 40 MSPS, and 2 mW in power-down mode.

Its very high throughput rate, single 3-V operation, very low-power consumption, and fully-integrated analog processing circuitry make the TLV990-40 an ideal CCD and video signal-processing solution for electronic video-camcorder applications.

This device is available in a 48-pin TQFP package and is specified over a –20°C to 75°C operating-temperature range.

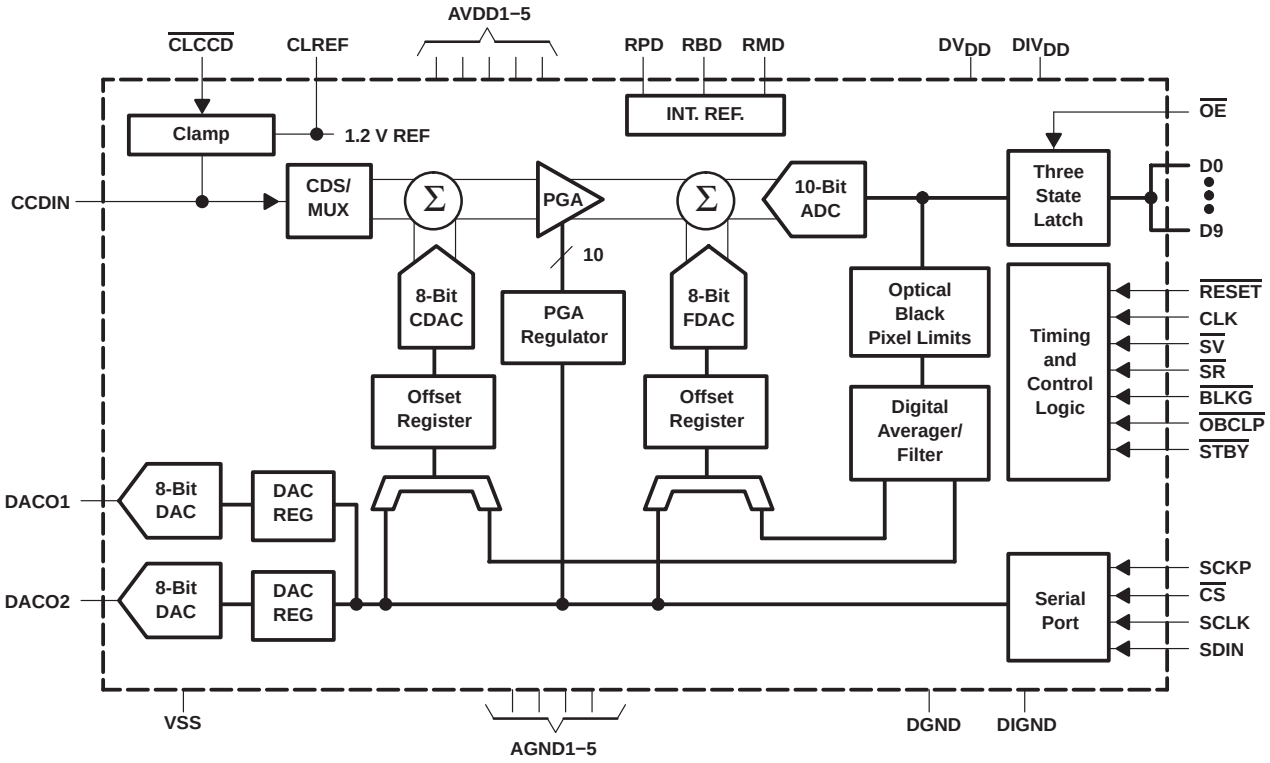


†The test register must be set to 1011 for 40 MSPS operation.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE DEVICE |
|---|---|
| | TQFP (PFB) |
| −20°C to 75°C | TLV990-40PFB |

## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| ADCCLK | 25 | I | ADC clock input |
| AGND1 | 44 | | Analog ground for internal CDS circuits |
| AGND2 | 4 | | Analog ground for internal PGA circuits |
| AGND3 | 20 | | Analog ground for internal DAC circuits |
| AGND4 | 32 | | Analog ground for internal ADC circuits |
| AGND5 | 37 | | Analog ground for internal REF circuits |
| $AV_{DD1}$ | 43 | | Analog supply voltage for internal CDS circuits, 3 V |
| $AV_{DD2}$ | 3 | | Analog supply voltage for internal PGA circuits, 3 V |
| $AV_{DD3}$ | 19 | | Analog supply voltage for internal DAC circuits, 3 V |
| $AV_{DD4}$ | 33 | | Analog supply voltage for internal ADC circuits, 3 V |
| $AV_{DD5}$ | 41 | | Analog supply voltage for internal ADC circuits, 3 V |
| $\overline{BLKG}$ | 36 | I | Control input. The CDS operation is disabled when BLKG is pulled low. |
| $\overline{CLCCD}$ | 47 | I | CCD signal clamp control input |
| CCDIN | 1 | I | CCD input |
| CLREF | 48 | O | Clamp reference voltage output |
| CP | 34, 35 | I | Connect this pin to $AV_{DD}$. |
| $\overline{CS}$ | 28 | I | Chip select. A logic low on this input enables the serial port. |
| D0 – D9 | 7–16 | O | 10-bit 3-state ADC output data or offset DACs test data |
| DACO1 | 21 | O | Digital-to-analog converter output1 |
| DACO2 | 22 | O | Digital-to-analog converter output2 |
| DGND | 5 | | Digital ground |
| DIGND | 18 | | Digital interface circuit ground |
| $DIV_{DD}$ | 17 | | Digital interface circuit supply voltage, 1.8 V− 4.4 V |
| $DV_{DD}$ | 6 | | Digital supply voltage, 3 V |
| NC | 2 | I | Not connected |
| $\overline{OBCLP}$ | 31 | I | Optical black level and offset calibration control input. Active low. |
| $\overline{OE}$ | 24 | I | Output data enable. Active low. |
| RBD | 38 | O | Internal bandgap reference for external decoupling |
| $\overline{RESET}$ | 29 | I | Hardware-reset input, active low. This signal forces a reset of all internal registers |
| RMD | 39 | O | Ref− output for external decoupling |
| RPD | 40 | O | Ref+ output for external decoupling |
| SDIN | 27 | I | Serial data input to configure the internal registers |
| SCKP | 23 | I | Selects the polarity of SCLK. 0 – active low (high when SCLK is not running), 1 – active high (low when SCLK is not running) |
| SCLK | 26 | I | Serial clock input. This clock synchronizes the serial data transfer. |
| $\overline{SR}$ | 45 | I | CCD reference level sample clock input |
| $\overline{STBY}$ | 30 | I | Hardware power-down control input, active low |
| $\overline{SV}$ | 46 | I | CCD signal level sample clock input |
| $V_{SS}$ | 42 | | Silicon substrate, normally connected to analog ground |

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $AV_{DD}$, $DV_{DD}$, $DIV_{DD}$ . . . . . −0.3 V to 6.5 V
Analog input voltage range . . . . . −0.3 V to $AV_{DD}$+0.3 V
Digital input voltage range . . . . . −0.3 V to $DV_{DD}$+0.3 V
Operating virtual junction temperature range, $T_J$ . . . . . −40°C to 150°C
Operating free-air temperature range, $T_A$ . . . . . −20°C to 75°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

#### power supplies

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog supply voltage | $AV_{DD}$ | 2.7 | 3 | 3.3 | V |
| Digital supply voltage | $DV_{DD}$ | 2.7 | 3 | 3.3 | V |
| Digital interface supply voltage | $DIV_{DD}$ | 1.8 | | 4.4 | V |

#### digital inputs, $DIV_{DD}$ = 3 V, $DV_{DD}$ = 3 V

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| High-level input voltage, $V_{IH}$ | $0.8DIV_{DD}$ | | | V |
| Low-level input voltage, $V_{IL}$ | | | $0.2DIV_{DD}$ | V |
| Input ADCCLK frequency | | | 40 | MHz |
| ADCCLK pulse duration, clock high, $t_{w(MCLKH)}$ | 12.5 | | | ns |
| ADCCLK pulse duration, clock low, $t_{w(MCLKL)}$ | 12.5 | | | ns |
| Input SCLK frequency | | | 40 | MHz |
| SCLK pulse duration, clock high, $t_{w(SCLKH)}$ | 12.5 | | | ns |
| SCLK pulse duration, clock low, $t_{w(SCLKL)}$ | 12.5 | | | ns |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $AV_{DD}$=$DV_{DD}$=3 V, ADCCLK=40 MHz (unless otherwise noted)

### total device

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | $AV_{DD}$ operating current | | | 56 | | mA |
| | $DV_{DD}$ operating current | | | 8 | | mA |
| | Device power consumption | | | 200 | | mW |
| | Power consumption in power-down mode | | | 2 | | mW |
| INL | Full channel integral nonlinearity | $AV_{DD}$=$DV_{DD}$= 2.7 V – 3.3 V, Using best fit method | | ±1.75 | ±2.15 | LSB |
| DNL | Full channel differential nonlinearity | $AV_{DD}$=$DV_{DD}$= 2.7 V – 3.3 V, ADCCLK=18 MSPS, 10 bits | | ±0.5 | ±0.99 | LSB |
| | No missing code | | | Assured | | |
| | Full channel output latency | | | 6 | | CLK cycles |

### analog-to-digital converter (ADC)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| ADC resolution in CCD mode | | | 10 | | Bits |
| Full scale input span | | | 2 | | $V_{P-P}$ |
| Conversion rate | | | | 40 | MHz |

### correlated double sample (CDS) and programmable gain amplifier (PGA)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CDS and PGA sample rate | | | | 40 | MHz |
| CDS full-scale input span | Single-ended input | | | 1 | V |
| Input capacitance of CDS | | | 4 | | pF |
| Minimum PGA gain | | | 0 | 1 | dB |
| Maximum PGA gain | | 35 | 36 | 37 | dB |
| PGA gain resolution | | | 0.045 | | dB |
| PGA programming code resolution | | | 10 | | Bits |

### internal digital-to-analog converters (DAC) for offset correction

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | DAC resolution | | | 8 | | Bits |
| INL | Integral nonlinearity | | | ±0.5 | | LSB |
| DNL | Differential nonlinearity | | | ±0.5 | | LSB |
| | Output settling time | To 1% accuracy | | 80 | | ns |

## electrical characteristics over recommended operating free-air temperature range, $T_A$ = 25°C, $AV_{DD}$=$DV_{DD}$=3 V, ADCCLK=40 MHz (unless otherwise noted)

### user digital-to-analog converters (DAC)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | DAC resolution | | | 8 | | Bits |
| INL | Integral nonlinearity | | | ±0.75 | | LSB |
| DNL | Differential nonlinearity | | | ±0.5 | | LSB |
| | Output voltage range | | 0 | | $V_{DD}$ | V |
| | Output settling time | 10 pF external load, settle to 1 mV | | 4 | | µs |

### reference voltages

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Internal bandgap voltage reference | | 1.43 | 1.50 | 1.58 | V |
| | Temperature coefficient | | | 100 | | ppm/°C |
| | ADC Ref+ | Externally decoupled | | 2 | | V |
| | ADC Ref− | | | 1 | | V |

### digital specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Logic inputs** | | | | | | |
| $I_{IH}$ | High-level input current | $DIV_{DD}$ = 3 V | −10 | | 10 | µA |
| $I_{IL}$ | Low-level input current | | −10 | | 10 | |
| $C_i$ | Input capacitance | | | 5 | | pF |
| **Logic outputs** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 50 µA, $DIV_{DD}$ = 3 V | | $DIV_{DD}$−0.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 50 µA, $DIV_{DD}$ = 3 V | | 0.4 | | V |
| $I_{OZ}$ | High-impedance-state output current | | | ±10 | | µA |
| $C_o$ | Output capacitance | | | 5 | | pF |

### key timing requirements

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SRW}$ | SR pulse width | Measured at 50% of pulse height | 10 | | | ns |
| $t_{SVW}$ | SV pulse width | | 10 | | | ns |
| $t_{OD}$ | ADCCLK-to-output data delay | | | 6 | | ns |
| $t_{CSF}$ | CS falling edge to SCLK rising edge | | 0 | | | ns |
| $t_{CSR}$ | SCLK falling edge to CS rising edge | | 5 | | | ns |

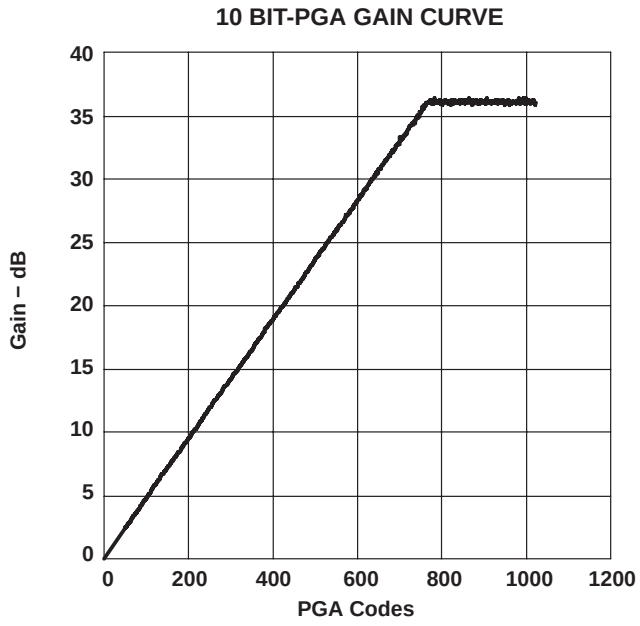



**Figure 1**

## TYPICAL CHARACTERISTICS

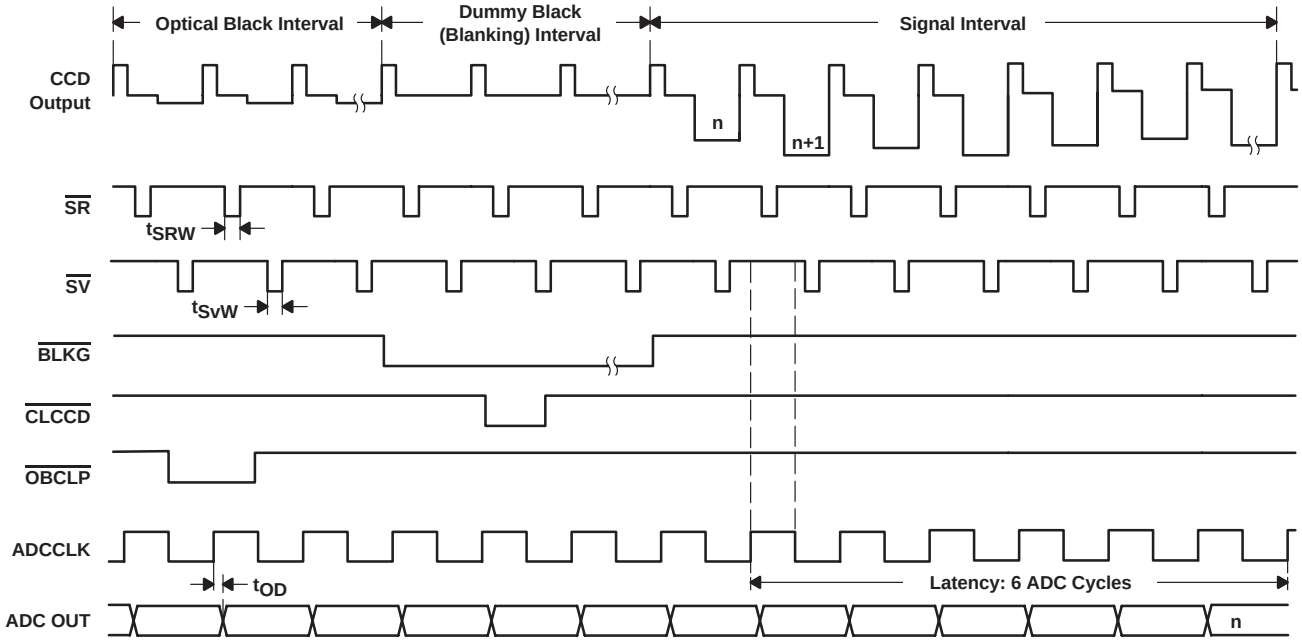



**Figure 2. System Operation Timing Diagram**

## TYPICAL CHARACTERISTICS

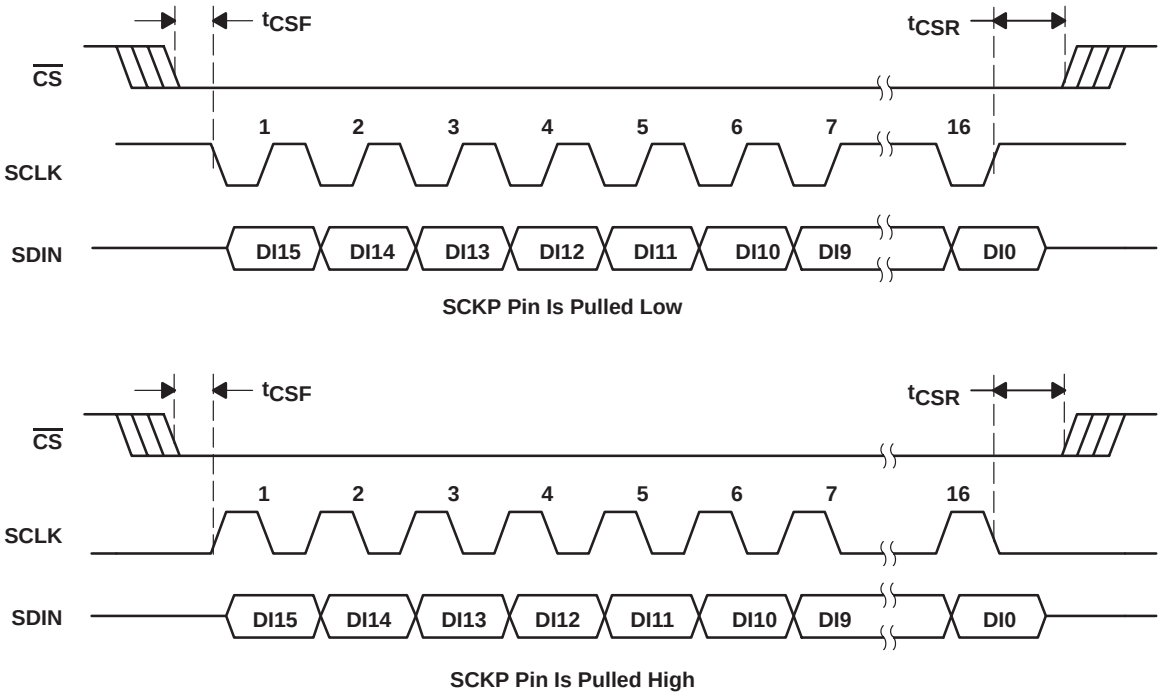
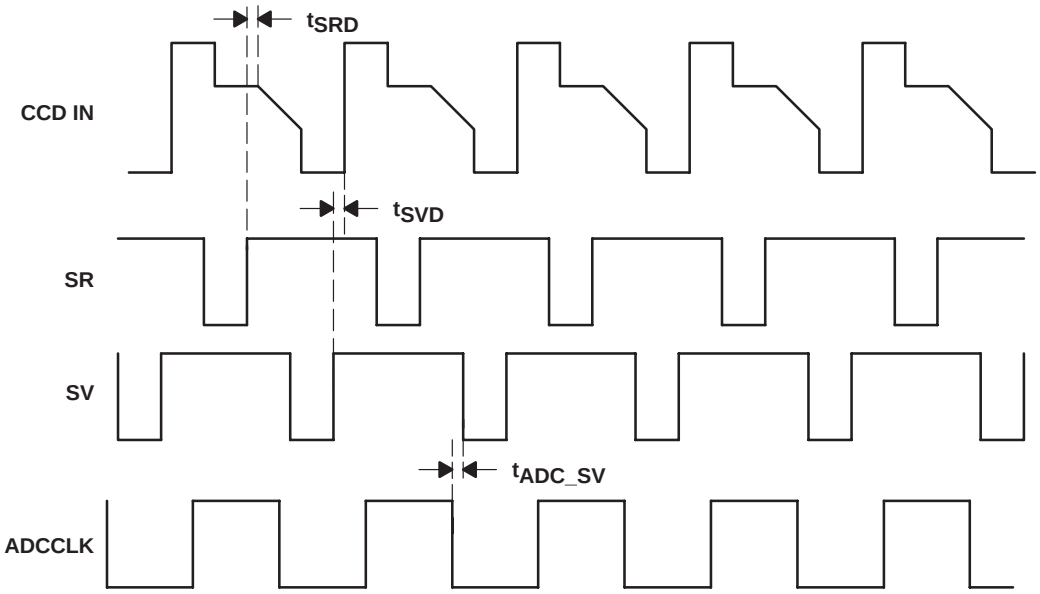



**Figure 3. Serial Interface Timing Diagram**

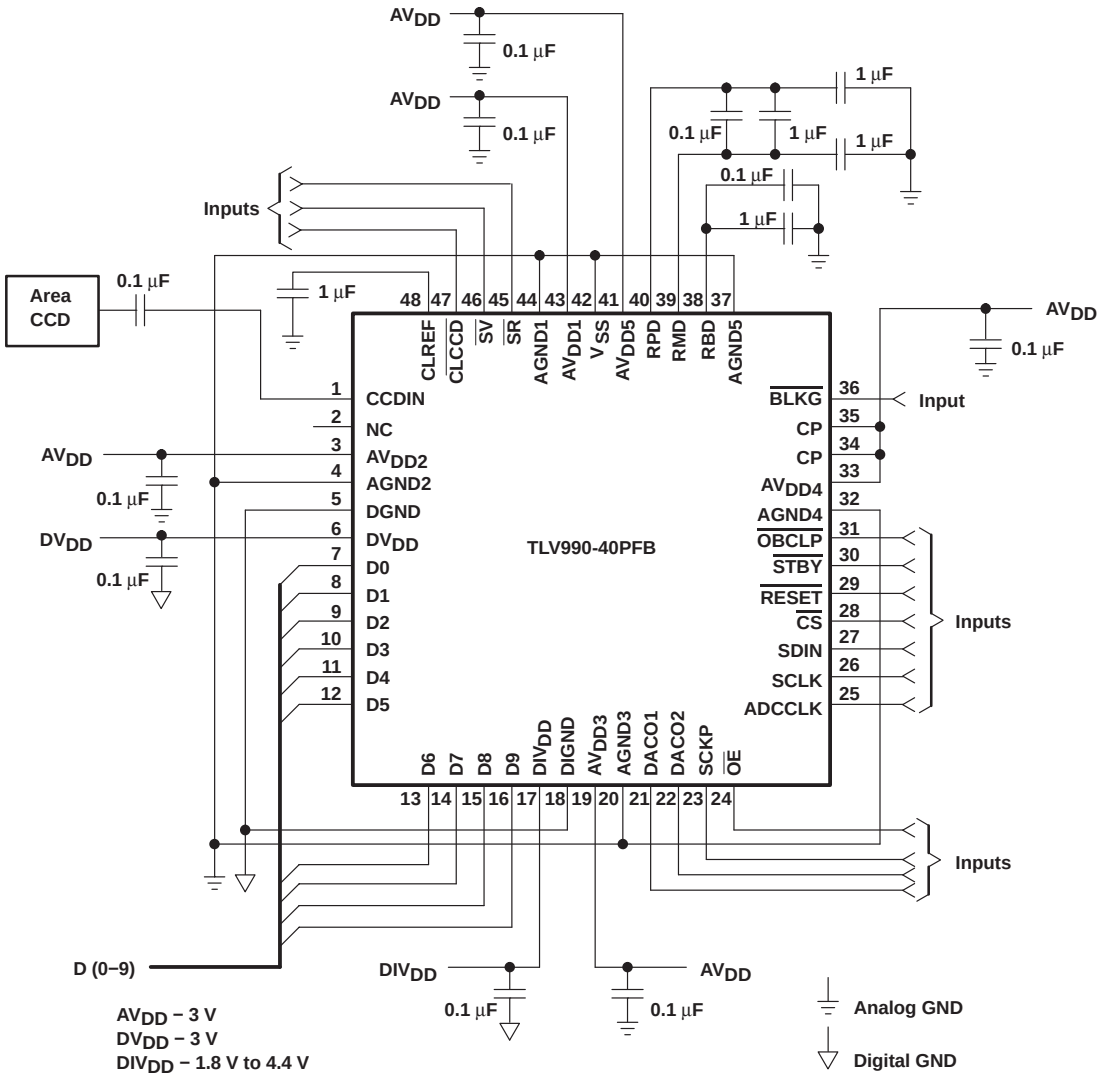
## TYPICAL CHARACTERISTICS




| TIMING PARAMETER | | MIN | TYP | MAX | EXPLANATION |
|---|---|---|---|---|---|
| $t_{SRD}$ | Delay between sample reset (SR) rising edge and actual sampling instant (ns) | 6 | | | This is the fixed internal delay in the chip. The reset value of the CCD waveform should be stable until the end of this period. |
| $t_{SVD}$ | Delay between sample video (SV) rising edge and actual instant of video signal sampling (ns) | 6 | | | This is the fixed internal delay in the chip. The video signal value of the CCD waveform should be stable until the end of this period. |
| $t_{ADC\_SV}$ | Time between ADCCLK falling edge and SV falling edge | 3 | | | The timing margin required to ensure the ADCCLK positive half cycle is in between two SV pulses |

**Figure 4. Detailed Internal Timing Diagram**

## APPLICATION INFORMATION




NOTE: All analog outputs should be buffered if the load is resistive, or if the load is capacitive and greater than 2 pF.

**Figure 5. Typical Application Connection**

## REGISTER DEFINITION

### serial input data format

| DI15 | DI14 | DI13 | DI12 | DI11 | DI10 | DI9 | DI8 | DI7 | DI6 | DI5 | DI4 | DI3 | DI2 | DI1 | DI0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | A3 | A2 | A1 | A0 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| A3 | A2 | A1 | A0 | | D9–D0 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Control register1 | 10-bit data be to written into the selected register |
| 0 | 0 | 0 | 1 | PGA gain register | |
| 0 | 0 | 1 | 0 | User DAC1 register | |
| 0 | 0 | 1 | 1 | User DAC2 register | |
| 0 | 1 | 0 | 0 | Coarse offset DAC | |
| 0 | 1 | 0 | 1 | Fine offset DAC | |
| 0 | 1 | 1 | 0 | Digital Vb register (sets reference code level at the ADC output during the optical black interval) | |
| 0 | 1 | 1 | 1 | Optical black setup register (sets the number of black pixels per line for digital averaging) | |
| 1 | 0 | 0 | 0 | Hot/cold pixel limit register (sets the limit for maximum positive deviation of optical black pixel from Vb value) | |
| 1 | 0 | 0 | 1 | Reserved | |
| 1 | 0 | 1 | 0 | Control register2 (sets the weight for digital filtering and video modes) | |
| 1 | 0 | 1 | 1 | Blanking data register (The data in this register appears at digital output during blanking (BLKG is low)) | |
| 1 | 1 | 0 | 0 | ADCCLK internal programmable delay register | |
| 1 | 1 | 0 | 1 | SR and SV internal programmable delay register | |
| 1 | 1 | 1 | 0 | Test register | |

### control register1 format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| STBY | PDD1 | PDD2 | ACD | AFD | OBM | X | SRSV | RTOB | RTSY |

### control register1 description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | STBY | Device power-down control: 1 = standby, 0 = active (default) |
| D8 | PDD1 | Power-down user DAC1: 1 = standby, 0 = active (default) |
| D7 | PDD2 | Power-down user DAC2: 1 = standby, 0 = active (default) |
| D6 | ACD | Coarse-offset DAC mode control:<br>0 = autocalibration (default), 1 = bypass autocalibration.<br>Note: When D6 is set to 0, D5 must also be set to 0 (automode). Otherwise, the automode will be disabled on both offset DACs. |
| D5 | AFD | Fine offset DAC mode control:<br>0 = autocalibration (default), 1 = bypass autocalibration.<br>Note: D5 can be set to 0 with or without D6 being set to 0. |
| D4 | OBM | This bit initiates the offset DACs starting sequence.<br>0 = coarse-offset DAC starts first (default)<br>1 = fine-offset DAC starts first |
| D3 | X | Reserved |
| D2 | SRSV | This bit specifies the polarity of SR and SV input pulses.<br>0 – SR/SV active low (default)<br>1 – SR/SV active high |
| D1 | RTOB | Writing 1 to this bit will reset calculated black-level results in the digital averager. |
| D0 | RTSY | Writing 1 to this bit will reset entire system to the default settings (edge sensitive). |

## REGISTER DEFINITION

### PGA register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Default PGA gain = 0000000000 or 0 dB

### user DAC1 and DAC2 registers format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | X | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Default user DAC register value = XX00000000

### coarse offset DAC register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | SIGN | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

### coarse offset DAC register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | X | Reserved |
| D8 | SIGN | Coarse DAC sign bit, 0 = + sign (default), 1 = − sign |
| D7−D0 | | Coarse DAC control data when the D6 in the control register is set at 1. |

Default coarse DAC register value = X000000000

### fine offset DAC register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | SIGN | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

### fine offset DAC register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | X | Reserved |
| D8 | SIGN | Fine DAC sign bit, 0 = + sign (default), 1 = − sign |
| D7−D0 | | Fine DAC control data when the D5 in the control register is set at 1. |

Default fine DAC register value = X000000000

### digital Vb (optical black level) register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Default Vb register value = 40 Hex

## REGISTER DEFINITION

### optical black setup register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| OMUX1 | OMUX0 | HYS | X | SOFW1 | SOFW0 | MP | PN2 | PN1 | PN0 |

### optical black setup register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D8, D9 | OMUX1, OMUX0 | These two bits multiplex digital output (data presented at D[9:0] pins):<br>OMUX1 OMUX0<br>0 0 D[9:0] = ADC output (default)<br>0 1 D[9:0] = ADC output<br>1 0 D[9] = fine/coarse (1/0) autocorrection flag<br>D[8] = coarse DAC sign<br>D[7:0] = coarse DAC value<br>1 1 D[9] = fine/coarse (1/0) autocorrection flag<br>D[8] = fine DAC sign<br>D[7:0] = fine DAC value |
| D7 | HYS | Sets the hysteresis<br>0 − Apply hysteresis to FDAC (default)<br>1 − No hysteresis |
| D6 | X | Reserved |
| D5, D4 | SOFW1, SOFW0 | These two bits set the digital filter weight when SOF is activated (the SOF bit in control register 2 is set to 1).<br>SOFW1 SOFW0 Weight<br>0 0 0 (default)<br>0 1 1<br>1 0 2<br>1 1 3 |
| D3 | MP | When this bit is 1, the number of optical black pixels to be averaged per line ($2^N$) is multiplied by 3.<br>By setting the MP and PN2−PN0 bits together, the number of optical black pixels can be programmed to have the following numbers:<br>1, 2, 3 (1X3), 4, 6 (2×3), 8, 12 (4×3), 16, 24 (8×3), 32, 48 (16×3), 64, 96 (32×3), and 192 (64×3).<br>Default: MP = 0, no multiplication |
| D2−D0 | PN2−PN0 | Number of optical black pixels per line to average = $2^N$<br>N can be 0, 1, 2, 3, 4, 5, and 6. Or number of pixels per line can be 1, 2, 4, 8 (default), 16, 32, or 64.<br>The maximum number of pixels per line is 64, even if N>6. |

Default optical black calibration register value = 0000000011

## REGISTER DEFINITION

### hot/cold pixel limit register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | HFIT |

### hot/cold pixel limit register description

| Bit | Name | Description |
|---|---|---|
| D9 − D1 | X | Reserved |
| D0 | HFIT | Set hot/cold pixel filter<br>0 − Apply Vb ± .8 hot/cold pixel filtering<br>1 − No hot/cold pixel filtering (default) |

Default hot/cold pixel limit register value = 0000000001

### control register2 format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| SOF | NOS | ASOF | VGND | INM | ACL | WT3 | WT2 | WT1 | WT0 |

### control register 2 description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9 | SOF | 0 – Normal mode (default)<br>1 – Start of frame (only used when exposure time is changed)<br>When this bit is set to 1, next positive ADCCLK edge indicates that next pixel line is the beginning of a new frame. The optical black correction will be performed with one line averaging only (digital filtering weight = 1) and without hot/cold pixel limits. |
| D8 | NOS | Internal test bit, add 255 to optical black pixels when this bit is set to 1; default = 0 |
| D7 | ASOF | Enable the auto SOF:<br>1 − Automatically enable SOF at major gain changes (no digital filtering for 1 line)<br>0 − No auto SOF (default) |
| D6 | VGND | Short VIDEOIN to GND when this bit is set to 1; default = 0 |
| D5 | INM | This bit selects the input modes.<br>0 − CCD mode (default)<br>1 − Video mode |
| D4 | ACL | 0 Video mode, autoclamp (default)<br>1 Video mode, manual clamp |
| D3−D0 | WT3−WT0 | These three bits set the weight for digital filtering.<br>WT3 WT2 WT1 WT0 — Weight (effect of the averaged result of each optical black pixel line on overall optical black averaging)<br>0 0 0 0 — 1<br>0 0 0 1 — 1/2<br>0 0 1 0 — 1/2<br>0 0 1 1 — 1/8<br>0 1 0 0 — 1/16<br>0 1 0 1 — 1/32<br>0 1 1 0 — 1/64<br>0 1 1 1 — 1/128 (default)<br>1 0 0 0 — 1/256 |

Default control register2 value = X000000000

## REGISTER DEFINITION

### blanking data register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | BDTA | 0 | 0 | 0 | 0 | 0 |

### blanking data register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D5 | BDTA | This register value appears at the digital output when BLKG is low. When this bit is set to 1, digital output during blanking will be VB. Register default value = 0. |

Default = 0000000000

### ADCCLK internal delay register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | ADL3 | ADL2 | ADL1 | ADL0 |

### ADCCLK internal delay register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9−D4 | X | Reserved |
| D3−D0 | ADL3−ADL0 | These four bits set the internal ADCCLK delay.<br>ADL3 ADL2 ADL1 ADL0 Typical internal delay<br>0 0 0 0 0 ns (default)<br>:<br>:<br>1 1 1 1 10 ns |

Default register value = XXXXXX0000

### SR and SV internal delay register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| X | X | SVL3 | SVL2 | SVL1 | SVL0 | SRL3 | SRL2 | SRL1 | SRL0 |

### SR and SV internal delay register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9−D8 | X | Reserved |
| D7−D4 | SVL3−SVL0 | These four bits set the internal SV delay.<br>SVL3 SVL2 SVL1 SVL0 Typical internal delay<br>0 0 0 0 0 ns (default)<br>:<br>:<br>1 1 1 1 10 ns |
| D3−D0 | SRL3−SRL0 | These four bits set the internal SR delay.<br>SRL3 SRL2 SRL1 SRL0 Typical internal delay<br>0 0 0 0 0 ns (default)<br>:<br>:<br>1 1 1 1 10 ns |

Default register value = XX00000000

## REGISTER DEFINITION

### test register format

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| TB9 | TB8 | TB7 | TB6 | X | X | TB3 | TB2 | X | X |

Default register value =0110000000

These bits must be set to 1011 for 40 MSPS

### test register description

| BIT | NAME | DESCRIPTION |
|---|---|---|
| D9−D6 | TB9−TB6 | These four bits are used to program internal DC bias current. The bias current programming uses the following equation:<br>$I_{bias}$ = 8 μA + (code) × 2 μA<br>Hence, $I_{bias}$ varies from 8 μA (code=0000) to 38 μA (code=1111), with a linear step of 2 μA.<br>Default code is 0110. These bits must be set to 1011 for 40 MSPS |
| D5, D4 | | Reserved |
| D3 | TB3 | 1 – use external reference, power down internal reference<br>0 – use internal reference (default) |
| D2 | TB2 | This bit selects test input mode.<br>0 − Single-ended input on CCDIN pin,<br>1 − Differential input on both CCDIN and VIDEOIN pins |
| D1, D0 | | Reserved |

## PRINCIPLES OF OPERATION

### CCD mode operation

The output from the CCD sensor is first fed to a correlated double sampler (CDS) through the CCDIN pin. The CCD signal is sampled and held during the reset reference interval and the video signal interval. By subtracting two resulting voltage levels, the CDS removes low frequency noise from the output of the CCD sensor and obtains the voltage difference between the CCD reference level and the video level of each pixel. Two sample/hold control pulses (SR and SV) are required to perform the CDS function.

The CCD output is capacitively coupled to the TLV990-40. The ac-coupling capacitor is clamped to establish proper dc bias during the dummy pixel interval by the $\overline{\text{CLCCD}}$ input. The bias at the input to the TLV990-40 is set to 1.2 V. Normally, $\overline{\text{CLCCD}}$ is applied at sensor's line rate. A capacitor, with a value ten times larger than that of the input ac-coupling capacitor, should be connected between the CLREF pin and the AGND.

When operating the TLV990-40 at its maximum speed, the CCD internal source resistance should be smaller than 50 Ω. Otherwise CCD output buffering is required.

The signal is sent to the PGA after the CDS function is complete. The PGA gain can be adjusted from 0 to 36 dB by programming the internal gain register via the serial port. The PGA is digitally controlled with 10-bit resolution on a linear dB scale, resulting in a 0.045-dB gain step. The gain can be expressed by the following equation,

Gain = PGA code × 0.045 dB

Where PGA code has a range of 0 to 767.

## PRINCIPLES OF OPERATION

### ADC

The ADC employs a pipelined architecture to achieve high throughput and low power consumption. Fully-differential implementation and digital-error correction ensure 10-bit resolution.

The latency of the ADC data output is 6 ADCCLK cycles, as shown in Figure 1. Pulling the OE pin (pin 24) high puts the ADC output in high impedance.

### user DACs

The TLV990-40 includes two user DACs that can be used for external analog settings. The output voltage of each DAC can be independently set and has a range of 0 V up to the supply voltage, with an 8-bit resolution. When the user DACs are not used in a camera system, they can be put in the standby mode by programming control bits in the control register.

### internal timing

The SR and SV signals are required to operate the CDS, as previously explained. The user needs to synchronize the SR and SV clocks with the CCD signal waveform. The output of the ADC is read out to external circuitry by the ADCCLK signal, which is also used internally to control both ADC and PGA operations. It is required that the positive half cycle of the ADCCLK signal always falls in between two adjacent SV pulses as shown in Fig. 1. The user can then fine tune the ADCCLK timing in relation to the CDS timing to achieve optimal performance.

The $\overline{\text{CLCCD}}$ signal is used to activate the input clamping and the $\overline{\text{OBCLP}}$ signal is used to activate auto-optical black and offset correction.

### input blanking function

Large input transients may occur at the TLV990-40's input during some period of operation which can saturate the input circuits and cause long recovery time. To prevent circuit saturation the TLV990-40 includes an input blanking function that blocks the input signals by disabling the CDS operation whenever the BLKG input is pulled low. The TLV990-40 digital output will be set by the blanking data register after BLKG is pulled low.

**NOTE:**

If the BLKG pulse is located before the OBCLP pulse, there must be at least 4 pixels between the rising edge of the BLKG pulse and the falling edge of the OBCLP pulse. If the BLKG pulse is located after the OBCLP, the minimum number of pixels between the falling edge of the OBCLP and the falling edge of the BLKG pulse should be equal to the number of optical black pixels per line + 4.

### 3-wire serial interface

A simple 3-wire (SCLK, SDIN, and $\overline{\text{CS}}$) serial interface is provided to allow writing to the TLV990-40 internal registers. Serial clock SCLK can be run at a maximum frequency of 40 MHz. Serial data SDIN is 16 bits long. The two leading null bits are followed by four address bits for which the internal register is to be updated, and then ten bits of data to be written to the register. The $\overline{\text{CS}}$ pin must be held low to enable the serial port. Data transfer is initiated by the incoming SCLK after $\overline{\text{CS}}$ falls.

The SCLK polarity is selectable by pulling the SCKP pin either high or low.

## PRINCIPLES OF OPERATION

### device reset

When pin RESET (pin 29) is pulled low, all internal registers are set to their default values. The device also resets itself when it is first powered on. In addition, the TLV990-40 has a software-reset function that resets the device when writing a control bit to the control register.

See the *register definition* section for the register default values.

### voltage references

An internal precision-voltage reference of 1.5 V nominal is provided. This reference voltage is used to generate the ADC Ref− voltage of 1 V and Ref+ of 2 V. It is also used to set the clamp voltage. All internally-generated voltages are fixed values and cannot be adjusted.

### power-down mode (standby)

The TLV990-40 implements both hardware and software power-down modes. Pulling pin $\overline{\text{STBY}}$ (pin 30) low puts the device in the low-power standby mode. Total supply current drops to about 0.6 mA. Setting a power-down control bit in the control register can also activate the power-down mode. The user can still program all internal registers during the power-down mode.

### power supply

The TLV990-40 has several power-supply pins. Each major internal analog block has a dedicated $AV_{DD}$ supply pin. All internal digital circuitry is powered by $DV_{DD}$. Both $AV_{DD}$ and $DV_{DD}$ are 3-V nominal.

The $DIV_{DD}$ and DIGND pins supply power to the output digital driver (D9−D0). The $DIV_{DD}$ is independent of the $DV_{DD}$ and can be operated from 1.8 V to 4.4 V. This allows the outputs to interface with digital ASICs requiring different supply voltages.

### ground and decoupling

All ground pins of the TLV990-40 are not internally connected and must be connected externally to PCB ground.

General practices should apply to the PCB design to limit high-frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. In the case of power supply decoupling, 0.1-μF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Recommended external decoupling for the three voltage-reference pins is shown in Figure 4. Since their effectiveness depends largely on the proximity to the individual supply pin, all decoupling capacitors should be placed as close as possible to the supply pins.

To reduce high-frequency and noise coupling, it is highly recommended that digital and analog grounds be shorted immediately outside the package. This can be accomplished by running a low-impedance line between DGND and AGND under the package.

## PRINCIPLES OF OPERATION

### automatic optical black and offset correction

In the TLV990-40, the optical black and system channel-offset corrections are performed by an autodigital feedback loop. Two DACs are used to compensate for both channel offset and optical black offset. A coarse correction DAC (CDAC) is located before PGA gain stage, and a fine correction DAC (FDAC) is located after the gain stage. The digital-calibration system is capable of correcting the optical black and channel offset down to one ADC LSB accuracy.

The TLV990-40 automatically starts autocalibration whenever the $\overline{\text{OBCLP}}$ input is pulled low. The $\overline{\text{OBCLP}}$ pulse should be wide enough to cover one positive half cycle of the ADCCLK, as shown in Figure 1.

For each line, the optical black pixels plus the channel offset are sampled and converted to digital data by the ADC. A digital circuit averages the data during the optical black pixels. The averaged result is compared digitally with the desired output code stored in the Vb register (default is 40H), then the FDAC is adjusted by control logic to make the ADC output equal to the Vb. If the offset is out of the range of the FDAC (±225 ADC LSBs), the error is corrected by both the CDAC and the FDAC. The CDAC increments or decrements by one CDAC LSB, depending on whether the offset is negative of positive, until the output is within the range of the FDAC. The remaining residue is corrected by the FDAC.

The relationship among the FDAC, CDAC, and ADC in terms of number of ADC LSBs is as follows:

1 FDAC LSB = 1 ADC LSB,

1 CDAC LSB = PGA linear gain $\times$ n ADC LSB

where n is:

4 for $0 \leq$ gain code $< 64$
1.5 for $64 \leq$ gain code $< 96$
1 for $96 \leq$ gain code $< 128$
1 for $128 \leq$ gain code

For example, if PGA gain = 2 (6 dB), then, 1 CDAC LSB = 2 x 4 ADC LSBs = 8 ADC LSBs.

After autocalibration is complete, the ADC's digital output during CCD signal interval can be expressed by the following equation:

ADC output [D9−D0] = CCD_input $\times$ PGA gain + Vb,

Where Vb is the desired black level selected by user. The total offset, including optical black offset, is calibrated to be equal to the Vb by adjusting the offset correction DACs during autocalibration.

A weighted rolling average of the optical black pixels is taken during averaging. The weighting factor can be programmed in control register2. The weighting factor determines the speed of convergence of the digital filtering implemented within the CCD signal processor. Weighting factors closer to 1 result in faster convergence. As the weighting factor decreases towards its minimum value of 1/128, the speed of convergence of the digital filtering decreases.

The algorithm also takes *hot pixels* and *cold pixels* into consideration. A hot optical black pixel is a defective pixel that generates too much charge, while a cold pixel is the one that generates very little or no charge. A digital comparator compares the digitized optical black pixels with user-selected hot and cold pixel limits. If the optical black pixel value is out of range, then that *hot* or *cold pixel* is replaced with the value of the previous pixel.

## PRINCIPLES OF OPERATION

### automatic optical black and offset correction (continued)

Due to different exposure times, there might be a sudden optical black level shift at the start of each frame. Thus, a quick optical black level correction is desirable. The user can set an internal control bit (the SOF bit in control register2) to automatically disable the hot/cold pixel limits and to set the digital filtering weighting factor to 1 (equivalent to one-line averaging). In this way the optical black correction could be performed very quickly for the first line of each frame.

The number of black pixels in each line is programmable. The number of black pixels per line that can be averaged is $2^N$, where N can be any integer from 0 to 6.

The autocalibration feature can be bypassed if the user prefers to directly program the offset DAC registers. Switching the autocalibration mode to the direct-programming mode requires two register writes. First, the control bits for the offset DACs in the control register must be changed, then the desired offset value for the register is loaded to the offset DAC registers for proper error correction. If the total offset, including optical black level is less than ±255 ADC LSBs, only the FDAC needs to be programmed. When switching from direct-programming mode to autocalibration mode, the previous DAC register values, rather than default DAC register values, are used as starting offsets.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TLV990-40PFB | NRND | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TLV990-40PFBG4 | NRND | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

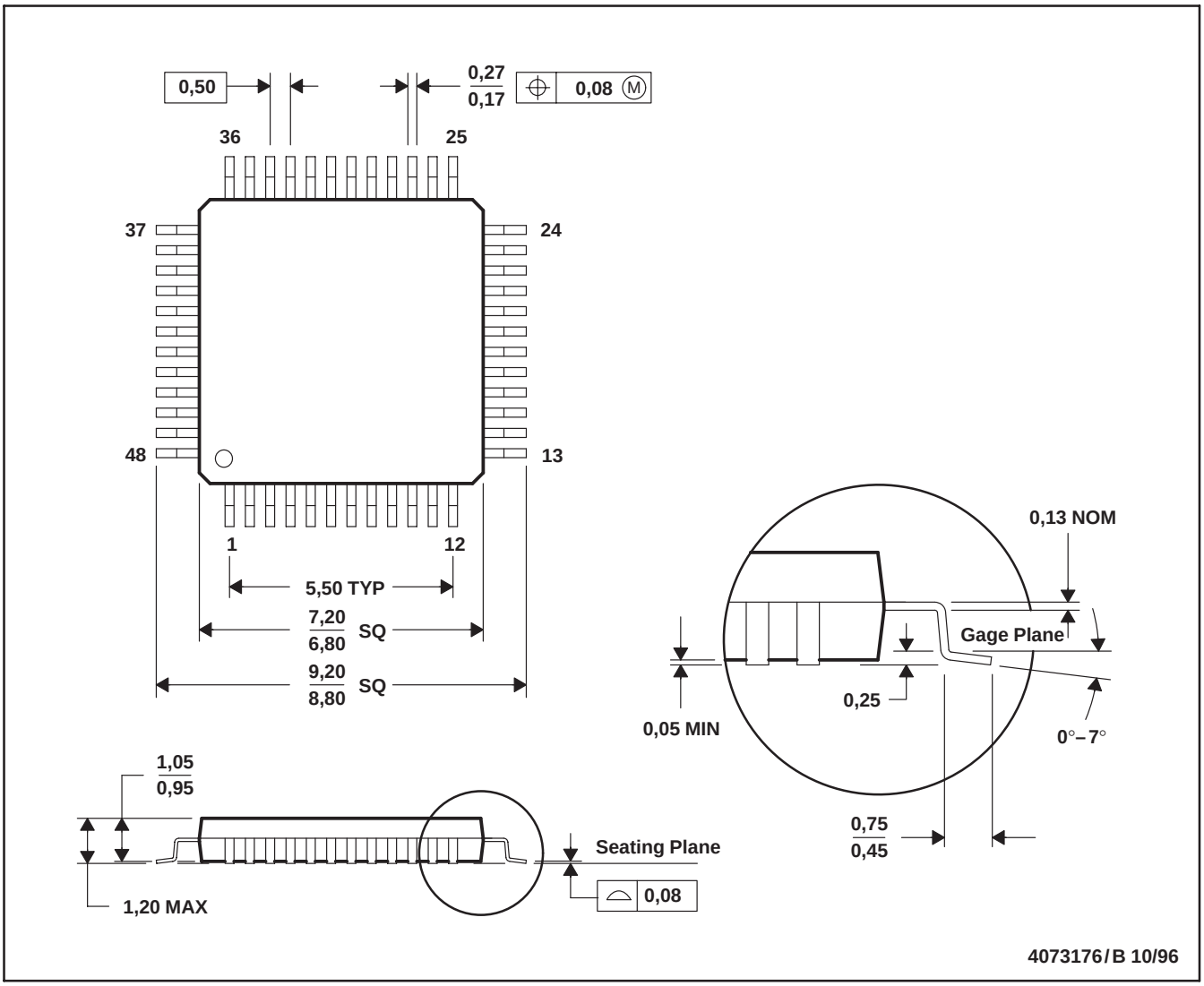
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

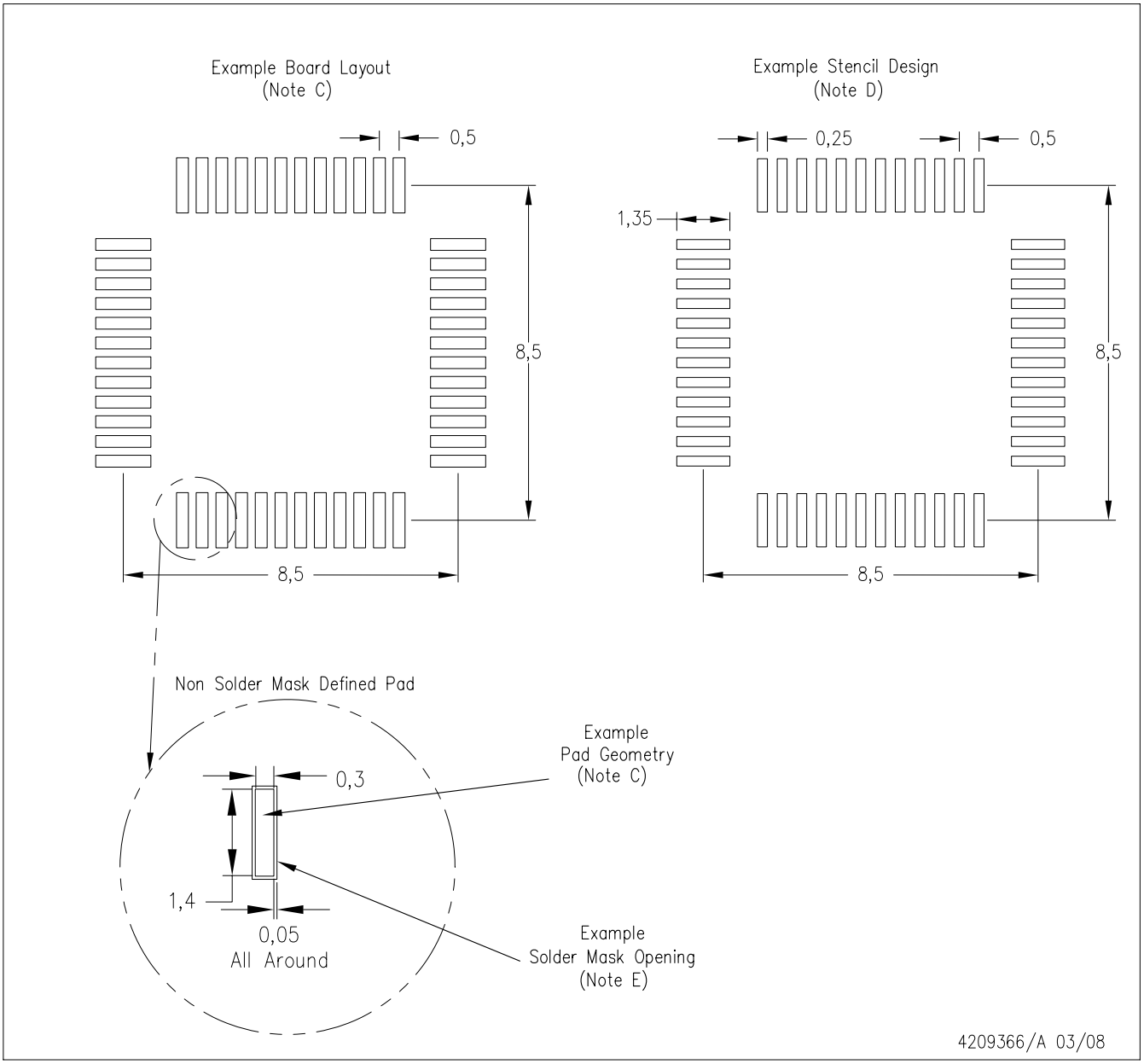
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

**PFB (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV990-40PFB | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -20 to 75 | TLV990-40 | Samples |

(1) The marketing status values are defined as follows:
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**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

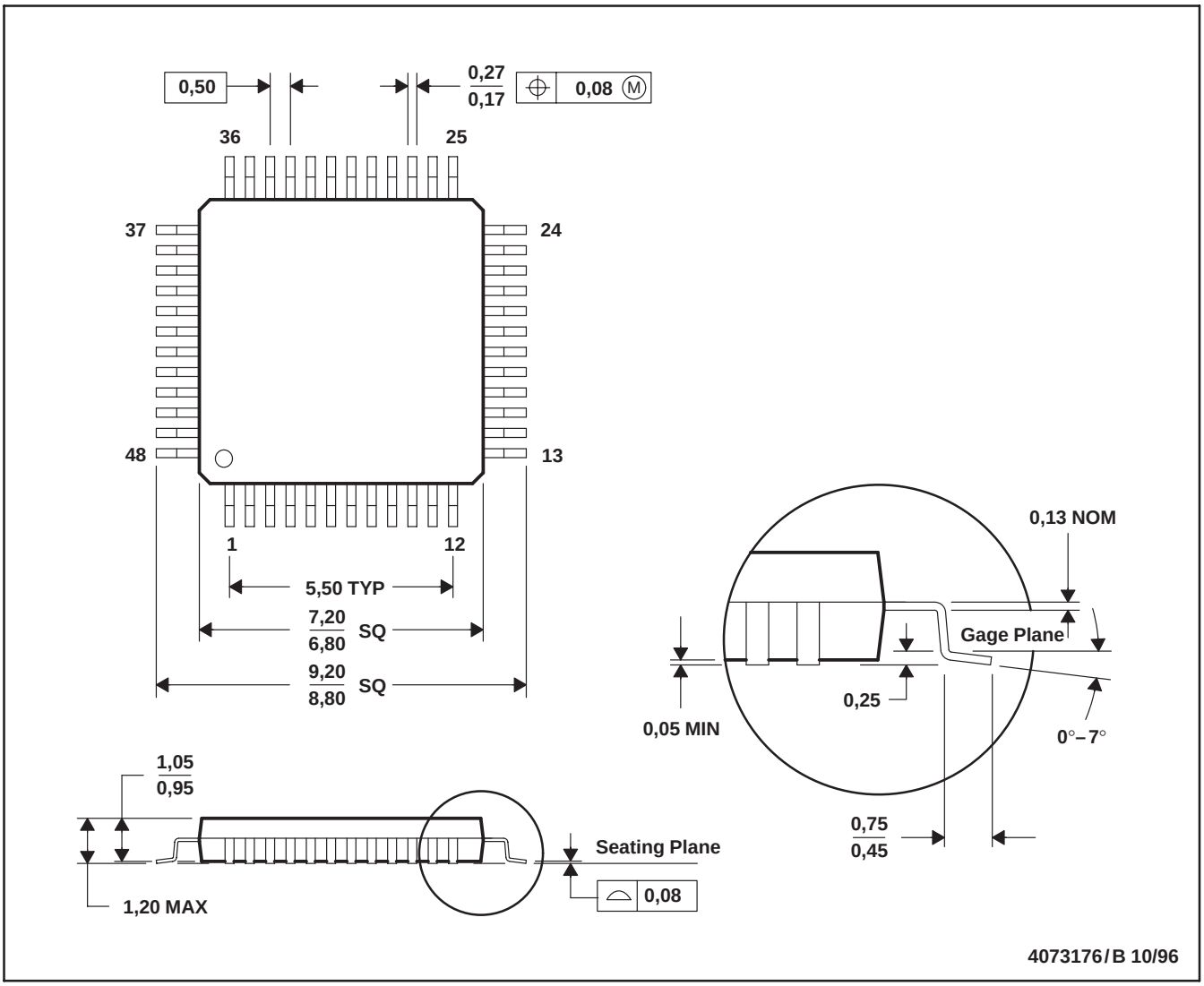
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

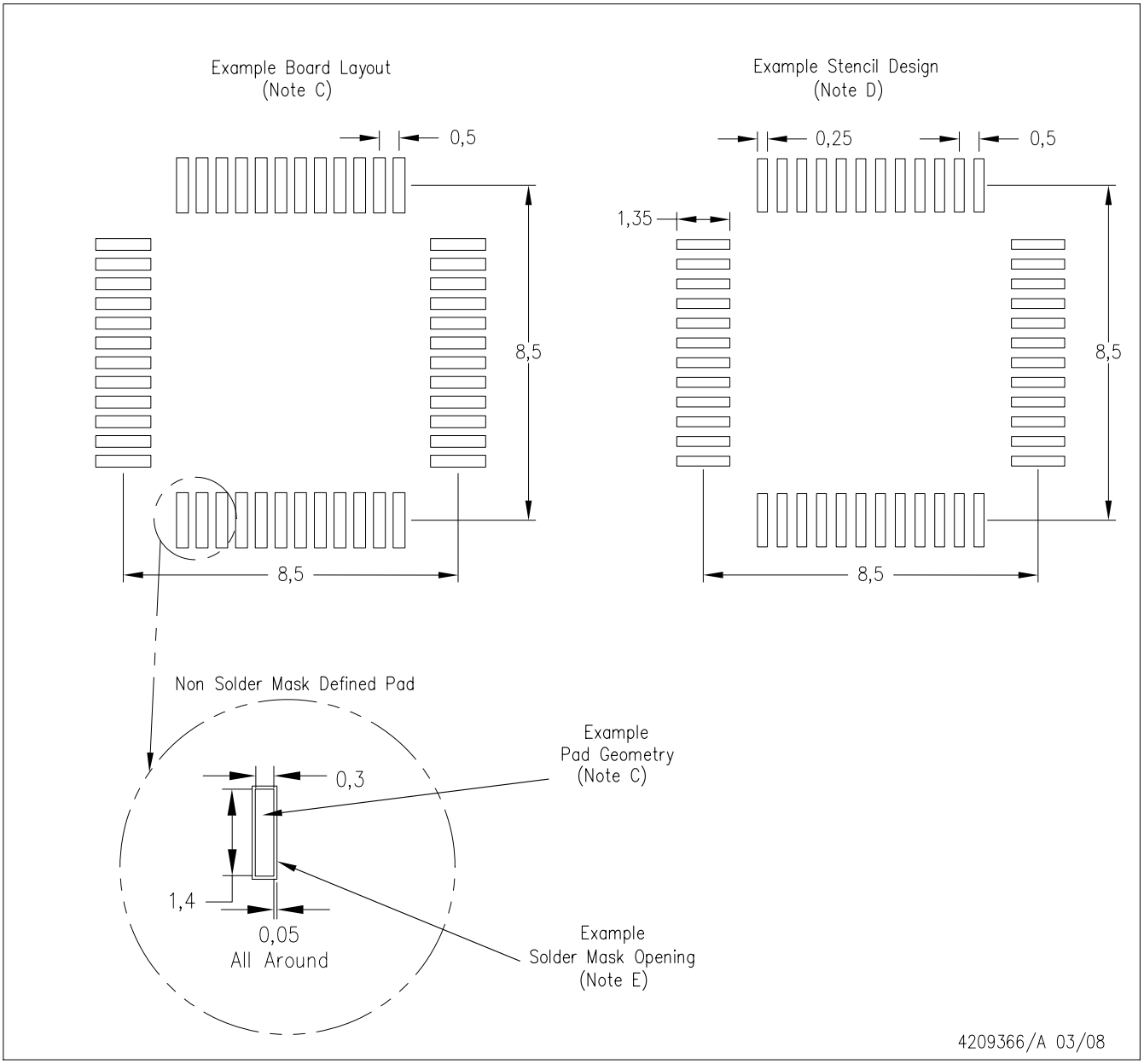
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

**PFB (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)

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