DAC31x1EVM User Guide

This document is intended to serve as a basic user's guide for the DAC31x1 EVM. The EVM provides a basic platform to evaluate the DAC31x1, which is a 500 MSPS, high speed digital-to-analog converter. The DAC3171 is a single-channel DAC with 14-bit LVDS input. The DAC3171 is pin compatible with the single-channel, 12- and 10-bit, 500 MSPS digital-to-analog converter, DAC3161 and DAC3151. The DAC3174EVM GUI is used for the DAC31x1EVM.

The EVM includes the CDCE62005 clocking source which provides the clocks required for the DAC and the pattern generator. This EVM is ideally suited for mating with the TSW1400 pattern generation card for evaluating WCDMA, LTE, or other high performance modulation schemes.

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1 EVM Block Diagram

Figure 1 shows the configuration of the EVM with the TSW1400 used for the pattern generation.

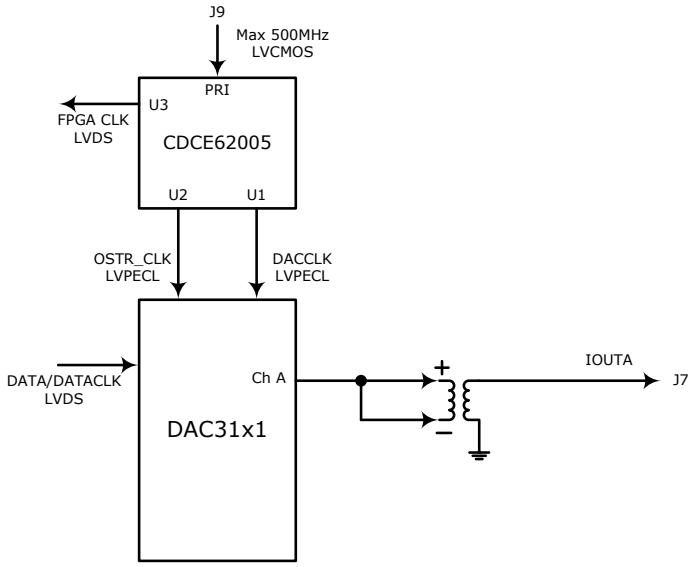


Figure 1. EVM Block Diagram

2 Software Control

2.1 Installation Instructions

The following steps ensure proper installation of the DAC3174 software:

- Open the folder named *DAC3174_Installer_vxpx* (xpx represents the latest version)
- Run Setup.exe
- Follow the on-screen instructions
- Once installed, launch by clicking on the DAC3174_GUI_vxpx program in Start → Texas Instruments DACs
- When plugging in the USB cable for the first time, you are prompted to install the USB drivers
  - When a pop-up screen opens, select *Continue Downloading*.
  - Follow the on-screen instructions to install the USB drivers
  - If needed, you can access the drivers directly in the install directory

2.2 Software Operation

The software allows programming control of the DAC device and the CDCE device. The front panel provides a tab for full programming of each device. The GUI tabs provides more convenient and simplified interface to the most-used registers of each device.

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2.2.1 Input Control Options

Figure 2 illustrates the input control options.

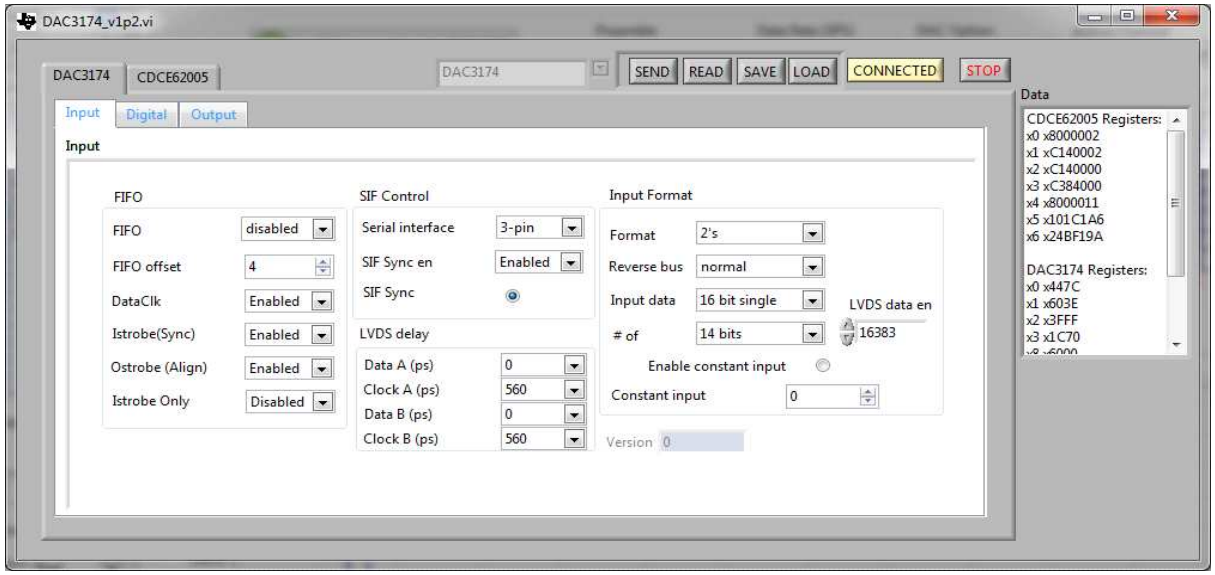


Figure 2. Input Control Options

- **FIFO:** Allows the configuration of the FIFO and FIFO sync sources
- **SIF Control:** Provides control of the Serial Interface (3-wires or 4-wires) and Serial Interface Sync (SIF Sync)
- **LVDS Delay:** Provides internal delay of either the LVDS data or LVDS data clock to help meet the input setup and input hold time
- **Input Format:** Provides control of the input data format (that is, 2's complement or offset binary)

2.2.2 Digital Block Options

Figure 3 illustrates the digital block options.

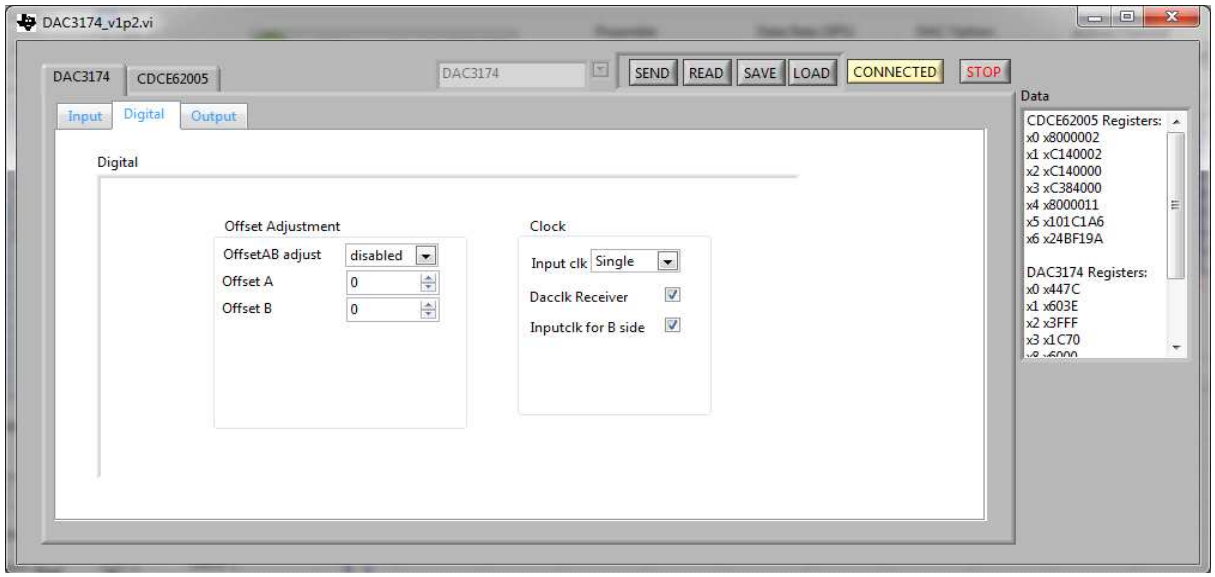


Figure 3. Digital Block Options

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- **Clock Receiver Sleep:** Allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- **Offset Adjustment:** Allows adjustment of the DC offset to minimize the LO feedthrough of the modulator output. Writing the register for Offset B generates an autosync in the QMC OFFSET block.

2.2.3 Output Control Options

Figure 4 illustrates the output control options.

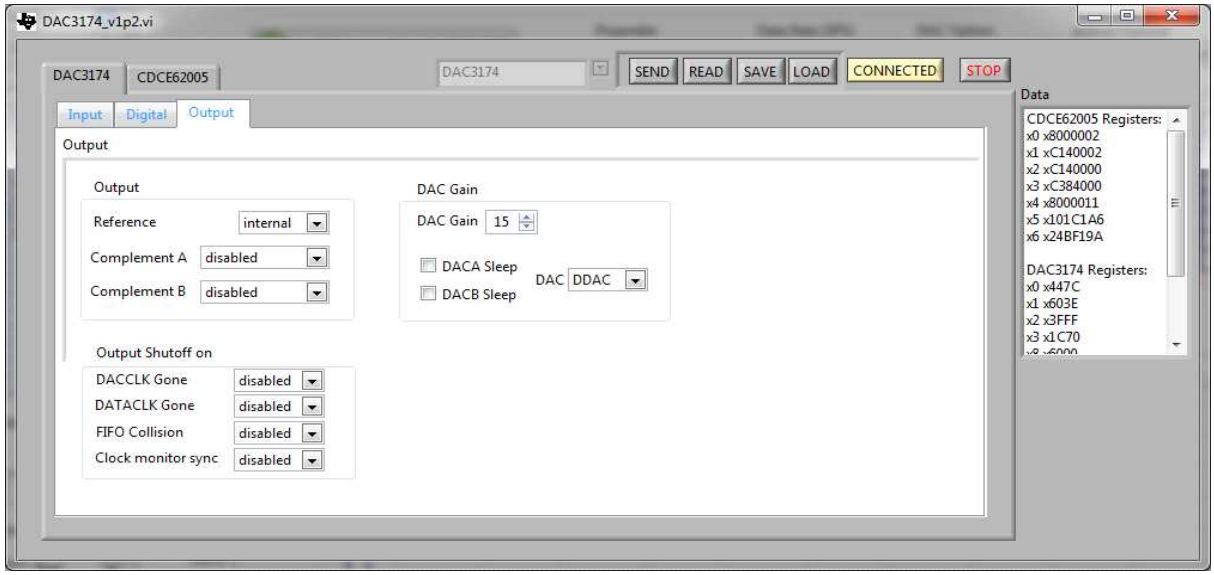


Figure 4. Output Control Options

- **Output:** Allows the configuration of reference, output polarity, and output delay
- **DAC Gain:** Configures the full-scale DAC current and DAC31x1 mode
  - DAC Gain = 15 for 20 mA full-scale current
  - DAC31x1 = DDAC
- **Output Shutoff On:** Allows outputs to shut-off when an alarm event occurs

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2.2.4 CDCE62005

Figure 5 shows the CDCE62005 tab, configured for the DAC31x1.

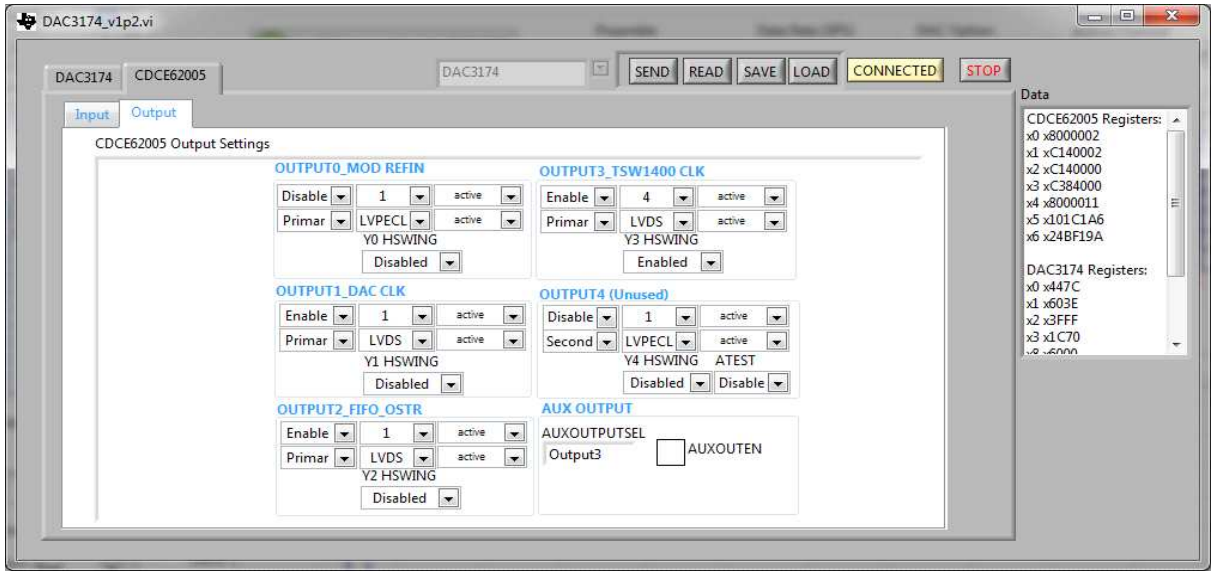


Figure 5. CDCE62005 Tab Configured for DAC31x1

Clock frequency control is determined by register values in the *CDCE62005* tab. Please refer to the CDCE62005 datasheet (SCAS862) for detailed explanations of the register configuration to change the clock frequency.

The following CDCE62005 outputs are critical to proper operation of the DAC31x1:

1. OUTPUT1_DAC_CLK: DAC31x1 Sampling clock.
2. OUTPUT3_TSW1400_CLK: TSW1400 FPGA clock.

To configure the CDCE62005 registers, open the DAC3174 GUI, click the **Load** button and open the file "dac3174_reg.txt" file. This should automatically configure the CDCE62005 registers.

2.2.5 Register Control

- **Send:** Sends the register configuration to all devices
- **Read:** Reads the register configuration from the DAC31x1 device
- **Load:** Load a register file for all devices. Sample configuration files for common frequency plans are located in the install directory.
  - Select the **Load** button
  - Double click on the data folder
  - Double click on the desired register file
  - Click **Send All** to ensure all of the values are loaded properly
- **Save Regs:** Saves the register configuration for all devices

2.2.6 Miscellaneous Settings

- **Reset USB:** Toggle this button if the USB port is not responding. This generates a new USB handle address.
  Note: Reset the board and click the **Reset USB** button on the GUI after every power cycle.
- **Exit:** Stops the program

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3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

3.1 Test Block Diagram

The test set-up for general testing of the DAC31x1 with the TSW1400 pattern generation card is shown in Figure 6.

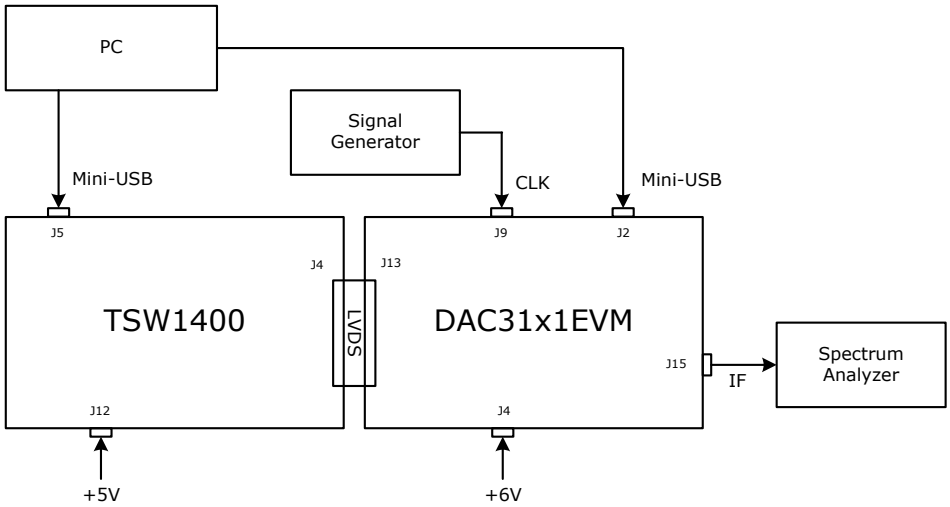


Figure 6. Test Setup Block Diagram

3.2 Test Set-up Connection

- TSW1400 Pattern Generator
  1. Connect a 5-V power supply to J12, the 5V_IN jack of the TSW1400 EVM.
  2. Connect the PC's USB port to J5, mini-USB port of the TSW1400.
- DAC31x1 EVM
  1. Connect the J13 connector of the DAC31x1 EVM to the J4 connector of the TSW1400 EVM.
  2. Connect 6 V to J3, the power in jack of the DAC31x1 EVM.
  3. Connect the PC's USB port to J2, the USB port of the DAC31x1 EVM. The cable should be a standard A to mini-B connector cable.
  4. Provide a 1.5 Vrms, 500-MHz max clock at J9, the CLKIN SMA port of the DAC31x1 EVM.
  5. Connect the RF output port of J15 to the spectrum analyzer.

3.3 TSW1400 Quick Start Operation

Please reference the TSW1400 user's guide (SLWU079) for more detailed explanations of the TSW1400 set-up and operation. This document assumes the TSW1400 software is installed and functioning properly.

Two-tone test configuration from High Speed Data Converter Pro:

- Enter *Tone BW*. 5M for two-tone case means tone-spacing. For single-tone, *Tone BW* can be '1'
- Enter desired number of tones
- Select *Tone Center* for the baseband shifting
- Select *Tone selection*. For a complex pattern select *I/Q* and select *Real* for real pattern.
- Enter *Data Rate (SPS)* for the DAC sampling frequency
- Select *DAC Option* between *2's Complement* and *Offset binary*

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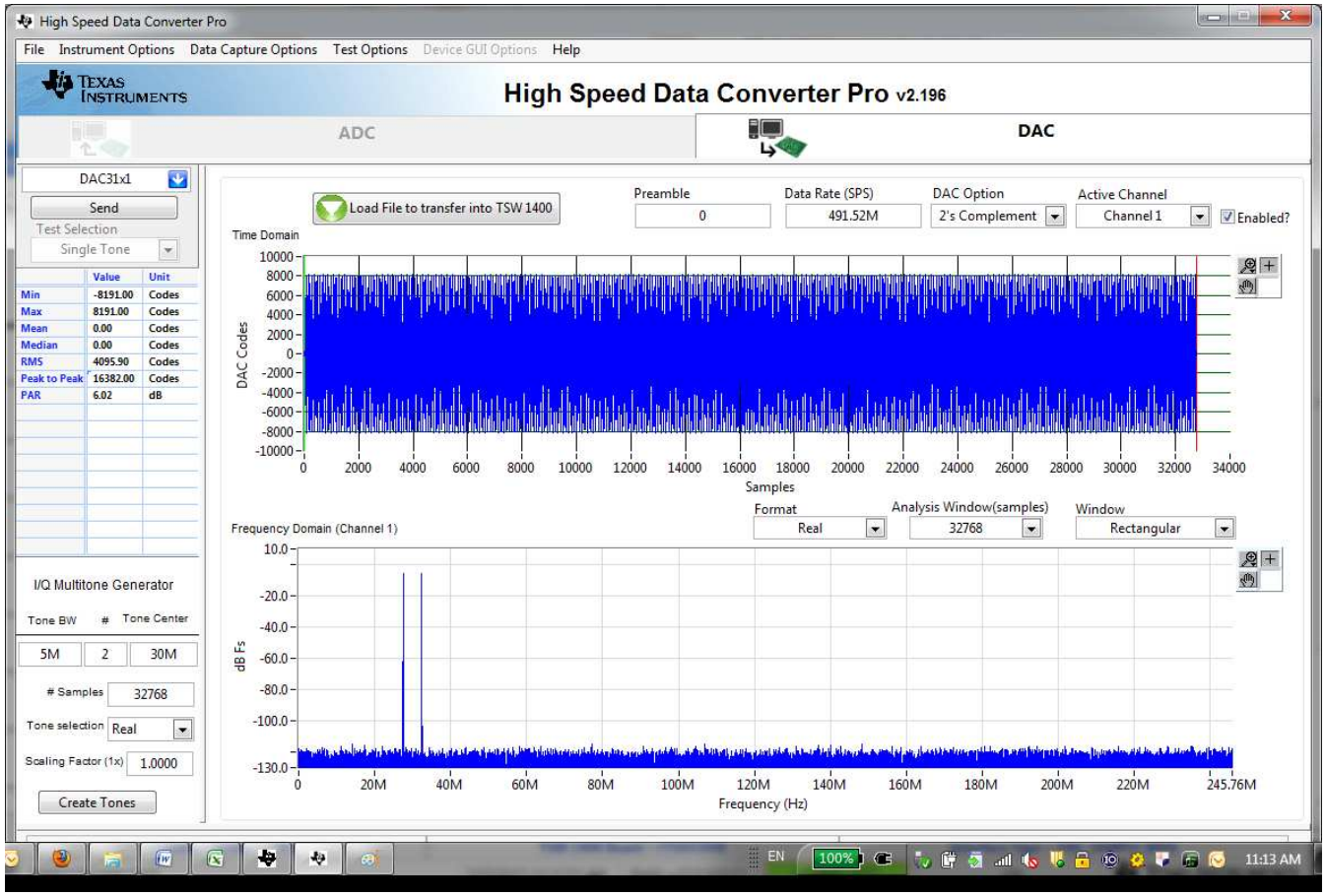


Figure 7. TSW1400 Two-Tone Programming GUI

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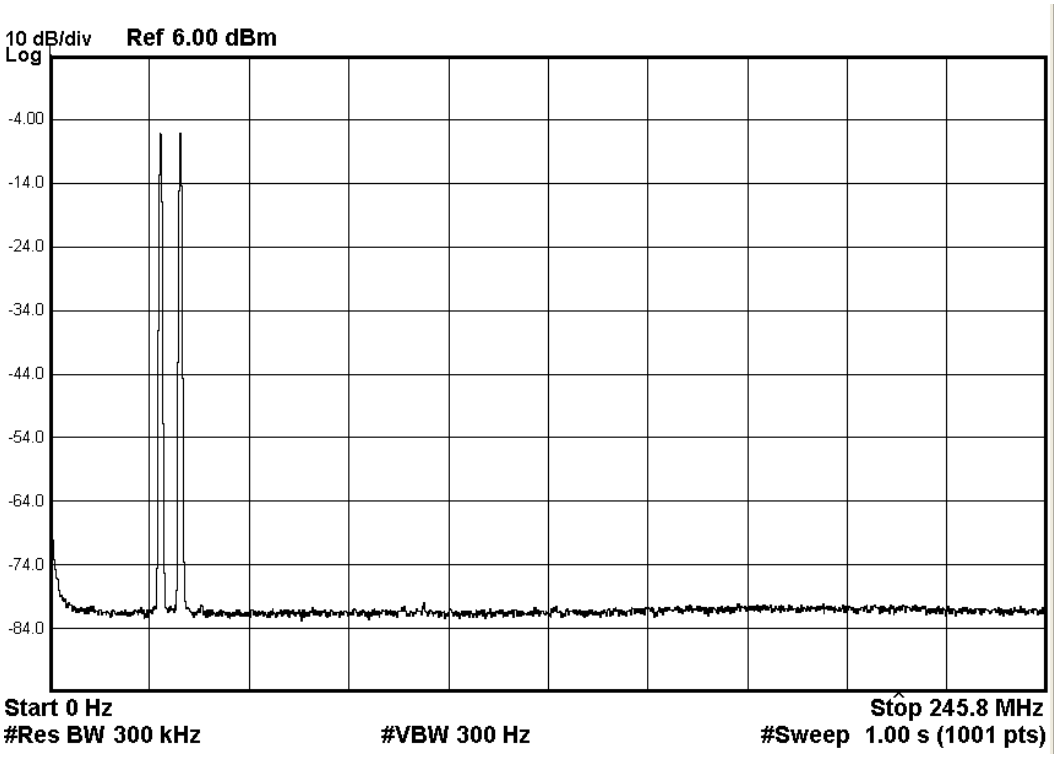


Figure 8. Captured Two-Tone from Spectrum Analyzer

3.4 DAC3174 Software Quick Start Guide

The following steps provide a quick start guide to the DAC3174 software:

- Provide the clock input 491.52 MHz at 1.5 Vrms at J9 SMA connector of the DAC31x1 EVM
- Turn on power to the board and press the reset button on the EVM
- Press the **Reset USB Port** button in the GUI and verify USB communication
- Switch to the *INPUT* tab of the GUI
- Press the *RESET* tab until the USB is CONNECTED
- Click **Load**, browse to the installation folder and load the example file “dac3174_reg.txt”. This file contains settings for DAC3174 running at 491.52 MSPS. Load this file and wait a couple of seconds for the settings to go into effect.
- Verify the spectrum using the spectrum analyzer at the IF outputs of the DAC EVM (J7)

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3.5 DAC3171 Output Performance for WCDMA

5 MHz of WCDMA signal is measured for Adjacent Channel Power Ratio (ACPR) performance, as shown in Figure 9. Measured ACPR shows –76.37 dB and –76.09 dB at the adjacent channel and –80.33 dB and –79.86 dB at the alternate channel.

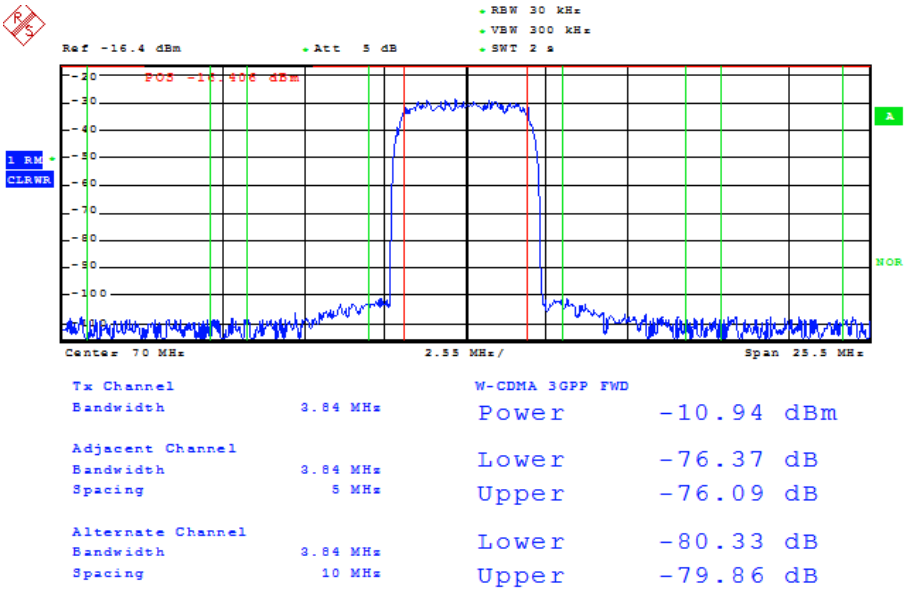


Figure 9. DAC3171 WCDMA 5-MHz Output (IF = 70 MHz)

20 MHz of WCDMA 4 carrier signal is measured for ACPR performance as shown in Figure 10. Measured ACPR shows –71.24 dB and –71.17 dB at the adjacent channel and –72.04 dB and –71.67 dB at the alternate channel.

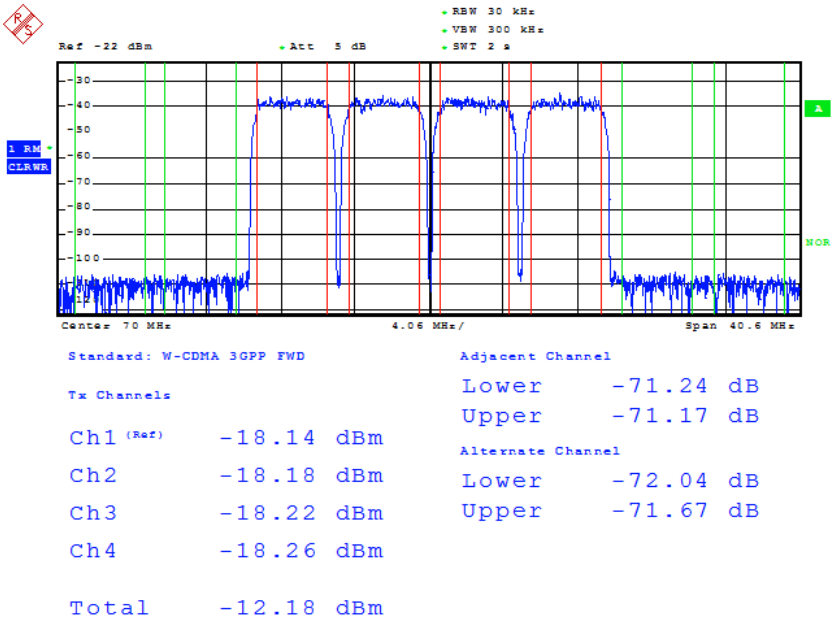


Figure 10. DAC3171 WCDMA 4 Carriers 20-MHz Output (IF = 70 MHz)

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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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