NSS30101LT1G

30 V, 2 A, Low $V_{CE(sat)}$ NPN Transistor

ON Semiconductor's e^2PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e^2PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	50	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	1.0	A
Collector Current − Peak	I_{CM}	2.0	A

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	310 2.5	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 1)	403	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	710 5.7	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 2)	176	°C/W
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{Dsingle}$	575	mW
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

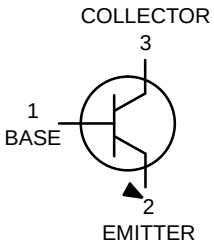
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

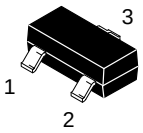
1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 X 1.0 inch Pad.

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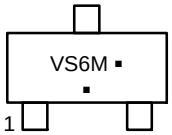
30 VOLTS
2.0 AMPS
NPN LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 100 mΩ





SOT−23 (TO−236)
CASE 318
STYLE 6

MARKING DIAGRAM



VS6 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NSS30101LT1G	SOT−23 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	−	Vdc
Collector−Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	50	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	−	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	−	0.1	μAdc
Collector−Emitter Cutoff Current (V_{CES} = 30 Vdc)	I_{CES}	−	0.1	μAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc)	I_{EBO}	−	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) (I_C = 50 mA, V_{CE} = 5.0 V) (I_C = 0.5 A, V_{CE} = 5.0 V) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	 300 300 200	 − 900 −	
Collector−Emitter Saturation Voltage (Note 3) (I_C = 1.0 A, I_B = 100 mA) (I_C = 0.5 A, I_B = 50 mA) (I_C = 0.1 A, I_B = 1.0 mA)	$V_{CE(sat)}$	 − − −	 0.200 0.125 0.075	V
Base−Emitter Saturation Voltage (Note 3) (I_C = 1.0 A, I_B = 0.1 A)	$V_{BE(sat)}$	−	1.1	V
Base−Emitter Turn−on Voltage (Note 3) (I_C = 1.0 mA, V_{CE} = 2.0 V)	$V_{BE(on)}$	−	1.1	V
Cutoff Frequency (I_C = 100 mA, V_{CE} = 5.0 V, f = 100 MHz	f_T	100	−	MHz
Output Capacitance (f = 1.0 MHz)	C_{obo}	−	15	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

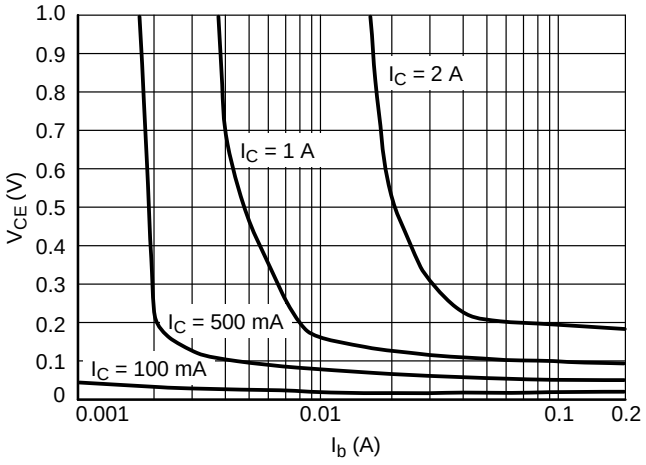


Figure 1. V_{CE} versus I_b

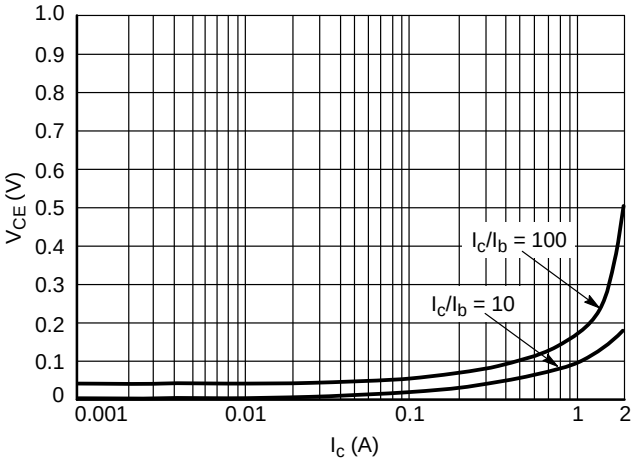


Figure 2. V_{CE} versus I_c

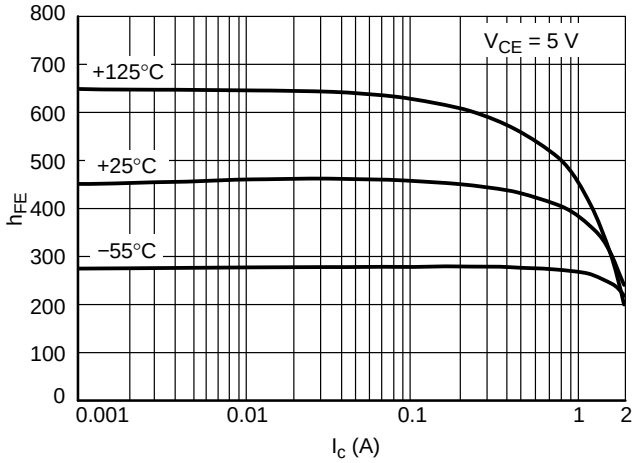


Figure 3. h_{FE} versus I_C

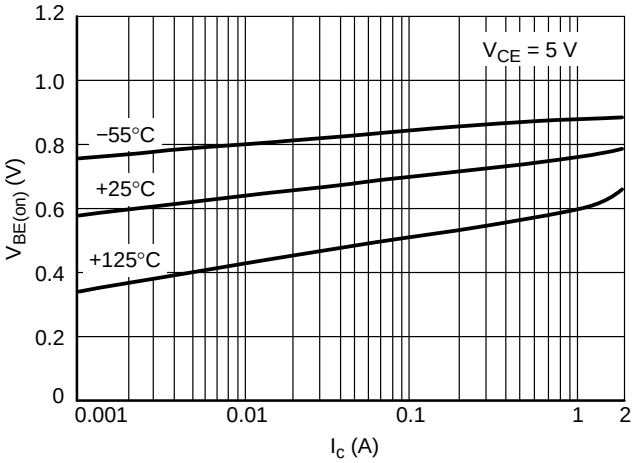


Figure 4. $V_{BE(on)}$ versus I_C

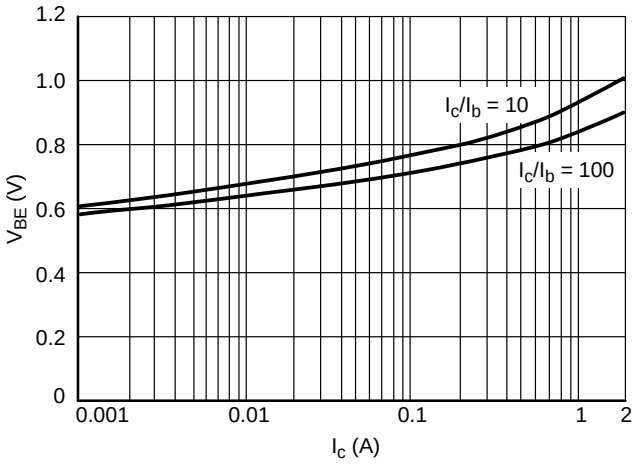


Figure 5. $V_{BE(sat)}$ versus I_C

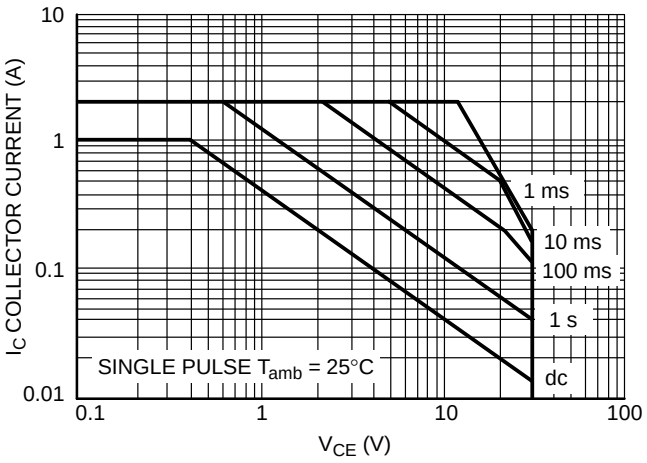


Figure 6. Safe Operating Area

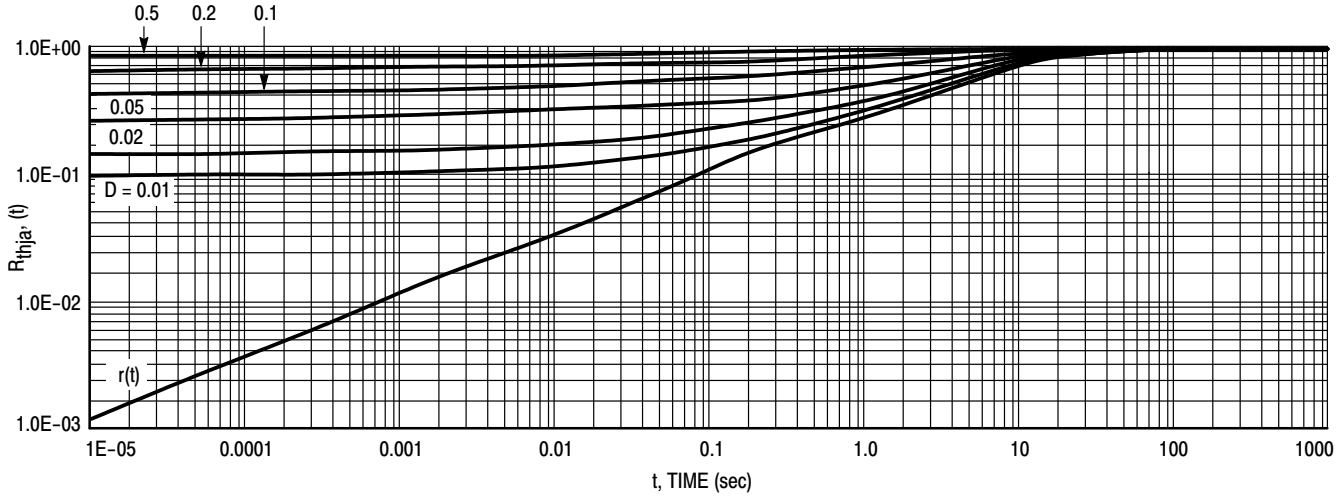
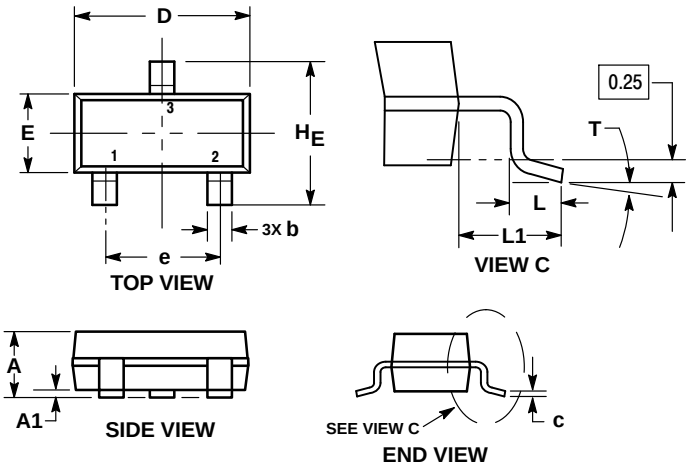


Figure 7. Normalized Thermal Response

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AR

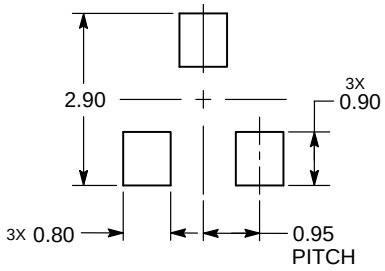


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	−−−	10°	0°	−−−	10°

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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