bq24640 High-Efficiency Synchronous Switched-Mode Super Capacitor Charger

1 Features

- Charge Super Capacitor Pack From 2.1 V to 26 V
- CC/CV Charge Profile From 0 V Without Precharge
- 600-kHz NMOS-NMOS Synchronous Buck Controller
- Over 90% Efficiency for up to 10-A Charge Current
- 5-V to 28-V VCC Input Voltage Range
- Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±3% Charge Current Regulation
- High Integration
  - Internal Loop Compensation
  - Internal Digital Soft Start
- Safety
  - Input Overvoltage Protection
  - Capacitor Temperature Sensing Hot and Cold Charge Suspend
  - Thermal Shutdown
- Status Outputs
  - Adapter Present
  - Charger Operation Status
- Charge Enable Pin
- 30-ns Driver Dead Time and 99.5% Maximum Effective Duty Cycle
- Automatic Sleep Mode for Low Power Consumption
  - <15-µA Off-State Super Capacitor Discharge Current
  - <1.5-mA Off-State Input Quiescent Current

2 Applications

- Memory Backup Systems
- Industrial UPS Systems and Power Transient Buffering
- Bridge Power to Buffer the Battery

3 Description

The bq24640 device is a highly integrated switched-mode super capacitor charge controller. The device offers a constant-frequency synchronous PWM controller with high accuracy charge current, voltage regulation, and charge status monitoring.

The bq24640 charges a super capacitor in two phases: constant current and constant voltage (CC/CV). The device can charge super capacitors from 0 V with current set on the ISET pin. When the super capacitor voltage reaches the programmed target voltage, charge current begins tapering down.

The bq24640 enters a low-current sleep mode (<15 µA) when the input voltage falls below the output capacitor voltage.

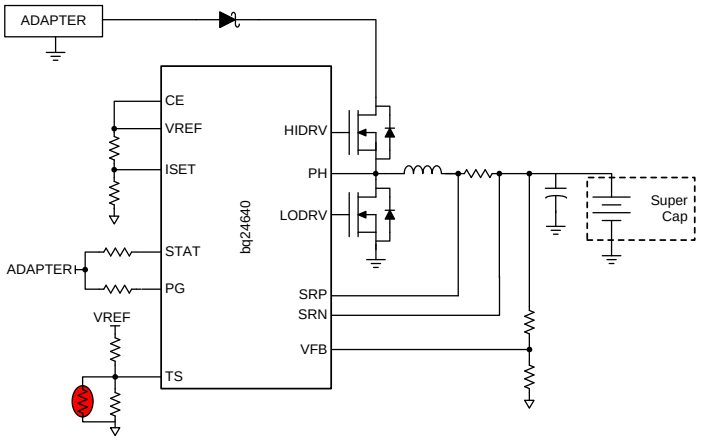
The bq24640 has an input CE pin to enable and disable charge, and the STAT and $\overline{PG}$ output pins report charge and adapter status. The TS pin on the bq24640 monitors the temperature of the capacitor and suspends charge during hot and cold conditions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24640	VQFN (16)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 8
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 12
7.4 Device Functional Modes ... 16
8 Application and Implementation ... 17
8.1 Application Information ... 17
8.2 Typical Application ... 17
9 Power Supply Recommendations ... 21
10 Layout ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Examples ... 22
11 Device and Documentation Support ... 23
11.1 Device Support ... 23
11.2 Documentation Support ... 23
11.3 Community Resources ... 23
11.4 Trademarks ... 23
11.5 Electrostatic Discharge Caution ... 23
11.6 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

4 Revision History

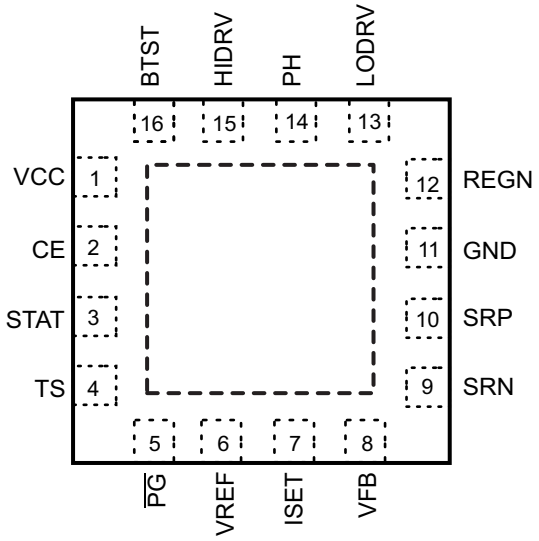
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2010) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Copyright © 2010–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

RVA Package
16-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BTST	16	P	PWM high-side driver positive supply. Connect the 0.1-µF bootstrap capacitor from PH to BTST.
CE	2	I	Charge enable, active HIGH logic input. HI enables charge, and LO disables charge. Connect to pullup rail with 10-kΩ resistor. It has an internal 1-MΩ pulldown resistor.
GND	11	P	Low-current sensitive analog/digital ground. On PCB layout, connect with thermal pad underneath the IC.
HIDRV	15	O	PWM high-side driver output. Connect to the gate of the high-side N-channel power MOSFET with a short trace.
ISET	7	I	Charge current set point. The voltage is set through a voltage divider from VREF to ISET and to GND. $I_{CHG} = \frac{V_{ISET}}{20 \times R_{SR}}$
LODRV	13	O	PWM low-side driver output. Connect to the gate of the low-side N-channel power MOSFET with a short trace.
$\overline{PG}$	5	O	Open-drain active-low adapter status output. Connect to pullup rail through LED and 10-kΩ resistor. The LED turns on when a valid is detected, and off in the sleep mode.
PH	14	P	Switching node, charge current output inductor connection. Connect the 0.1-µF bootstrap capacitor from PH to BTST.
REGN	12	P	PWM low-side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from REGN to GND pin close to the IC. Use for low-side driver and high-side driver bootstrap voltage by small signal Schottky diode from REGN to BTST.
SRN	9	I	Charge current-sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from SRN pin to GND for common-mode filtering.
SRP	10	P/I	Charge current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from SRP pin to GND for common-mode filtering.
STAT	3	O	Open-drain charge status output to indicate various charger operation. Connect to the pullup rail through the LED and 10-kΩ (see Table 4).
TS	4	I	Temperature qualification voltage input for negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor-divider from VREF to TS to GND. Recommend SEMITEC 103AT-2 10-kΩ thermister.

(1) P - Power, I - Input, O - Output

Copyright © 2010–2015, Texas Instruments Incorporated

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VCC	1	P	IC power positive supply. Connect through a 10-Ω resistor to the cathode of input diode. Place a 1-µF ceramic capacitor from VCC to GND and place it as close as possible to IC to filter out the noise.
VFB	8	I	Charge voltage analog feedback adjustment. Connect a resistor divider from output to VFB to GND to adjust the output voltage. The internal regulation limit is 2.1V.
VREF	6	P	3.3-V reference voltage output. Place a 1-µF ceramic capacitor from VREF to GND pin close to the IC. This voltage could be used for programming charge current regulation on ISET and for thermal threshold on TS. It can be used as the pullup rail of STAT, and $\overline{PG}$.
Thermal pad		—	Exposed pad beneath the IC. Always solder thermal pad to the board, and have vias on the thermal pad plane star-connecting to GND and ground plane for high-current power converter. It also serves as a thermal pad to dissipate the heat.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage (2)	VCC, SRP, SRN, STAT, $\overline{PG}$, CE	–0.3	33	V
	PH	–2	33	
	VFB(3)	–0.3	16	
	REGN, LODRV, TS	–0.3	7	
	BTST, HIDRV with respect to GND	–0.3	39	
	VREF, ISET	–0.3	3.6	
Maximum difference voltage	SRP–SRN	–0.5	0.5	V
Temperature	Junction, T_J	–40	155	°C
	Storage, T_{stg}	–55	155	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult the Package Option Addendum at the end of the data sheet for thermal limitations and considerations.
(3) Must have a series resistor between output to VFB if output voltage is expected to be greater than 16 V. Usually the resistor-divider top resistor will take care of this.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2010–2015, Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage (with respect to GND)	VCC, SRP, SRN, STAT, $\overline{PG}$, CE	–0.3	28	V
	PH	–2	30	
	VFB	–0.3	14	
	REGN, LODRV, TS	–0.3	6.5	
	BTST, HIDRV with respect to GND	–0.3	34	
	ISET	–0.3	3.3	
	VREF		3.3	
Maximum difference voltage	SRP–SRN	–0.2	0.2	V
Junction temperature, T_J		0	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq24640 RVA (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	81	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.77	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

5 V ≤ V(VCC) ≤ 28 V, 0°C < T < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{VCC_OP}	VCC input voltage operating range		5		28	V
QUIESCENT CURRENTS						
I_{OUT}	Total output discharge current (sum of currents into VCC, BTST, PH, SRP, SRN, VFB), VFB ≤ 2.1V	$V_{UVLO} < V_{VCC} < V_{SRN}$ (sleep mode)			15	µA
I_{AC}	Adapter supply current into VCC pin	$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{UVLO}$, CE = LOW		1	1.5	mA
		$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{VCCLOWV}$, CE = HIGH, charge done		2	5	
		$V_{VCC} > V_{SRN}$, $V_{VCC} > V_{VCCLOWV}$, CE = HIGH, Charging, Qg_total = 20 nC, V_{VCC} = 20 V		25		
CHARGE VOLTAGE REGULATION						
V_{FB}	Feedback regulation voltage			2.1		V
	Charge voltage regulation accuracy	T_J = 0°C to 85°C	–0.5%		0.5%	
		T_J = –40°C to 125°C	–0.7%		0.7%	
I_{VFB}	Leakage current into VFB pin	VFB = 2.1 V			100	nA

Copyright © 2010–2015, Texas Instruments Incorporated

Electrical Characteristics (continued)

5 V ≤ V(VCC) ≤ 28 V, 0°C < T < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT REGULATION						
V_{ISET1}	ISET voltage range				2	V
V_{IREG_CHG}	SRP-SRN current sense voltage range	$V_{IREG_CHG} = V_{SRP} - V_{SRN}$			100	mV
K_{ISET1}	Charge current set factor (amps of charge current per volt on ISET pin)	RSENSE = 10 mΩ		5		A/V
	Charge current regulation accuracy	V_{IREG_CHG} = 40 mV	–3%		3%	
		V_{IREG_CHG} = 20 mV	–5%		5%	
		V_{IREG_CHG} = 5 mV	–25%		25%	
		V_{IREG_CHG} = 1.5 mV	–50%		50%	
I_{ISET}	Leakage current into ISET pin	V_{ISET1} = 2 V			100	nA
INPUT UNDERVOLTAGE LOCKOUT COMPARATOR (UVLO)						
V_{UVLO}	AC undervoltage rising threshold	Measure on VCC	3.65	3.85	4	V
V_{UVLO_HYS}	AC undervoltage hysteresis, falling			350		mV
VCC LOWV COMPARATOR						
V_{LOWV_FALL}	Falling threshold, disable charge	Measure on VCC		4.1		V
V_{LOWV_RISE}	Rising threshold, resume charge			4.35	4.5	V
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
V_{SLEEP_FALL}	Sleep falling threshold	$V_{VCC} - V_{SRN}$ to enter sleep mdoe	40	100	150	mV
V_{SLEEP_HYS}	Sleep hysteresis			500		mV
	Sleep rising delay	VCC falling below SRN, Delay to pull up $\overline{PG}$		1		µs
	Sleep falling delay	VCC rising above SRN, Delay to pull down $\overline{PG}$		30		ms
	Sleep rising shutdown deglitch	VCC falling below SRN, Delay to enter sleep mode		100		ms
	Sleep falling powerup deglitch	VCC rising above SRN, Delay to exit sleep mode		30		ms
OUT OVERVOLTAGE COMPARATOR						
V_{OV_RISE}	Overvoltage rising threshold	As percentage of V_{VFB}		104%		
V_{OV_FALL}	Overvoltage falling threshold	As percentage of V_{VFB}		102%		
INPUT OVERVOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC overvoltage rising threshold	Measured on VCC	31	32	33	V
V_{ACOV_HYS}	AC overvoltage falling hysteresis			1		V
	AC overvoltage rising deglitch	Delay to disable charge		1		ms
	AC overvoltage falling deglitch	Delay to resume charge		1		ms
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature Increasing		145		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			15		°C
	Thermal shutdown rising deglitch	Temperature Increasing		100		µs
	Thermal shutdown falling deglitch	Temperature Decreasing		10		ms
THERMISTOR COMPARATOR						
V_{LTF}	Cold temperature rising threshold	As percentage to V_{VREF}	72.5%	73.5%	74.5%	
V_{LTF_HYS}	Rising hysteresis	As percentage to V_{VREF}	0.2%	0.4%	0.6%	
V_{HTF}	Hot temperature rising threshold	As percentage to V_{VREF}	36.4%	37%	37.6%	
V_{TCO}	Cutoff temperature rising threshold	As percentage to V_{VREF}	33.7%	34.4%	35.1%	
	Deglitch time for temperature out-of-range detection	$V_{TS} < V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		400		ms

Copyright © 2010–2015, Texas Instruments Incorporated

Electrical Characteristics (continued)

5 V ≤ V(VCC) ≤ 28 V, 0°C < T < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Deglitch time for temperature in-valid-range detection	$V_{TS} > V_{LTF} – V_{LTF_HYS}$ or $V_{TS} > V_{TCO}$, or $V_{TS} > V_{HTF}$		20		ms
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{OC}	Charge overcurrent rising threshold	Current rising, in nonsynchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} < 2 V		45.5		mV
		Current rising, as percentage of $V_{(IREG_CHG)}$, in synchronous mode, V_{SRP} > 2.2 V		160%		
	Charge overcurrent threshold floor	Minimum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2 V		50		mV
	Charge overcurrent threshold ceiling	Maximum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2 V		180		mV
CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
$V_{ISYNSET}$	Charge undercurrent falling threshold	Switch from CCM to DCM, V_{SRP} > 2.2 V	1	5	9	mV
LOW CHARGE CURRENT COMPARATOR						
V_{LC}	Low charge current (average) falling threshold to force into nonsynchronous mode	Measure $V_{(SRP-SRN)}$		1.25		mV
V_{LC_HYS}	Low charge current rising hysteresis			1.25		mV
V_{LC_DEG}	Deglitch on both edges			1		µs
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	$V_{VCC} > V_{UVLO}$ (0–35 mA load)	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, $V_{VCC} > V_{UVLO}$	35			mA
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{VCC} > 10 V, CE = HIGH (0–40 mA load)	5.7	6	6.3	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0 V, $V_{VCC} > V_{UVLO}$, CE = HIGH	40			mA
PWM HIGH-SIDE DRIVER (HIDRV)						
$R_{DS_HI_ON}$	High-side driver (HSD) turnon resistance	$V_{BTST} – V_{PH}$ = 5.5 V		3.3	6	Ω
$R_{DS_HI_OFF}$	High-side driver turnoff resistance	$V_{BTST} – V_{PH}$ = 5.5 V		1	1.3	Ω
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold voltage	VBTST – VPH when low side refresh pulse is requested	4	4.2		V
PWM LOW-SIDE DRIVER (LODRV)						
$R_{DS_LO_ON}$	Low-side driver (LSD) turnon resistance			4.1	7	Ω
$R_{DS_LO_OFF}$	Low-side driver turnoff resistance			1	1.4	Ω
PWM DRIVERS TIMING						
	Driver Dead-Time	Dead time when switching between LSD and HSD, no load at LSD and HSD		30		ns
PWM OSCILLATOR						
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of VCC		7%		
	PWM switching frequency		510	600	690	kHz
INTERNAL SOFT START (8 STEPS TO REGULATION CURRENT ICHG)						
	Soft start steps			8		step
	Soft start step time			1.6		ms

Copyright © 2010–2015, Texas Instruments Incorporated

Electrical Characteristics (continued)

5 V ≤ V(VCC) ≤ 28 V, 0°C < T < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC IO PIN CHARACTERISTICS (CE, STAT, $\overline{PG}$)						
V_{IN_LO}	CE input low threshold voltage				0.8	V
V_{IN_HI}	CE input high threshold voltage		2.1			V
V_{BIAS_CE}	CE input bias current	V_{CE} = 3.3 nV (CE has internal 1-MΩ pulldown resistor)			6	µA
V_{OUT_LO}	STAT, $\overline{PG}$ output low saturation voltage	Sink current = 5 mA			0.5	V
I_{OUT_HI}	Leakage current	V = 32 V			1.2	µA

6.6 Typical Characteristics

Table 1. Table of Graphs

	FIGURES
Power Up (VREF, REGN, $\overline{PG}$)	Figure 1
Charge Enable and Disable	Figure 2
Current Soft Start (CE = HIGH)	Figure 3
Continuous Conduction Mode Switching Waveform	Figure 5
Discontinuous Conduction Mode Switching Waveform	Figure 6
Charge Profile	Figure 7

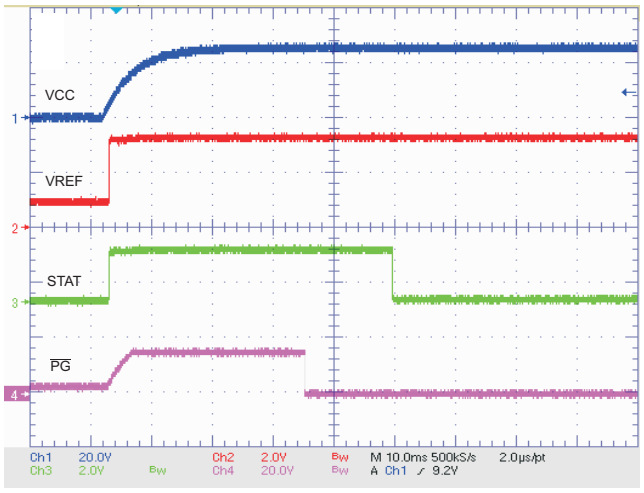


Figure 1. Power Up

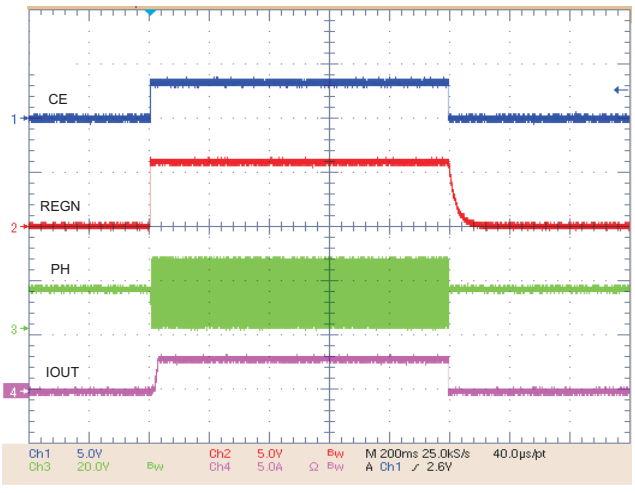


Figure 2. Charge Enable and Disable

Copyright © 2010–2015, Texas Instruments Incorporated

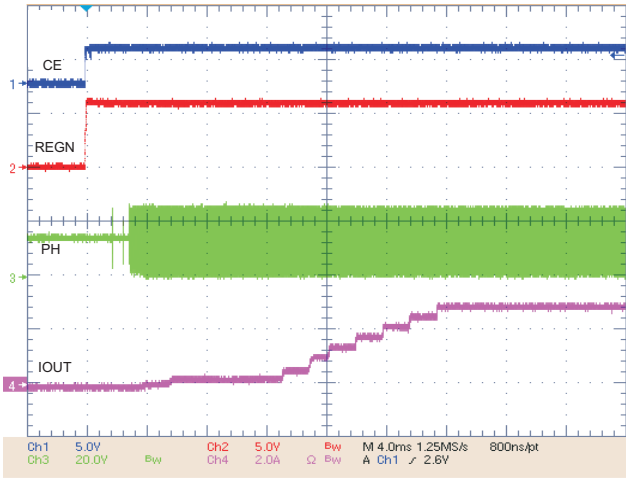


Figure 3. Current Soft Start (CE = HIGH)

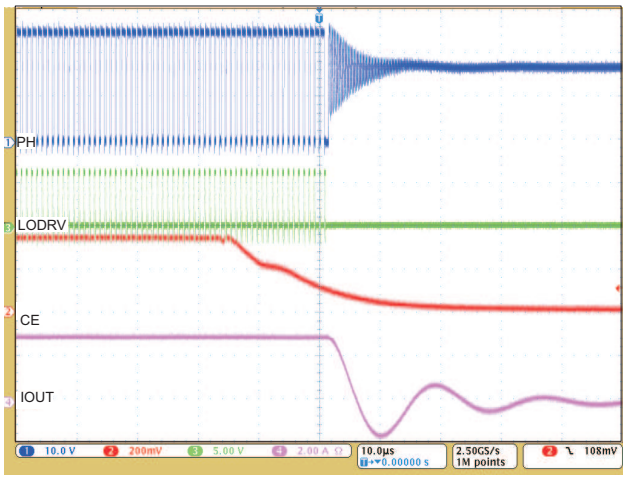


Figure 4. Charge Stops on CE LOW

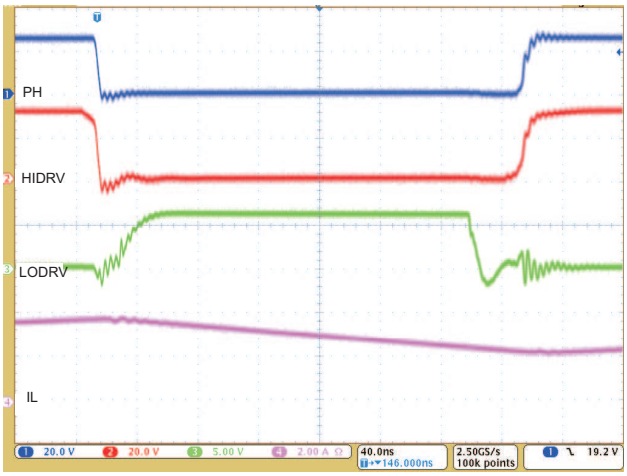


Figure 5. Continuous Conduction Mode

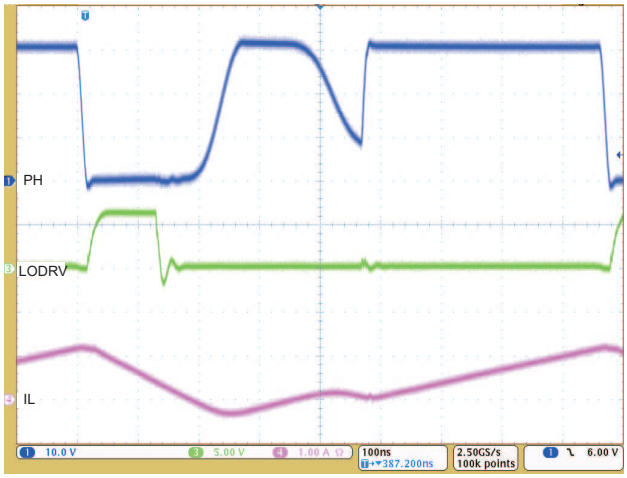


Figure 6. Discontinuous Conduction Mode

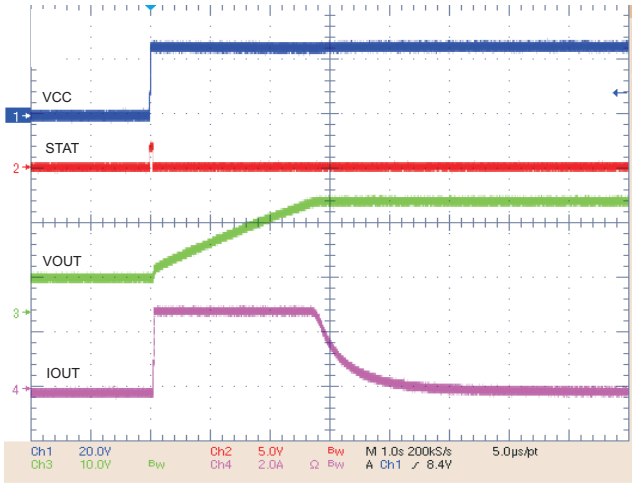


Figure 7. Charge Profile

7 Detailed Description

7.1 Overview

The bq24640 device is a stand-alone, integrated super capacitor charger. The device employs a switched-mode synchronous buck PWM controller with constant switching frequency.

Charging begins in one of two phases (depending upon super capacitor voltage): constant current (fast-charge current regulation), and constant voltage (fast-charge voltage regulation). Constant current can be configured through the ISET pin, allowing for flexibility in the super capacitor charging profile. During charging, the integrated fault monitors of the device, such as output overvoltage protection (V_{OV_RISE}), thermal shutdown (internal T_{SHUT} and TS pin), and input voltage protection (V_{ACOV} and V_{UVLO}), ensure super capacitor safety.

The bq24640 has two status pins (STAT and $\overline{PG}$) to indicate the charging status and input voltage (AC adapter) status. These pins can be used to drive LEDs or communicate with a host processor.

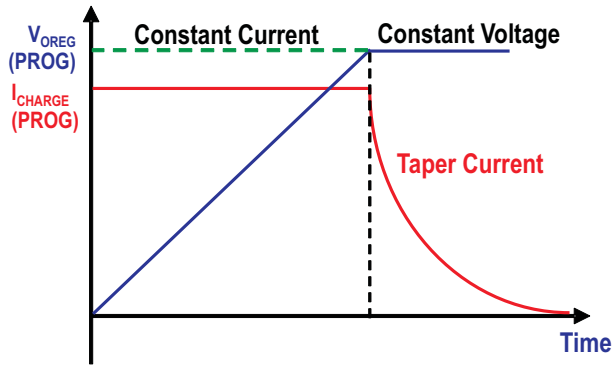
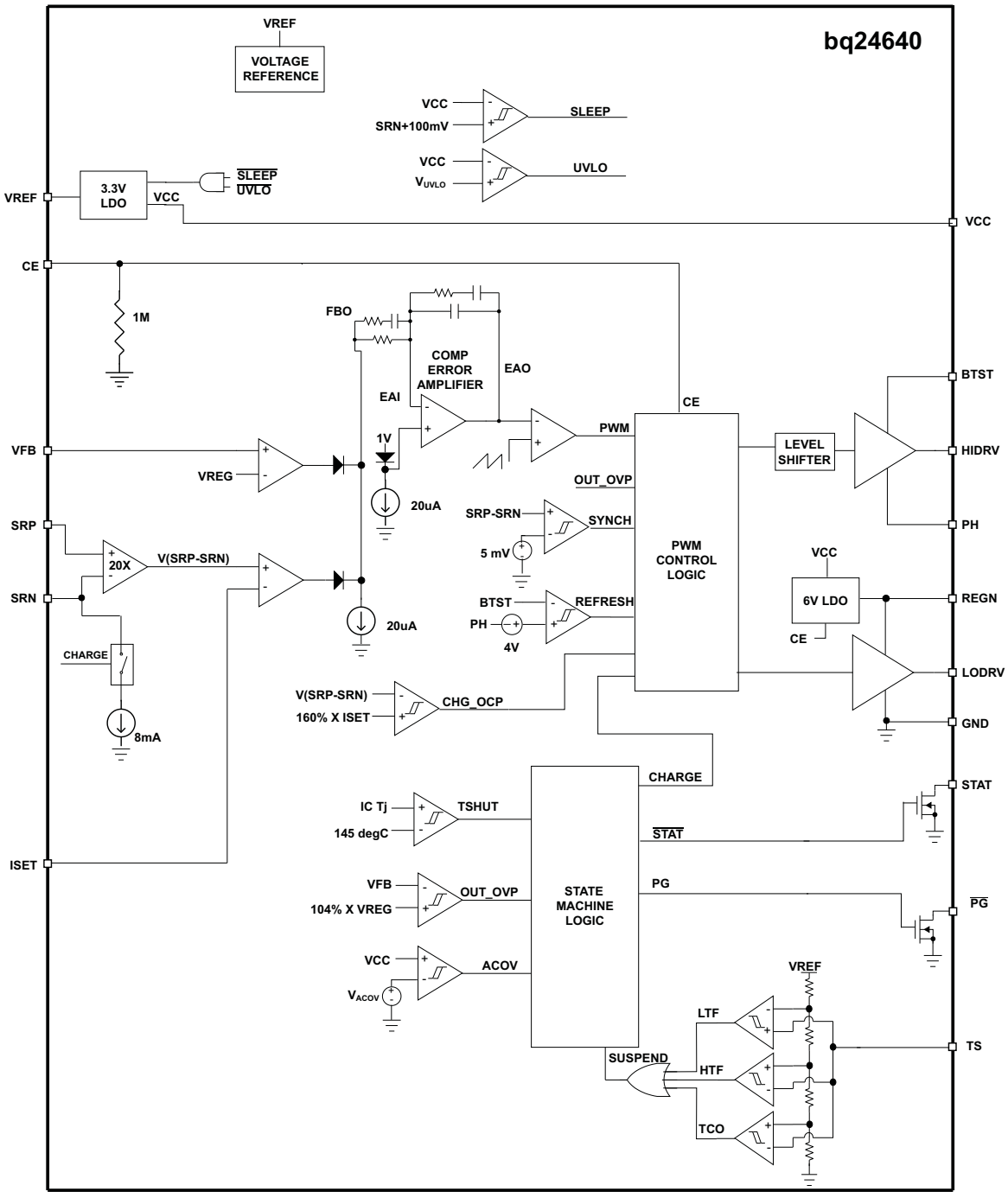


Figure 8. Typical Charging Profile

Copyright © 2010–2015, Texas Instruments Incorporated

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage Regulation

The bq24640 uses a high-accuracy voltage regulator for the charging voltage. The charge voltage is programmed through a resistor-divider from the output to ground, with the midpoint tied to the VFB pin. The voltage at the VFB pin is regulated to 2.1 V, giving Equation 1 for the regulation voltage:

$$V_{OUT} = 2.1V \times \left[1 + \frac{R2}{R1}\right] \quad (1)$$

where

- R2 is connected from VFB to the output, and R1 is connected from VFB to GND.

7.3.2 Output Current Regulation

The ISET input sets the maximum charging current. Output current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 100 mV. Thus, for a 10-mΩ sense resistor, the maximum charging current is 10 A. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET}}{20 \times R_{SR}} \quad (2)$$

The input voltage range of ISET is from 0 V to 2 V. The SRP and SRN pins are used to sense voltage across R_{SR} with default value of 10 mΩ. However, resistors of other values can also be used. A larger sense resistor will give a larger sense voltage and a higher regulation accuracy, but this comes at the expense of higher conduction loss.

7.3.3 Power Up

The bq24640 uses a sleep comparator to determine if the source of power on the VCC pin is a valid supply to charge the capacitor. If the VCC voltage is above the UVLO threshold and greater than the SRN voltage, and all other conditions are met, bq24640 will then start to charge (see *Enable and Disable Charging*). If the SRN voltage is greater than VCC, the bq24640 enters a low quiescent current sleep mode to minimize current drain from the capacitor (<15 µA).

If VCC is below the UVLO threshold, the device is disabled.

7.3.4 Enable and Disable Charging

The following conditions have to be valid before charge is enabled:

- CE is HIGH.
- The device is not in undervoltage lockout (UVLO) mode and not in VCCLOWV.
- The device is not in sleep mode (that is, VCC > SRN).
- The VCC voltage is lower than the AC overvoltage threshold (VCC < V_{ACOV}).
- 30-ms delay is complete after initial power up.
- The REGN LDO and VREF LDO voltages are at the correct levels.
- Thermal shutdown (TSHUT) is not valid.
- TS fault is not detected.

One of the following conditions will stop ongoing charging:

- CE is LOW.
- Adapter is removed, thus causing the device to enter VCCLOWV.
- The device is in sleep mode (that is, VCC < SRN).
- Adapter is over voltage.
- The REGN or VREF LDOs voltage are not valid.
- TSHUT IC temperature threshold is reached.
- TS voltage goes out of range indicating the temperature is too hot or too cold.

Copyright © 2010–2015, Texas Instruments Incorporated

Feature Description (continued)

7.3.5 Automatic Internal Soft-Start Charger Current

The charger automatically soft starts the charger regulation current to ensure there is no overshoot or stress on the output capacitor. The soft start consists of stepping up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts around 1.6 ms, for a typical rise time of 13 ms. No external components are needed for this function.

7.3.6 Converter Operation

The synchronous buck PWM converter uses a fixed-frequency voltage mode with feed-forward control scheme. A type III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter is selected to give a resonant frequency of 12 kHz to 17 kHz, where resonant frequency, f_o, is given by:

$$f_o = \frac{1}{2\pi \sqrt{L_o C_o}} \quad (3)$$

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the duty-cycle of the converter. The ramp height is 7% of the input adapter voltage making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset in order to allow zero percent duty-cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.98% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4.2 V for more than 3 cycles, then the high-side N-channel power MOSFET is turned off and the low-side N-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-PH) voltage is detected to fall low again due to leakage current discharging the BTST capacitor below the 4.2 V, and the reset pulse is issued.

The fixed-frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, output voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region.

7.3.7 Synchronous and Nonsynchronous Operation

The charger operates in synchronous mode when the SRP-SRN voltage is above 5 mV (0.5-A inductor current for a 10-mΩ sense resistor). During synchronous mode, the internal gate drive logic ensures there is break-before-make complimentary switching to prevent shoot-through currents. During the 30-ns dead time where both FETs are off, the body-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turnon keeps the power dissipation low, and allows safely charging at high currents. During synchronous mode the inductor current is always flowing and converter operates in continuous conduction mode (CCM), creating a fixed two-pole system.

The charger operates in nonsynchronous mode when the SRP-SRN voltage is below 5 mV (0.5-A inductor current on 10-mΩ sense resistor). The charger is forced into nonsynchronous mode when the super capacitor voltage is lower than 2 V or when the average SRP-SRN voltage is lower than 1.25 mV (125 mA on 10-mΩ sense resistor).

During nonsynchronous operation, the body-diode of lower-side MOSFET can conduct the positive inductor current after the high-side N-channel power MOSFET turns off. When the load current decreases and the inductor current drops to zero, the body diode will be naturally turned off and the inductor current will become discontinuous. This mode is called Discontinuous Conduction Mode (DCM). During DCM, the low-side N-channel power MOSFET will turn on when the bootstrap capacitor voltage drops below 4.2 V, then the low-side power MOSFET will turn off and stay off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The low-side MOSFET on-time is required to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle.

Copyright © 2010–2015, Texas Instruments Incorporated

Feature Description (continued)

At very low currents during nonsynchronous operation, there may be a small amount of negative inductor current during the recharge pulse. The charge must be low enough to be absorbed by the input capacitance. Whenever the converter goes into zero percent duty-cycle, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (only recharge pulse) either, and there is almost no discharge from the output.

During the DCM mode the loop response automatically changes and has a single-pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage.

7.3.8 Input Overvoltage Protection (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. When the adapter voltage reaches the ACOV threshold, charge is disabled.

7.3.9 Output Overvoltage Protection

The converter will not allow the high-side FET to turn-on until the output voltage goes below 102% of the regulation voltage. This allows one-cycle response to an overvoltage condition – such as occurs when the load is removed. An 8-mA current sink from SRP-SRN to GND is on during charge and allows discharging the output capacitors.

7.3.10 Cycle-by-Cycle Charge Overcurrent Protection

The charger has a secondary cycle-to-cycle overcurrent protection. The charger monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the overcurrent threshold.

7.3.11 Thermal Shutdown Protection

The VQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 145°C. The charger stays off until the junction temperature falls below 130°C.

7.3.12 Temperature Qualification

The controller continuously monitors load temperature by measuring the voltage between the TS pin and GND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the temperature must be within the V(LTF) to V(HTF) thresholds. If temperature is outside of this range, the controller suspends charge and waits until the temperature is within the V(LTF) to V(HTF) range. During the charge cycle the temperature must be within the V(LTF) to V(TCO) thresholds. If temperature is outside of this range, the controller suspends charge and waits until the temperature is within the V(LTF) to V(HTF) range. The controller suspends charge by turning off the PWM charge FETs. If the TS function is not required, R9 and R10 can be the same value so the voltage on TS is 1.65 V with VREF as the reference supply.

Copyright © 2010–2015, Texas Instruments Incorporated

Feature Description (continued)

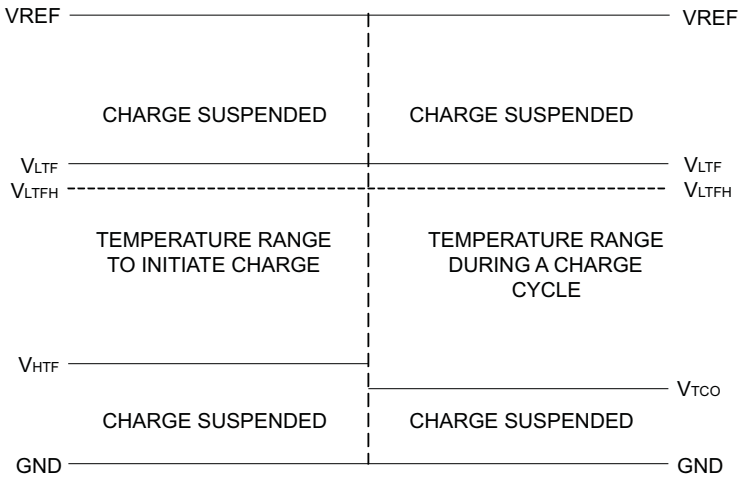


Figure 9. TS Pin, Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor is selector, the value RT1 and RT2 can be determined by using the following equations:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1\right)} \quad (4)$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (5)$$

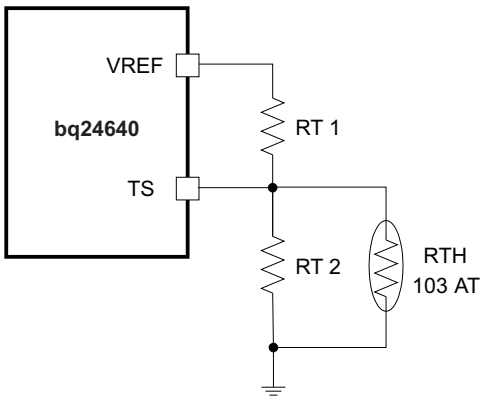


Figure 10. TS Resistor Network

7.3.13 CE (Charge Enable)

The CE digital input is used to disable or enable the charge process. A high-level signal on this pin enables charge, provided all the other conditions for charge are met (see ***Enabling and Disabling Charge***). A high-to-low transition on this pin also resets all timers and fault conditions. There is an internal 1-MΩ pulldown resistor on the CE pin, so if CE is floated the charge will not turn on.

Copyright © 2010–2015, Texas Instruments Incorporated

Feature Description (continued)

7.3.14 $\overline{\text{PG}}$ Output

The open-drain $\overline{\text{PG}}$ (power good) output indicates when the VCC voltage is present. The open-drain FET turns on whenever bq24640 is not in UVLO mode and not in sleep mode (that is, V(VCC) > V(SRN) and V(VCC) > V(UVLO)). The $\overline{\text{PG}}$ pin can be used to drive an LED or communicate to the host processor.

7.3.15 Charge Status Outputs

The open-drain STAT output indicates various charger operations as shown in Table 2. These status pins can be used to drive LEDs or communicate with the host processor.

NOTE

OFF indicates that the open-drain transistor is turned off.

Table 2. STAT Pin Definition

CHARGE STATE	STAT
CE high	ON
Sleep mode	OFF
Charge Suspend (TS), Input or Output Overvoltage, CE low	Blinking

7.4 Device Functional Modes

7.4.1 Constant Current Mode

If the super capacitor voltage is less than the programmed target voltage (that is, VFB pin is less than V_{FB}) when charging is enabled, then charging will resume in constant current mode. In this mode, the super capacitor charge current will be constant and regulated as per the ISET and current sense resistor (between SRP and SRN) settings.

7.4.2 Constant Voltage Mode

When the super capacitor voltage is between the target charge voltage and OVP condition (that is, $V_{FB} \leq$ VFB pin $< V_{OV_RISE}$), then the device will be in constant voltage mode. In this mode, the super capacitor voltage will be constant and regulated as per the VFB setting while the charge current will taper down.

Copyright © 2010–2015, Texas Instruments Incorporated

8 Application and Implementation

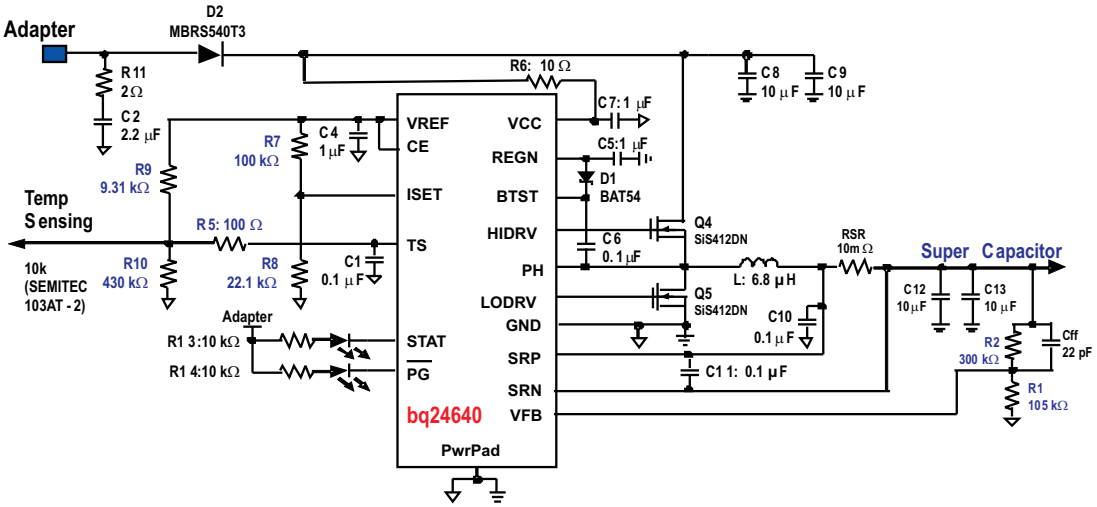
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq24640 super capacitor charger is ideal for high current charging (up to 10 A). The bq24640EVM evaluation module is a complete charge module for evaluating the bq24640. The application curves were taken using the bq24640EVM. Refer to the EVM user's guide (SLUU410) for EVM information.

8.2 Typical Application



V_{IN} = 19 V, V_{OUT} = 8.1 V, I_{charge} = 3 A, Temperature range 0–45°C

Figure 11. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
AC adapter voltage (VIN)	19 V
Battery charge voltage	8.1 V
Battery charge current (during constant current phase)	3 A

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The bq24640 has a 600-kHz switching frequency to allow the use of small inductor and capacitor values. The inductor saturation current must be higher than the charging current (ICHG) plus half the ripple current (IRIPPLE):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (6)$$

The inductor ripple current depends on input voltage (VIN), duty cycle (D = V_{OUT} / V_{IN}), switching frequency (fs), and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \quad (7)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

8.2.2.2 Input Capacitor

Input capacitor must have enough ripple current rating to absorb input switching ripple current. The worst-case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (8)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and must be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A 25-V rating or higher capacitor is preferred for 20-V input voltage. The 20-µF capacitance is suggested for typical of 3-A to 4-A charging current.

8.2.2.3 Output Capacitor

Output capacitor also must have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (9)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{1}{8LCfs^2}\left(V_{OUT} - \frac{V_{OUT}^2}{V_{IN}}\right) \quad (10)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The bq24640 has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor must be designed from 12 kHz to 17 kHz. The preferred ceramic capacitor is 25 V or higher rating, X7R or X5R.

8.2.2.4 Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching charger. The gate drivers are internally integrated into the IC with 6 V of gate drive voltage. 30-V or higher voltage rating MOSFETs are preferred for 20-V input voltage and 40-V or higher rating MOSFETs are preferred for 20-V to 28-V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For top side MOSFET, FOM is defined as the product of the ON-resistance of the MOSFET, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For bottom-side MOSFET, FOM is defined as the product of the ON-resistance of the MOSFET, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD}; \quad FOM_{bottom} = R_{DS(on)} \times Q_G \quad (11)$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

Copyright © 2010–2015, Texas Instruments Incorporated

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), ON-resistance of the MOSFET ($R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (F), turnon time (t_{on}), and turnoff time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times f_S \quad (12)$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100ºC junction temperature rise. The second term represents the switching loss. The MOSFET turnon and turnoff times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}}$$

where

- Q_{SW} is the switching charge
- Ion is the turn-on gate driving current
- IOFF is the turn-off gate driving current. (13)

If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (14)$$

Gate driving current total can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{PLT}), total turnon gate resistance (R_{ON}) and turnoff gate resistance R_{OFF}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (15)$$

The conduction loss of the bottom-side MOSFET is calculated with Equation 16 when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \quad (16)$$

If the SRP-SRN voltage decreases below 5 mV (the charger is also forced into nonsynchronous mode when the average SRP-SRN voltage is lower than 1.25 mV), the low-side FET will be turned off for the remainder of the switching cycle to prevent negative inductor current.

As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The maximum charging current in nonsynchronous mode can be up to 0.9 A (0.5 A typical) for a 10-mΩ charging current-sensing resistor considering IC tolerance. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum nonsynchronous mode charging current.

MOSFET gate driver power loss contributes to the dominant losses on controller IC, when the buck converter is switching. Choosing the MOSFET with a small Q_{g_total} will reduce the IC power loss to avoid thermal shutdown.

$$P_{ICLoss_driver} = V_{IN} \times Q_{g_total} \times f_S$$

where

- Q_{g_total} is the total gate charge for both upper and lower MOSFET at 6-V VREGN. (17)

8.2.2.5 Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second-order system. The voltage spike at VCC pin may be beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent an overvoltage event on VCC pin.

There are several methods to damping or limit the overvoltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the overvoltage level to an IC safe level. However these two solutions may not have low cost or small size.

Copyright © 2010–2015, Texas Instruments Incorporated

A cost effective and small size solution is shown in Figure 12. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result, the overvoltage spike is limited to a safe level. D1 is used for reverse-voltage protection for VCC pin. C2 is the VCC pin decoupling capacitor and must be placed as close as possible to the VCC pin. The R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high-voltage spike. C2 value must be less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect for hot plug-in. R1 and R2 package must be sized enough to handle inrush current power loss according to resistor manufacturer's datasheet. The filter components value must always be verified with real application and minor adjustments may must fit in the real application circuit.

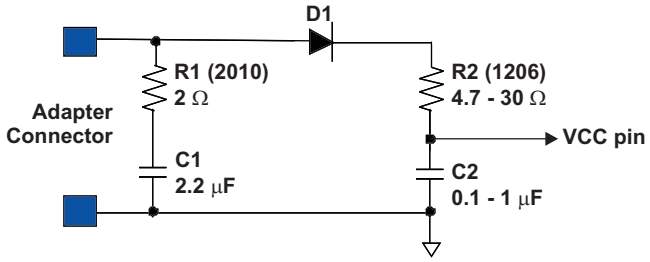


Figure 12. Input Filter

8.2.2.6 Inductor, Capacitor, and Sense Resistor Selection Guidelines

The bq24640 provides internal loop compensation. With this scheme, best stability occurs when the LC resonant frequency, f_o, is approximately 12 kHz to 17 kHz. Table 4 provides a summary of typical LC components for various charge currents.

See *Inductor Selection* for information on controlling ripple current.

Table 4. Typical Inductor, Capacitor, and Sense Resistor Values as a Function of Charge Current

CHARGE CURRENT	2 A	4 A	6 A	8 A	10 A
Output Inductor Lo	10 µH	6.8 µH	4.7 µH	3.3 µH	3.3 µH
Output Capacitor Co	15 µF	20 µF	30 µF	40 µF	40 µF
Sense Resistor	10 mΩ	10 mΩ	10 mΩ	10 mΩ	10 mΩ

Table 5. Component List for Typical System Circuit of Figure 11

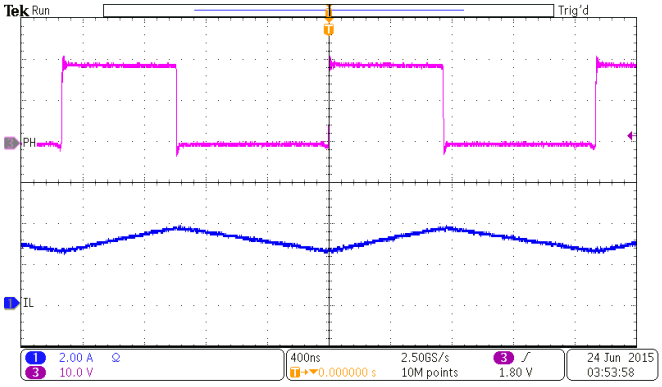
PART DESIGNATOR	QTY	DESCRIPTION
Q4, Q5	2	N-channel MOSFET, 30 V, 12 A, PowerPAK 1212-8, Vishay-Siliconix, Sis412DN
D1	1	Diode, Dual Schottky, 30 V, 200 mA, SOT23, Fairchild, BAT54C
D2	1	Schottky Diode, 40 V, 5 A, SMC, ON Semiconductor, MBRS540T3
D3, D4	2	LED Diode, Green, 2.1 V, 10 mΩ, Vishay-Dale, WSL2010R0100F
R_{SR}	1	Sense Resistor, 10 mΩ, 1%, 1 W, 2010, Vishay-Dale, WSL2010R0100F
L	1	Inductor, 6.8 µH, 5.5 A, Vishay-Dale IHLP2525CZ
C8, C9, C12, C13	4	Capacitor, Ceramic, 10 µF, 35 V, 20%, X7R
C4, C5	2	Capacitor, Ceramic, 1 µF, 16 V, 10%, X7R
C7	1	Capacitor, Ceramic, 1 µF, 50 V, 10%, X7R
C1, C6, C11	3	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R
C2	1	Capacitor, Ceramic, 2.2 µF, 50 V, 10%, X7R
C_{ff}	1	Capacitor, Ceramic, 22 pF, 35 V, 10%, X7R
C10	1	Capacitor, Ceramic, 0.1 µF, 35 V, 10%, X7R
R1	1	Resistor, Chip, 105 kΩ, 1/16 W, 0.5%
R2	1	Resistor, Chip, 300 kΩ, 1/16 W, 0.5%
R7	1	Resistor, Chip, 100 kΩ, 1/16 W, 0.5%
R8	1	Resistor, Chip, 22.1 kΩ, 1/16 W, 0.5%
R9	1	Resistor, Chip, 9.31 kΩ, 1/16 W, 1%

Copyright © 2010–2015, Texas Instruments Incorporated

Table 5. Component List for Typical System Circuit of Figure 11 (continued)

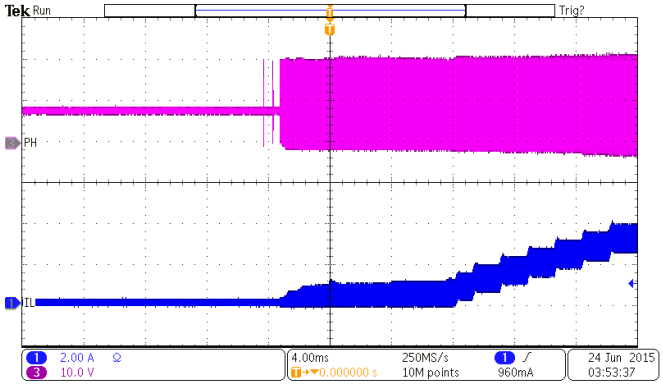
PART DESIGNATOR	QTY	DESCRIPTION
R10	1	Resistor, Chip, 430 kΩ, 1/16 W, 1%
R11	1	Resistor, Chip, 2 Ω, 1 W, 5%
R13, R14	2	Resistor, Chip, 100 kΩ, 1/16 W, 5%
R5	1	Resistor, Chip, 100 Ω, 1/16 W, 0.5%
R6	1	Resistor, Chip, 10 Ω, 0.25 W, 5%

8.2.3 Application Curves



V_{IN}: 19 V V_{CAP}: 8 V I_{CHG} = 3 A

Figure 13. Continuous Conduction Mode



V_{IN}: 19 V V_{CAP}: 8 V I_{CHG} = 3 A

Figure 14. Battery Charging Soft Start (by Asserting CE Low to High)

9 Power Supply Recommendations

For proper operation of bq24640, VCC must be from 5 V to 28 V. To begin charging, VCC must be higher than SRN by at least 500 mV (otherwise, the device will be in sleep mode). TI recommends an input voltage of at least 1.5 V to 2 V higher than the super capacitor voltage, taking into consideration the DC losses in the high-side FET (Rdson), inductor (DCR), the input diode drop, and current-sense resistor (between SRP and SRN). Power limit for the input supply must be greater than the maximum power required for super capacitor charging.

10 Layout

10.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 15) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place the input capacitor as close as possible to switching MOSFET supply and ground connections and use the shortest copper trace connection. These parts must be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC must be placed close to the switching MOSFET gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
3. Place the inductor input terminal to switching MOSFET output terminal as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor must be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area)

Copyright © 2010–2015, Texas Instruments Incorporated

Layout Guidelines (continued)

and do not route the sense leads through a high-current path (see Figure 15 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.

5. Place the output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections must be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Route analog ground separately from power ground and use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC, use analog ground copper pour, but avoid power pins to reduce inductive and capacitive noise coupling. Connect analog ground to GND pin using thermal pad as the single ground connection point to connect analog ground and power ground together, or use a 0-Ω resistor to tie analog ground to power ground (thermal pad must tie to analog ground in this case). A star-connection under thermal pad is highly recommended.
8. It is critical to solder the exposed thermal pad on the backside of the IC package to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
9. Decoupling capacitors must be placed next to the IC pins and make trace connection as short as possible.
10. All via size and number should be enough for a given current path.

Refer to the EVM design (SLUU410) for the recommended component placement with trace and via locations.

For the QFN information, refer to *Quad Flatpack No-Lead Logic Packages* (SCBA017) and *QFN/SON PCB Attachment Application Report* (SLUA271).

10.2 Layout Examples

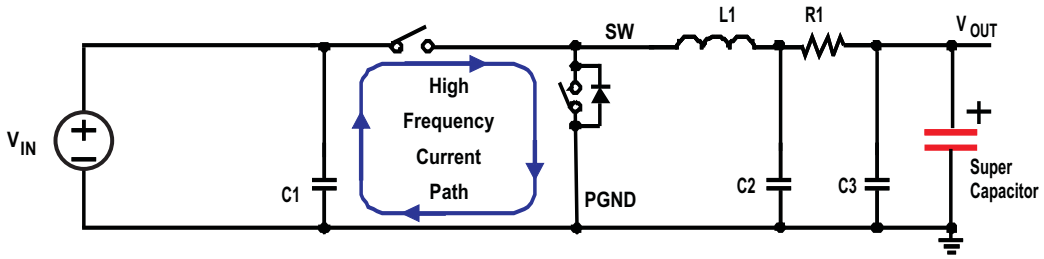


Figure 15. High-Frequency Current Path

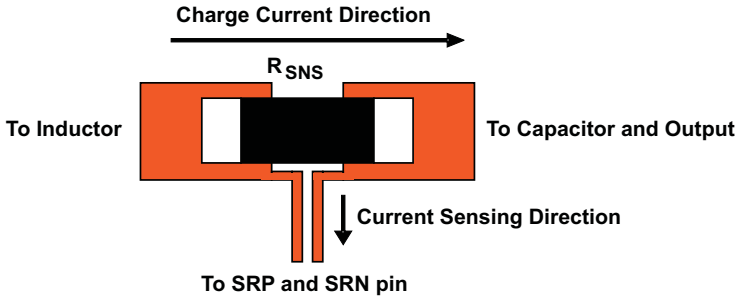


Figure 16. Sensing Resistor PCB Layout

Copyright © 2010–2015, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *bq24600/20/40 EVM (HPA421) Multi Cell Synchronous Switch-Mode Charger*, SLUU410
- *Quad Flatpack No-Lead Logic Packages*, SCBA017
- *QFN/SON PCB Attachment*, SLUA271

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2010–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24640RVAR	ACTIVE	VQFN	RVA	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OGA	Samples
BQ24640RVAT	ACTIVE	VQFN	RVA	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OGA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

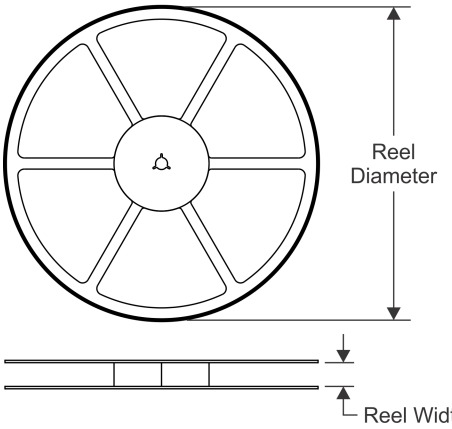
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

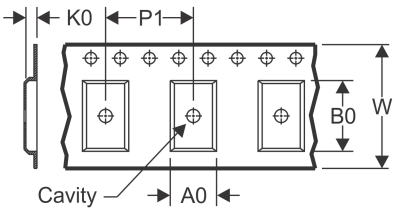
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

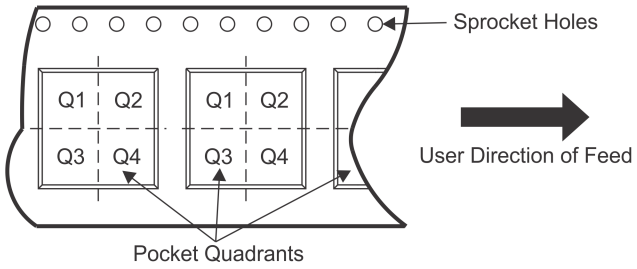


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

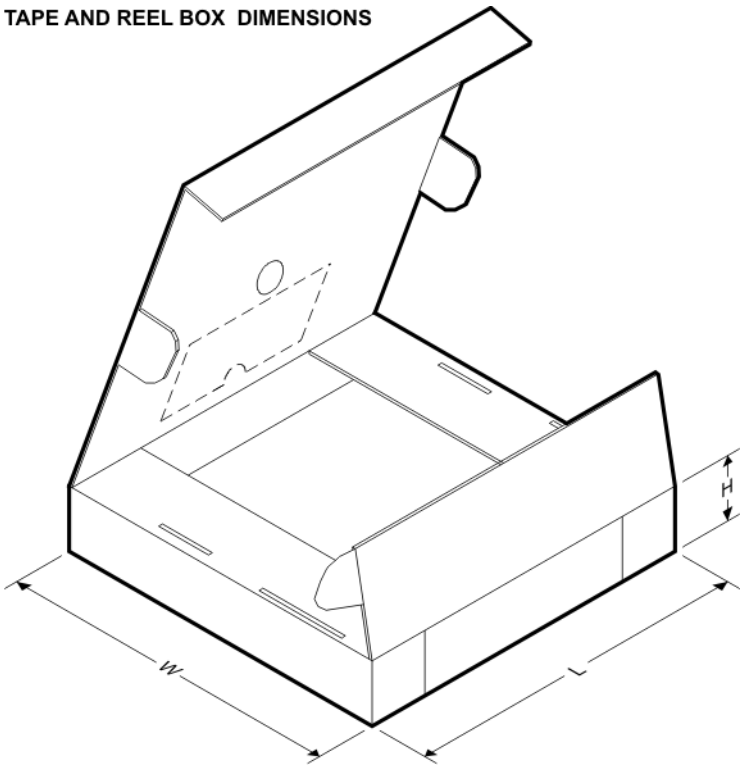
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24640RVAR	VQFN	RVA	16	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24640RVAT	VQFN	RVA	16	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

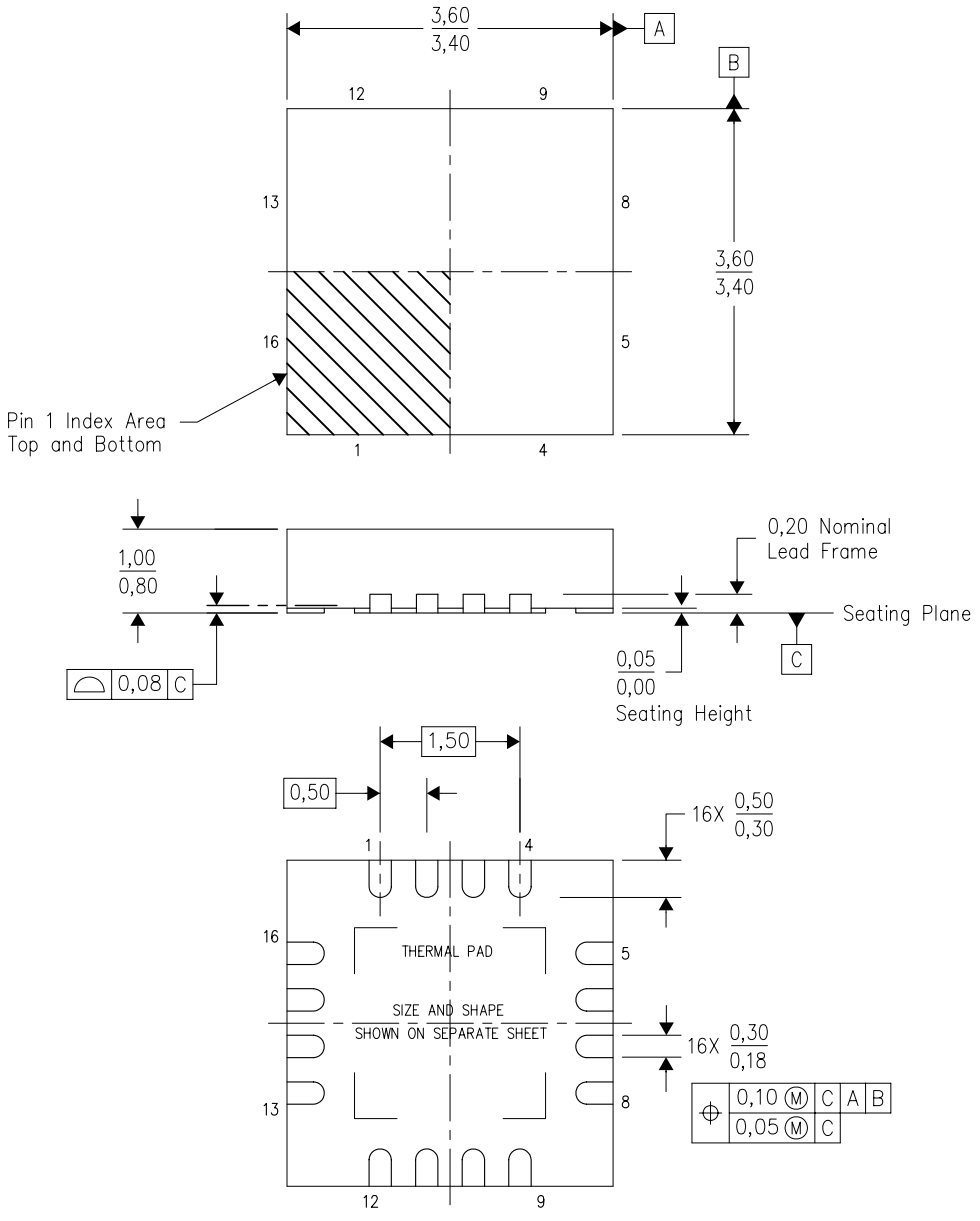
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24640RVAR	VQFN	RVA	16	3000	367.0	367.0	35.0
BQ24640RVAT	VQFN	RVA	16	250	210.0	185.0	35.0

RVA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4209676/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

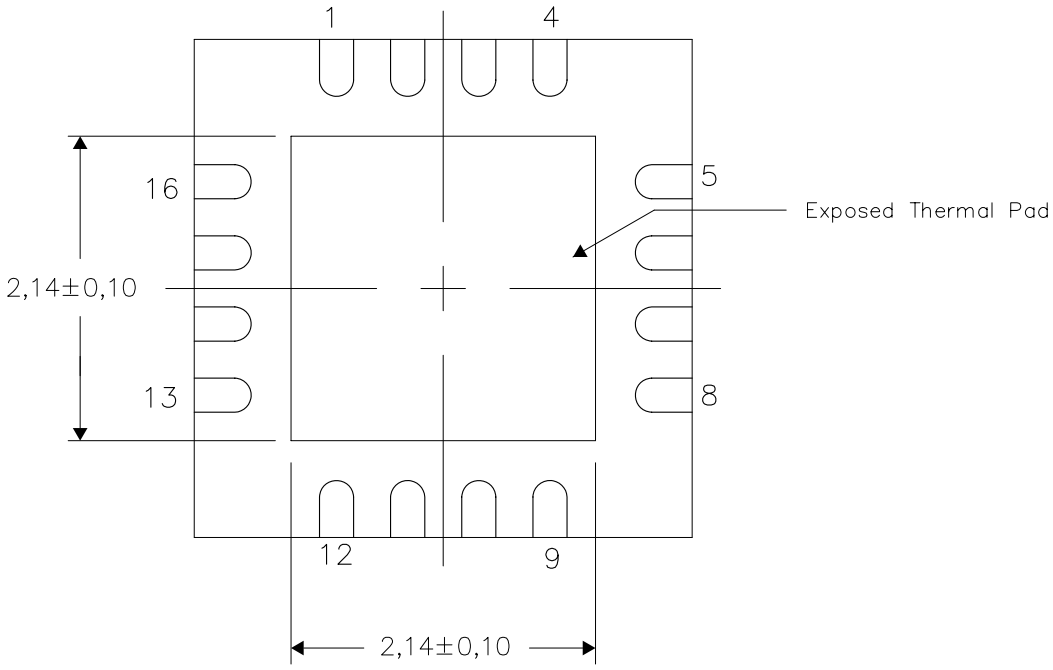
RVA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

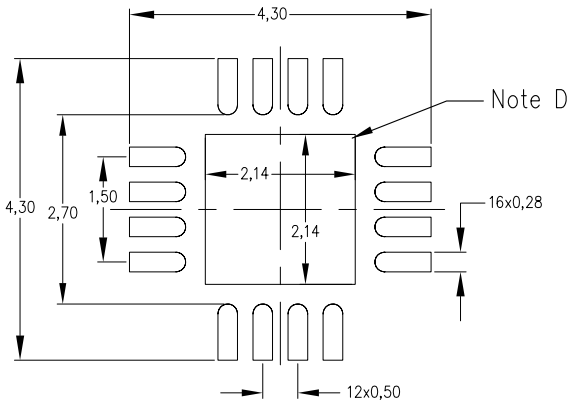
Exposed Thermal Pad Dimensions

4209715/B 05/11

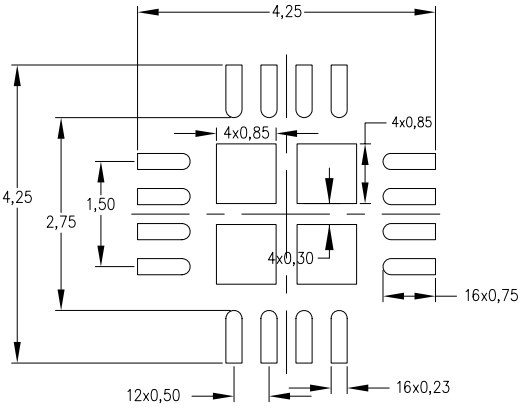
NOTE: All linear dimensions are in millimeters

RVA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

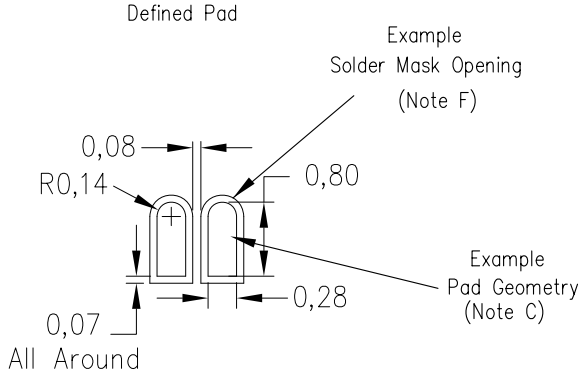


Example Stencil Design
0.125mm Stencil Thickness
(Note E)

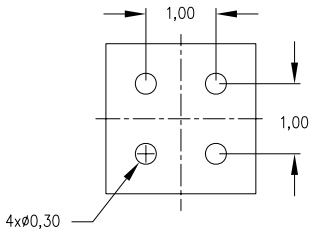


63% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad



Example Via Layout Design
may vary depending on constraints
(Note D, F)



4211274/B 05/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated