HV9150

High-Voltage Output Hysteretic-Mode Step-Up DC/DC Controller

Features

- 6V to 500V Wide Output Voltage Range
- 2.7V Low Input Voltage
- 5W Maximum Output Power with External MOSFET Driver
- Built-in Charge Pump Converter for the Gate Driver
- Programmable Switching Frequency from 40 kHz to 400 kHz
- Four Programmable Duty Cycles from 50% to 87.5%
- FB Return Ground Switch for Power-Saving Applications
- Built-In Delay Timer for Internal Protection
- Non-Isolated DC/DC Converter

Applications

- Portable Electronic Equipment
- MEMS
- Printers

General Description

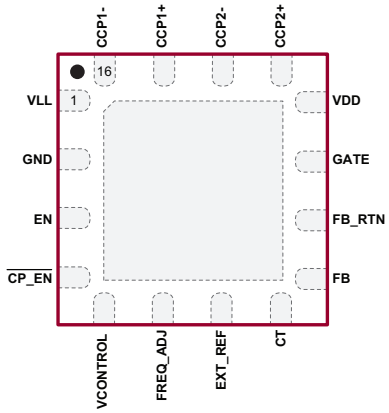
The HV9150 is a high output voltage Hysteretic mode step-up DC/DC controller that has a built-in charge pump converter and a linear regulator for a wide range of input voltage. The Charge Pump Converter mode is ideal for battery-powered applications. The internal converter can provide a minimum of 5V gate driver output voltage (at V_{IN} = 2.7V) to the external N-channel MOSFET. The range of 2.7V to 4.5V input supply voltage is ideal for battery-powered applications, such as portable electronic equipment. The internal linear regulator is selected when a higher supply voltage rail is available in the system.

A feedback return ground path switch is also integrated into the device to minimize the quiescent current during the controller shutdown. This feature provides power savings for energy-critical applications.

In addition, a built-in timer is available to protect the internal circuit and help dissipate the energy from the external high-voltage storage capacitor. This device is designed for systems requiring high-voltage and low-current applications such as MEMS devices.

Package Type

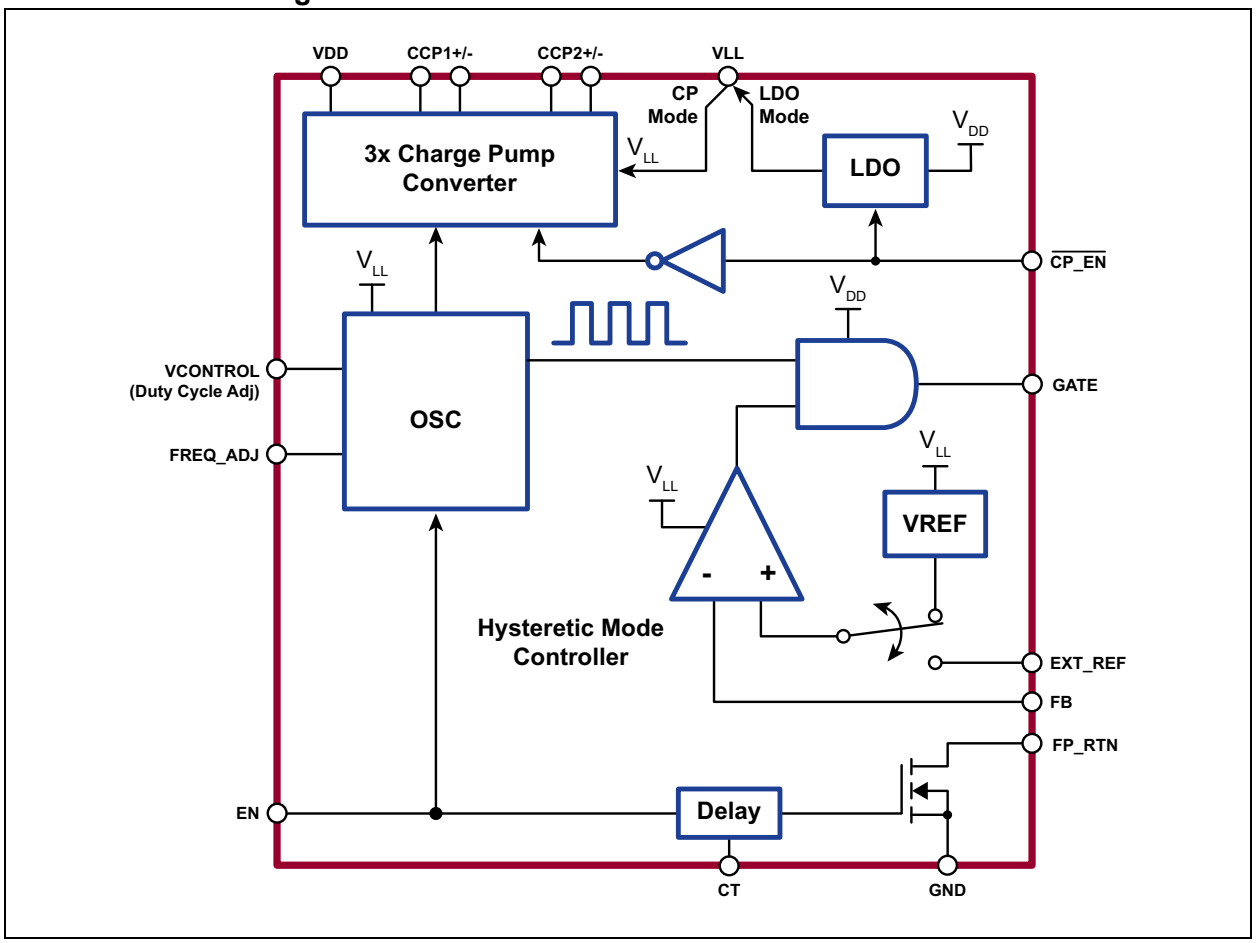
16-lead QFN
(Top View)



Pads are at the bottom of the package. Center heat slug is at ground potential. See Table 3-1 for pin information.

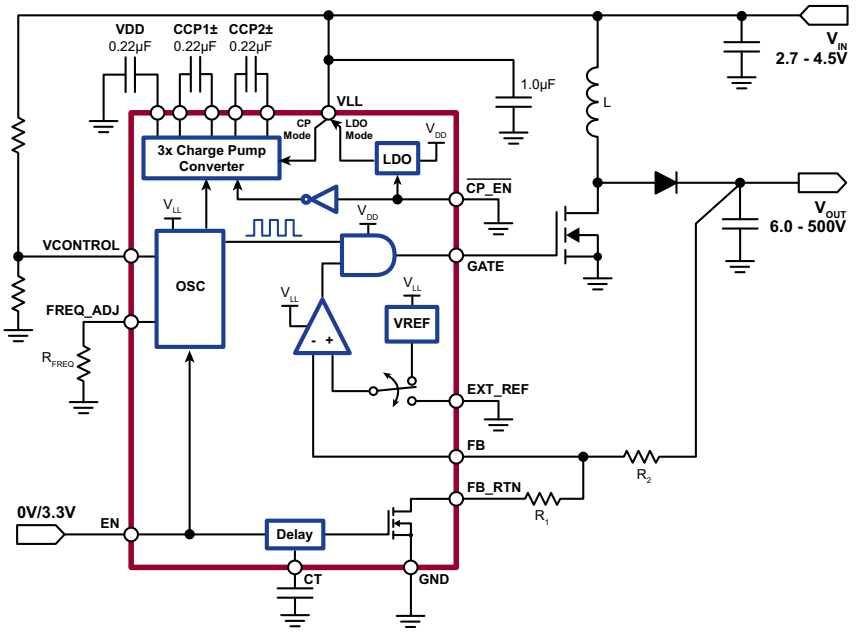
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Functional Block Diagram

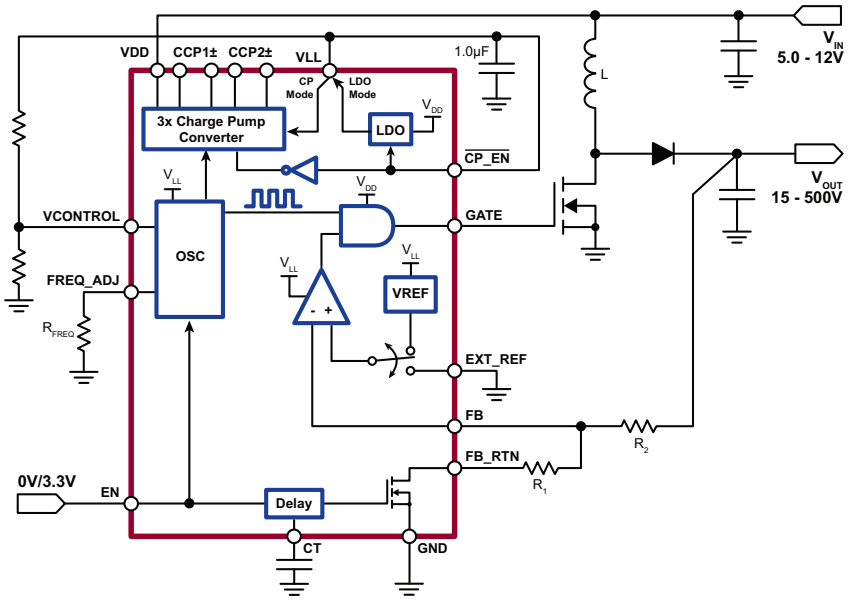


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Typical Application Circuits



Charge Pump (CP) Mode



Linear Regulator (LDO) Mode

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input Voltage Supply, V_{LL} ..... –0.5V to +5V
Charge Pump Output Voltage, V_{DD} ..... –0.5V to +13.6V
Logic Input Levels ..... –0.5V to V_{LL} +0.5V
Operating Ambient Temperature, T_A ..... –25°C to +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Power Dissipation (On a 3 x 4-inch FR4 PCB at T_A= 25°C):
16-lead QFN ..... 3000 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Voltage (CP Mode)	V_{LL}	2.7	—	4.5	V	
High-level Input Voltage	V_{IH}	0.8 V_{LL}	—	V_{LL}	V	
Low-level Input Voltage	V_{IL}	0	—	0.2 V_{LL}	V	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating supply voltages and temperatures; unless otherwise noted, T_J = 25°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
POWER SUPPLY							
Quiescent V_{LL} Supply Current (EN = ‘0’)		$I_{LLQ(off)}$	—	—	2	µA	
VLL Supply Current (EN = ‘1’)	GATE = NC	$I_{LL(on)}$	—	—	1.5	mA	f_{OSC} = 100 kHz, V_{LL} = 4.5V
	GATE = 300 pF		—	—	4		
VDD Supply Current (EN = ‘1’)	GATE = NC	$I_{DD(on)}$	—	—	1	mA	f_{OSC} = 100 kHz, V_{DD} = 12.6V
	GATE = 300 pF		—	—	2.5		
Quiescent VDD Supply Current (EN = ‘0’)		$I_{DDQ(off)}$	—	—	2	µA	
High-level Logic Input Current		I_{IH}	—	—	1	µA	V_{IH} = V_{LL}
Low-level Logic Input Current		I_{IL}	—	—	–1	µA	V_{IL} = 0V
Gate Driver Output Voltage	V_{LL} = 4.5V GATE = NC	GATE	10.2	—	12.3	V	
	V_{LL} = 2.7V GATE = NC		5	—	6.9		
Linear Regulator Output Voltage		$V_{LL(LDO)}$	3	—	3.6	V	

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating supply voltages and temperatures; unless otherwise noted T_J = 25°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
FEEDBACK (FB)							
Internal Feedback Reference Voltage	Accuracy	V_{REF}	1.22	1.25	1.28	V	
	Range		1.2	1.25	1.3		T_A = –25 to 85°C
Input Bias Current		I_{BIAS}	—	—	1	µA	EXT_REF is selected.
External Reference Voltage	Range	EXT_REF	0	—	V_{LL}–1.4	V	
	Trigger INT Reference		0	—	0.12	V	During EN positive triggering
	Trigger EXT Reference		0.5	—	V_{LL}–1.4	V	
On-resistance, R_{DS}		FB_RTN	—	—	500	Ω	I_O= 2 mA
Breakdown Voltage, BV			—	—	13.5	V	
GATE DRIVER OUTPUT (GATE)							
Rise Time		t_r	—	—	36	ns	C_L = 300 pF, V_{DD} = 12V
Fall Time		t_f	—	—	12	ns	
Pull-up Resistance	V_{DD} = 5V	R_{UP}	—	—	45	Ω	I_O = 20 mA
	V_{DD} = 12V		—	—	30		I_O = 50 mA
Pull-down Resistance	V_{DD} = 5V	R_{DOWN}	—	—	15	Ω	I_O = 20 mA
	V_{DD} = 12V		—	—	12		I_O = 50 mA
Oscillator Frequency		f_{GATE}	—	½ f_{OSC}	—	kHz	
CHARGE PUMP CONVERTER							
Charge Pump Output Voltage		V_{DD}	5	3 V_{LL}–1.8	12.6	V	2.7V ≤ V_{LL} ≤ 4.5V C_{CP1} = 220 nF C_{CP2} = 220 nF C_{CP3} = 220 nF
Oscillator Frequency	Accuracy	f_{OSC}	170	195	220	kHz	R_{FREQ} = 270 kΩ, V_{LL}= 3.3V
	Range		40	—	400		Over R_{FREQ} range
Oscillator Frequency Tolerance		Δf	—	15	—	%	50 kHz ≤ f_{OSC} ≤ 250 kHz
Duty Cycle	Accuracy	DC	86	87.5	90	%	R_{FREQ} = 270 kΩ
	Range		—	0	—	%	0 < V_{CNTL} ≤ 0.18 V_{LL}
			—	50	—	%	0.22 V_{LL} < V_{CNTL} ≤ 0.38 V_{LL}
			—	62.5	—	%	0.42 V_{LL} < V_{CNTL} ≤ 0.58 V_{LL}
			—	75	—	%	0.62 V_{LL} < V_{CNTL} ≤ 0.78 V_{LL}
			—	87.5	—	%	0.82 V_{LL} < V_{CNTL} ≤ V_{LL}
Duty Cycle Adjustment		$V_{CONTROL}$	0	—	V_{LL}	V	See Table 4-2.
Frequency Adjustment Resistor		R_{FREQ}	120k	—	1.2M	Ω	
Maximum Charge Pump Output Resistance	Pull-up	R_{CP}	—	—	20	Ω	V_{LL} = 2.7V, I_O = 10 mA
	Pull-down		—	—	20		

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Over recommended operating supply voltages and temperatures; unless otherwise noted T_J = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Output Ripple at V_{DD}	V_{RIPPLE}	—	—	100	mV	2.7V ≤ V_{LL} ≤ 4.5V f_{OSC} = 200 kHz C_{CP1} = 220 nF C_{CP2} = 220 nF C_{CP3} = 220 nF C_{GATE} = 300 pF BW = 20 MHz
DELAY TIMER						
Shutdown Delay Timer	t_{DELAY}	—	240	—	ms	C_T = 1 µF

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–25	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
16-lead QFN	θ_{JA}	—	33	—	°C/W	

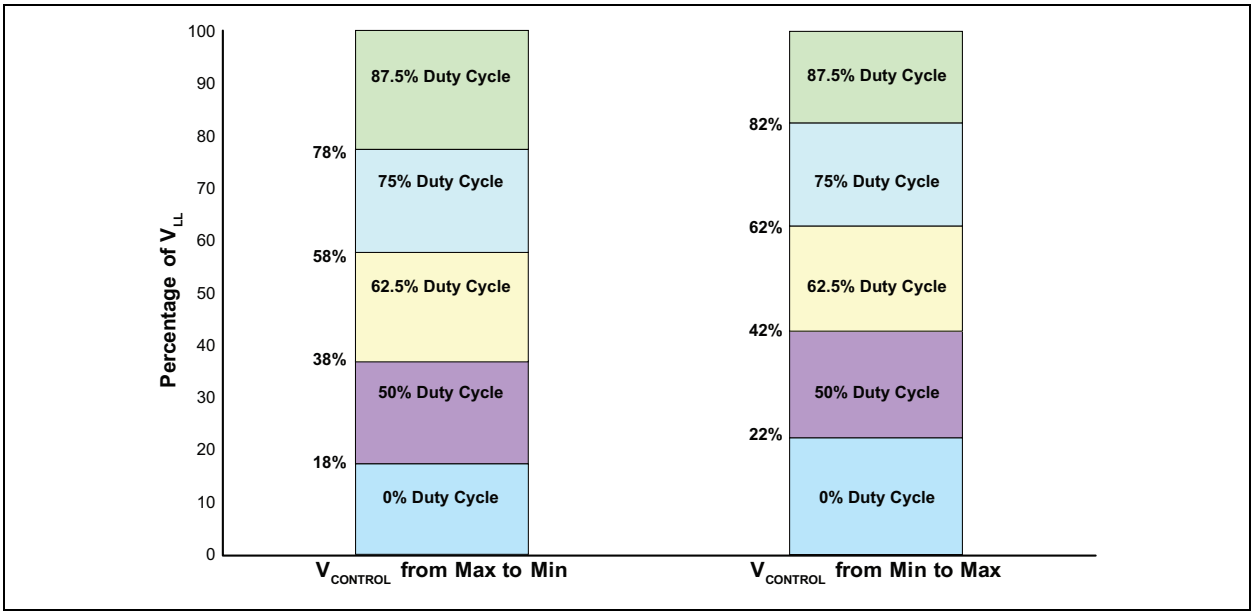


FIGURE 1-1: *Duty Cycle Selection Hysteresis at $V_{CONTROL}$ Pin at 25°C.*

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Timing Waveforms

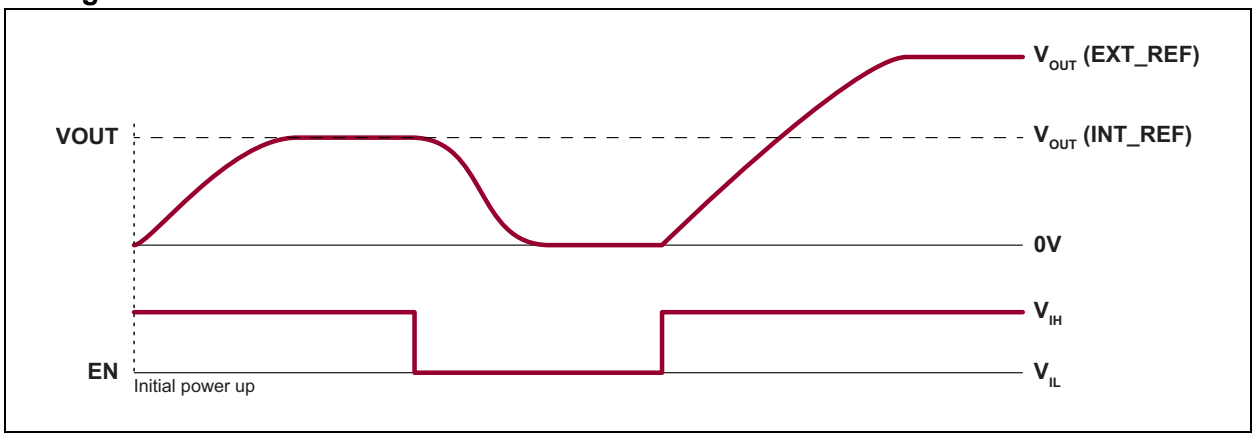


FIGURE 1-2: *Enabling to use the External Voltage Reference.*

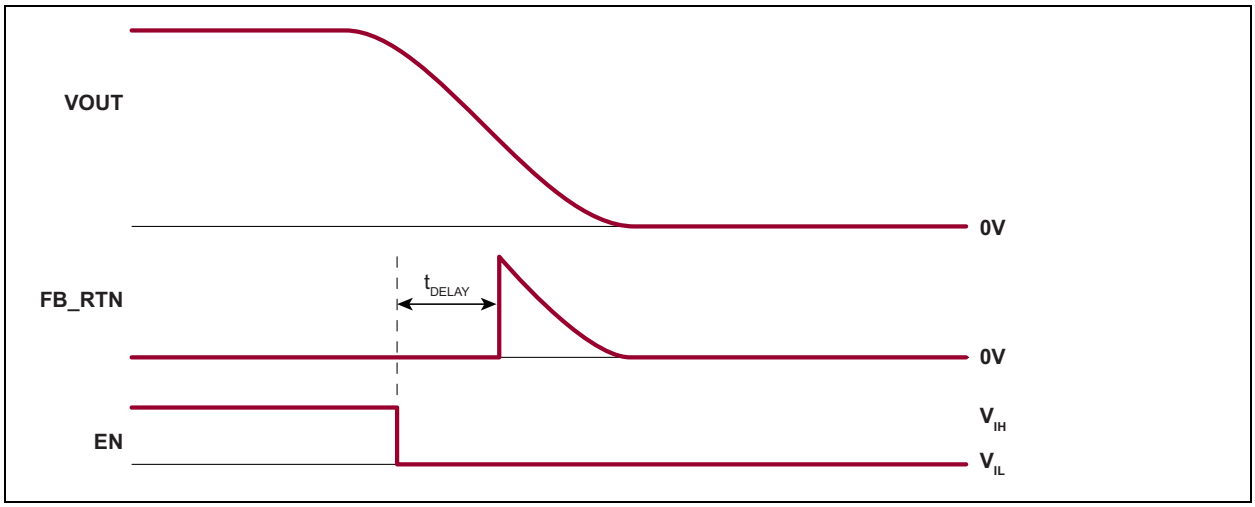


FIGURE 1-3: *Delay Time at FB_RTN.*

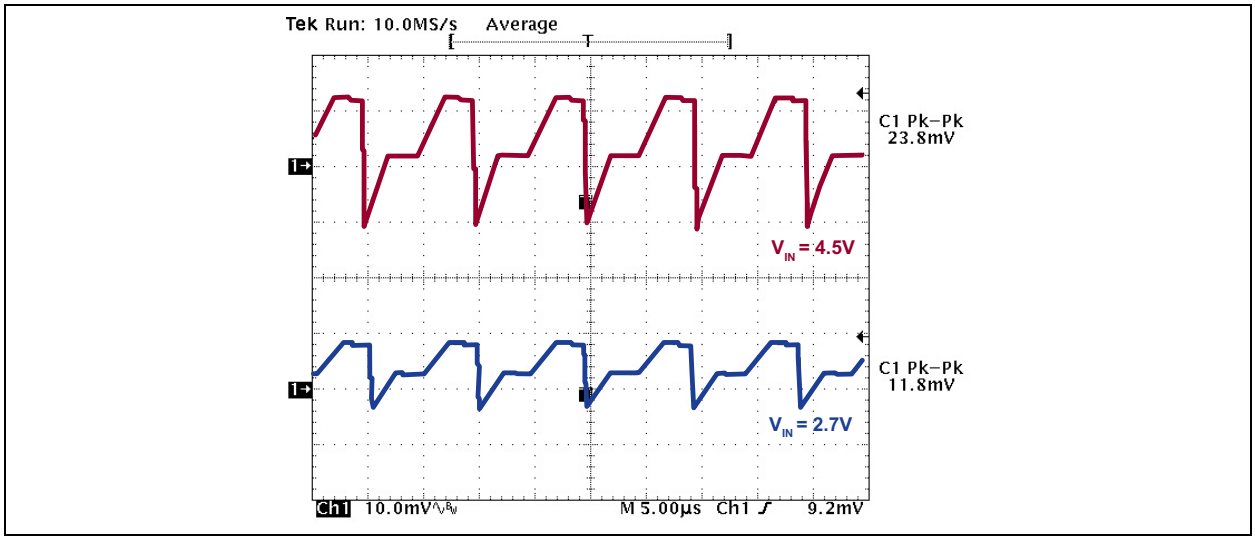


FIGURE 1-4: *VCP Noise.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

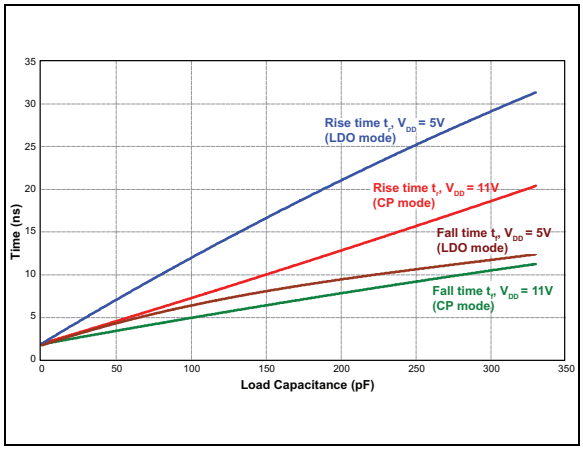


FIGURE 2-1: *Gate Driver Rise Time (t_r) and Fall Time (t_f) vs. Load Capacitance at 25°C.*

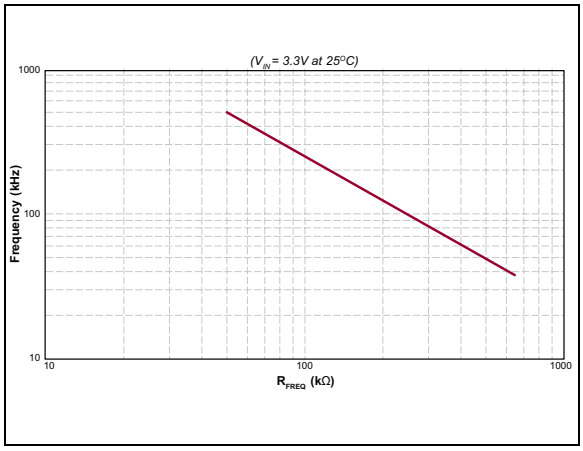


FIGURE 2-2: *f_{GATE} vs. R_{FREQ}.*

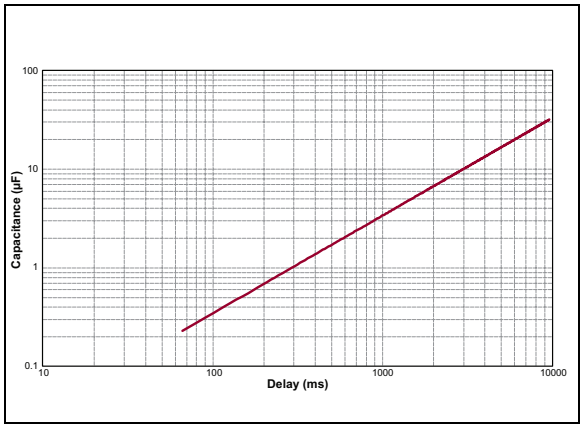


FIGURE 2-3: *C_T Capacitor Value vs. Delay Time at 25°C.*

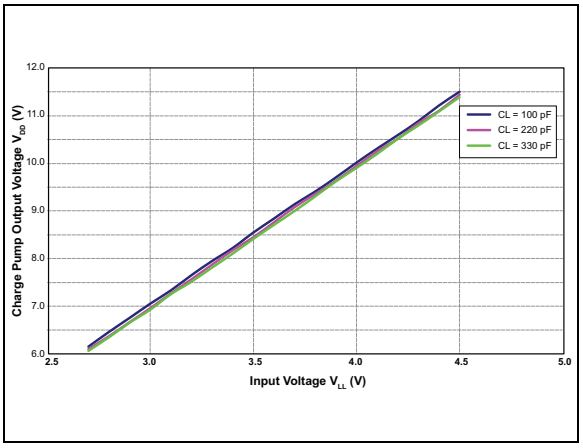


FIGURE 2-4: *Charge Pump Output Voltage vs. Input Voltage at 25°C.*

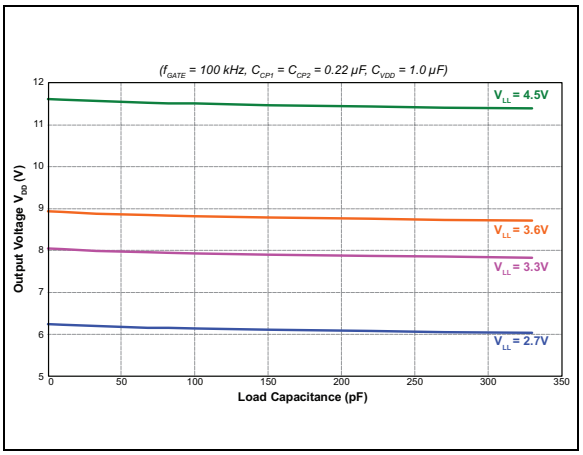


FIGURE 2-5: *Charge Pump Output Voltage vs. Load Capacitance at 25°C.*

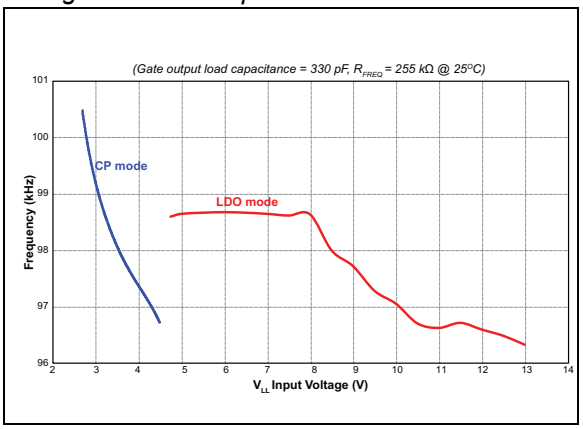


FIGURE 2-6: *Gate Driver Switching Frequency vs. V_{LL} Input Voltage.*

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3.0 PIN DESCRIPTION

The details of the pins of HV9150 16-lead QFN are listed in Table 3-1. Refer to **Package Type** for the pin locations.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VLL	Input supply voltage
2	GND	Ground connection
3	EN	Enable
4	$\overline{\text{CP_EN}}$	Charge pump/LDO enable input
5	VCONTROL	Duty cycle adjustment voltage control input
6	FREQ_ADJ	Frequency adjustment
7	EXT_REF	External reference voltage input
8	CT	Timing capacitor
9	FB	Feedback input voltage
10	FB_RTN	Feedback return
11	GATE	Gate control output
12	VDD	Charge pump output voltage
13	CCP2+	Charge pump storage capacitor #2 plus terminal
14	CCP2–	Charge pump storage capacitor #2 minus terminal
15	CCP1+	Charge pump storage capacitor #1 plus terminal
16	CCP1–	Charge pump storage capacitor #1 minus terminal
Center Pad		Substrate connection (at ground potential)

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4.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 4-1 to power up and power down the HV9150.

TABLE 4-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove all inputs.
2	Apply V_{IN}.	2	Remove V_{IN}.
3	Set all inputs to a known state.	3	Disconnect ground.

4.1 Hysteretic Mode Controller

A Hysteretic mode controller consists of an oscillator, a voltage reference, a comparator and a driver. Both the internal oscillator and the duty cycle of the gate driver are running at a fixed rate.

As this device is designed for a step-up conversion, a pulse train is used to control the switch of a classical switching boost converter. The pulse train is gated by the output of the comparator, which compares the feedback of the output voltage with the voltage reference.

If the output voltage reaches the target voltage, the comparator will turn off the pulse train. When the output voltage drops below the target voltage, the comparator will pass the pulse train to the switch and start the inductor charging cycle. The advantage of this Hysteretic mode controller is its stability and simple operation. The diagram in Figure 4-1 shows a Hysteretic Mode controller and a classical boost converter.

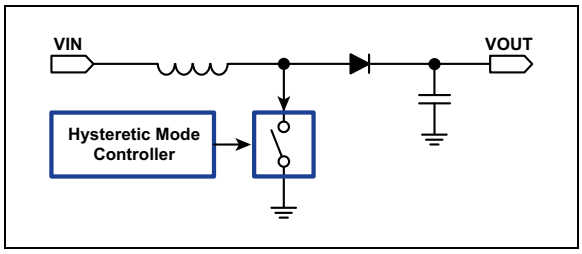


FIGURE 4-1: *A Hysteretic Mode Controller and a Classical Boost Converter.*

4.2 Internal Oscillator

This device has an internal oscillator which generates the reference clock for the Hysteretic mode controller. The controller is running at half of the frequency of the internal oscillator. This oscillator is powered by the V_{LL} power supply pin. The frequency of the oscillator is set by the external resistor R_{FREQ}, and this frequency is inversely proportional to the value of R_{FREQ}. Its characteristic is shown in Figure 2-2, f_{GATE} vs. R_{FREQ} diagram, where f_{GATE} = 1/2 f_{OSC}. See Equation 4-1.

EQUATION 4-1:

$$f_{OSC} = \frac{1}{4 \times R_{FREQ} \times C}$$

Where: C = 4.75 pF

4.3 Voltage Reference (V_{REF})

The voltage reference is used by the comparator to compare it with the feedback voltage and the boost converter output. This device provides the options of using either its internal voltage reference or an external voltage reference.

The internal voltage reference provides a stable 1.25V with a tolerance of ±2.5%. With the use of ±1% tolerance feedback resistors, the output can be achieved with a tolerance of ±4.5%. In order to use the internal voltage reference, the EXT_REF pin must be connected to ground.

If the output voltage of the boost converter is required to have high precision and tight tolerance, the external voltage reference can be used to achieve that purpose. The external reference voltage must be between 0.5V and V_{LL}–1.4V and connected to the EXT_REF pin. A single low-to-high transition must be presented at the EN pin to trigger the device to select an external voltage reference. If no enable control signal is available in the application, this signal can be easily mimicked by a simple RC circuit. See Figure 4-2.

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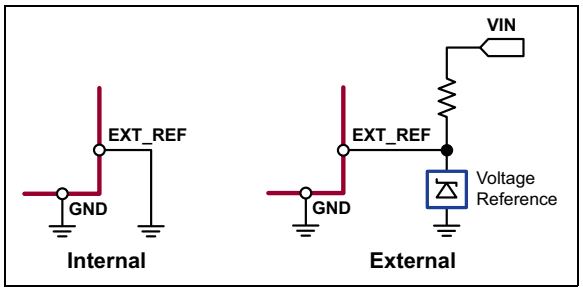


FIGURE 4-2: *Voltage Connection Reference.*

4.4 Gate Driver (Gate)

The MOSFET gate driver of this controller is especially designed to drive the gate of the external MOSFET up to 12V. A high pulse voltage will help minimize the on-resistance of the external MOSFET transistor. A lower on-resistance improves the overall efficiency and heat dissipation.

This gate driver is powered by the supply voltage V_{DD} which can be generated by either the internal charge pump converter (CP mode) or the external power supply (LDO mode), depending on the available voltage supply rail of the application. See **Typical Application Circuits**.

4.5 Charge Pump Converter (CP Mode)

A 3X charge pump converter is integrated into this device to provide a 5V to 12V rail for the gate driver. (See Figure 4-3.) It can be activated by setting CP_EN to ground. A 3.3V supply is more common and easily available for digital logic systems. However, this voltage level is less desirable for driving a high-voltage MOSFET to obtain a lower on-resistance, which improves efficiency.

To reduce the number of supply rails used in the system, an internal two-stage charge pump converter is added, which can boost the 3.3V supply voltage to 8V. Compared to a 3.3V gate driver, an 8V gate driver output will substantially improve the on-resistance of the external MOSFET.

The charge pump input can operate with an input voltage from 2.7V to 4.5V. Its input and output are connected to the V_{LL} and V_{DD} pins, respectively.

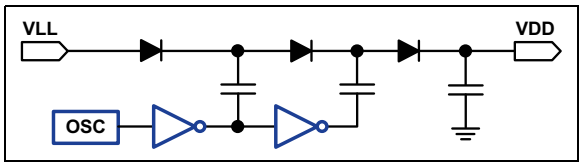


FIGURE 4-3: *A 3X Charge Pump Converter.*

4.6 Linear Regulator (LDO Mode)

In some applications, efficiency may be a key factor, and higher voltage rails such as 5V, 6V, 9V or 12V may be available in the system. The internal charge pump converter cannot operate with these voltage levels because of the maximum output voltage limit of the charge pump converter. At the same time, these voltage levels are high enough to provide adequate supply for the gate driver.

Under this circumstance, an internal linear regulator is used to replace the charge pump converter. This linear regulator input can accept voltage from 5V to 12V and generate a 3.3V output to supply the internal circuit. This linear regulator can be activated by setting CP_EN to V_{LL}.

In a scenario when the device is operating in LDO mode and in Shutdown state (EN = '0'), the voltage at V_{LL} is undefined. To wake up the controller device, a voltage above 2.7V has to be presented at the enable pin (EN).

4.7 FB Ground Return Switch (FB_RTN)

Any DC/DC controller requires feedback from the output to monitor its operation so that it can regulate its output accordingly. A simple resistor network is used in conjunction with a feedback ground switch as a feedback path. The purpose of this feedback ground switch is to save power consumed by the feedback resistor network when the controller is disabled. This function is quite useful for power saving, especially for battery-operated applications.

4.8 Shutdown Timer and Timing Capacitor (C_T)

A shutdown timer is also integrated into the controller for safety purposes. When the controller shuts down from its normal operation, the converter's initial output is still at its high level. If the feedback ground return switch is disabled at the same time, a current path is created from the output via the feedback resistor and the internal protection clamping diode at the FB pin. (See Figure 4-4.) Depending upon the value of the FB resistor, this momentarily conducting current can be high enough to damage this clamping diode. To avoid this potential problem, a timer is added to the disable function to keep the feedback ground switch to on position for a short period of time. This on-time duration is controlled by an external capacitor C_T. The larger the capacitor value is, the longer the on-time is. Its characteristic is shown in Figure 2-3.

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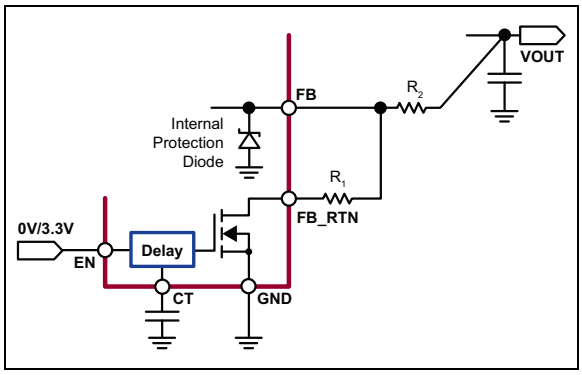


FIGURE 4-4: *Internal Protection Diode at FB Pin.*

4.9 Hysteretic Controller Enable

The controller enable pin (EN), serves two main purposes. The most obvious function is to turn on and off the controller, and the other function is to act as a trigger to activate the device to accept external voltage reference.

For any applications requiring a highly precise voltage reference, an external voltage reference should be used. To activate the device to accept the external voltage reference, a low-to-high transition has to appear at the EN pin while the voltage at the EXT_REF pin is above 0.5V.

If the system lacks enable function control, an RC circuit can be used to mimic this function to allow the external voltage reference. Refer to Figure 4-5.

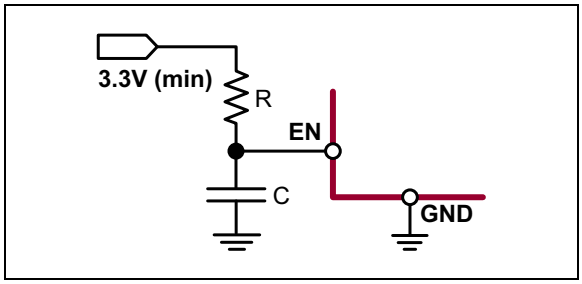


FIGURE 4-5: *Simple RC Circuit for EN Pin.*

4.10 Duty Cycle Control ($V_{CONTROL}$)

The input voltage at the $V_{CONTROL}$ pin manages the duty cycle of the internal oscillator output to the gate driver. All internal comparators are powered by the V_{LL} supply and all their input threshold voltages are referenced to V_{LL} voltage. A voltage divider formed by the two external resistors shown in Figure 4-6 can be adjusted accordingly to select the desired duty cycle of the pulse signal to the gate driver. See Table 4-2.

TABLE 4-2: DUTY CYCLE SELECTION

$V_{CONTROL}$	Duty Cycle
0 V_{LL} to 0.18 V_{LL}	0%
0.22 V_{LL} to 0.38 V_{LL}	50%
0.42 V_{LL} to 0.58 V_{LL}	62.5%
0.62 V_{LL} to 0.78 V_{LL}	75%
0.82 V_{LL} to 1 V_{LL}	87.5%

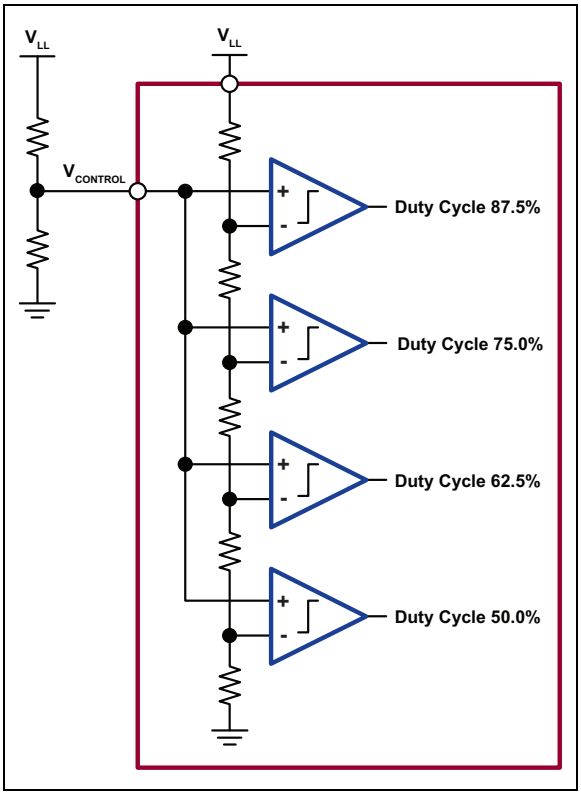


FIGURE 4-6: *Duty Cycle Control Circuit.*

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4.11 Design Procedure

There are several parameters that a user needs to consider for the DC/DC converter design. The input voltage, output voltage and output power requirement are usually defined at the beginning. The other parameters that may be included are: operating frequency, inductor value, duty cycle and the on-resistance of the MOSFET. There is some degree of flexibility in deciding the values of these parameters. The following provides the user a general design approach:

4.11.1 STEP 1

Since this DC/DC controller device is operating in a Discontinuous Conduction mode, determine the inductance and the switching frequency with Equation 4-2.

EQUATION 4-2:

Given:

D = Duty cycle
R = Load resistance of the high voltage output
V_i = Minimum input voltage
V_o = Output voltage

Unknown:

L = Inductance
f_{GATE} = Driver switching frequency

Where:

$$V_o = \frac{V_i}{2} \times \left(1 + \sqrt{1 + \frac{4D^2}{K}}\right)$$

$$K = \frac{2 \times L \times f_{GATE}}{R}$$

The maximum duty cycle can be computed with Equation 4-3.

EQUATION 4-3:

$$D_{MAX} = 1 - \frac{V_i}{V_o}$$

Then, the user can select any duty cycle less than D_{MAX}. Choosing the largest possible setting is highly recommended.

To compensate for the limited efficiency, the user can add the efficiency factor into the load resistance R. With the above equation, the product of L and f_{GATE} is determined. The product will also limit the design.

4.11.2 STEP 2

The standard inductor is usually sold in an incremental inductance value, for example, 10 µH, 22 µH, 33 µH or 47 µH. The user can choose the inductance based on the size of the inductor, the peak current, the maximum operating frequency and the DC resistance. After the value of L is decided, the gate driver switching frequency can be computed. The required R_{FREQ} resistance can be found in the f_{GATE} vs. R_{FREQ} diagram. (See Figure 2-2.) Next, the user may check the peak current of the inductor with Equation 4-4. The saturation current of the inductor must be larger than I_{PEAK}.

EQUATION 4-4:

$$I_{PEAK} = \frac{V_i \times D}{L \times f_{GATE}}$$

4.11.3 STEP 3

The most important factors in determining the MOSFET are the breakdown voltage, the current capability, the on-resistance, the minimum V_{GS} threshold voltage and the input capacitance.

The HV9150 gate driver is designed to drive a maximum of 300 pF capacitive load. Therefore, the maximum input capacitance of the external MOSFET should be less than 300 pF. The minimum breakdown voltage must be larger than the required DC/DC converter output voltage. If the breakdown voltage is too low, the output will never reach the required voltage output. A MOSFET with high on-resistance will limit the peak current charging the inductor. The user can use a simple RL charging circuit equation to determine its final charging current. See Equation 4-5.

EQUATION 4-5:

$$I_L = \frac{V_i}{R_{ON}}\left[1 - \exp\left(-\frac{D}{f_{GATE}} \times \frac{R_{ON}}{L}\right)\right]$$

It is recommended that the calculated value of I_L is within 95% of the I_{PEAK} calculated in Equation 4-4. An on-resistance of less than 1Ω is usually a good starting point.

If the final circuit is short on the output current capability, the user can do any or all of the following to boost the output:

1. Increase the duty cycle.
2. Decrease the f_{GATE}.
3. Use a MOSFET with lower on-resistance.

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NOTES:

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5.0 PACKAGE MARKING INFORMATION

5.1 Packaging Information

16-lead QFN



Example

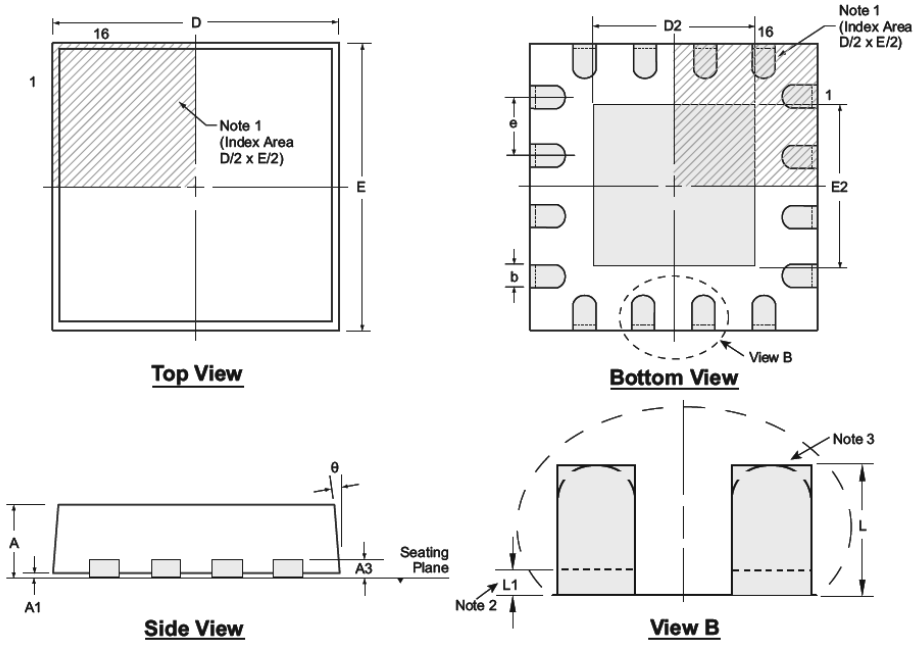


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

16-Lead QFN Package Outline (K6)

3.00x3.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	2.85*	1.50	2.85*	1.50	0.50 BSC	0.20†	0.00	0°
	NOM	0.90	0.02		0.25	3.00	1.65	3.00	1.65		0.30†	-	-
	MAX	1.00	0.05		0.30	3.15*	1.80	3.15*	1.80		0.45	0.15	14°

JEDEC Registration MO-220, Variation VEED-4, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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APPENDIX A: REVISION HISTORY

Revision B (March 2019)

- Updated **AC Electrical Characteristics** table.

Revision A (February 2017)

- Converted Supertex Doc# DSFP-HV9150 to Microchip DS20005689B
- Changed the quantity of the 16-lead QFN K6 package from 3000/Reel to 3300/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9150	=	High-Voltage Output Hysteretic-Mode Step-Up DC/DC Controller
Package:	K6	=	16-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3300/Reel for a K6 Package

Example:

a) HV9150K6-G: High-Voltage Output Hysteretic-Mode Step-Up DC/DC Controller, 16-lead VQFN Package, 3300/Reel

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