TMPx75-Q1 Automotive Grade Temperature Sensor With I²C and SMBus Interface in Industry-Standard LM75 Form Factor and Pinout

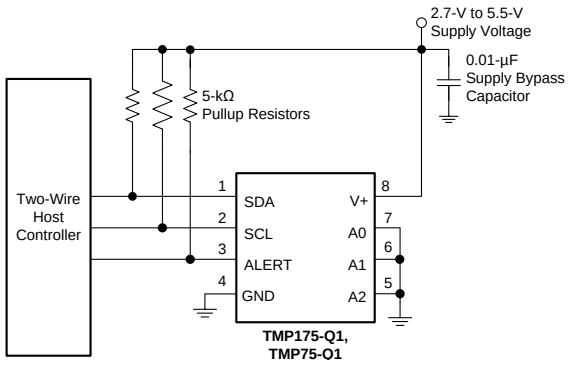
1 Features

- AEC-Q100 Qualified with:
  - Temperature Grade 1: –40°C to +125°C Ambient Operation Temperature Range
  - HBM ESD Classification Level 2
  - CDM ESD Classification Level C6
- TMP175-Q1 Accuracy:
  - ±1°C (Typical) from –40°C to +125°C
  - ±2°C (Maximum) from –40°C to +125°C
- TMP75-Q1 Accuracy:
  - ±1°C (Typical) from –40°C to +125°C
  - ±3°C (Maximum) from –40°C to +125°C
- TMP175-Q1: 27 Addresses
- TMP75-Q1: 8 Addresses, NIST Traceable
- Digital Output: SMBus™, Two-Wire, and I²C Interface Compatibility
- Resolution: 9 to 12 Bits, User-Selectable
- Low Quiescent Current: 50-µA, 0.1-µA Standby
- Wide Supply Range: 2.7 V to 5.5 V
- Small 8-Pin VSSOP and 8-Pin SOIC Packages

2 Applications

- Climate Controls
- Infotainment Processor Management
- Airflow Sensors
- Battery Control Units
- Engine Control Units
- UREA Sensors
- Water Pumps
- HID Lamps
- Airbag Control Units

Simplified Schematic



3 Description

The TMP75-Q1 and TMP175-Q1 devices are digital temperature sensors ideal for negative temperature coefficient (NTC) and positive temperature coefficient (PTC) thermistor replacement. The devices offer a typical accuracy of ±1°C without requiring calibration or external component signal conditioning. Device temperature sensors are highly linear and do not require complex calculations or look-up tables to derive the temperature. The on-chip, 12-bit, analog-to-digital converter (ADC) offers resolutions down to 0.0625°C. The devices are available in the industry-standard, LM75, 8-pin SOIC and VSSOP footprint.

The TMP175-Q1 and TMP75-Q1 feature SMBus, two-wire, and I²C interface compatibility. The TMP175-Q1 device allows up to 27 devices on one bus. The TMP75-Q1 allows up to eight devices on one bus. The TMP175-Q1 and TMP75-Q1 both feature an SMBus alert function.

The TMP175-Q1 and TMP75-Q1 devices are ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications. The TMP75-Q1 production units are 100% tested against sensors that are NIST-traceable and are verified with equipment that are NIST-traceable through ISO/IEC 17025 accredited calibrations.

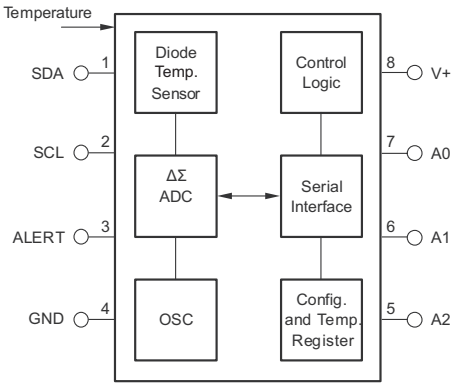
The TMP175-Q1 and TMP75-Q1 devices are specified for operation over the temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMPx75-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TMP175-Q1 and TMP75-Q1 Internal Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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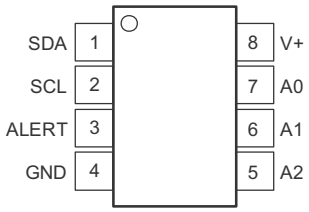
4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release.

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5 Pin Configuration and Functions

DGK, D Packages
8-Pin VSSOP, SOIC
Top View



NOTE: Pin 1 is determined by orienting the package marking as indicated in the diagram.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.
2	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.
3	ALERT	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
4	GND	—	Ground
5	A2	I	Address select. Connect to GND, V+, or (for the TMP175-Q1 device only) leave these pins floating.
6	A1		
7	A0		
8	V+	I	Supply voltage, 2.7 V to 5.5 V

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply, V+		7	V
Input voltage(2)	–0.5	7	V
Input current		10	mA
Operating temperature	–55	127	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltage rating applies to all TMP175-Q1 and TMP75-Q1 input voltages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	2.7		5.5	V
Operating free-air temperature, T_A	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP175-Q1, TMP75-Q1 DGK (SOIC), D (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	104.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

at T_A = –40°C to +125°C and V+ = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE INPUT								
	Range				–40		125	°C
	Accuracy (temperature error)		–25°C to +85°C	TMP175-Q1		±0.5	±1.5	°C
				TMP75-Q1		±0.5	±2	
			–40°C to +125°C	TMP175-Q1		±1	±2	
				TMP75-Q1		±1	±3	
	Accuracy (temperature error) vs supply					0.2	±0.5	°C/V
	Resolution(1)		Selectable			0.0625		°C
DIGITAL INPUT/OUTPUT								
	Input capacitance					3		pF
V_{IH}	High-level input logic				0.7 (V+)		6	V
V_{IL}	Low-level input logic				–0.5		0.3 (V+)	V
I_{IN}	Leakage input current		0 V ≤ V_{IN} ≤ 6 V				1	µA
	Input voltage hysteresis		SCL and SDA pins			500		mV
V_{OL}	Low-level output logic	SDA	I_{OL} = 3 mA		0	0.15	0.4	V
		ALERT	I_{OL} = 4 mA		0	0.15	0.4	
	Resolution		Selectable			9 to 12		Bits
	Conversion time		9 bits			27.5	37.5	ms
			10 bits			55	75	
			11 bits			110	150	
			12 bits			220	300	
	Timeout time				25	54	74	ms
POWER SUPPLY								
	Operating range				2.7		5.5	V
I_Q	Quiescent current		Serial bus inactive			50	85	µA
			Serial bus active, SCL frequency = 400 kHz			100		
			Serial bus active, SCL frequency = 3.4 MHz			410		
I_{SD}	Shutdown current		Serial bus inactive			0.1	3	µA
			Serial bus active, SCL frequency = 400 kHz			60		
			Serial bus active, SCL frequency = 3.4 MHz			380		
TEMPERATURE RANGE								
	Specified range				–40		125	°C
	Operating range				–55		127	°C

(1) Specified for 12-bit resolution.

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6.6 Timing Requirements

see the *Timing Diagrams* and *Two-Wire Timing Diagrams* sections for additional information(1)

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	V+	0.001	0.4	0.001	2.38	MHz
$t_{(BUF)}$	Bus-free time between STOP and START condition	See the *Timing Diagrams* section	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time		4	900	4	120	ns
$t_{(SUDAT)}$	Data setup time		100		10		ns
$t_{(LOW)}$	SCL clock low period	V+ , see the *Timing Diagrams* section	1300		280		ns
$t_{(HIGH)}$	SCL clock high period	See the *Timing Diagrams* section	600		60		ns
t_FD	Data fall time	See the *Timing Diagrams* section		300		150	ns
t_RC	Clock rise time	See the *Two-Wire Timing Diagrams* section		300		40	ns
		SCLK ≤ 100 kHz, see the *Timing Diagrams* section		1000			ns
t_FC	Clock fall time	See the *Two-Wire Timing Diagrams* section		300		40	ns

(1) Values are based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not specified and are not production tested.

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6.7 Typical Characteristics

at T_A = 25°C and V+ = 5 V (unless otherwise noted)

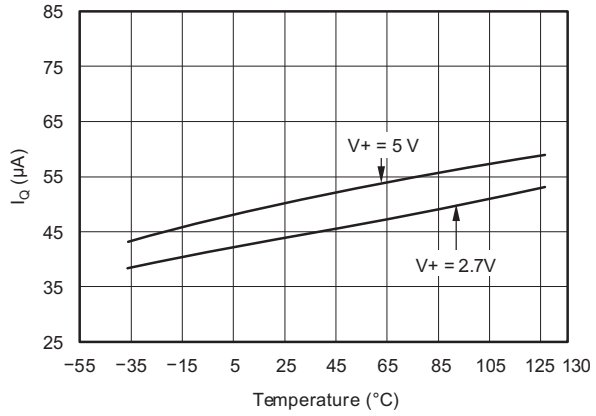


Figure 1. Quiescent Current vs Temperature

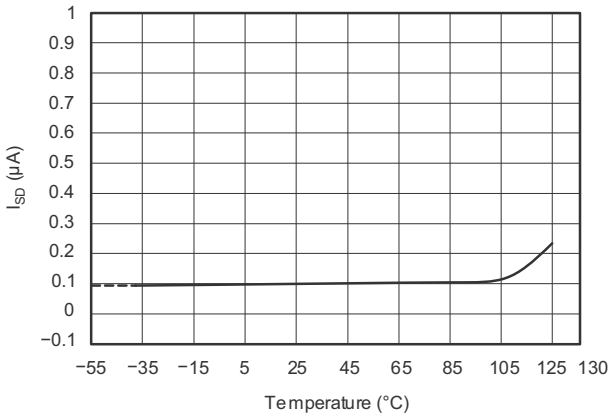


Figure 2. Shutdown Current vs Temperature

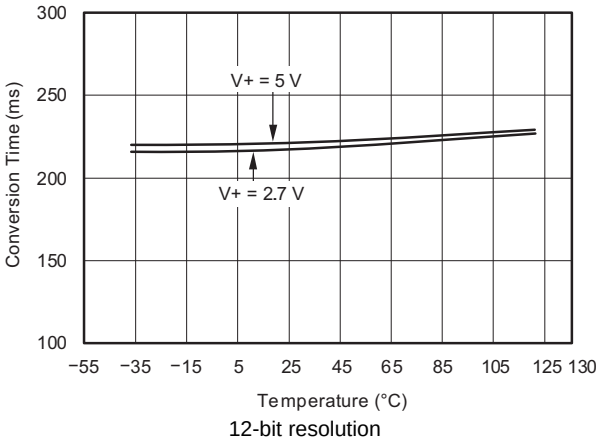


Figure 3. Conversion Time vs Temperature

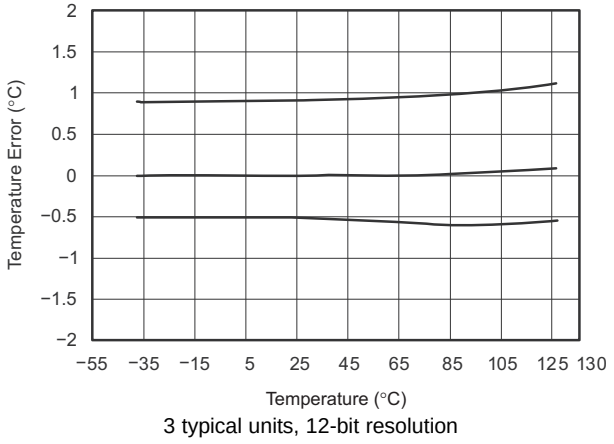


Figure 4. Temperature Error vs Temperature

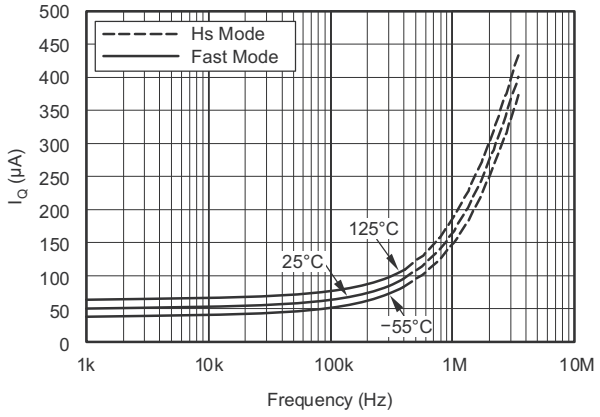


Figure 5. Quiescent Current With Bus Activity vs Temperature

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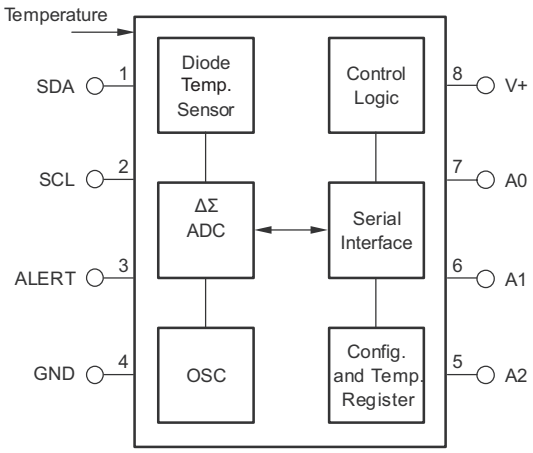
7 Detailed Description

7.1 Overview

The TMP175-Q1 and TMP75-Q1 devices are digital temperature sensors that are optimal for thermal management and thermal protection applications. The TMP175-Q1 and TMP75-Q1 are two-wire, SMBus, and I^2C interface compatible. The devices are specified over a temperature range of –40°C to +125°C. The *Functional Block Diagram* section shows the internal block diagram of the TMP175-Q1 and TMP75-Q1 devices.

The temperature sensor in the TMP175-Q1 and TMP75-Q1 devices is the chip itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only Temperature register. The Temperature register of the TMP175-Q1 or TMP75-Q1 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 6 and Table 7. The first 12 bits are used to indicate temperature with all remaining bits equal to zero. The data format for temperature is listed in Table 1. Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits (MSBs) in the Temperature register are used with the unused least significant bits (LSBs) set to zero.

Table 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

7.3.2 Serial Interface

The TMP175-Q1 and TMP75-Q1 operate only as slave devices on the SMBus, two-wire, and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP175-Q1 and TMP75-Q1 support the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2.38-MHz) modes. All data bytes are transmitted MSB first.

7.3.2.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device a START condition is initiated, indicated by pulling the data line (SDA) from a high to a low logic level when SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the master generates a STOP condition indicated by pulling SDA from low to high when SCL is high.

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7.3.2.2 Serial Bus Address

To communicate with the TMP175-Q1 and TMP75-Q1, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP175-Q1 features three address pins to allow up to 27 devices to be addressed on a single bus interface. Table 2 describes the pin logic levels used to properly connect up to 27 devices. A 1 indicates that the pin is connected to the supply (VCC) and a 0 indicates that the pin is connected to GND; *float* indicates that the pin is left unconnected. The state of the A0, A1, and A2 pins is sampled on every bus communication and must be set prior to any activity on the interface.

Table 2. Address Pins and Slave Addresses for the TMP175-Q1

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111
Float	0	0	1110000
Float	0	Float	1110001
Float	0	1	1110010
Float	1	0	1110011
Float	1	Float	1110100
Float	1	1	1110101
Float	Float	0	1110110
Float	Float	1	1110111
0	Float	0	0101000
0	Float	1	0101001
1	Float	0	0101010
1	Float	1	0101011
0	0	Float	0101100
0	1	Float	0101101
1	0	Float	0101110
1	1	Float	0101111
0	Float	Float	0110101
1	Float	Float	0110110
Float	Float	Float	0110111

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The TMP75-Q1 features three address pins, allowing up to eight devices to be connected per bus. Pin logic levels are described in Table 3. The address pins of the TMP175-Q1 and TMP75-Q1 are read after reset, at start of communication, or in response to a two-wire address acquire request. After the state of the pins are read, the address is latched to minimize power dissipation associated with detection.

Table 3. Address Pins and Slave Addresses for the TMP75-Q1

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

7.3.2.3 Writing and Reading to the TMP175-Q1 and TMP75-Q1

Accessing a particular register on the TMP175-Q1 and TMP75-Q1 devices is accomplished by writing the appropriate value to the Pointer register. The value for the Pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP175-Q1 and TMP75-Q1 requires a value for the Pointer register (see Figure 7).

When reading from the TMP175-Q1 and TMP75-Q1 devices, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command; see Figure 9 for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the TMP175-Q1 and TMP75-Q1 remember the Pointer register value until it is changed by the next write operation.

Register bytes are sent MSB first, followed by the LSB.

7.3.2.4 Slave Mode Operations

The TMP175-Q1 and TMP75-Q1 can operate as a slave receiver or slave transmitter.

7.3.2.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP175-Q1 or TMP75-Q1 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer register. The TMP175-Q1 or TMP75-Q1 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP175-Q1 and TMP75-Q1 acknowledge reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

7.3.2.4.2 Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a Not-Acknowledge bit on reception of any data byte, or by generating a START or STOP condition.

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7.3.2.5 SMBus Alert Function

The TMP175-Q1 and TMP75-Q1 support the SMBus alert function. When the TMP75-Q1 and TMP175-Q1 are operating in interrupt mode (TM = 1), the ALERT pin of the TMP75-Q1 or TMP175-Q1 can be connected as an SMBus alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP75-Q1 or TMP175-Q1 is active, the devices acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit is high if the temperature is greater than or equal to T_{HIGH}. This bit is low if the temperature is less than T_{LOW}; see Figure 10 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its ALERT status. If the TMP75-Q1 or TMP175-Q1 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP75-Q1 or TMP175-Q1 loses the arbitration, its ALERT pin remains active.

7.3.2.6 General Call

The TMP175-Q1 and TMP75-Q1 respond to a two-wire, general-call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP175-Q1 and TMP75-Q1 latches the status of their address pins, but do not reset. If the second byte is 00000110, the TMP175-Q1 and TMP75-Q1 latches the status of their address pins and resets their internal registers to their power-up values.

7.3.2.7 High-Speed Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP175-Q1 and TMP75-Q1 devices do not acknowledge this byte, but do switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 2.38 MHz. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP175-Q1 and TMP75-Q1 switch the input and output filter back to fast-mode operation.

7.3.2.8 Time-out Function

The TMP175-Q1 resets the serial interface if either SCL or SDA is held low for 54 ms (typical) between a START and STOP condition. The TMP175-Q1 releases the bus if it is pulled low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained for the SCL operating frequency.

7.3.3 Timing Diagrams

The TMP175-Q1 and TMP75-Q1 devices are two-wire, SMBus, and I^2C interface compatible. Figure 6 to Figure 10 describe the various operations on the TMP175-Q1. The following list provides bus definitions. Parameters for Figure 6 are defined in the *Timing Requirements* table.

Bus Idle: Both the SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge bit on the last byte that is transmitted by the slave.

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7.3.3.1 Two-Wire Timing Diagrams

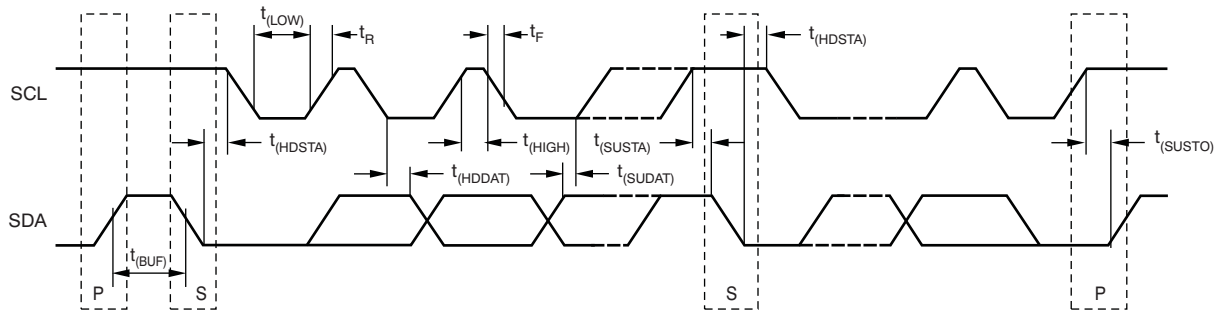


Figure 6. Two-Wire Timing Diagram

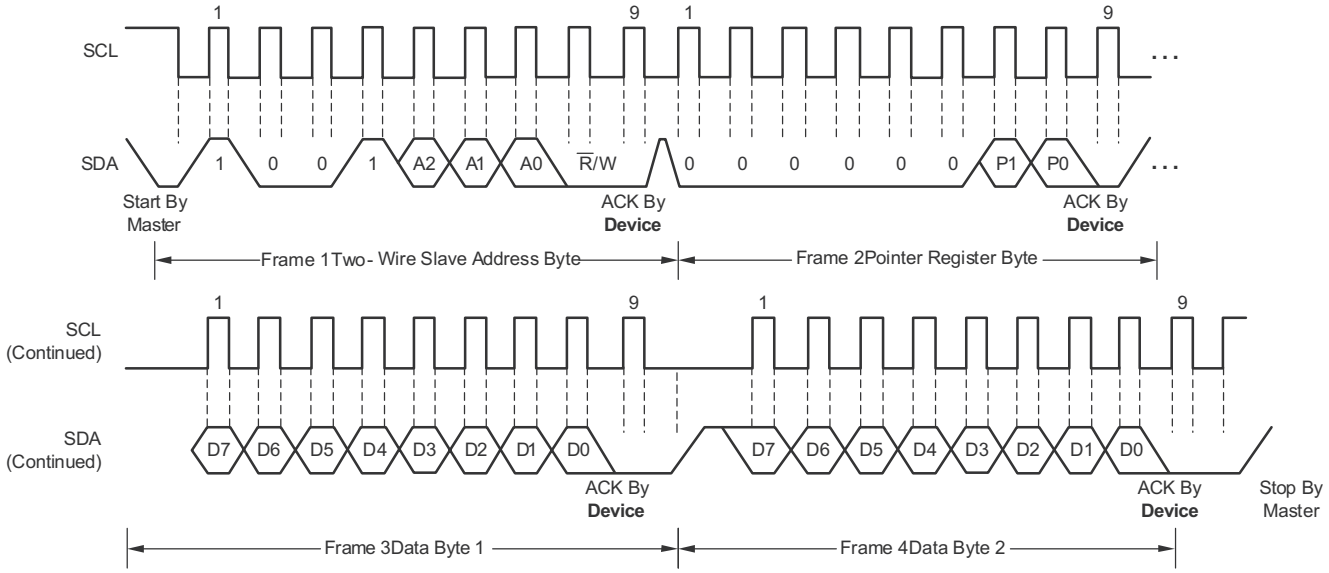


Figure 7. Two-Wire Timing Diagram for the TMP75-Q1 Write Word Format

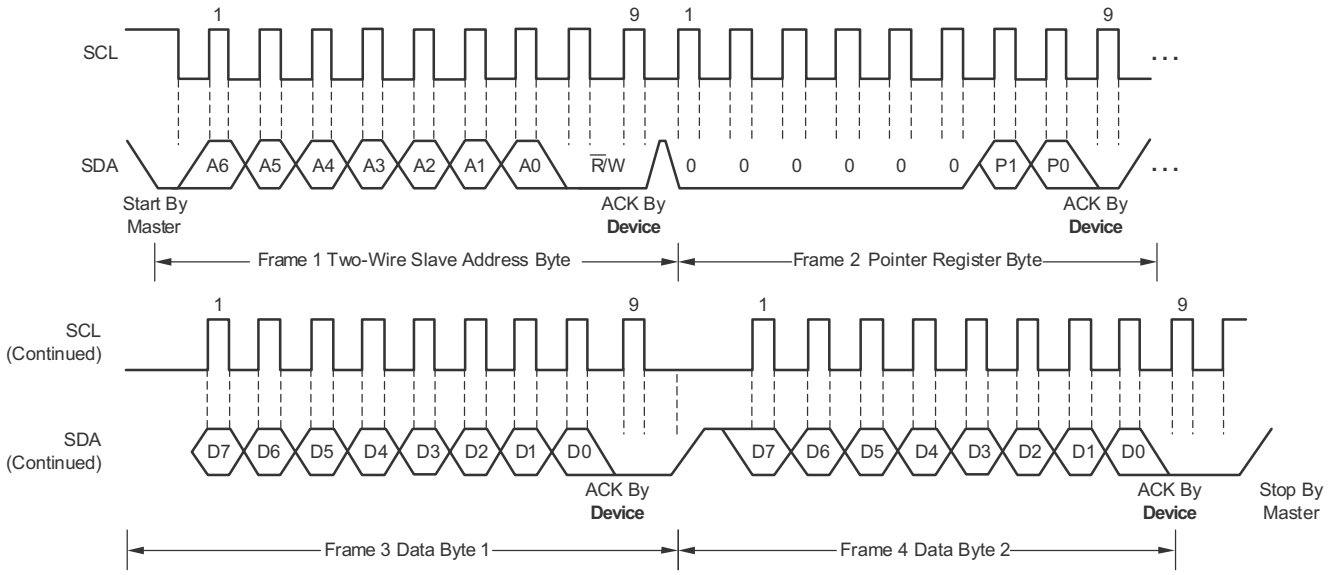
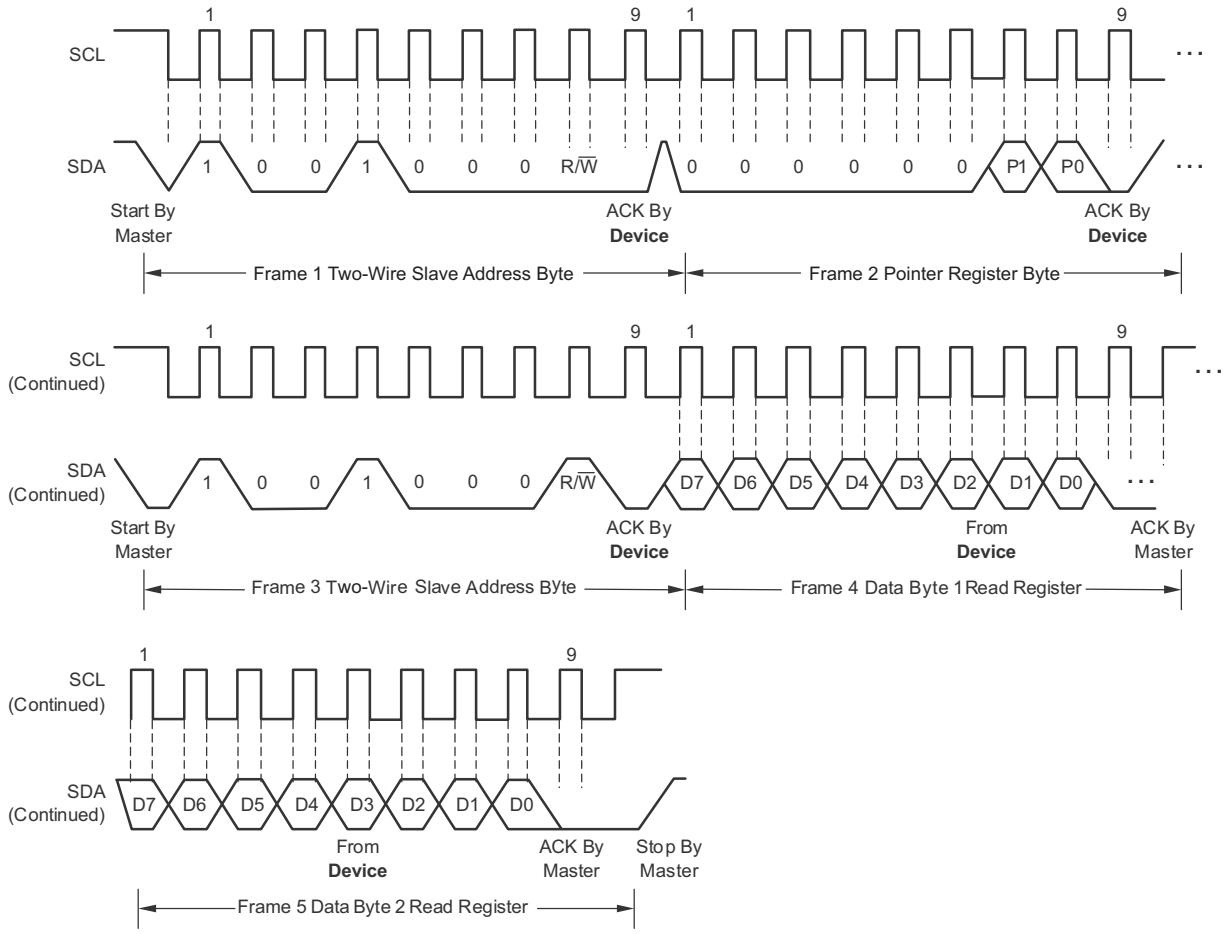


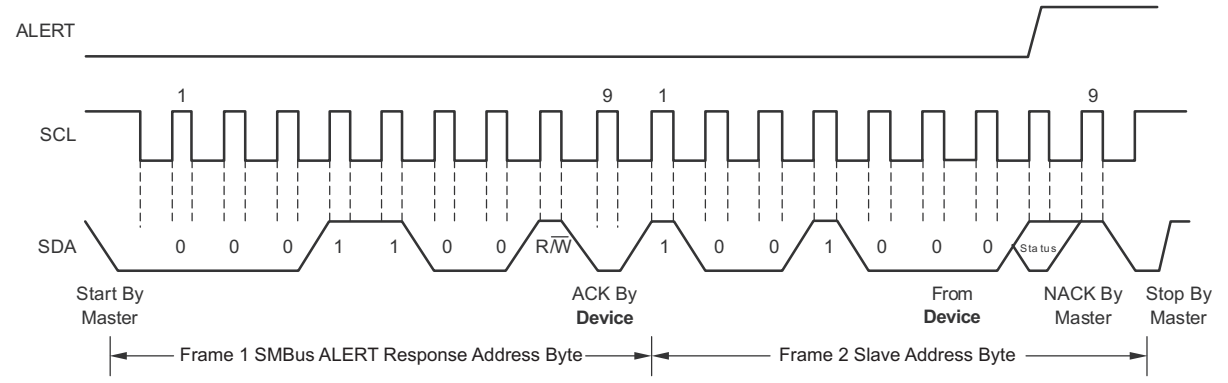
Figure 8. Two-Wire Timing Diagram for the TMP175-Q1 Write Word Format

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NOTE: Address pins A0, A1, and A2 = 0.

Figure 9. Two-Wire Timing Diagram for Read Word Format



NOTE: Address pins A0, A1, and A2 = 0.

Figure 10. Timing Diagram for SMBus ALERT

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7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

The shutdown mode of the TMP175-Q1 and TMP75-Q1 devices lets the user save maximum power by shutting down all device circuitry other than the serial interface, thus reducing current consumption to typically less than 0.1 µA. Shutdown mode is enabled when the SD bit is 1; the device shuts down when the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

7.4.2 One-Shot (OS)

The TMP175-Q1 and TMP75-Q1 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP175-Q1 and TMP75-Q1 when continuous temperature monitoring is not required. When the configuration register is read, OS always reads zero.

7.4.3 Thermostat Mode (TM)

The thermostat mode bit of the TMP175-Q1 and TMP75-Q1 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

7.4.3.1 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and remains active until the temperature falls below the value in the $T_{(LOW)}$ register. For more information on the comparator mode, see the *High- and Low-Limit Registers* section.

7.4.3.2 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds $T_{(HIGH)}$ or goes below the $T_{(LOW)}$ registers. The ALERT pin is cleared when the host controller reads the Temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Registers* section.

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7.5 Programming

7.5.1 Pointer Register

Figure 11 shows the internal register structure of the TMP175-Q1 and TMP75-Q1. The 8-bit Pointer register of the devices is used to address a given data register. The Pointer register uses the two LSBs to identify which of the data registers must respond to a read or write command. Table 4 identifies the bits of the Pointer register byte. Table 5 describes the pointer address of the registers available in the TMP175-Q1 and TMP75-Q1. The power-up reset value of P1/P0 is 00.

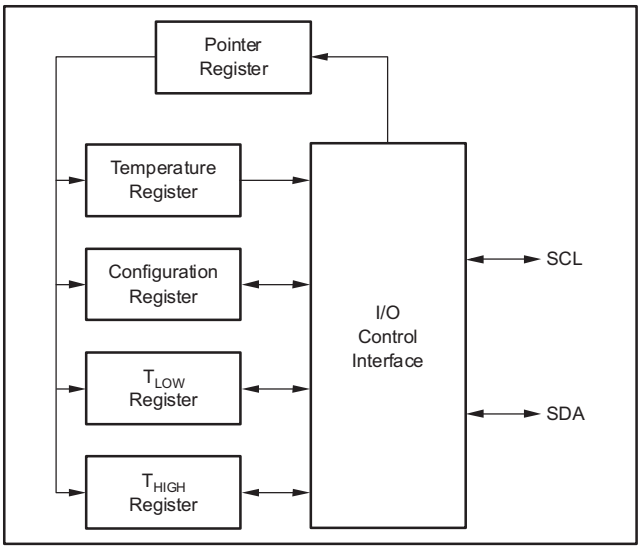


Figure 11. Internal Register Structure of the TMP175-Q1 and TMP75-Q1

Table 4. Pointer Register Byte (pointer = N/A) [reset = 00h]

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 5. Pointer Addresses of the TMP175-Q1 and TMP75-Q1

P1	P0	TYPE	REGISTER
0	0	R only, default	Temperature register
0	1	R/W	Configuration register
1	0	R/W	T_{LOW} register
1	1	R/W	T_{HIGH} register

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7.5.2 Temperature Register

The Temperature register of the TMP175-Q1 or TMP75-Q1 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are described in Table 6 and Table 7. Byte 1 is the most significant byte and is followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Following the power-up or reset value, the Temperature register reads 0°C until the first conversion is complete.

Table 6. Byte 1 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 7. Byte 2 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

7.5.3 Configuration Register

The Configuration register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the TMP175-Q1 and TMP75-Q1 is shown in Table 8, followed by a breakdown of the register bits. The power-up or reset value of the Configuration register are all bits equal to 0.

Table 8. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

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7.5.3.1 Polarity (POL)

The Polarity bit of the TMP175-Q1 lets the user adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When the POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is shown in Figure 12.

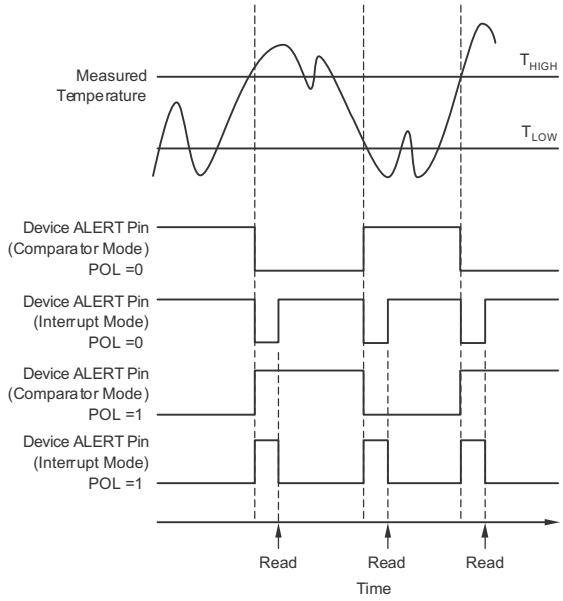


Figure 12. Output Transfer Function Diagrams

7.5.3.2 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert can be programmed using the fault queue. The fault queue is provided to prevent a false alert resulting from environmental noise. The fault queue requires consecutive fault measurements in order to trigger the Alert function. Table 9 defines the number of measured faults that can be programmed to trigger an Alert condition in the device. For the T_{HIGH} and T_{LOW} register format and byte order, see the *High- and Low-Limit Registers* section.

Table 9. Fault Settings of the TMP175-Q1 and TMP75-Q1

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

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7.5.3.3 Converter Resolution (R1/R0)

The Converter Resolution bits control the resolution of the internal analog-to-digital (ADC) converter. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 10 identifies the resolution bits and the relationship between resolution and conversion time.

Table 10. Resolution of the TMP175-Q1 and TMP75-Q1

R1	R0	RESOLUTION	CONVERSION TIME (Typical)
0	0	9 bits (0.5°C)	27.5 ms
0	1	10 bits (0.25°C)	55 ms
1	0	11 bits (0.125°C)	110 ms
1	1	12 bits (0.0625°C)	220 ms

7.5.4 High- and Low-Limit Registers

In comparator mode (TM = 0), the ALERT pin of the TMP175-Q1 and TMP75-Q1 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When cleared, the ALERT pin only becomes active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General-Call Reset command. This action also clears the state of the internal registers in the device, returning the device to comparator mode (TM = 0).

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Both operational modes are represented in Figure 12. Table 11, Table 12, Table 13, and Table 14 describe the format for the T_{HIGH} and T_{LOW} registers. The most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are:

T_{HIGH} = 80°C and T_{LOW} = 75°C

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature register.

Table 11. Byte 1 of the T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4

Table 12. Byte 2 of the T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H3	H2	H1	H0	0	0	0	0

Table 13. Byte 1 of the T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

Table 14. Byte 2 of the T_{LOW} Register

D7	D6	D5	D4	D3	D2	D1	D0
L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the Alert function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the Alert output even if the converter is configured for 9-bit resolution.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP175-Q1 and TMP75-Q1 devices are used to measure the printed circuit board (PCB) temperature of where the device is mounted. The TMP175-Q1 and TMP75-Q1 feature SMBus, two-wire, and I^2C interface compatibility, with the TMP175-Q1 allowing up to 27 devices on one bus and the TMP75-Q1 allowing up to eight devices on one bus. The TMP175-Q1 and TMP75-Q1 both feature a SMBus Alert function. The TMP175-Q1 and TMP75-Q1 require no external components for operation except for pullup resistors on SCL, SDA, and ALERT, although a 0.1-µF bypass capacitor is recommended.

The sensing device of the TMP175-Q1 and TMP75-Q1 devices is the device itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

8.2 Typical Application

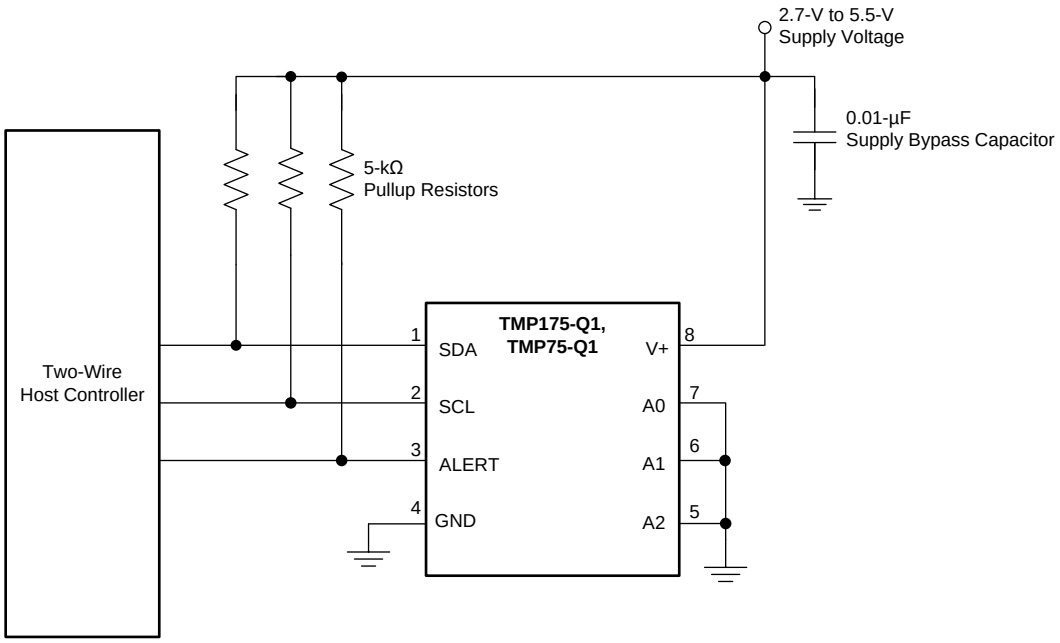


Figure 13. Typical Connections of the TMP175-Q1 and TMP75-Q1

8.2.1 Design Requirements

The TMP175-Q1 and TMP75-Q1 devices requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistor is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ, but must not exceed 3 mA of current on the SCL and SDA pins and must not exceed 4 mA on the ALERT pin. A 0.1-µF bypass capacitor is recommended, as shown in Figure 13. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V_S through the pullup resistors. For the TMP175-Q1, to configure one of 27 different addresses on the bus, connect A0, A1, and A2 to either the GND or the V+ pin or float these pins. Float indicates that the pin is left unconnected. For the TMP75-Q1, to configure one of eight different addresses on the bus, connect A0, A1, and A2 to either the GND or V+ pin.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

Place the TMP175-Q1 and TMP75-Q1 devices in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

8.2.3 Application Curve

Figure 14 shows the step response of the TMP175-Q1 and TMP75-Q1 devices to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 s. The time-constant result depends on the PCB where the TMPx175 devices are mounted. For this test, the TMP175-Q1 and TMP75-Q1 devices were soldered to a two-layer PCB that measured 0.375 inches × 0.437 inches.

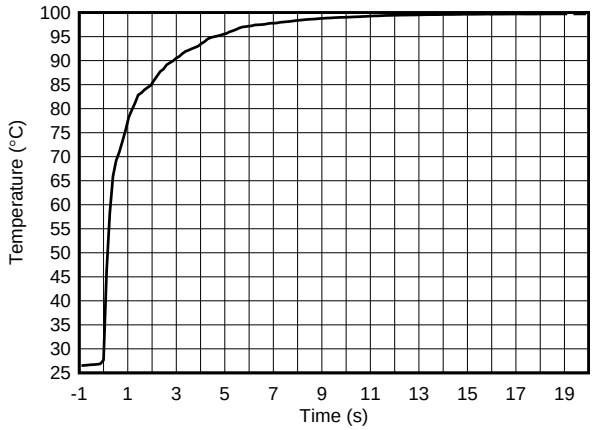


Figure 14. Temperature Step Response

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9 Power Supply Recommendations

The TMP175-Q1 and TMP75-Q1 devices operate with power supplies in the range of 2.7 V to 5.5 V. A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins SDA, SCL, and ALERT through 5-kΩ pullup resistors.

10.2 Layout Example

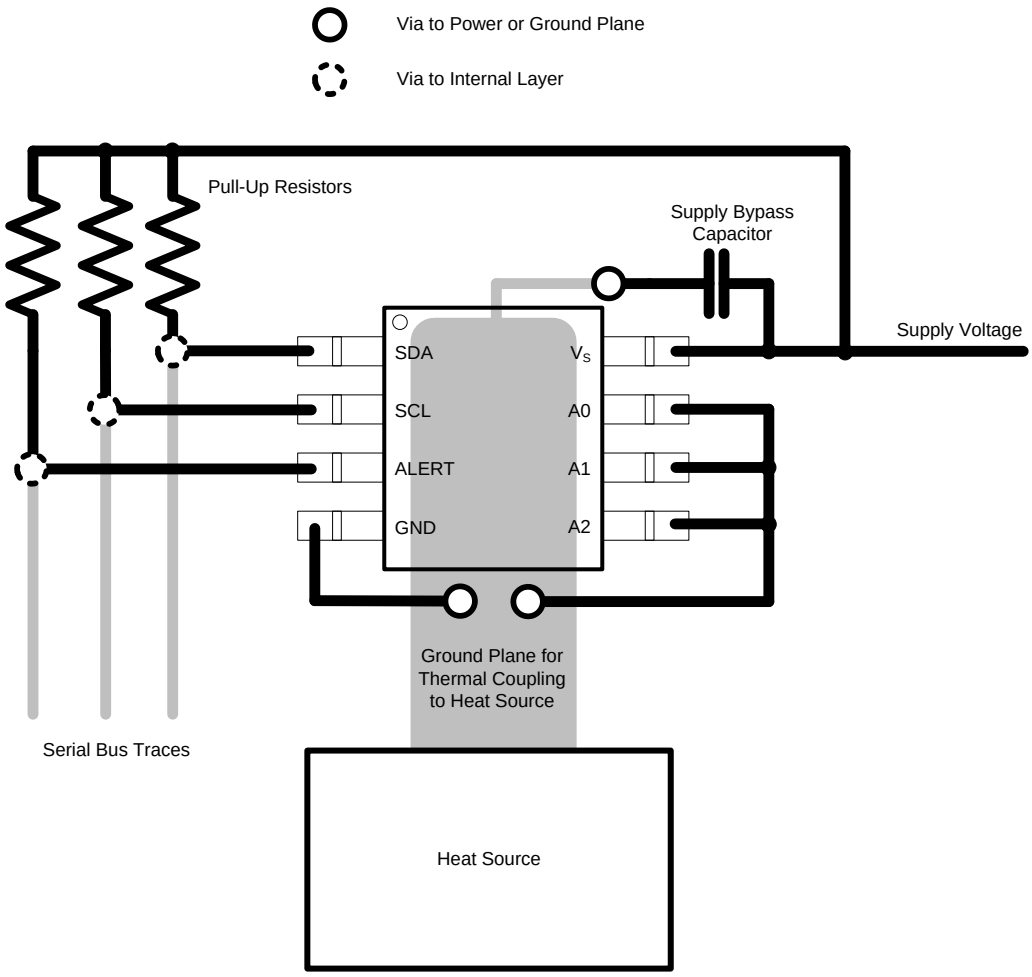


Figure 15. Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 15. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMP175-Q1	Click here	Click here	Click here	Click here	Click here
TMP75-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
SMBus is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP175AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	175Q	Samples
TMP175AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T175Q1	Samples
TMP75AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	75Q1	Samples
TMP75AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T75Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

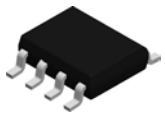
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP175-Q1, TMP75-Q1 :

- Catalog: TMP175, TMP75

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

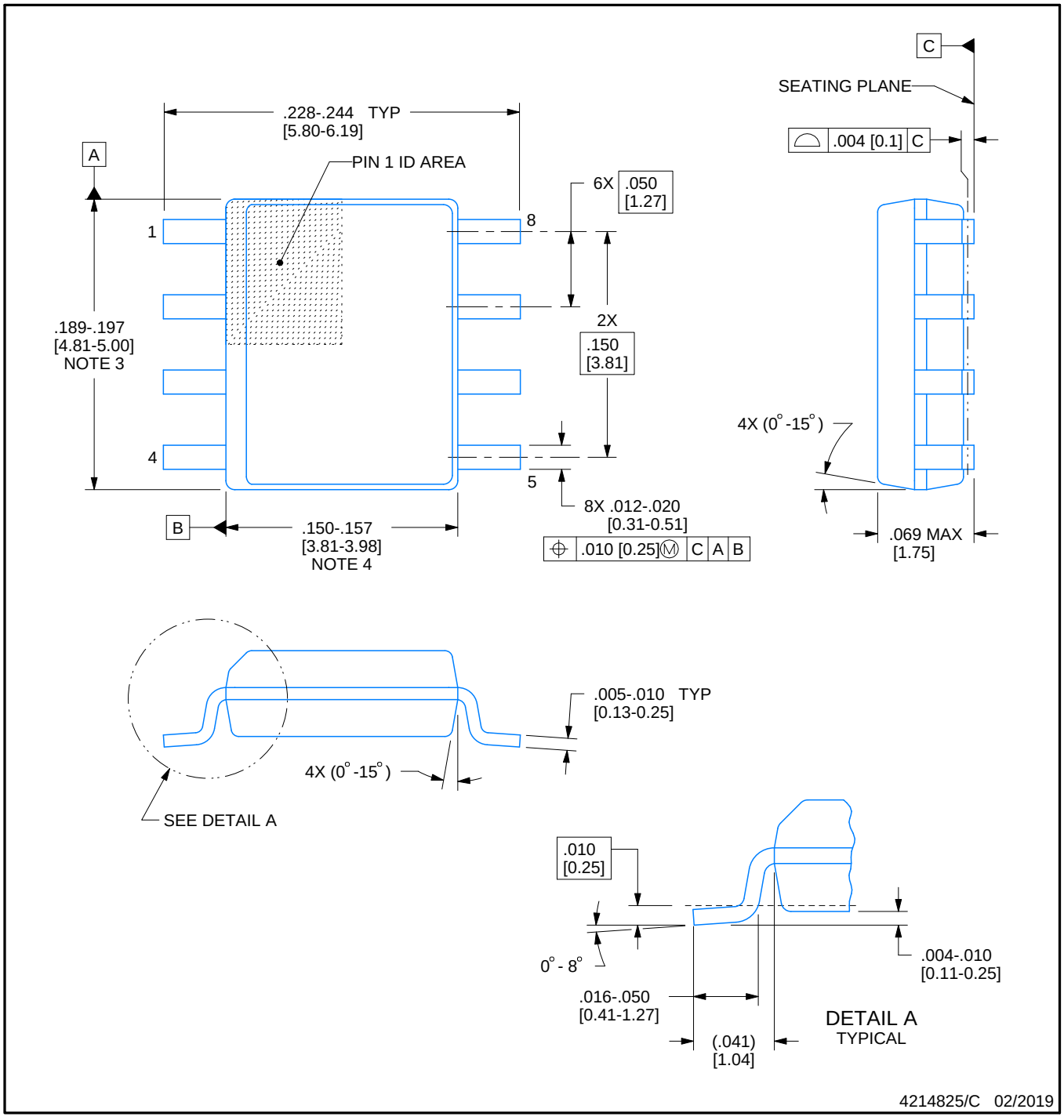


PACKAGE OUTLINE

D0008A

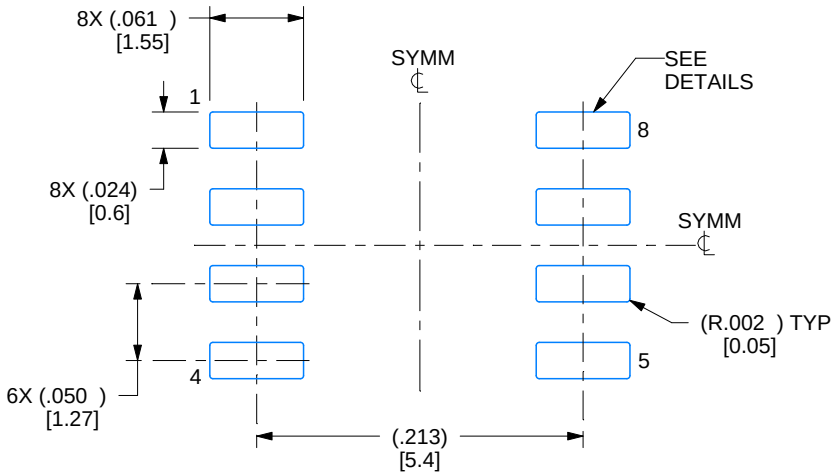
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

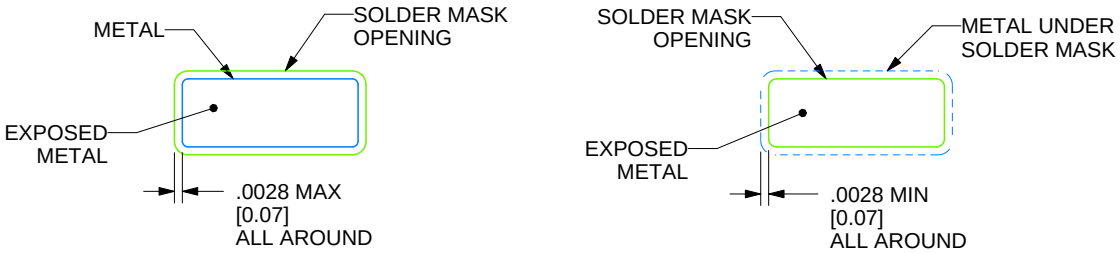


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

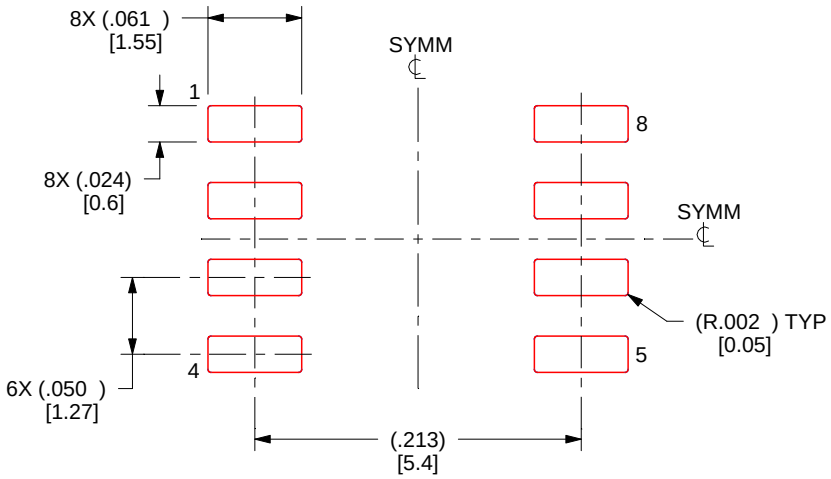
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



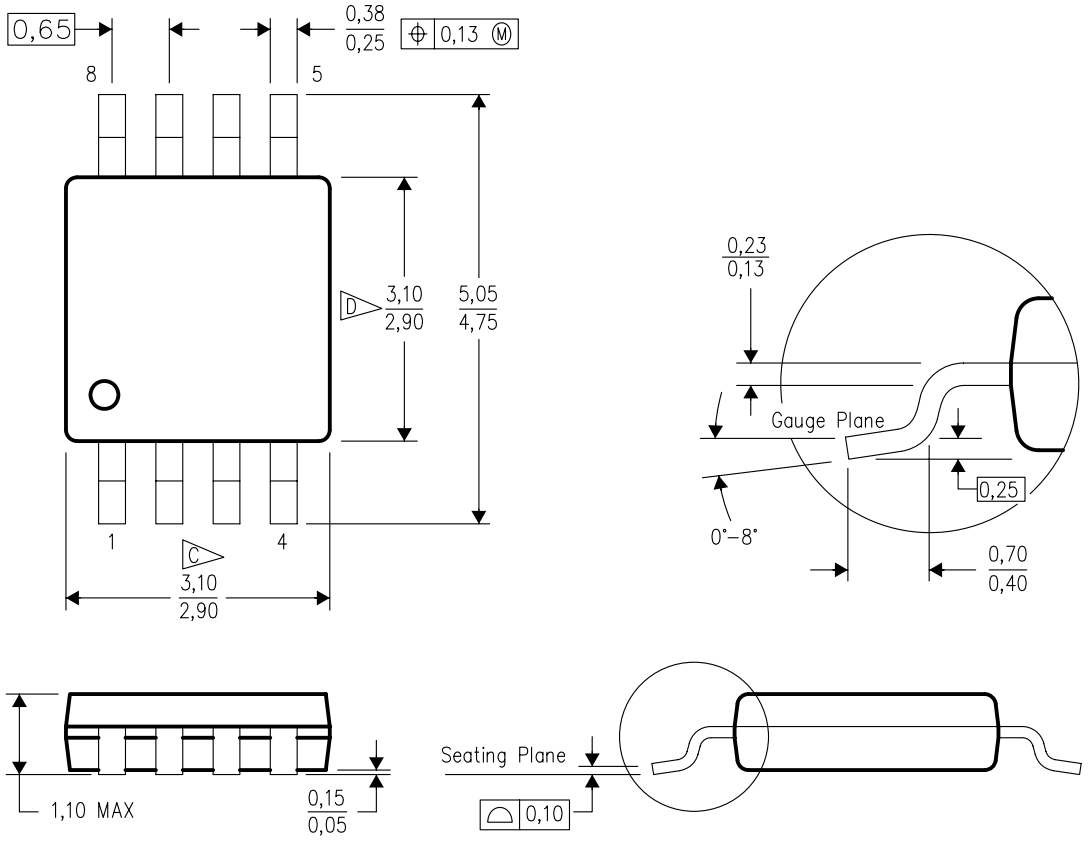
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

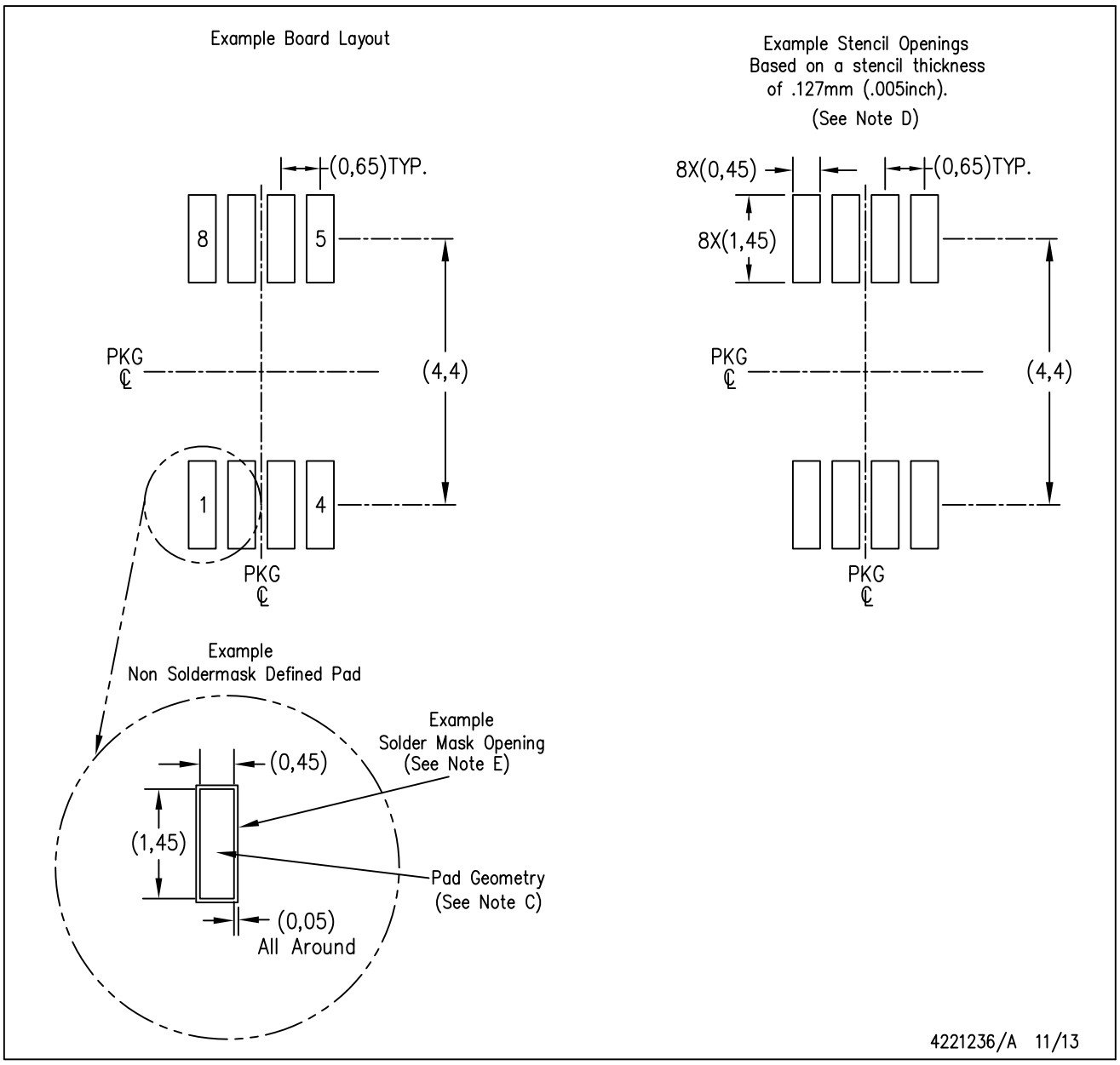
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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