+5 Volt Electronic eFuse

NIS6351

The NIS6351 is a cost effective, resettable fuse which can greatly enhance the reliability of a USB application from both catastrophic and shutdown failures.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits and to protect the input side circuitry from reverse currents. It includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue its operation.

Features

- 85 mΩ Max $R_{DS(on)}$
- Integrated Reverse Current Protection
- Adjustable Output Current Limit Protection with Thermal Shutdown
- IEC61000−4−2 Level 4 ESD Protection for V_{bus} up to ±7 kV
- Fast Response Overvoltage Clamp Circuit with Selectable Level
- Internal Undervoltage Lockout Circuit
- Digital Enable with Separate FLAG for Fault Identification
- Integrated Current Monitoring
- Both Latching and Auto−Retry Options Available
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive Infotainment
- USB 2.0/3.0/3.1 VBUS
- USB Type−C PD Charging
- Solid State Drives
- Mother Boards

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WDFNW10, 3 x 3
CASE 515AB

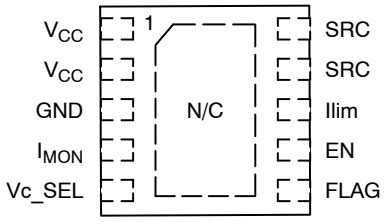
MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

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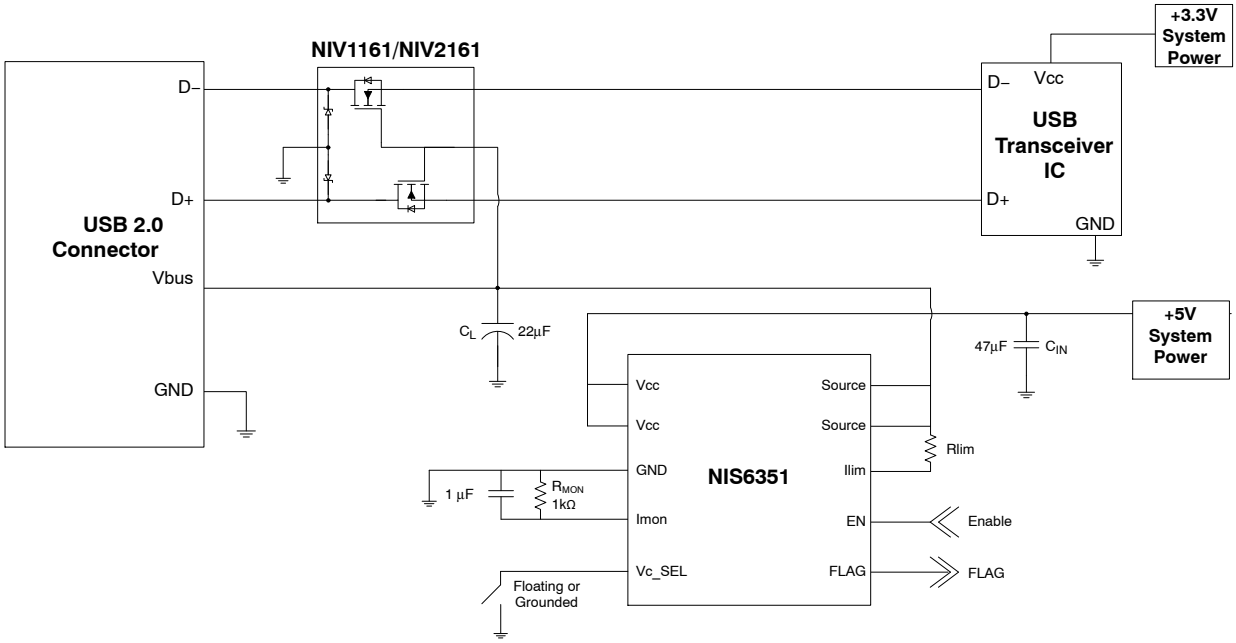


Figure 1. Typical USB 2.0 Application Circuit

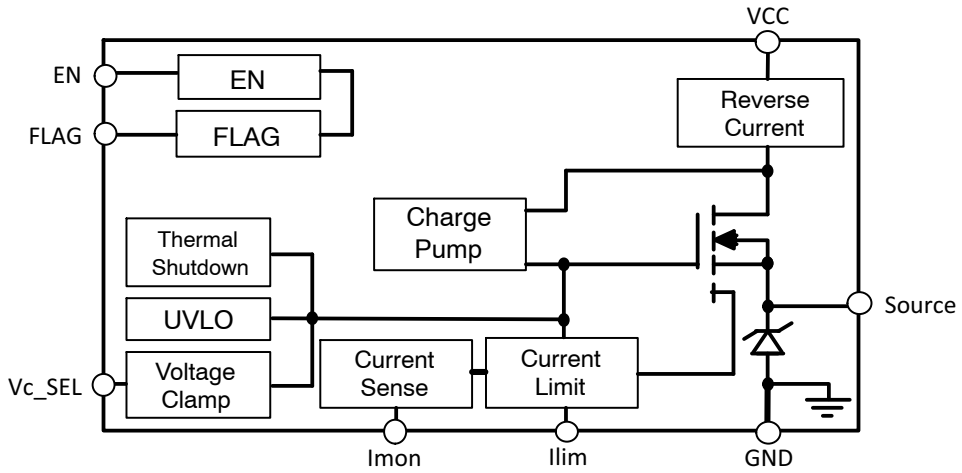


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1, 2	V_{CC}	Positive input voltage to the device. (Low ESR capacitor of minimum 47 μF from V_{CC} to GND is required)
3	GND	Negative input voltage to the device. This is used as the internal reference for the IC.
4	I_{MON}	This pin can be used to monitor the output current by using an external pull−down resistor and de−coupling capacitor.
5	Vc_SEL	The Vc_SEL pin allows the overvoltage clamp to be set at either a 5.6 V or 6.2 V minimum.
6	FLAG	If a thermal fault occurs, the voltage on this pin will go to a low state to signal a monitoring circuit that the device is in thermal shutdown.
7	EN	When this pin is pulled low the eFuse is turned off. It can be used to enable or disable the output of the device by pulling it to ground using an open drain or open collector device, as it has an internal pull−up.
8	Ilim	A resistor between this pin and the source pin sets the overload and short circuit current limit levels.
9, 10	Source	Source of the internal power FET and the output terminal of the fuse
11	N/C (EP)	(Exposed Pad) This pad to be used as heatsink only with no electrical connection. It should be connected to a large area of copper on the PCB, or to the PCB's GND plane.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady−state (V_{CC} to GND) Transient (100 ms)	V_{CC}	−0.3 to +10 −0.3 to +10	V
Output Voltage, operating, steady−state (SRC to GND)	V_{OUT}	−0.3 to +20	V
Voltage range on ILIM pin	V_{ILIM}	−0.3 to +20	V
Voltage range on Enable pin	V_{EN}	−0.3 to 5	V
Voltage range on FLAG pin	V_{FLAG}	−0.3 to 6	V
Voltage range on all other pins		−0.3 to 5	V
Electrostatic Discharge Human Body Model (All pins) Charged Device Model (All pins) IEC61000−4−2 Contact (Source pins, with 22 μF C_{SOURCE} condition)	ESD	 ±2 ±1 ±7	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{JA}	40	°C/W
Thermal Characterization Parameter, Junction−to−Lead (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	ψ_{J-L}	21	°C/W
Thermal Characterization Parameter, Junction−to−Board (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	ψ_{J-B}	13	°C/W
Total Continuous Power Dissipation @ T_A = 25°C (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu) Derate above 25°C	P_{max}	3.1 25	W mW/°C
Operating Ambient Temperature Range	T_A	−40 to 125	°C
Operating Junction Temperature Range	T_J	−40 to 150	°C
Non−operating Temperature Range	T_{STG}	−55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 5 V, C_L = 22 μF, R_{limit} = 15 Ω, T_A = −40 to 125°C)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (enabling of chip to ID = 100 mA with 5 Ω resistive load)	T_{dly}		1500		μs
ON Resistance (Note 1)	$R_{DS(on)}$		50	85	mΩ
T_J = 140°C (Note 2)			64		
Continuous Current T_A = 25°C (Note 2)	I_d			3	A
Off State Leakage (V_{in} = 12 V, EN = 0)	I_{OFF_LEAK}			1	μA
THERMAL LATCH					
Shutdown Temperature (Note 3)	T_{SD}	150	175	200	°C
UNDER/OVERVOLTAGE PROTECTION					
V_{OUT} Maximum (V_{CC} = 16 V with Vc_SEL pin floating)	$V_{out-clamp}$	6.2	6.9	7.5	V
V_{OUT} Maximum (V_{CC} = 16 V with Vc_SEL pin pulled low (0V))	$V_{out-clamp}$	5.6	6.1	6.5	V
Over Voltage Response Time	$T_{vout-clamp}$		11	20	μs
Undervoltage Lockout (Turn on, Voltage Going High)	V_{UVLO}	3.4	3.8	4.6	V
UVLO Hysteresis	V_{Hyst}		0.35		V
Under Voltage Response Time, VCC Falling, −5 V/ms	T_{uvlo}		2	6	μs
Under Voltage Response, VCC Rising, +5 V/ms			5	10	μs
CURRENT LIMIT					
Current Limit	I_{OL}		3.0		A
Short Circuit Current	I_{sc}	0.6	0.9	1.2	A
Current Limit Response Time	T_{ilim}		2.0	10	μs
REVERSE CURRENT LIMIT					
Reverse current blocking threshold (V_{out}−V_{in}) (Note 4)	V_{rev-th}	25	100	250	mV
Reverse current limit response time (dV_{in}/dt = −5 V/1 ms, 20 μF Load)	$V_{rev-resp}$	4	7	12	μs
SLEW RATE CONTROL					
Slew Rate	SR		1	3	ms
CURRENT MONITOR					
No Load Current (EN = high, I_{load} = 0 A)	I_{mon-o}	0	100	200	μA
Gain (I − I_{MON}/I_{out}, @ I_{out} = 1 A, R_{MON} = 1 kΩ, C_{MON} = 1 μF)	$I_{mon-gain}$	0.9	1.0	1.1	mA/A
ENABLE					
Logic Level Low (Output Disabled)	V_{in-low}			0.4	V
Logic Level High (Output Enabled) (Note 5)	$V_{in-high}$	1.1			V
High State Maximum Voltage	V_{in-max}			5	V
Logic Low Sink Current (V_{EN} = 0 V)	I_{in-low}		15	35	μA
De−glitch Filter−delay	Filter−delay	2	10	50	μs
FLAG					
Fault Output Low Voltage (Fault Detected)	Fault−low			0.7	V
Fault Output High Voltage (No Fault Detected)	Fault−high	2.5		5.0	V
Logic High Source Current	Flag−I_{OH}		60		μA
Maximum Fan Out for Fault Signal (guaranteed by design)	Fan			2	Units

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 5 V, C_L = 22 μF, R_{limit} = 15 Ω, T_A = −40 to 125°C)

Characteristics	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE					
Bias Current	I_{Bias}				μA
Operational (I_{Load} = 0 A, EN = 1, FLAG = high)			300	800	
Shutdown (EN = 0)			100	200	
Thermal Fault			100	200	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse test: Pulse width 300 s, duty cycle 2%
2. Verified by design.
3. eFuse is latched off until the En/Fault pin is pulled low and then released or a power on reset is applied to the device. If an auto−retry part is used the device will automatically attempt to turn on once the internal temperature is less than 135°C.
4. Once the device has entered shutdown mode due to a reverse current event, it will re-enable its output when $V_{IN} > V_{OUT}$ for at least 100 μs. The slew rate SR will be applied when the output is re-enabled.
5. A voltage level higher than Vin−high min (1.1 V) must be present to ensure a Logic Level High on the Enable pin.

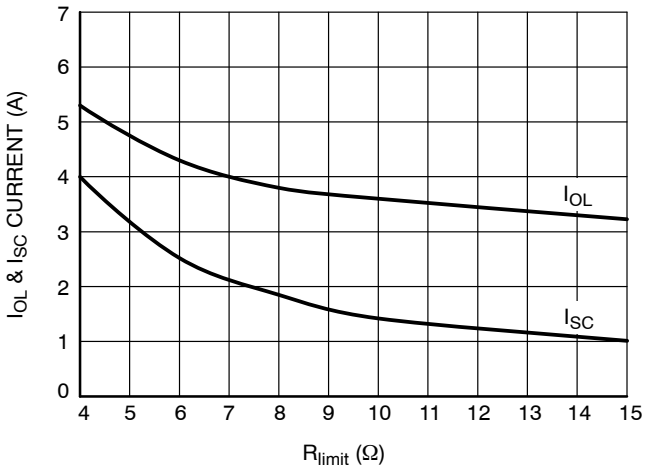


Figure 3. Current Limit vs. R_{limit} for Direct Current Sensing

APPLICATIONS INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The output voltage, which is controlled by an internal dv/dt circuit, will slew from 0 V to the rated output voltage in 1 ms.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip.

The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the Vclamp level. This operation can be seen in Figure 5.

An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (VCC) and ground.

The VCC line can generate spike noise in fast transient conditions such as short circuit, and this high peak can cause over−stress and malfunction. To prevent this, a low ESR capacitor (i.e. MLCC) of at least 47 μF is required.

Reverse Current Protection

The NIS6351 monitors and protects against reverse current events, which can be the result of a malfunction in the power supply or noise induced in the input voltage rail under certain load characteristics (for example, when the load is largely capacitive).

The protection mechanism disables the eFuse's output and triggers when the reverse voltage drop exceeds 100 mV in magnitude and this condition remains for at least 4 μs.

The NIS6351 automatically re−enables its output once the input voltage exceeds the output voltage for at least 100 μs.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the Vclamp voltage, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

The Vc_SEL pin can be used to select the Vclamp level. By allowing this pin to float high, the Vclamp value will be set to 6.2 − 7.5 V. By pulling this pin low (to 0V), the Vclamp value will be set to 5.6 − 6.5 V. This allows the NIS6351 to be used in both short and long haul USB applications where the VBUS voltage is adjusted for cable loss compensation. This operation can be seen in Figure 5.

Thermal Protection

The NIS6351 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. If a latching device is used, output power can be restored by either recycling the input power or toggling the enable pin. An auto−retry device will automatically try to restore output power on its own.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events.

FLAG

The FLAG pin sends information to other devices regarding the state of the chip. This pin is connected to an internal pull−up so that it behaves as active high. The FLAG pin remains at logic level high during normal operation and gets pulled low and subsequently turns the device off when one of the following conditions occurs:

1. EN pin set to Logic Level Low (Output Disabled)
2. Thermal fault
3. UVLO − Undervoltage Lockout
4. Reverse current fault

Enable

The Enable feature provides a digital interface to control the output of the eFuse. This pin is meant for push−pull operation and is connected to an internal pull−up so that it behaves as active high. When pulled low by an external circuitry (below 0.5 V), the eFuse output is turned off. Leakage current in this condition is described in the electrical characteristics table.

IMON (Current Monitor)

The current monitor "IMON" pin provides a small current proportional to the main device current which is passing through the device. This pin must have a decoupling capacitor to filter out internal sampling noise. A resistor connected between the IMON pin and GND converts the IMON current into a GND referenced voltage. The recommended resistor value of 1 kΩ will give about 1 V for every 1 A of device current. The IMON voltage to output current relationship is given in the below equation.

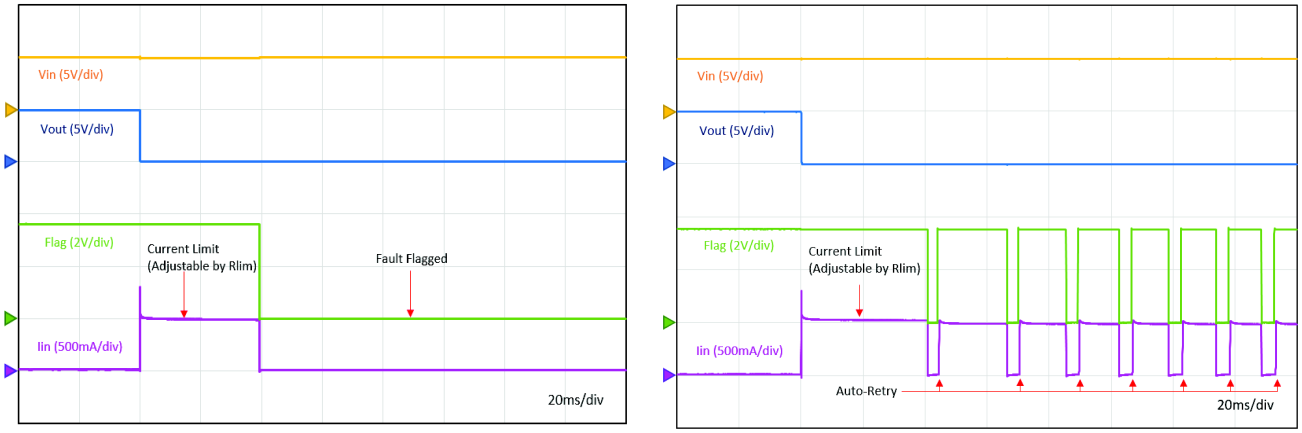
$$V_{MON} = R_{MON} \times \left(\frac{I_d}{1000}\right)$$

Although there is no maximum value that this resistor can be, the value should be limited to 3 kΩ for best operation of the IMON function. This pin can be floated if this function is not needed thus saving a few mA of leakage current.

Latching vs. Auto−Retry

This device features two options regarding its reset ability after a thermal shutdown event. These are called latching and auto−retry which are respectively marked MT1 and MT2 as part number suffixes. Upon reaching a thermal shutdown state, a latching device (MT1) will remain shutdown with no power supplied to the output (SRC pins). The only way to reset the device is to either perform a power cycle on the VCC bus or pull the EN pin low (<0.4 V). By doing either of these actions, the fault state is cleared and the device is allowed to pull−up the output to its normal, high state.

Instead of remaining in thermal shutdown, an Auto−retry device (MT2) will automatically attempt to pull up the output once the die temperature cools to < 135°C. If the fault remains on the output during this attempt, the device will once again enter a short period of current limiting that will eventually lead to thermal shutdown for which the auto−retry process will repeat indefinitely.



Latch version **Auto−Retry version**

Figure 4. Output Short Circuit

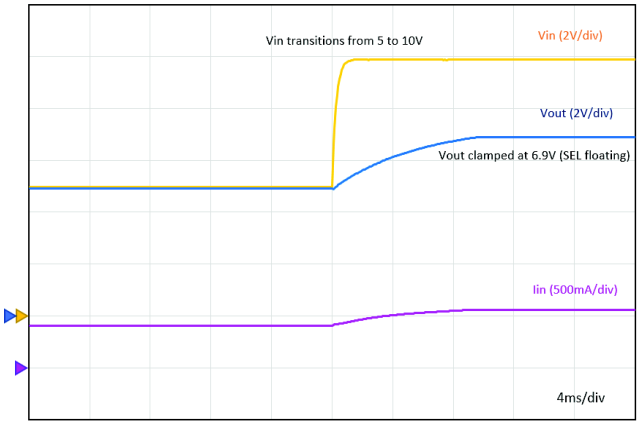


Figure 5. Output Voltage Protection

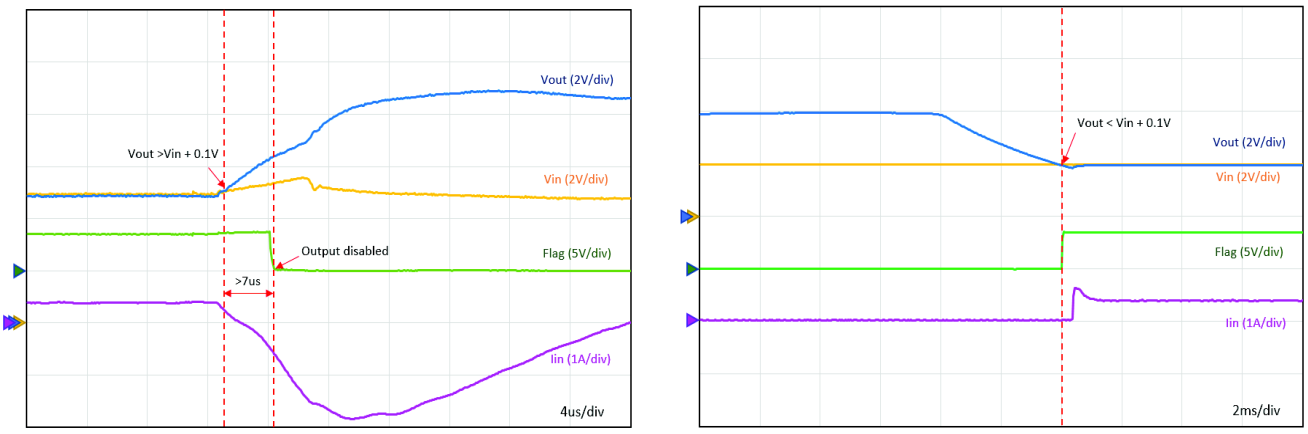


Figure 6. Reverse Current Protection

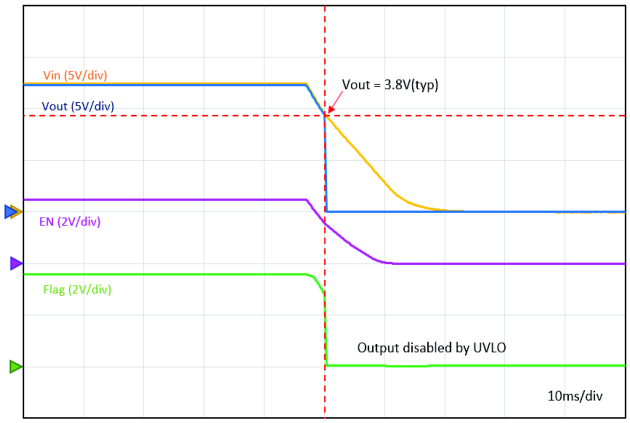


Figure 7. UVLO

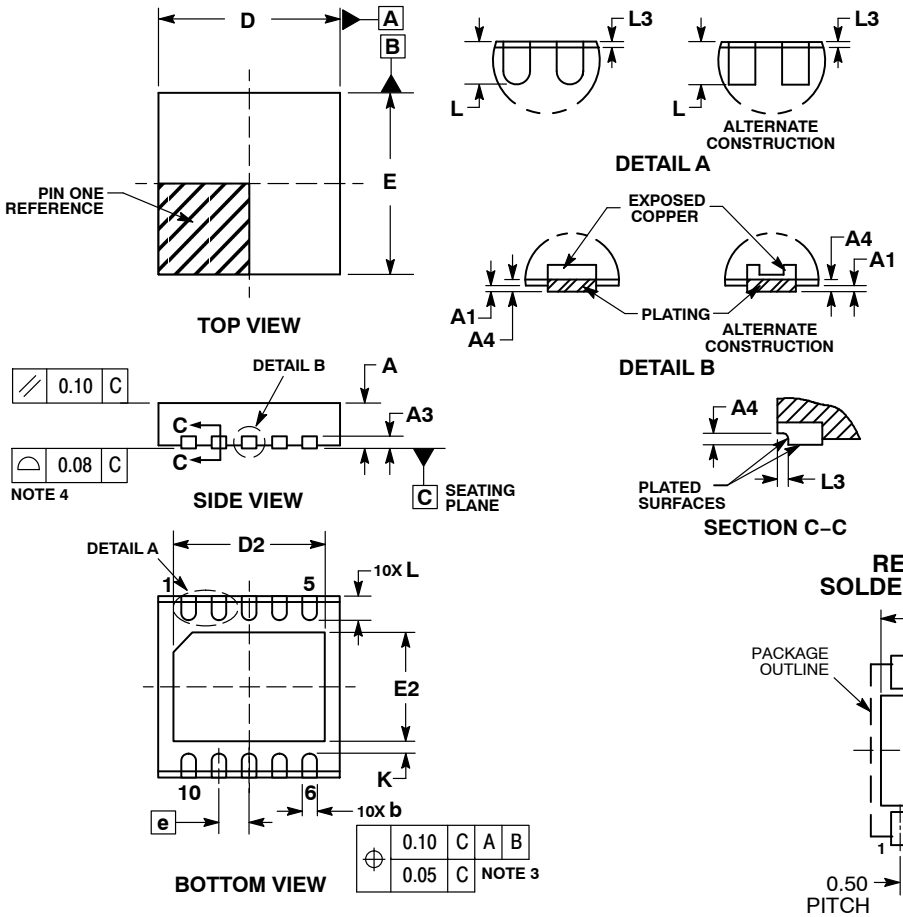
ORDERING INFORMATION

Device	Shutdown Version	Marking	Package	Shipping†
NIS6351MT1TXG	Latching	6351	WDFNW10 (Pb−Free)	3000 / Tape and Reel
NIS6351MT2TXG	Auto−Retry	6351H		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

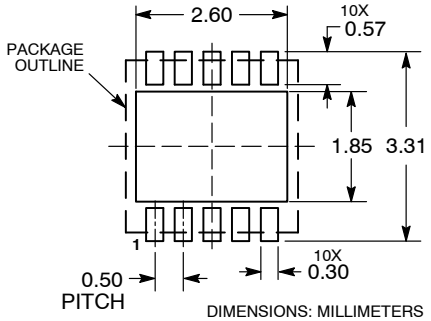
WDFNW10, 3x3, 0.5P
CASE 515AB
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L3		0.05 REF	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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