

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- Low Threshold
- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Linear Amplifiers
- Analog Switches
- Power Management
- Telecommunication Switches

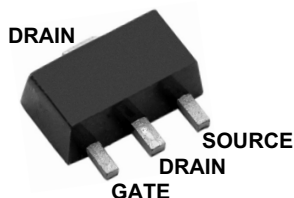
General Description

The TP2424 low-threshold Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Type

3-lead SOT-89
(Top view)



See [Table 2-1](#) for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^{\circ}C$ unless otherwise specified. All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	-240	—	—	V	$V_{GS} = 0V$, $I_D = -250 \mu A$
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1 mA$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/ $^{\circ}C$	$V_{GS} = V_{DS}$, $I_D = -1 mA$ (Note 1)
Gate Body Leakage Current	I_{GSS}	—	—	-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	-10	μA	$V_{GS} = 0V$, $V_{DS} = \text{Maximum rating}$
		—	—	-1	mA	$V_{DS} = 0.8 \text{ Maximum rating}$, $V_{GS} = 0V$, $T_A = 125^{\circ}C$ (Note 1)
On-State Drain Current	$I_{D(ON)}$	-0.3	—	—	A	$V_{GS} = -4.5V$, $V_{DS} = -25V$
		-0.8	—	—	A	$V_{GS} = -10V$, $V_{DS} = -25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	10	Ω	$V_{GS} = -4.5V$, $I_D = -150 mA$
		—	—	8	Ω	$V_{GS} = -10V$, $I_D = -500 mA$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	0.75	%/ $^{\circ}C$	$V_{GS} = -10V$, $I_D = -500 mA$ (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G _{FS}	150	—	—	mmho	V _{DS} = −25V, I _D = −200 mA
Input Capacitance	C _{ISS}	—	—	200	pF	V _{GS} = 0V, V _{DS} = −25V, f = 1 MHz
Common Source Output Capacitance	C _{OSS}	—	—	100	pF	
Reverse Transfer Capacitance	C _{RSS}	—	—	40	pF	
Turn-On Delay Time	t _{d(ON)}	—	—	20	ns	V _{DD} = −25V, I _D = −250 mA, R _{GEN} = 25Ω
Rise Time	t _r	—	—	30	ns	
Turn-Off Delay Time	t _{d(OFF)}	—	—	35	ns	
Fall Time	t _f	—	—	25	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V _{SD}	—	—	−1.5	V	V _{GS} = 0V, I _{SD} = −500 mA (Note 1)
Reverse Recovery Time	t _{rr}	—	300	—	ns	V _{GS} = 0V, I _{SD} = −500 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C . Pulse test: 300 μs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-89	θ_{JA}	—	133	—	$^\circ\text{C/W}$	Note 1

Note 1: Mounted on an FR5 board, 25 mm x 25 mm x 1.57 mm

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at $T_A = 25^\circ\text{C}$ (Note 2) (W)	I_{DR} (Note 1) (mA)	I_{DRM} (A)
3-lead SOT-89	-316	-1.9	1.6	-316	-1.9

Note 1: I_D (continuous) is limited by maximum rated T_J .

2: Mounted on an FR5 board, 25 mm x 25 mm x 1.57 mm

TP2424

2.0 PIN DESCRIPTION

The details on the pins of TP2424 are listed in [Table 2-1](#). Refer to [Package Type](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2, 4	Drain	Drain
3	Source	Source

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for TP2424.

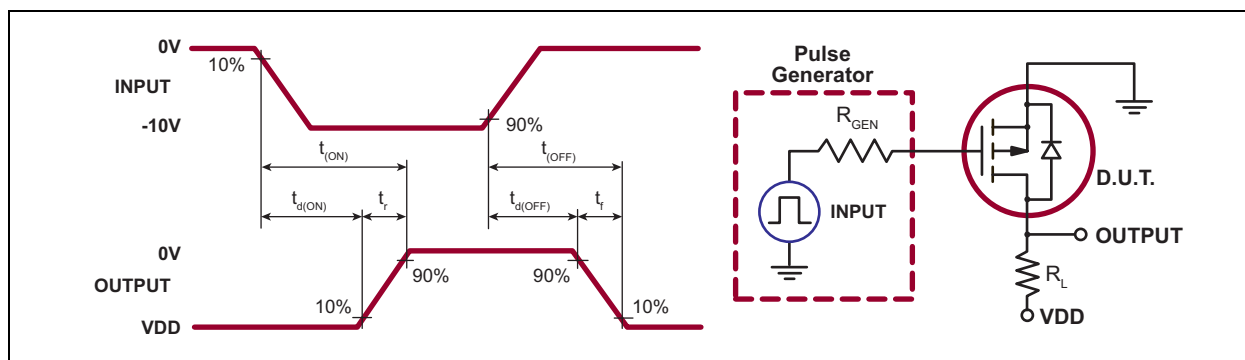


FIGURE 3-1: Switching Waveforms and Test Circuit.

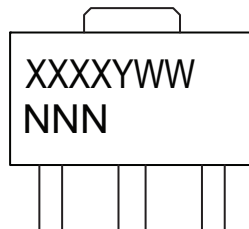
TABLE 3-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(TH)}$ (Maximum) (V)	$I_{D(ON)}$ (Minimum) (mA)
-240V	8	-2.4	-800

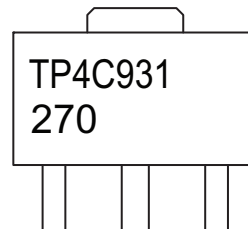
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

3-lead SOT-89



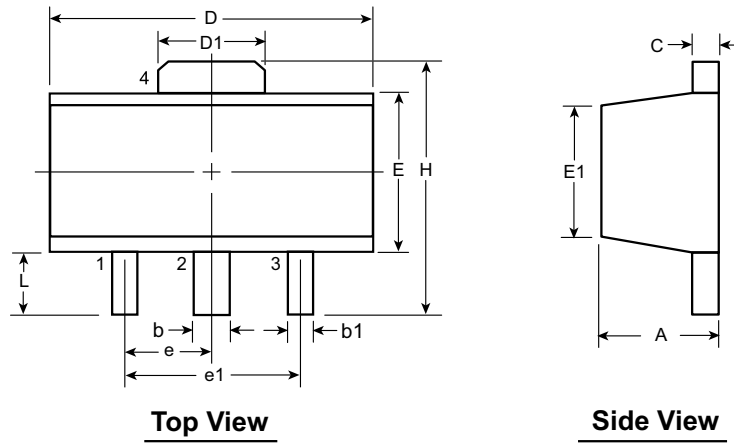
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.73 [†]
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2019)

- Converted Supertex Doc# DSFP-TP2424 to Microchip DS20005959A
- Added a pin function table
- Changed the package marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO. Device XX Package Options - X Environmental - X Media Type	Example: a) TP2424N8-G: P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-89, 2000/Reel
Device: TP2424 = P-Channel Enhancement-Mode Vertical DMOS FET Package: N8 = 3-lead SOT-89 Environmental: G = Lead (Pb)-free/RoHS-compliant Package Media Type: (blank) = 2000/Reel for an N8 Package	

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ISBN: 978-1-5224-5178-5

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