12-Bit, 65 MSPS IF to Baseband Diversity Receiver

AD6652

FEATURES

SNR = 90 dB in 150 kHz bandwidth (to Nyquist @ 61.44 MSPS)
Worst harmonic = 83 dBc (to Nyquist @ 61.44 MSPS)
Integrated dual-channel ADC:
- **Sample rates up to 65 MSPS**
- **IF sampling frequencies to 200 MHz**
- **Internal ADC voltage reference**
- **Integrated ADC sample-and-hold inputs**
- **Flexible analog input range (1 V to 2 V p-p)**
- **Differential analog inputs**
- **ADC clock duty cycle stabilizer**
- **85 dB channel isolation/crosstalk**

Integrated wideband digital downconverter (DDC):
- **Crossbar switched DDC inputs**
- **Digital resampling for noninteger decimation**
- **Programmable decimating FIR filters**
- **Flexible control for multicarrier and phased array**
- **Dual AGC stages for output level control**
- **Dual 16-bit parallel or 8-bit link output ports**
- **User-configurable built-in self-test (BIST) capability**
- **Energy-saving power-down modes**

APPLICATIONS

Communications
Diversity radio systems
Multimode digital receivers:
- **GSM, EDGE, PHS, AMPS, UMTS, WCDMA, CDMA-ONE, IS95, IS136, CDMA2000, IMT-2000**

I/Q demodulation systems
Smart antenna systems
General-purpose software radios
Broadband data applications
Instrumentation and test equipment

FUNCTIONAL BLOCK DIAGRAM

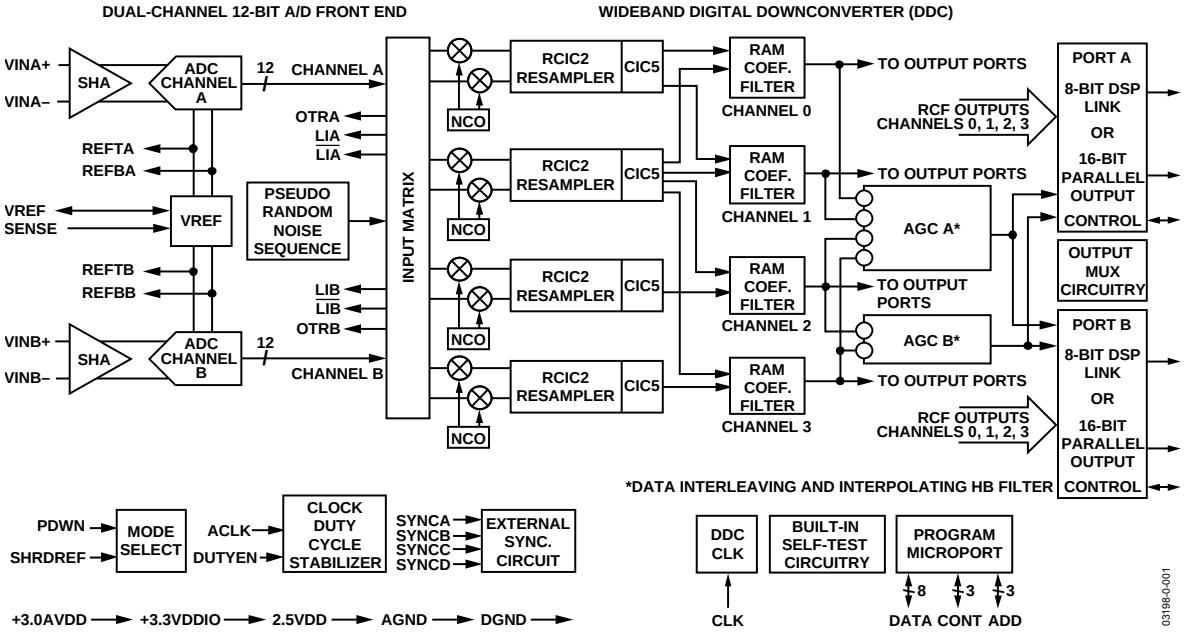

Figure 1.

Rev. 0

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REVISION HISTORY

7/04—Revision 0: Initial Version

PRODUCT DESCRIPTION

The AD6652 is a mixed-signal IF to baseband receiver consisting of dual 12-bit 65 MSPS ADCs and a wideband multimode digital downconverter (DDC). The AD6652 is designed to support communications applications where low cost, small size, and versatility are desired. The AD6652 is also suitable for other applications in imaging, medical ultrasound, instrumentation, and test equipment.

The dual ADC core features a multistage differential pipelined architecture with integrated output error correction logic. Both ADCs feature wide bandwidth differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

ADC data outputs are internally connected directly to the receiver's digital downconverter (DDC) input matrix, simplifying layout and reducing interconnection parasitics. Overrange bits are provided for each ADC channel to alert the user to ADC clipping. Level indicator bits are also provided for each DDC input port that can be used for external digital VGA control.

The digital receiver has four reconfigurable channels and provides extraordinary processing flexibility. The receiver input matrix routes the ADC data to individual channels, or to all four receive processing channels. Each receive channel has five cascaded signal processing stages: a 32-bit frequency translator (numerically controlled oscillator (NCO)), two fixed-coefficient decimating filters (CIC), a programmable RAM coefficient decimating FIR filter (RCF), and an interpolating half-band filter/AGC stage. Following the CIC filters, one, several, or all channels can be configured to use one, several, or all the RCF filters. This permits the processing power of four 160-tap RCF FIR filters to be combined or used individually.

After FIR filtering, data can be routed directly to the two external 16-bit output ports. Alternatively, data can be routed through two additional half-band interpolation stages, where up to four channels can be combined (interleaved), interpolated, and processed by an automatic gain control (AGC) circuit with 96 dB range. The outputs from the two AGC stages are also routed directly to the two external 16-bit output ports. Each output port has a 16-bit parallel output and an 8-bit link port to permit seamless data interface with DSP devices such as the TS-101 TigerSHARC® DSP. A multiplexer for each port selects one of six data sources to appear on the device outputs pins.

The AD6652 is part of the Analog Devices SoftCell® multimode and multicarrier transceiver chipset. The SoftCell receiver digitizes a wide spectrum of IF frequencies and then downconverts the desired signals to baseband using individual channel NCOs. The AD6652 provides user-configurable digital filters for removal of undesired baseband components, and the data is then passed on to an external DSP, where demodulation and other signal processing tasks are performed to complete the information retrieval process. Each receive channel is independently configurable to provide simultaneous reception of the carrier to which it is tuned. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

High dynamic range decimation filters offer a wide range of decimation rates. The RAM-based architecture allows easy reconfiguration for multimode applications. The decimating filters remove unwanted signals and noise from the channel of interest. When the channel occupies less bandwidth than the input signal, this rejection of out-of-band noise is referred to as *processing gain*. By using large decimation factors, this processing gain can improve the SNR of the ADC by 20 dB or more. In addition, the programmable RAM coefficient filter allows antialiasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter.

Flexible power-down options allow significant power savings, when desired.

PRODUCT HIGHLIGHTS

- Integrated dual 12-bit 65 MSPS ADC.
- Integrated wideband digital downconverter (DDC).
- Proprietary, differential SHA input maintains excellent SNR performance for input frequencies up to 200 MHz.
- Crossbar-switched digital downconverter input ports.
- Digital resampling permits noninteger relationships between the ADC clock and the digital output data rate.
- Energy-saving power-down modes.
- 32-bit NCOs with selectable amplitude and phase dithering for better than −100 dBc spurious performance.
- CIC filters with user-programmable decimation and interpolation factors.
- 160-tap RAM coefficient filter for each DDC channel.
- Dual 16-bit parallel output ports and dual 8-bit link ports.
- 8-bit microport for register programming, register readback, and coefficient memory programming.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
AVDD	Full	IV	2.75	3.0	3.3	V
VDD	Full	IV	2.25	2.5	2.75	V
VDDIO	Full	IV	3.0	3.3	3.6	V
$T_{AMBIENT}$		IV	−40	+25	+85	°C

ADC DC SPECIFICATIONS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 2.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION	Full	IV	12			Bits
INTERNAL VOLTAGE REFERENCE						
Output Voltage Error (1 V Mode)	Full	IV		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1		mV
INPUT REFERRED NOISE						
Input Span = 1 V Internal	25°C	V		0.54		LSB rms
Input Span = 2 V Internal	25°C	V		0.27		LSB rms
ANALOG INPUT						
Input Span = 1.0 V	Full	IV		1		V p-p
Input Span = 2.0 V	Full	IV		2		V p-p
Input Capacitance	Full	V		7		pF
REFERENCE INPUT RESISTANCE	Full	V		7		kΩ
MATCHING CHARACTERISTICS						
Offset Error	Full	V		±0.1		% FSR
Gain Error	Full	V		±0.1		% FSR

ADC SWITCHING SPECIFICATIONS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 3.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	IV	65			MSPS
Minimum Conversion Rate	Full	V			1	MSPS
ACLK Period	Full	V	15.4			ns
ACLK Pulse Width High[1]	Full	V	6.2	ACLK/2		ns
ACLK Pulse Width Low[1]	Full	V	6.2	ACLK/2		ns
DATA OUTPUT PARAMETERS						
Wake-Up Time[2]	Full	V		2.5		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		2		Cycles

[1] Duty cycle stabilizer enabled.
[2] Wake-up time is dependent on the value of decoupling capacitors, typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

ADC AC SPECIFICATIONS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference.

Table 4.

Parameter (Conditions)		Temp	Test Level	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO[1] (WITHOUT HARMONICS)							
Analog Input Frequency	10.4 MHz	25°C	V		90		dB
		Full	V		90		dB
	25.0 MHz	25°C	II	85	90		dB
		Full	V		90		dB
	68.0 MHz	25°C	II	84	89.5		dB
		Full	V		88.5		dB
	101 MHz	25°C	V		88.0		dB
	150 MHz	25°C	V		87.5		dB
	200 MHz	25°C	V		85		dB
WORST HARMONIC (2nd or 3rd)[1]							
Analog Input Frequency	10.4 MHz	25°C	V		−85		dBc
		Full	V		−83		dBc
	25 MHz	25°C	II		−83	−71	dBc
		Full	V		−80		dBc
	68 MHz	25°C	II		−80		dBc
		Full	V		−76		dBc
	101 MHz	25°C	V		−79		dBc
	150 MHz	25°C	V		−72		dBc
	200 MHz	25°C	V		−69		dBc
TWO-TONE IMD REJECTION (TWO TONES SEPARATED BY 1 MHz)[2]							
Analog Inputs = 15/16 MHz		25°C	V		−81		dBc
Analog Inputs = 55/56 MHz		25°C	V		−79		dBc
CHANNEL ISOLATION/CROSSTALK[3]		Full	V		85		dB

[1] Analog Input A or B = single tone @ −1 dB below full scale, 150 kHz DDC filter bandwidth.
[2] Analog Input A or B = each single tone @ −7 dB below full scale, 5 MHz DDC filter bandwidth.
[3] Analog Inputs A and B = each single tone @ −1 dB below full scale at 4.3 MHz and 68 MHz, 150 kHz DDC filter bandwidth.

ELECTRICAL CHARACTERISTICS

AVDD = 3.0 V, VDD = 2.5 V, VDDIO = 3.3 V, 61.44 MSPS, −1.0 dBFS differential input, 1.0 V internal reference, unless otherwise noted.

Table 5.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS						
Logic Compatibility	Full	IV		3.3 V CMOS		
Logic 1 Voltage	Full	IV	2.0			V
Logic 0 Voltage	Full	IV			0.8	V
Logic 1 Current	Full	IV	−10		+10	µA
Logic 0 Current	Full	IV	−10		+10	µA
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV		3.3 V CMOS/TTL		
Logic 1 Voltage (V_{OH}) (I_{OH} = 0.25 mA)	Full	IV	2.4	VDDIO − 0.2		V
Logic 0 Voltage (V_{OL}) (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
SUPPLY CURRENTS						
Narrow Band (150 kHz BW) (61.44 MHz CLK) Four Individual Channels						
I_{AVDD}	25°C	II	160	200	215	mA
I_{VDD}	25°C	II	240	280	300	mA
I_{VDDIO}	25°C	II	25	40	45	mA
CDMA (1.25MHz BW) (61.44 MHz CLK) Example[1]						
I_{AVDD}	25°C	V		200		mA
I_{VDD}	25°C	V		336		mA
I_{VDDIO}	25°C	V		68		mA
WCDMA (5 MHz BW) (61.44 MHz CLK) Example[1]						
I_{AVDD}	25°C	V		200		mA
I_{VDD}	25°C	V		330		mA
I_{VDDIO}	25°C	V		89		mA
TOTAL POWER DISSIPATION						
Narrow Band (150 kHz BW) (61.44 MHz CLK) Four Individual Channels	25°C	II	1.2	1.5	1.6	W
CDMA (61.44 MHz)[1]	25°C	V		1.7		W
WCDMA (61.44 MHz)[1]	25°C	V		1.7		W
ADC in Standby and DDC in Sleep Mode[2]	25°C	V		2.3		mW

[1] All signal processing stages and all DDC channels active.
[2] ADC standby power measured with ACLK inactive.

GENERAL TIMING CHARACTERISTICS

All timing specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V. CLOAD = 40 pF on all outputs, unless otherwise specified.

Table 6.

Parameter (Conditions)		Temp	Test Level	Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
t_{CLK}	CLK Period	Full	IV	15.4			ns
t_{CLKL}	CLK Width Low	Full	IV	6.2	$t_{CLK}/2$		ns
t_{CLKH}	CLK Width High	Full	IV	6.2	$t_{CLK}/2$		ns
$\overline{\text{RESET}}$ TIMING REQUIREMENTS							
t_{RESL}	$\overline{\text{RESET}}$ Width Low	Full	IV	30.0			ns
LEVEL INDICATOR OUTPUT SWITCHING CHARACTERISTICS							
t_{DLI}	↑CLK to LI (LIA, $\overline{\text{LIA}}$; LIB, $\overline{\text{LIB}}$) Output Delay Time	Full	IV	3.3		10.0	ns
SYNC TIMING REQUIREMENTS							
t_{SS}	SYNC(A,B,C,D) to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HS}	SYNC(A,B,C,D) to ↑CLK Hold Time	Full	IV	1.0			ns
PARALLEL PORT TIMING REQUIREMENTS (MASTER MODE)							
Switching Characteristics[1]							
$t_{DPOCLKL}$	↓CLK to ↑PCLK Delay (Divide-by-1)	Full	IV	6.5		10.5	ns
$t_{DPOCLKLL}$	↓CLK to ↑PCLK Delay (Divide-by-2, -4, or -8)	Full	IV	8.3		14.6	ns
t_{DPREQ}	↑PCLK to ↑PxREQ Delay					1.0	ns
t_{DPP}	↑PCLK to Px[15:0] Delay					0.0	ns
Input Characteristics							
t_{SPA}	PxACK to ↓PCLK Setup Time			7.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time			−3.0			ns
PARALLEL PORT TIMING REQUIREMENTS (SLAVE MODE)							
Switching Characteristics[1]							
t_{POCLK}	PCLK Period	Full	IV	12.5			ns
t_{POCLKL}	PCLK Low Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{POCLKH}	PCLK High Period (when PCLK Divisor = 1)	Full	IV	2.0	$0.5 \times t_{POCLK}$		ns
t_{DPREQ}	↑PCLK to ↑PxREQ Delay					10.0	ns
t_{DPP}	↑PCLK to Px[15:0] Delay					11.0	ns
Input Characteristics							
t_{SPA}	PxACK to ↓PCLK Setup Time		IV	1.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time		IV	1.0			ns
LINK PORT TIMING REQUIREMENTS							
Switching Characteristics[1]							
t_{RDLCLK}	↑PCLK to ↑LxCLKOUT Delay	Full	IV			2.5	ns
t_{FDLCLK}	↓PCLK to ↓LxCLKOUT Delay	Full	IV			0	ns
$t_{RLCLKDAT}$	↑LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.9	ns
$t_{FLCLKDAT}$	↓LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.2	ns

[1] The timing parameters for Px[15:0], PxREQ, and PxACK apply for Port A and B (x stands for A or B).

MICROPROCESSOR PORT TIMING CHARACTERISTICS

All timing specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V. CLOAD = 40 pF on all outputs, unless otherwise specified.

Table 7.

MICROPROCESSOR PORT, MODE INM (MODE = 0)		Temp	Test Level	Min	Typ	Max	Unit
MODE INM WRITE TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HWR}	$\overline{WR}$(R/$\overline{W}$) to RDY($\overline{DTACK}$) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to $\overline{WR}$(R/$\overline{W}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY($\overline{DTACK}$) Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{WR}$(R/$\overline{W}$) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{WR}$(R/$\overline{W}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE INM READ TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to $\overline{RD}$($\overline{DS}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns
MICROPROCESSOR PORT, MODE MNM (MODE = 1)		**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
MODE MNM WRITE TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	R/$\overline{W}$($\overline{WR}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data To R/$\overline{W}$($\overline{WR}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to R/$\overline{W}$($\overline{WR}$) Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	R/$\overline{W}$($\overline{WR}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE MNM READ TIMING							
t_{SC}	Control[1] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[1] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to $\overline{DS}$($\overline{RD}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns

[1] Specification pertains to control signals: R/W, ($\overline{WR}$), $\overline{DS}$, ($\overline{RD}$), and $\overline{CS}$.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
ELECTRICAL	
AVDD Voltage	−0.3 V to +3.9 V
VDD Voltage	−0.3 V to +2.75 V
VDDIO Voltage	−0.3 V to +3.9 V
AGND, DGND	−0.3 V to +0.3 V
ADC VINA, VINB Analog Input Voltage	−0.3 V to AVDD + 0.3 V
ADC Digital Input Voltage	−0.3 V to AVDD + 0.3 V
ADC OTRA, OTRB Digital Output Voltage	−0.3 V to VDDIO + 0.3 V
ADC VREF, REFA, REFB Input Voltage	−0.3 V to AVDD + 0.3 V
DDC Digital Input Voltage	−0.3 V to VDDIO + 0.3 V
DDC Digital Output Voltage	−0.3 V to VDDIO + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

256-lead CSPBGA, 17 mm sq.

θ_{JA} = 23°C/W, still air.

Estimate based on JEDEC JC51-2 model using horizontally positioned 4-layer board.

TEST LEVEL

I. 100% production tested.

II. 100% production tested at 25°C.

III. Sample tested only.

IV. Parameter guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. BGA Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DGND	PA7_LA7	A2	PA6_LA6	D1	D3	$\overline{CS}$	$\overline{RESET}$	MODE	SYNCD	OTRA	PDWN	AVDD	AVDD	AGND	AGND
B	Do Not Connect	PA4_LA4	PACH0_ LACLK OUT	A0	DGND	R/$\overline{W}$ ($\overline{WR}$)	D4	D6	SYNCC	SYNCA	LIA	DUTYEN	AVDD	AVDD	AGND	AGND
C	PA9	PA3_LA3	A1	$\overline{DS}$ ($\overline{RD}$)	D0	D2	D5	D7	$\overline{DTACK}$ (RDY)	SYNCB	$\overline{LIA}$	LIB	AVDD	AVDD	AGND	VIN+B
D	PA1_LA1	PA2_LA2	PACH1_ LACLKIN	VDD	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	AVDD	AVDD	AGND	VIN−B
E	PA8	PA5_LA5	n.c.	VDD	VDD	VDD	VDD	VDDIO	VDDIO	VDDIO	VDDIO	VDDIO	AVDD	AVDD	AGND	AGND
F	PA0_LA0	DGND	PA10	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	AGND
G	PA12	PA11	PA13	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	REFBB	REFTB
H	PAREQ	PA15	PA14	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	SENSE
J	CHIP_ID1	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	VREF
K	CHIP_ID3	PAACK	CHIP_ID0	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	REFBA	REFTA
L	PB6_LB6	PB7_LB7	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDIO	AVDD	AGND	AGND	AGND
M	CHIP_ID2	PB3_LB3	PB4_LB4	VDDIO	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDD	VDDIO	AVDD	AVDD	AGND	AGND
N	PAIQ	PBCH1_ LBCLK IN	PB2_LB2	VDDIO	VDDIO	VDDIO	VDDIO	VDD	VDD	VDD	VDD	VDDIO	AVDD	AVDD	AGND	VIN−A
P	DGND	PB0_LB0	PB8	PB10	PB14	VDDIO	PBACK	$\overline{LIB}$	n.c.	n.c.	OTRB	n.c.	AVDD	AVDD	AGND	VIN+A
R	PBIQ	PBCH0_L BCLKOUT	PB1_ LB1	PB9	PB12	PB15	n.c.	n.c.	n.c.	n.c.	n.c.	PDWN	AVDD	AVDD	AGND	AGND
T	DGND	PCLK	PB5_ LB5	PB11	PB13	PBREQ	n.c.	n.c.	n.c.	n.c.	DCLK	SHRDREF	AVDD	ACLK	AGND	AGND

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type	Function
POWER SUPPLY			
A13, B13, C13, D13, E13, F13, G13, H13, J13, K13, L13, M13, N13, P13, R13, T13, A14, B14, C14, D14, E14, M14, N14, P14, R14	AVDD	Power	3.0 V Analog Supply, 25 Pins.
D4, D5, D6, D7, E4, E5, E6, E7, M8, M9, M10, M11, N8, N9, N10, N11	VDD	Power	2.5 V Digital Core Supply, 16 Pins.
D8, D9, D10, D11, D12, E8, E9, E10, E11, E12, F12, G12, H12, J12, K12, L12, M4, M5, M6, M7, M12, N4, N5, N6, N7, N12, P6	VDDIO	Power	3.3 V Digital I/O Supply, 27 Pins.
A1, B5, F2, F4, F5, F6, F7, F8, F9, F10, F11, G4, G5, G6, G7, G8, G9, G10, G11, H4, H5, H6, H7, H8, H9, H10, H11, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, K4, K5, K6, K7, K8, K9, K10, K11, L3, L4, L5, L6, L7, L8, L9, L10, L11, P1, T1	DGND	Ground	Digital Ground, 56 Pins.
A15, A16, B15, B16, C15, D15, E15, E16, F14, F15, F16, G14, H14, H15, J14, J15, K14, L14, L15, L16, M15, M16, N15, P15, R15, R16, T15, T16	AGND	Ground	Analog Ground, 28 Pins.
MISCELLANEOUS			
E3, P9, P10, P12, R7, R8, R9, R10, R11, T7, T8, T9, T10	NC	N/A	No Connect, 13 Pins.
B1	DNC	N/A	Do Not Connect.

Pin No.	Mnemonic	Type	Function
ADC INPUTS			
P16	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
N16	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
C16	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
D16	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
J16	VREF	I/O	Voltage Reference Input/Output.
H16	SENSE	Input	Voltage Reference Mode Select.
T14	ACLK	Input	ADC Master Clock.
B12	DUTYEN	Input	Duty Cycle Stabilizer, Active High.
A12, R12	PDWN[1]	Input	Power-Down Enable, Active High.
T12	SHRDREF	Input	Shared Voltage Reference Select, Low = Independent, High = Shared.
ADC OUTPUTS			
A11	OTRA	Output	Out-of-Range Indicator for Channel A, High = Overrange.
P11	OTRB	Output	Out-of-Range Indicator for Channel B, High = Overrange.
K16	REFTA	Output	Top Reference Voltage, Channel A.
G16	REFTB	Output	Top Reference Voltage, Channel B.
K15	REFBA	Output	Bottom Reference Voltage, Channel A.
G15	REFBB	Output	Bottom Reference Voltage, Channel B.
DDC INPUTS			
A8	$\overline{\text{RESET}}$	Input	Master Reset, Active Low.
T11	DCLK	Input	DDC Master Clock.
T2	PCLK	I/O	Link Port Clock Output or Parallel Port Clock Input.
D3	PACH1_LACLKIN[2]	I/O	Channel ID Output Bit, MSB, for Parallel Port A, or Link Port A Data Ready Input. Function depends on logic state of 0x1B:7 of output port control register.
N2	PBCH1_LBCLKIN[2]	I/O	Channel ID Output Bit, MSB, for Parallel Port B, or Link Port B Data Ready Input. Function depends on logic state of 0x1D:7 of output port control register.
B10	SYNCA[3]	Input	Hardware Sync, Pin A, Routed to All Receiver Channels.
C10	SYNCB[3]	Input	Hardware Sync, Pin B, Routed to All Receiver Channels.
B9	SYNCC[3]	Input	Hardware Sync, Pin C, Routed to All Receiver Channels.
A10	SYNCD[3]	Input	Hardware Sync, Pin D, Routed to All Receiver Channels.
K3, J1, M1, K1	CHIP_ID[3:0][3]	Input	Chip ID Selector, Four Pins, Used in Conjunction with Access Control Register Bits 5–2.

Pin No.	Mnemonic	Type	Function
DDC OUTPUTS			
B11	LIA	Output	Level Indicator, Input A, Data A.
C11	$\overline{\text{LIA}}$	Output	Level Indicator, Input A, Data $\overline{\text{A}}$.
C12	LIB	Output	Level Indicator, Input B, Data B.
P8	$\overline{\text{LIB}}$	Output	Level Indicator, Input B, Data $\overline{\text{B}}$.
B3	PACH0_LACLKOUT[2]	Output	Channel ID Output Bit, LSB, for Parallel Port A, or Link Port A Clock Output. Function depends on logic state of 0x1B:7 of output port control register.
R2	PACH0_LBCLKOUT[2]	Output	Channel ID Output Bit, LSB, for Parallel Port B, or Link Port B Clock Output. Function depends on logic state of 0x1D:7 of output port control register.
F1, D1, D2, C2, B2, E2, A4, A2	PA[7:0]_LA[7:0]	Output	Link Port A Data or Parallel Port A Data [7:0], Eight Pins.
P2, R3, N3, M2, M3, T3, L1, L2	PB[7:0_LB[7:0]	Output	Link Port B Data or Parallel Port B Data [7:0], Eight Pins.
E1, C1, F3, G2, G1, G3, H3, H2	PA[15:8]	Output	Parallel Port A Data [15:8], Eight Pins.
P3, R4, P4, T4, R5, T5, P5, R6	PB[15:8]	Output	Parallel Port B Data [15:8], Eight Pins.
N1	PAIQ	Output	Parallel Port A I or Q Data Indicator, I = High, Q = Low.
R1	PBIQ	Output	Parallel Port B I or Q Data Indicator, I = High, Q = Low.
PARALLEL OUTPUT PORT CONTROL			
K2	PAACK	Input	Parallel Port A Acknowledge.
H1	PAREQ	Output	Parallel Port A Request.
P7	PBACK	Input	Parallel Port B Acknowledge.
T6	PBREQ	Output	Parallel Port B Request.
MICROPORT CONTROL			
C5, A5, C6, A6, B7, C7, B8, C8	D[7:0]	I/O	Bidirectional Microport Data, Eight Pins. This bus is three-stated when $\overline{\text{CS}}$ is high.
B4, C3, A3	A[2:0]	Input	Microport Address Bus, 3 Pins.
C4	$\overline{\text{DS}}(\overline{\text{RD}})$[4]	Input	Function depends upon MODE pin. Active Low Data Strobe when MODE = 1. Active Low Read Strobe when MODE = 0.
C9	$\overline{\text{DTACK}}$(RDY)[4, 5]	Output	Function depends upon MODE pin. Active Low Data Acknowledge when MODE = 1. Microport Status Pin when MODE = 0.
B6	R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)[4]	Input	Read/Write Strobe when MODE = 1. Active Low Write strobe when MODE = 0.
A9	MODE[4]	Input	Mode Select Pin. 0 = Intel mode, 1 = Motorola mode.
A7	$\overline{\text{CS}}$[3]	Input	Active Low Chip Select. Logic 1 three-states the microport data bus.

[1] PDWN pins must be the same logic level: both logic high or both logic low.
[2] PACH0 and PACH1 form a 2-bit output word in the parallel output mode that identifies the processing channel (0, 1, 2, or 3) whose data appears on Port A parallel outputs. Likewise, PBCH0 and PBCH1 identify the channel for Port B.
[3] Pins with a pull-down resistor of nominal 70 kΩ.
[4] Mode 0 is Intel nonmultiplexed (IMN), and Mode 1 is Motorola nonmultiplexed (MNM). Pin logic level corresponds to mode.
[5] Pins with a pull-up resistor of nominal 70 kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS

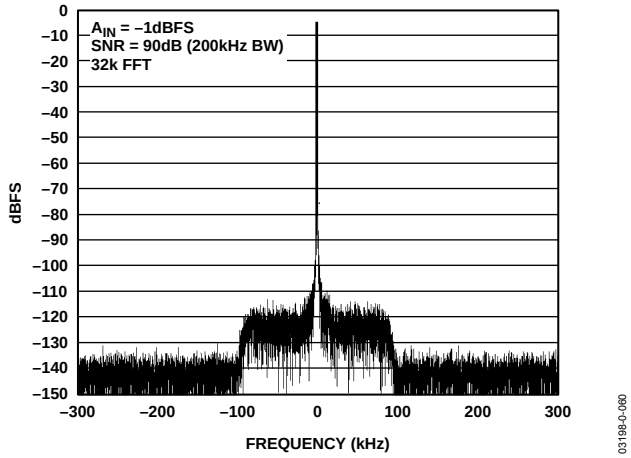


Figure 2. GSM/EDGE with Single Tone A_{IN} = 30 MHz; Encode = 61.44 MSPS

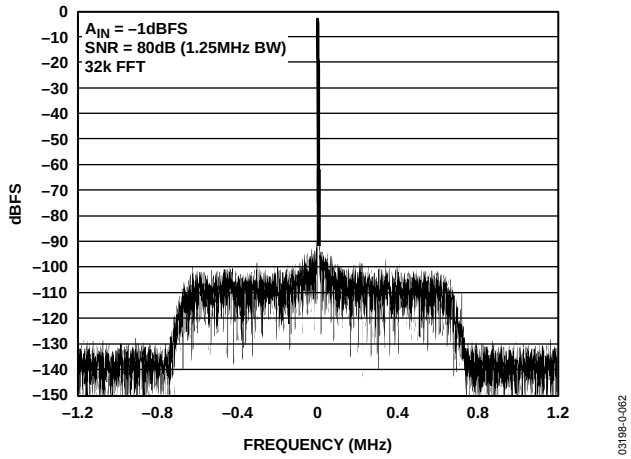


Figure 3. CDMA2000 with Single Tone A_{IN} = 76 MHz; Encode = 61.44 MSPS

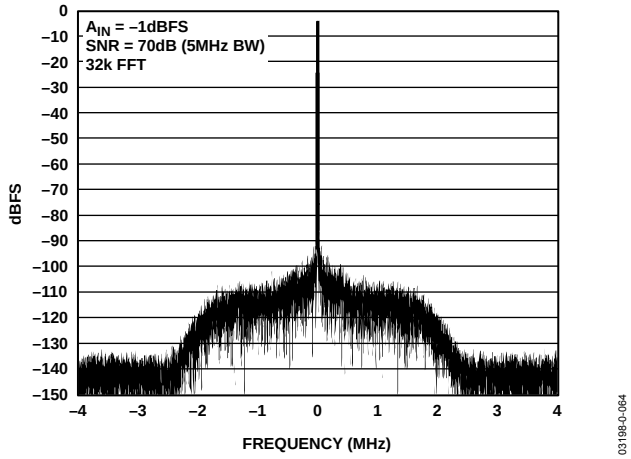


Figure 4. WCDMA with Single Tone A_{IN} = 169 MHz; Encode = 61.44 MSPS

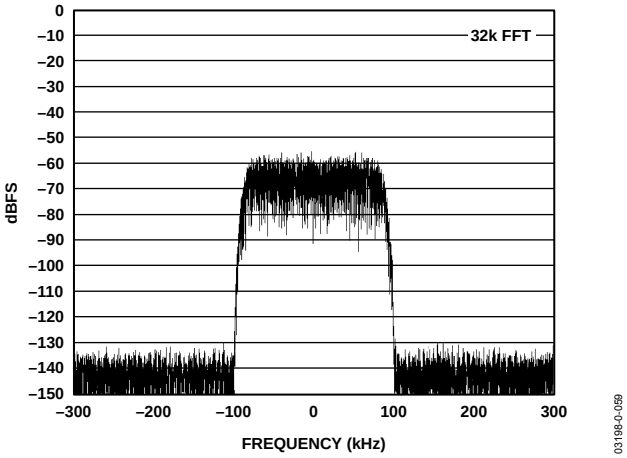


Figure 5. GSM/EDGE Carrier A_{IN} = 30 MHz; Encode = 61.44 MSPS

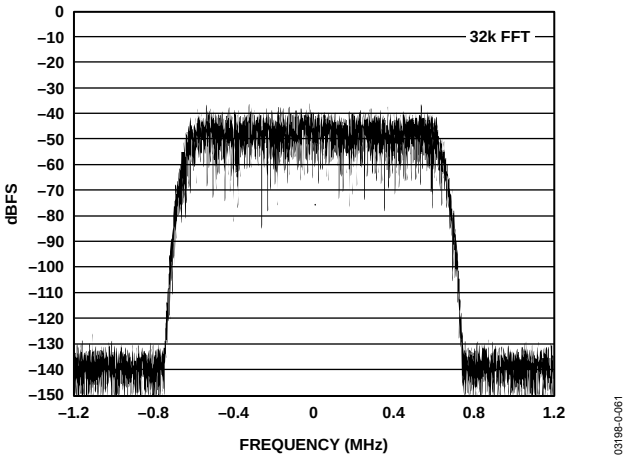


Figure 6. CDMA2000 Carrier A_{IN} = 76 MHz; Encode = 61.44 MSPS

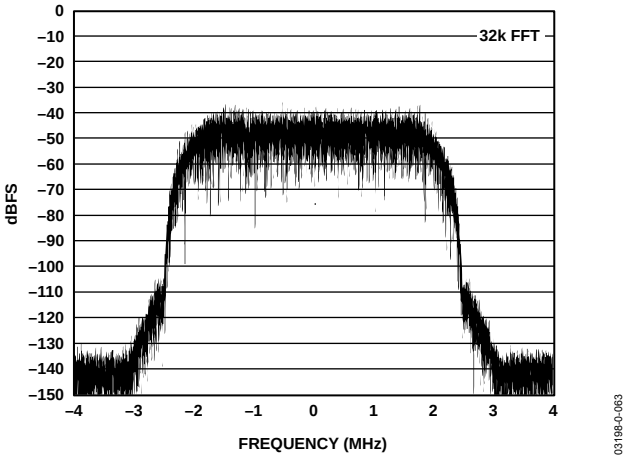


Figure 7. WCDMA Carrier A_{IN} = 169 MHz; Encode = 61.44 MSPS

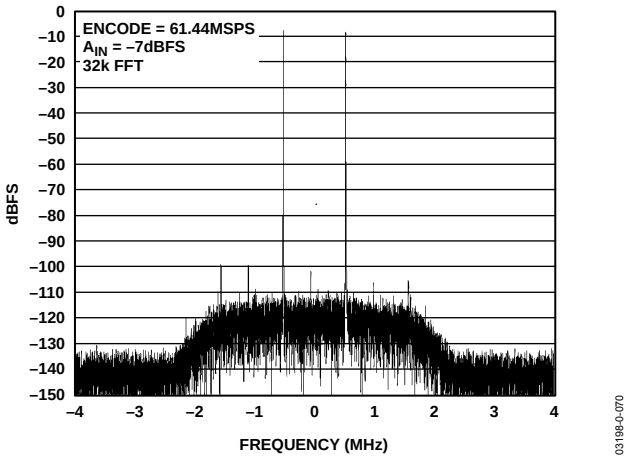


Figure 8. Two Tones at 15 MHz and 16 MHz

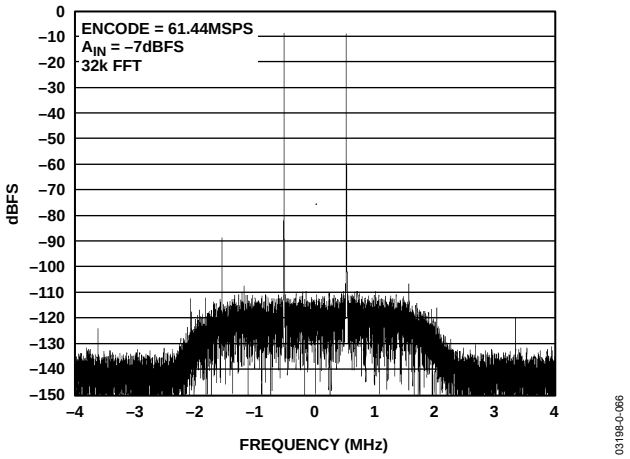


Figure 11. Two Tones at 55 MHz and 56 MHz

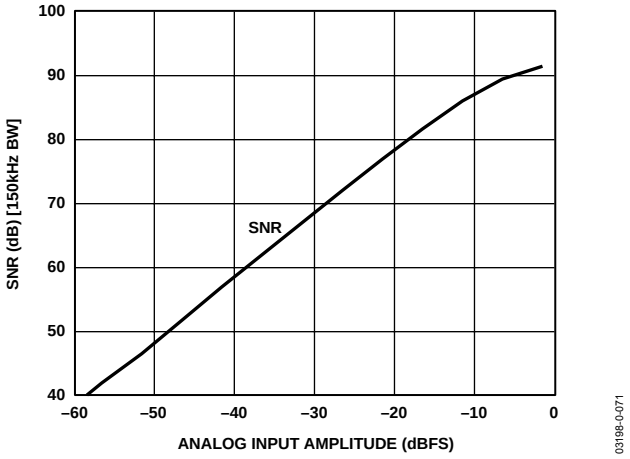


Figure 9. Noise vs. Analog Amplitude at 25 MHz

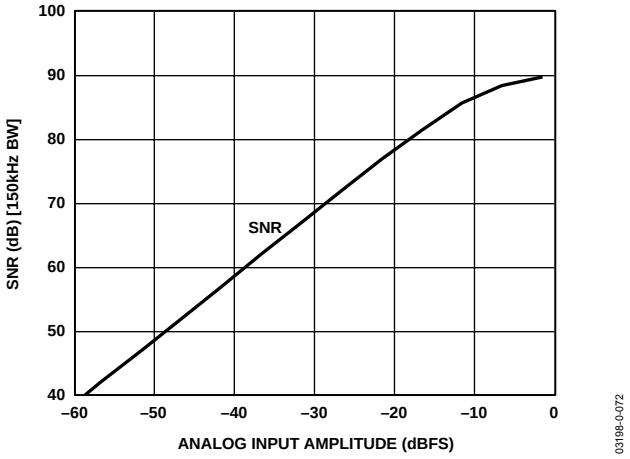


Figure 12. Noise vs. Analog Amplitude at 68 MHz

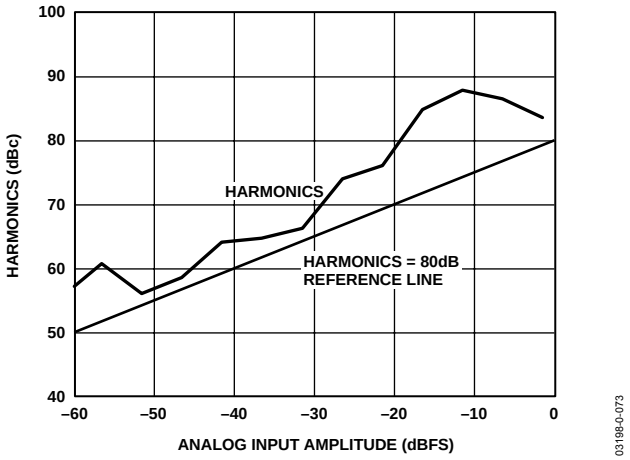


Figure 10. Harmonics vs. Analog Amplitude at 25 MHz

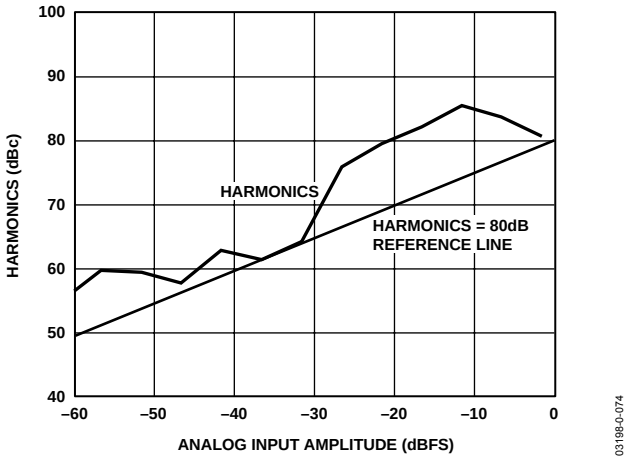


Figure 13. Harmonics vs. Analog Amplitude at 68 MHz

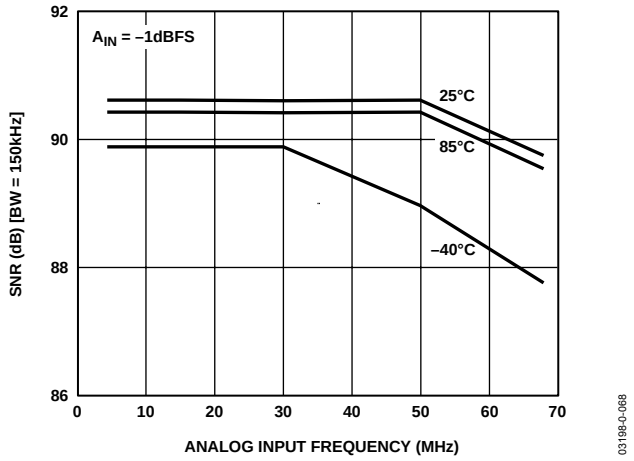


Figure 14. Noise vs. Analog Frequency

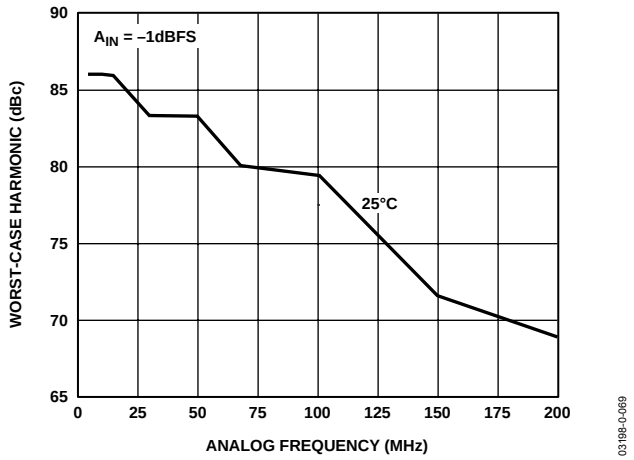


Figure 15. Harmonics vs. Analog Frequency

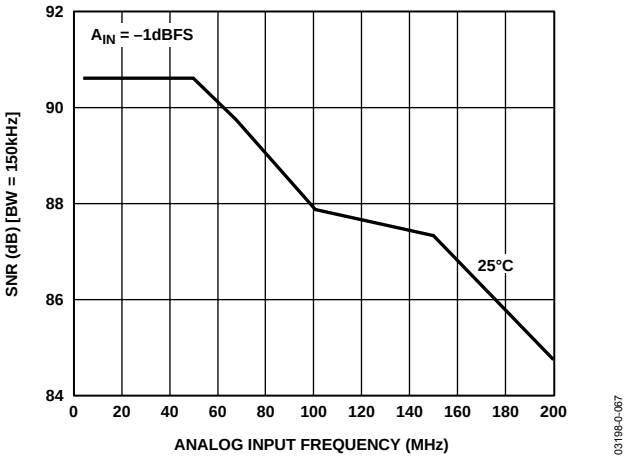


Figure 16. Noise vs. Analog Frequency (IF)

DDC TIMING DIAGRAMS

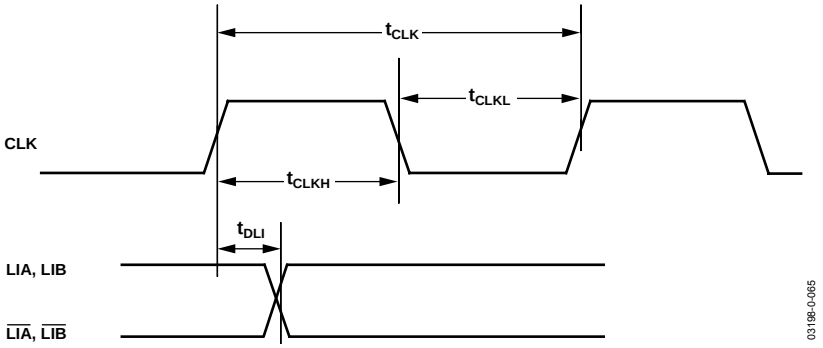


Figure 17. Level Indicator Output Switching Characteristics

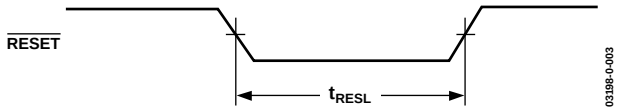


Figure 18. Reset Timing Requirements

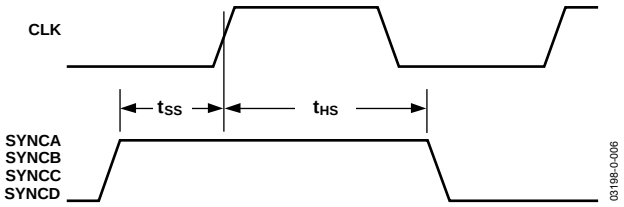


Figure 19. SYNC Timing Inputs

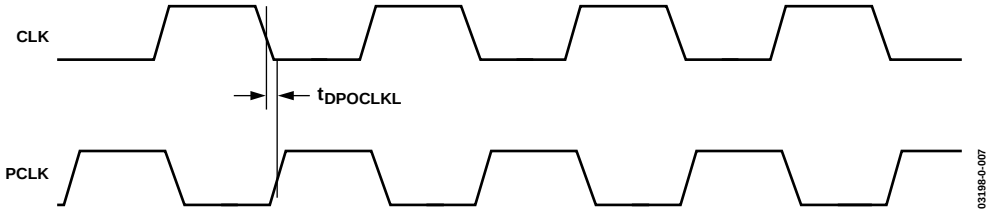


Figure 20. PCLK to CLK Switching Characteristics Divide-by-1

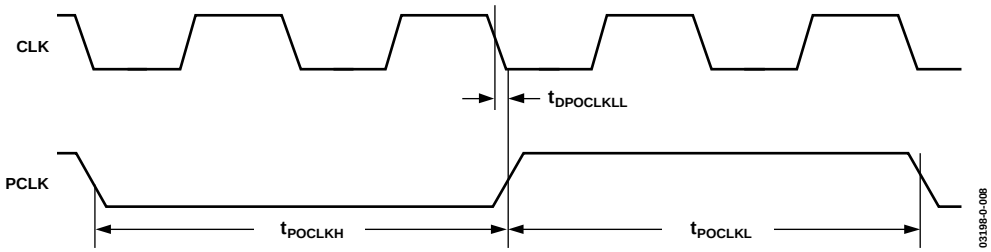


Figure 21. PCLK to CLK Switching Characteristics Divide-by-2, -4, or -8

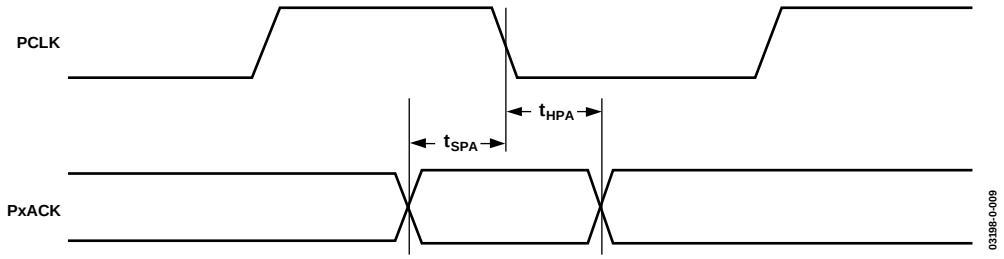


Figure 22. Master Mode PxACK to PCLK Setup and Hold Characteristics

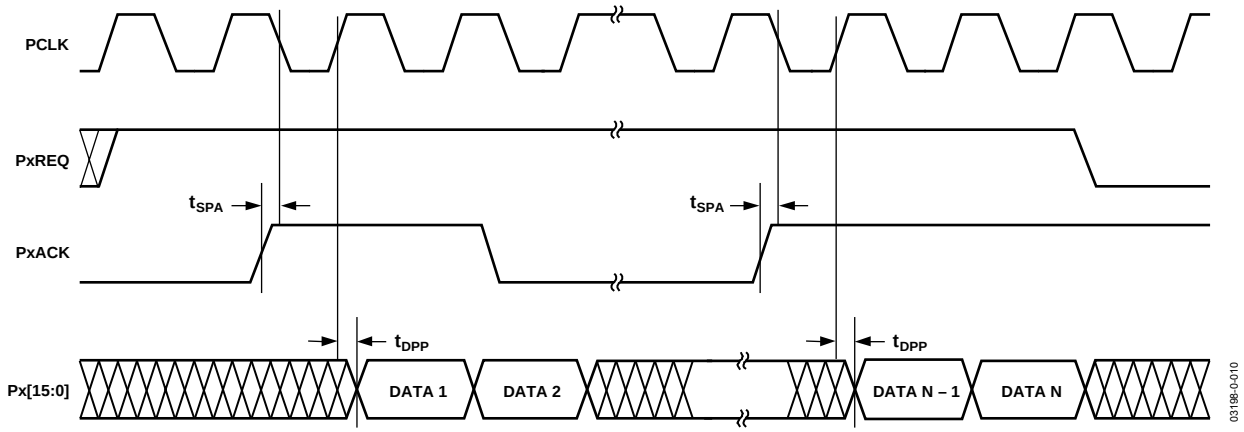


Figure 23. Master Mode PxACK to PCLK Switching Characteristics

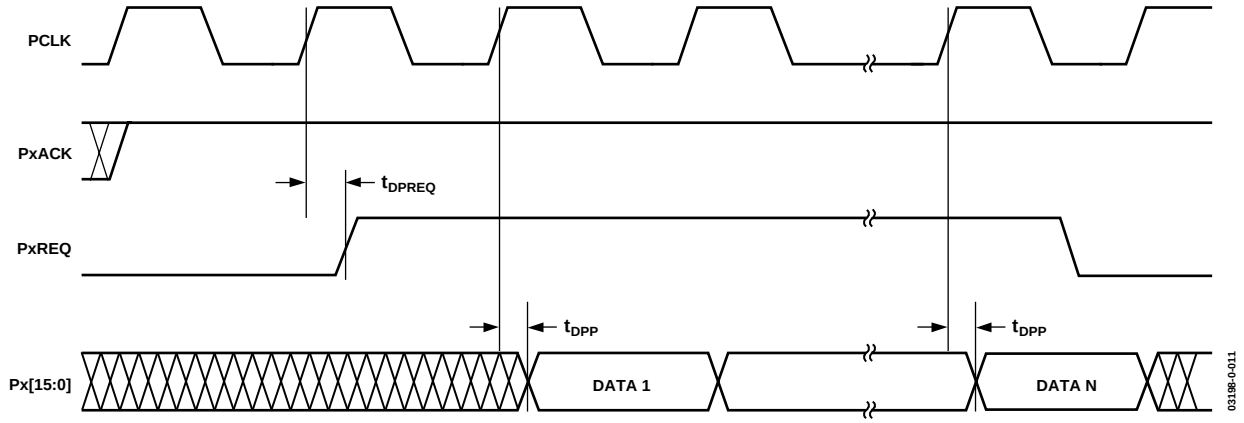


Figure 24. Master Mode PxREQ to PCLK Switching Characteristics

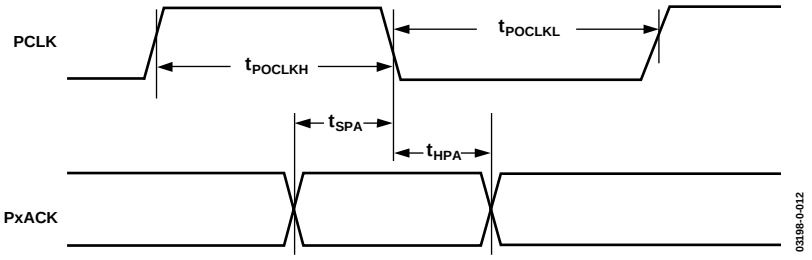


Figure 25. Slave Mode PxACK to PCLK Setup and Hold Characteristics

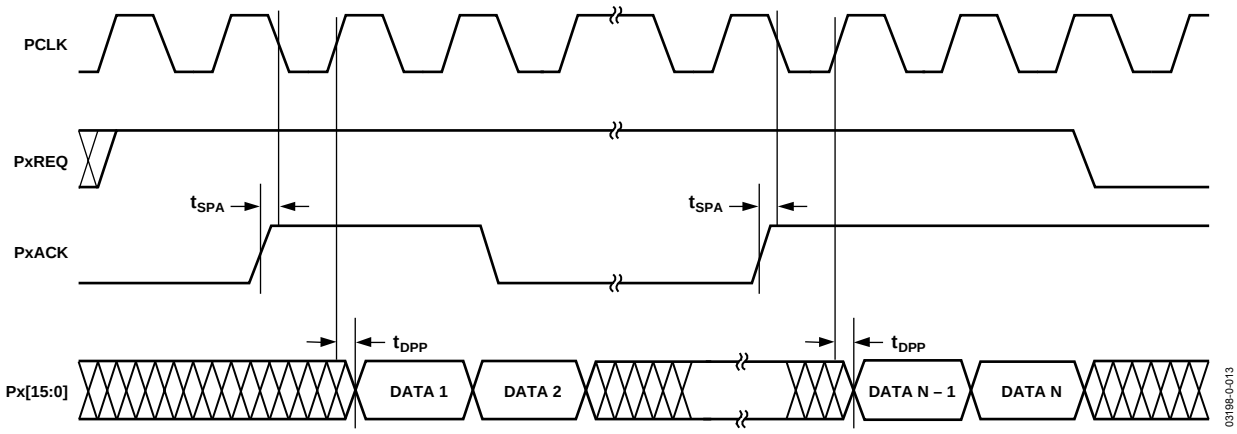


Figure 26. Slave Mode PxACK to PCLK Switching Characteristics

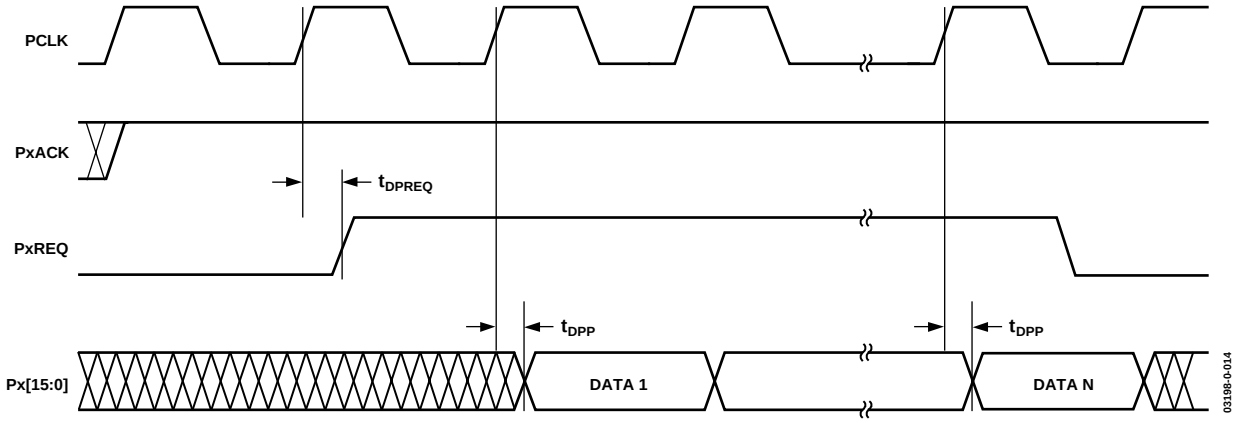


Figure 27. Slave Mode PxREQ to PCLK Switching Characteristics

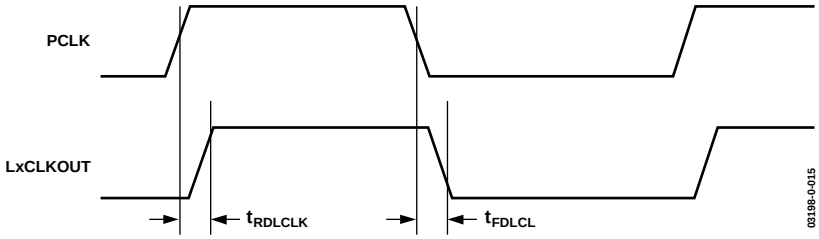


Figure 28. LxCLKOUT to PCLK Switching Characteristics

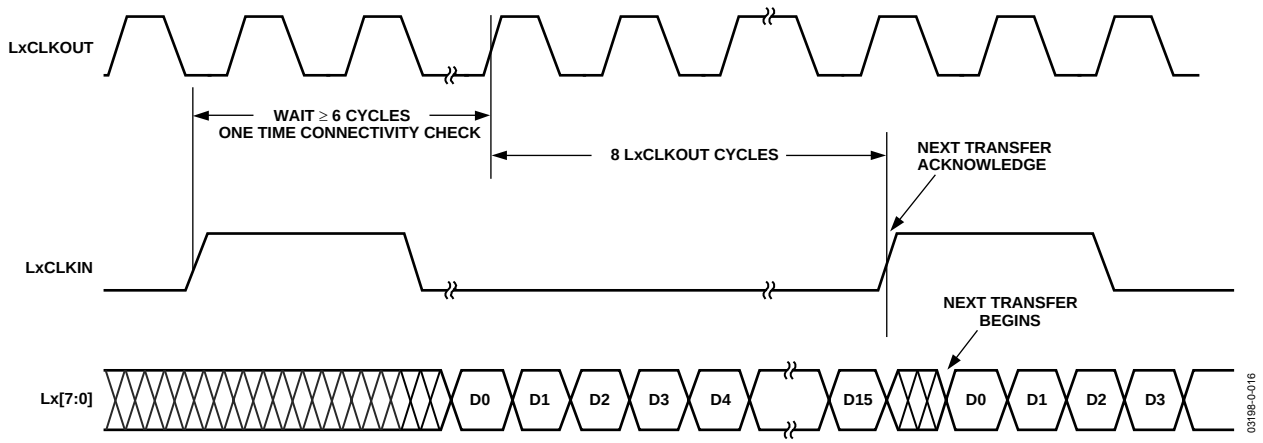


Figure 29. LxCLKIN to LxCLKOUT Data Switching Characteristics

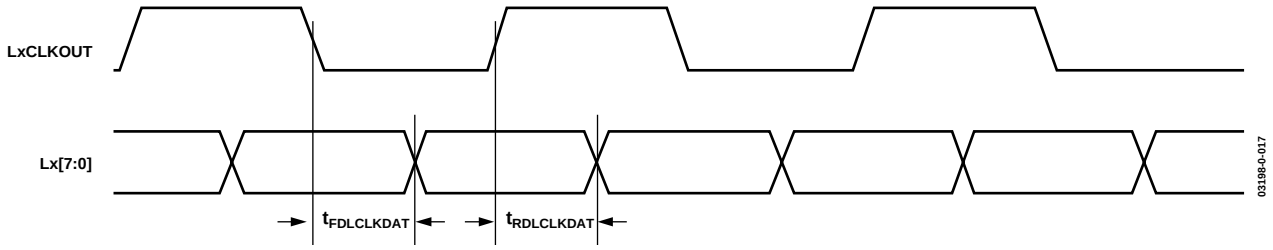


Figure 30. LxCLKOUT to Lx[7:0] Data Switching Characteristics

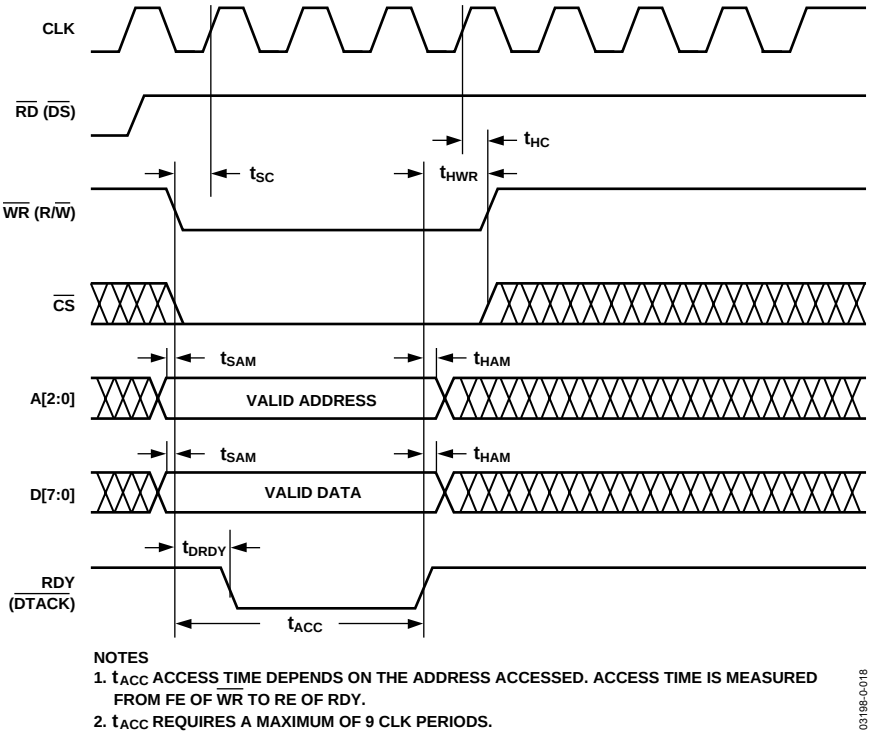
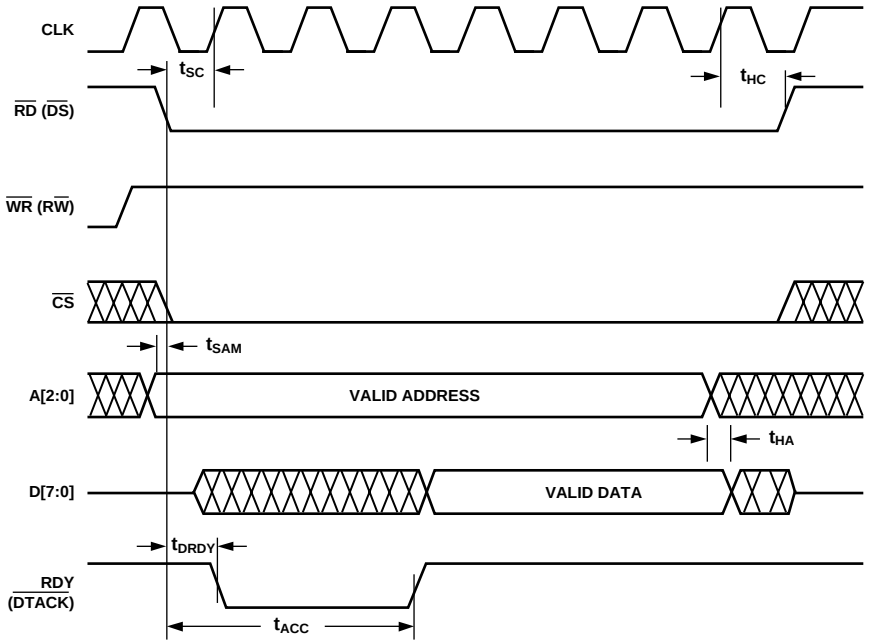


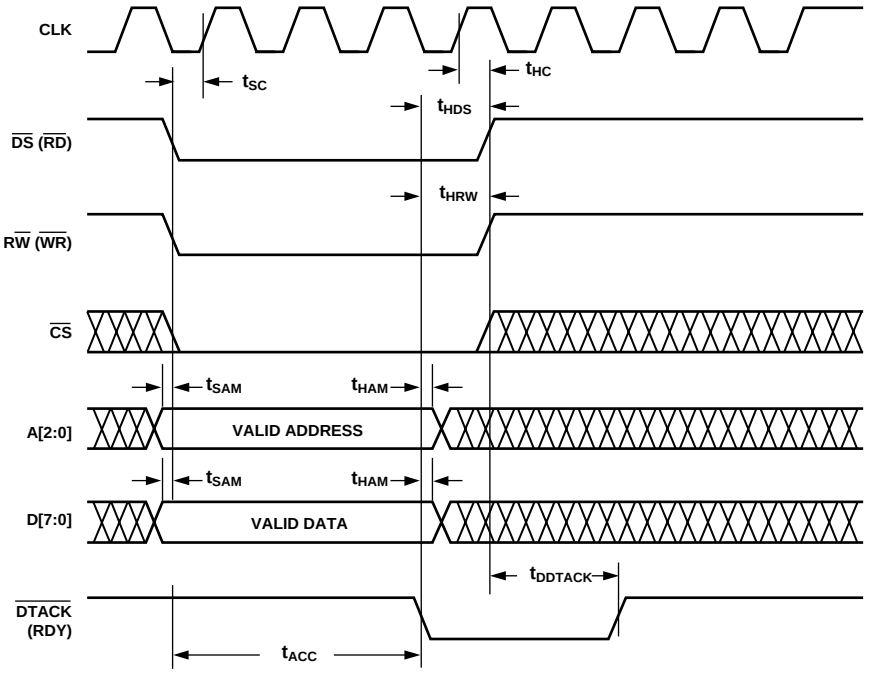
Figure 31. INM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

03198-0-019

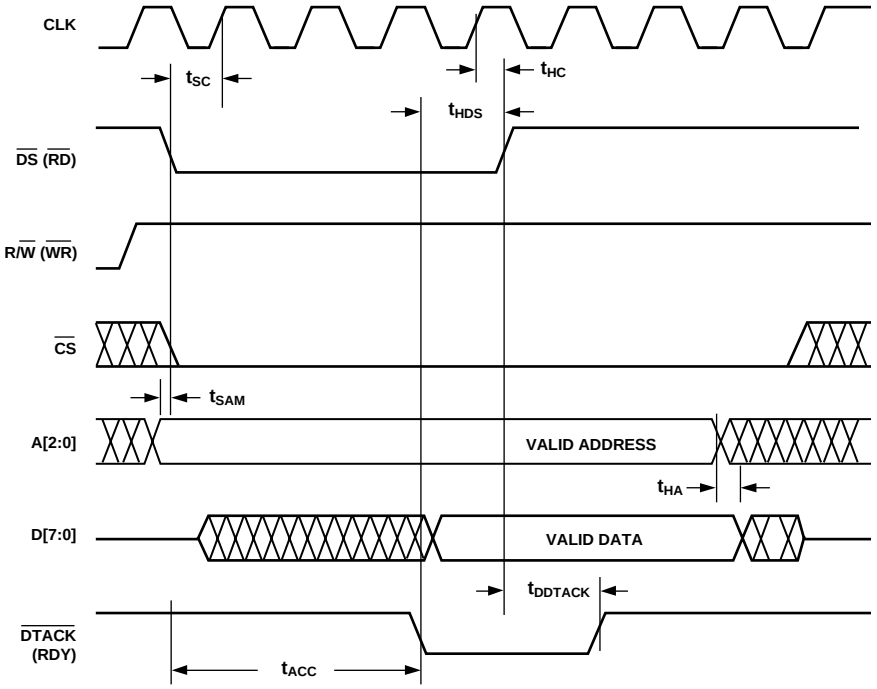
Figure 32. INM Microport Read Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF 9 CLK PERIODS.

03198-0-020

Figure 33. MNM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM THE FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

Figure 34. MNM Microport Read Timing Requirements

TERMINOLOGY

Crosstalk
Coupling onto one channel being driven by a (−0.5 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal. Measurement includes all spurs resulting from both direct coupling and mixing components.

IF Sampling (Undersampling)
Due to the effects of aliasing, an ADC is not necessarily limited to Nyquist sampling. Frequencies above Nyquist are aliased and appear in the first Nyquist zone (dc to Sample Rate/2). Care must be taken to limit the bandwidth of the sampled signal so that it does not overlap Nyquist zones and alias onto itself. IF sampling performance is limited by the bandwidth of the input SHA (sample-and-hold amplifier) and clock jitter. (Jitter adds more noise at higher input frequencies.)

Nyquist Sampling (Oversampling)
Oversampling occurs when the frequency components of the analog input signal are below the Nyquist frequency ($F_{clock}/2$), and requires that the analog input frequency be sampled at least two samples per cycle.

Out-of-Range Recovery Time
Out-of-range recovery time is the time it takes for the analog-to-digital converter (ADC) to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Processing Gain
When the tuned channel occupies less bandwidth than the input signal, this rejection of out-of-band noise is referred to as *processing gain*. By using large decimation factors, this processing gain can improve the SNR of the ADC by 20 dB or more. The following equation can be used to estimate processing gain:

$$Processing_Gain = 10\log\left[\frac{Sample_Rate/2}{Filter_Bandwidth}\right]$$

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the measured input signal to the rms sum of all other spectral components within the programmed DDC filter bandwidth, excluding the first six harmonics and dc. The value for SNR is expressed in decibels (dB).

Two-Tone IMD Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

ADC EQUIVALENT CIRCUITS

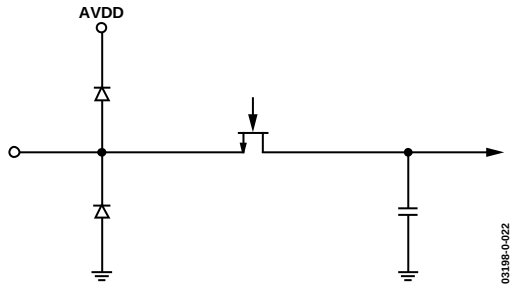


Figure 35. Analog Input Circuit

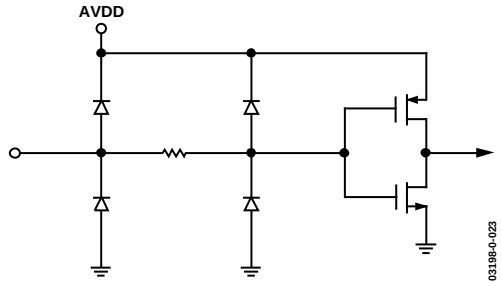


Figure 36. Digital Input

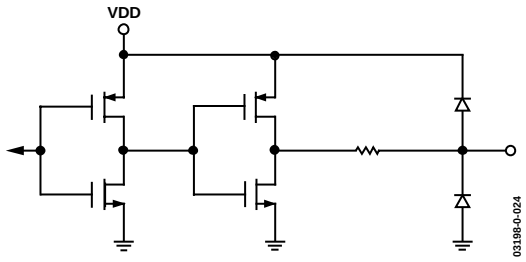


Figure 37. Digital Output

THEORY OF OPERATION

The AD6652 has two analog input channels, four digital filtering channels, and two digital output channels. The IF input signal passes through several stages before it appears at the output port(s) as a well-filtered, decimated digital baseband signal:

- 12-bit A/D conversion
- Frequency translation from IF to baseband using quadrature mixers and NCOs
- Second-order resampling decimating CIC FIR filter (rCIC2)
- Fifth-order decimating CIC FIR filter (CIC5)
- RAM coefficient decimating FIR filter (RCF)
- Automatic gain control (AGC)
- 2× interpolation and channel interleave

Any stage can be bypassed with the exception of the ADC front end. Any combination of processing channels can be combined or interleaved after the RCF stages to achieve demanding filtering objectives that are not possible with just one channel. In the following sections, each stage is examined to allow the user to fully utilize the AD6652's capabilities.

The dual ADC design is useful for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any fs/2 frequency segment from dc to 100 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 200 MHz analog input is permitted, but at the expense of increased ADC distortion.

In nondiversity applications, up to four GSM/EDGE-type carriers can be concurrently processed from the ADC stage. Wideband signals, such as WCDMA/CDMA2000, require the power of two AD6652 processing channels per carrier to adequately remove adjacent channel interference. When diversity techniques are employed, the number of carriers that can be processed is halved due to the dual processing requirement of diversity reception.

Flexible channel multiplexing in the digital downconverter (DDC) stage allows one to four channels to be interleaved onto one output port. Four synchronization input pins allow startup, frequency hop, and AGC functions to be precisely orchestrated with other devices. The NCO's phase can be set to produce a known offset relative to another channel or device.

Programming and control of the AD6652 is accomplished using an 8-bit parallel interface.

ADC ARCHITECTURE

The AD6652 front-end consists of two high performance, 12-bit ADCs, preceded by differential sample-and-hold amplifiers (SHA) that provide excellent SNR performance from dc to 200 MHz. A flexible, integrated voltage reference allows analog inputs up to 2 V p-p. Each channel is equipped with an overrange pin that toggles high whenever the analog input exceeds the upper or lower reference voltage boundary. ADC outputs are internally routed to the input matrix of the DDC stage for channel distribution. The ADC data outputs are not directly accessible to the user.

Each sample-and-hold amplifier (SHA) is followed by a pipelined switched capacitor ADC. The pipelined ADC is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Analog Input Operation

The analog inputs to the AD6652 are differential switched capacitor SHAs that have been designed for optimum performance while processing differential input signals. The AD6652 accepts inputs over a wide common-mode range; however, an input common-mode voltage V_{CM}, one-half of AVDD, is recommended to maintain optimal performance and to minimize signal-dependent errors.

Referring to Figure 38, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent upon the application. In IF undersampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, the shunt capacitors would limit the input bandwidth.

For best dynamic performance, the source impedances driving the differential analog inputs should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

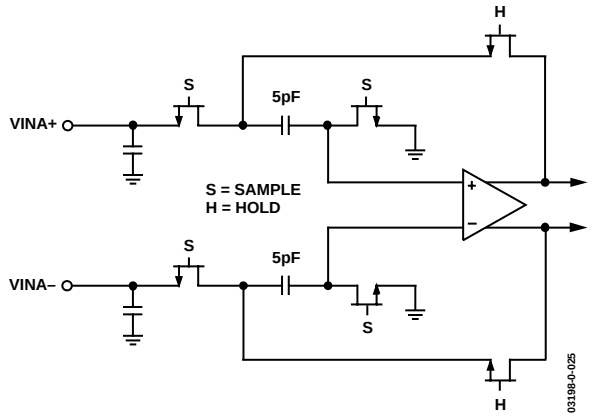


Figure 38. Switched-Capacitor SHA Input for One ADC Channel

The SHA should be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as follows:

$$VCM_{MIN} = VREF/2$$
$$VCM_{MAX} = (AVDD + VREF)/2$$

The minimum common-mode input level allows the AD6652 to accommodate ground-referenced inputs.

Although optimum performance is achieved with a differential input, a single-ended source can be driven into VIN+ or VIN−. In this configuration, one input accepts the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V p-p signal can be applied to VIN+, while a 1 V reference is applied to VIN−. The AD6652 then accepts a signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance might degrade significantly, compared to the differential case. However, the effect is less noticeable at lower analog input frequencies.

Differential Input Configurations

Optimum performance is achieved while driving the AD6652 inputs in a differential input configuration. For baseband applications to Nyquist, the AD8138 Differential Driver provides excellent performance and a flexible interface to the ADC The output common-mode voltage of the AD8138 is easily set to one-half of AVDD, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

At input frequencies above Nyquist, the performance of most amplifiers is not adequate to achieve the true performance of the AD6652 ADC stage.

This is especially true in IF undersampling applications in which input frequencies in the range of 70 MHz to 200 MHz are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure 39. Transformer T1 is a center-tapped, 1:4 impedance ratio broadband RF transformer. The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

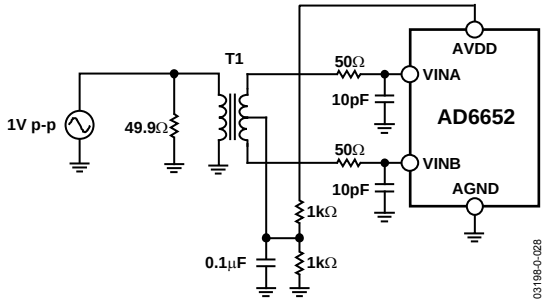


Figure 39. Differential AC-Coupled Input for One Channel of the AD6652

ADC Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD6652. The input span of the ADC tracks reference voltage changes linearly. An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as follows:

$$REFT = 1/2\ (AVDD + VREF)$$
$$REFB = 1/2\ (AVDD - VREF)$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

As shown by the equations above, the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage. Proper operation of the AD6652 requires that VREF be no less than 0.5 V and no greater than 1.0 V.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V, or adjusted within the same range, as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved with the reference set to the largest input span of 2 V p-p. The relative SNR degradation is 3 dB when changing from 2 V p-p mode to 1 V p-p mode.

If operation using an external reference voltage is desired, it can be substituted for the internal reference, as detailed in the External Reference Operation section.

Internal Reference Connection

A comparator within the AD6652 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 11. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 40), setting VREF to a FIXED 1 V reference output. Connecting the SENSE pin directly to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a fixed 0.5 V reference output. If a resistor divider is connected, as shown in Figure 41, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF programmable output defined as follows:

$$VREF = 0.5 \times (1 + R2/R1)$$

In all reference configurations, REFT and REFB drive the A/D conversion core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

The reference amplifier switch is located near the bottom left. The SENSE pin is shown connected to ground, which sets VREF to 1 V. Decoupling capacitors must be duplicated for the Channel B ADC core, if it is used. The Channel B ref amp and ADC core are identical to those of Channel A, but are not shown.

Table 11. Reference SENSE Operation

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	External Reference	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	0.5 × (1 + R2/R1)	2 × VREF (See Figure 42)
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

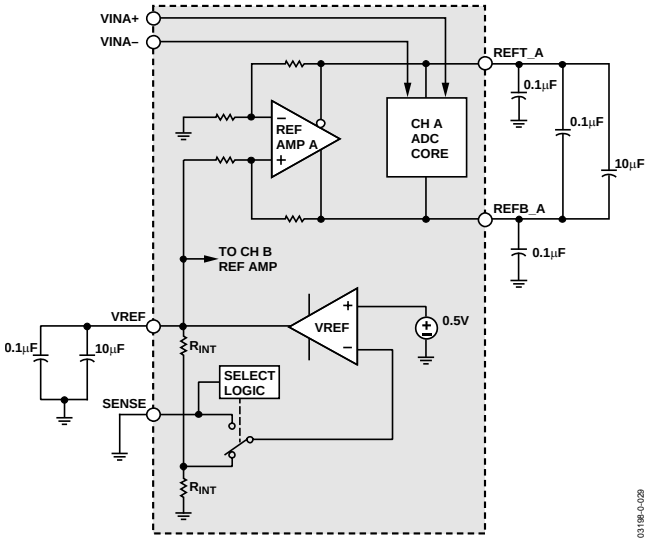


Figure 40. Fixed Internal Reference Configuration

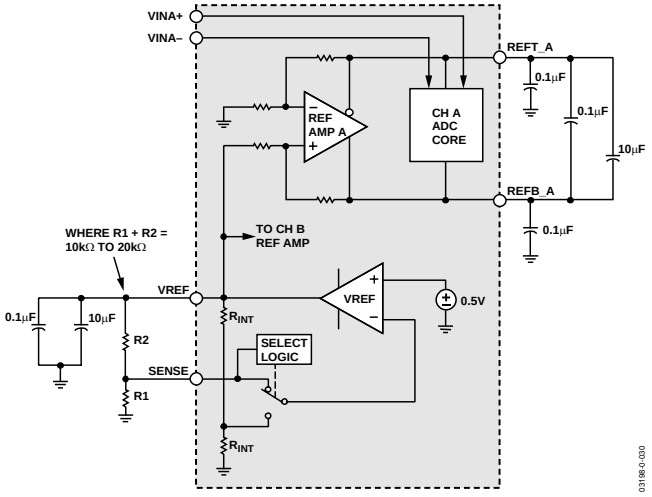


Figure 41. Programmable Reference Configuration

External Reference Operation

An external reference voltage can be used to enhance the gain accuracy of the ADC or improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) might be necessary to reduce gain-matching errors to an acceptable level. A high-precision external reference can also be selected to provide lower gain and offset temperature drift.

When the SENSE pin is tied to AVDD as in Figure 42, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V.

If the internal reference of the AD6652 is used to drive multiple ICs, the loading on VREF by the other converters must be considered. Figure 44 shows how the internal reference voltage is affected by loading.

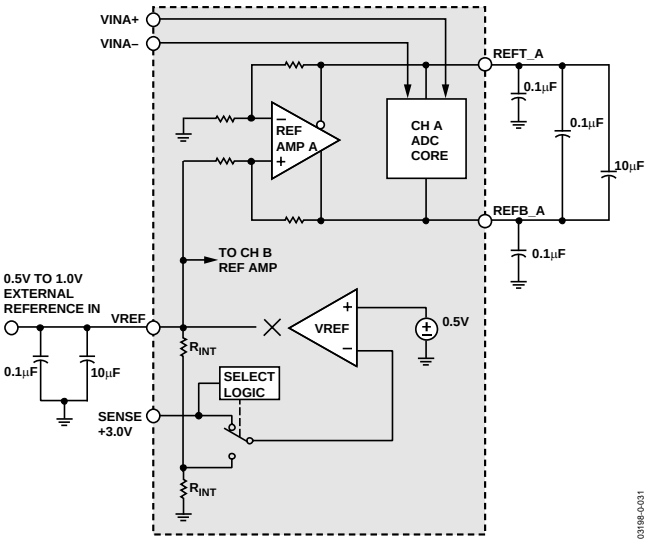


Figure 42. External Reference Operation with Connections Shown for Channel A Only

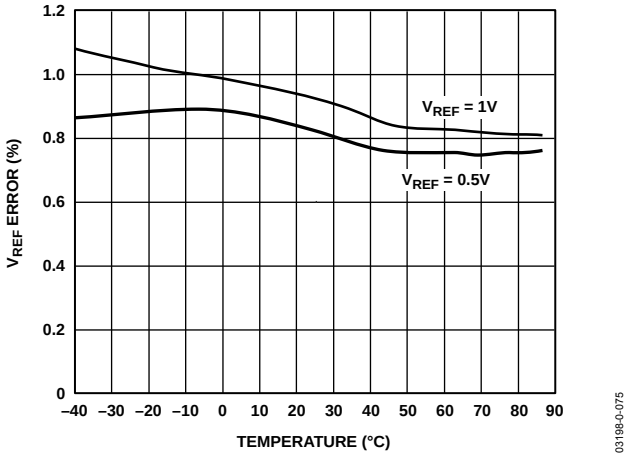


Figure 43. Typical VREF Drift

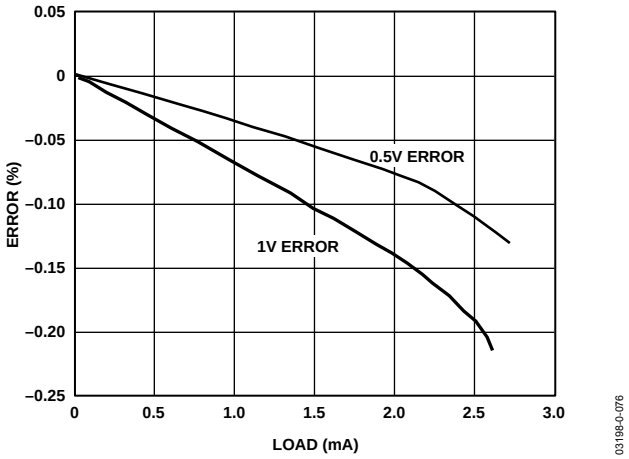


Figure 44. VREF Accuracy vs. Load

Shared Reference Mode

The shared reference mode allows the user to connect the references from the dual ADCs together for superior gain and offset matching performance. If the ADCs are to function independently, the reference decoupling should be treated independently and can provide superior isolation between the dual ADC channels. To enable shared reference mode, the SHRDREF pin must be tied high and the differential references must be externally shorted together, that is, REFTA must be shorted externally to REFTB and REFBA must be shorted externally to REFBB.

Clock Input Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result can be sensitive to ACLK clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD6652 contains a clock duty cycle stabilizer that re-times the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. Duty cycle stabilizing is engaged by setting DUTYEN to logic high. This allows a wide range of ACLK clock input duty cycles without affecting the performance of the AD6652 ADC stage.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 2 ms to 3 ms to allow the DLL to acquire and lock to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_A) can be calculated with the following equation:

$$SNR\ degradation = 20 \times \log10\ [1/2 \times p \times f_{INPUT} \times t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

To minimize clock jitter, treat the ACLK clock input as an analog signal. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the ACLK clock is generated from another type of source (by gating, dividing, or other methods), re-time it by the original clock at the last step.

ADC Power-Down Mode

The power dissipated by the AD6652 front-end ADC is proportional to its sampling rate. Normal ADC operation requires that both PDWN pins be set to logic low. The ADC can be placed in a power-down mode by setting both PDWN pins to logic high. Low power dissipation in power-down mode is achieved by shutting down the reference buffers and biasing networks of both ADC channels. Both power-down pins must be driven together either high or low for proper ADC operation.

For maximum power savings, the ACLK and analog input(s) should remain static while in standby mode, resulting in a typical power consumption of 1 mW for the ADC. If the clock inputs remain active while in standby mode, typical power consumption for the ADC is 12 mW.

ADC Wake-Up Time

The decoupling capacitors on REFT and REFB are discharged when entering standby mode, and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode. Shorter standby cycles result in proportionally shorter wake-up times. With the recommended 0.1 μF and 10 μF decoupling capacitors on REFT and REFB, it takes approximately 1 s to fully discharge the reference buffer decoupling capacitors, and 5 ms to restore full operation.

DIGITAL DOWNCONVERTER ARCHITECTURE OVERVIEW

DATA INPUT MATRIX

The digital downconverter (DDC) section features dual high speed 12-bit input ports that are capable of crossbar multiplexing of data to the four processing channels that follow the input matrix. In addition, a third input option to the matrix is available to facilitate BIST (built-in self-test). This option is a pseudorandom noise (PN) sequence. The dual input ports permit diversity reception of a carrier, or they can be treated as unrelated and independent inputs. Either input port or the PN sequence can be routed to any or all four tuner channels. This flexibility allows up to four signals to be processed simultaneously. Refer to the DDC Input Matrix section for a more complete description.

NUMERICALLY CONTROLLED OSCILLATOR

Frequency translation is accomplished with a 32-bit complex numerically controlled oscillator (NCO). Each of the four processing channels contains a separate NCO. Real data entering this stage is separated into in-phase (I) and quadrature (Q) components. This stage translates the input signal from a digital intermediate frequency (IF) to digital baseband. Phase and amplitude dither can be enabled on-chip to improve spurious performance of the NCO. A phase-offset word is available to create a known phase relationship between multiple AD6652s or between channels.

SECOND-ORDER rCIC FILTER

Following frequency translation is a resampling, fixed coefficient, high speed, second-order, resampling cascade integrator comb (rCIC2) filter, which reduces the sample rate based on the ratio between the decimation and interpolation registers. The resampler allows for noninteger relationships between the master clock and the output data rate. This stage can be bypassed by setting the decimation/interpolation ratio to 1.

FIFTH-ORDER CIC FILTER

The next stage is a fifth-order cascaded integrator comb (CIC5) filter, whose response is defined by the decimation rate. The purpose of these filters is to reduce the data rate to the final filter stage and to provide antialias filtering. The reduced data rate allows the RAM coefficient filter (RCF) stage to calculate more taps per output.

RAM COEFFICIENT FILTER

The RAM coefficient filter (RCF) stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 256 (1 to 32 in practice). Each RAM coefficient FIR filter (RCF in Figure 1) can handle a maximum of 160 taps. Two or more RCF stages can be combined using flexible channel configuration to increase the processing power beyond the 160 tap maximum.

The RCF outputs of each channel can be directly routed to one or both output ports or to an AGC stage, where selected DDC channels can be interleaved and interpolated in a half-band filter, if desired.

INTERPOLATING HALF-BAND FILTERS AND AGC

Processed RCF data can also be routed to two half-band interpolation stages, where up to four channels can be combined (interleaved), interpolated by a factor of two, and automatic gain control (AGC) applied. Each AGC stage has a dynamic range of 96.3 dB. These stages can be bypassed independently of each other. The outputs from the two AGC stages are routed to both output port multiplexers. Each output has a link port to permit seamless data interface with DSP devices such as the TigerSHARC. A multiplexer for each port selects one of the six data sources to appear at the device parallel or link output pins.

The overall filter response for the AD6652 is the composite of all decimating and interpolating stages. Each successive filter stage is capable of narrower transition bandwidths, but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage helps to minimize overall power consumption.

Figure 45 illustrates the basic function of the AD6652, that is, to select and filter a single carrier from a wide input spectrum and to down-convert it to baseband data. Figure 46 shows examples of the combined filter response of the rCIC2, CIC5, and RCF for narrowband and wideband carriers.

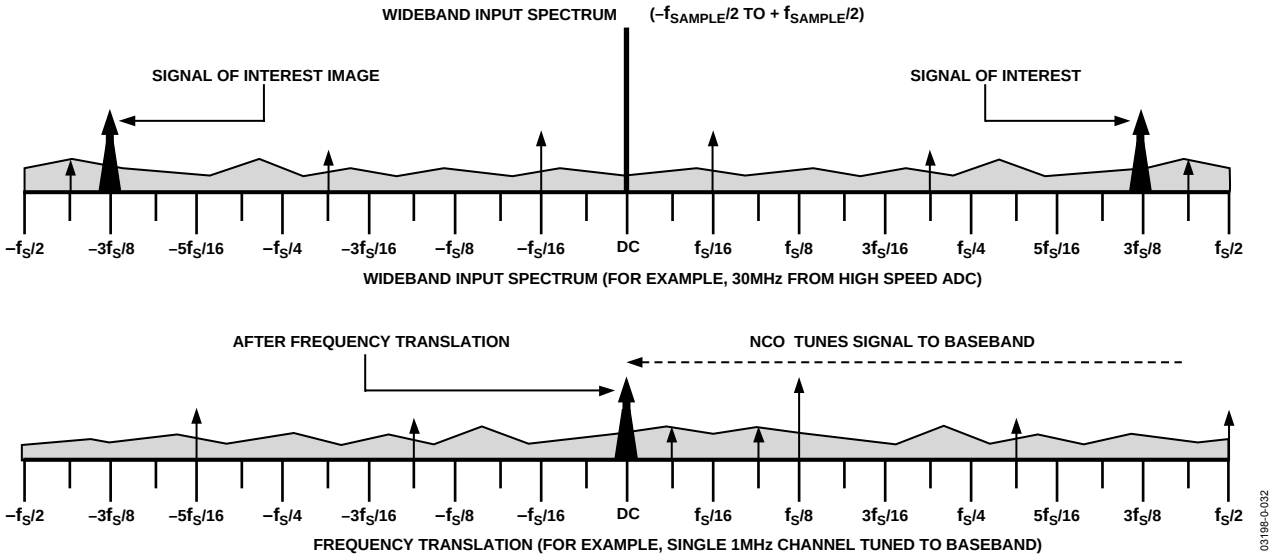


Figure 45. AD6652 Frequency Translation of Wideband Input Spectrum

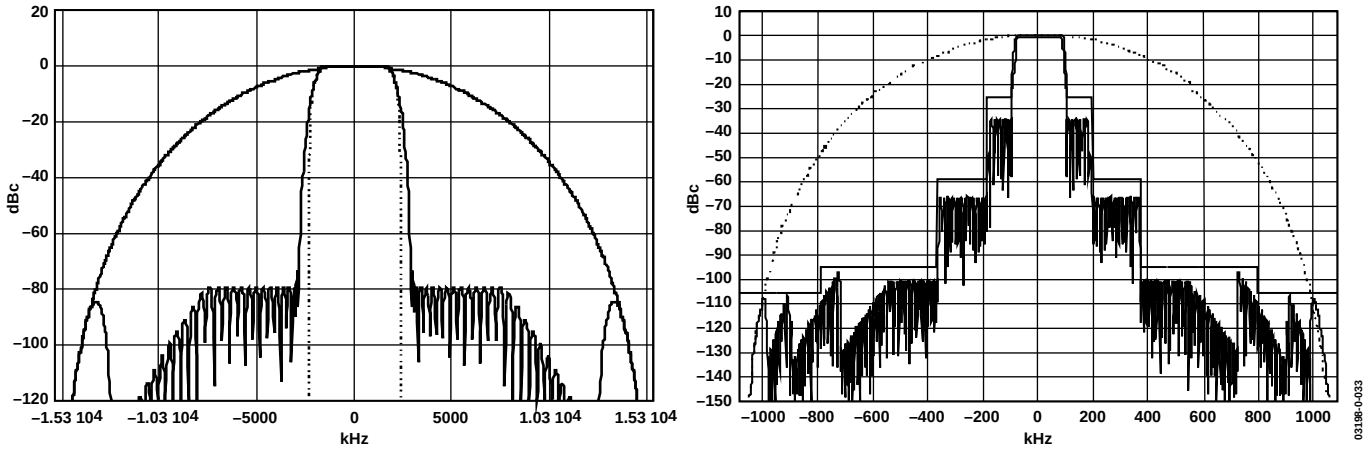


Figure 46. Filter Response (left) Meets UMTS (Wideband) Specifications. Narrower Filter (right) Designed for EDGE Application (65 MSPS ADC Conversion Rate and 541.6 kSPS DDC Output Rate)

CONTROL REGISTER AND MEMORY MAP ADDRESS NOTATION

The following sections make frequent references to programmable registers and the memory mapping structure of the AD6652. A good overview of the control registers and memory mapping structure is found beginning in the External Memory Map section. The following conventions are used in this addressing scheme:

- Control register addresses that begin with 0x indicate that the address that follows is in hexadecimal notation.
- All hexadecimal addresses are 8 bits wide, and each address can accommodate register data that is 20 bits wide; however, many of the available 20 bits per address are unused.
- A colon following an address indicates the specific bit number(s), in decimal format, of the function that is being described.
- Eight, 3-bit external memory map addresses are shown in decimal format in Table 22. Each of these addresses can accommodate 8 bits of register data.

Decimal Addressing Example: 7:4 indicates that this is an external memory address (no 0x prefix) and that the binary address is 111, because only 3 external address bits are assigned. Also, only Bit 4 of the 8-bit data field is described or referred to.

Hex Addressing Example: 0x0A:7–0 indicates that the binary address is 00001010 and that Bits 7 through 0 are involved with the function being described. Because this address begins with 0x, the user knows that it is not an external memory address, and can be either an individual channel address register or an output port control register, depending upon how it was routed using the external memory address registers.

The largest 8-bit address that is used in the hexadecimal address scheme is A9 or 169 decimal. This might not seem to be enough memory addressing capacity, but, because addresses are re-used with the external memory mapping scheme, there is no shortage of address capability.

DDC INPUT MATRIX

The digital downconverter stages feature dual high speed crossbar-switched input ports that allow the most flexibility in routing the two ADC data streams to the four receive processing channels. Crossbar switching means that any of the four processing channels can receive data from either Port A or Port B for a total of 16 possible combinations, as shown in Table 12. Input port routing is selected in *each* NCO's control register at 0x88:6.

Table 12. Crossbar-Switched Routing of the Two 12-Bit ADC Data Streams (A and B) Using the DDC Input Matrix

Channel 3	Channel 2	Channel 1	Channel 0
A	A	A	A
A	A	A	B
A	A	B	A
A	A	B	B
A	B	A	A
A	B	A	B
A	B	B	A
A	B	B	B
B	A	A	A
B	A	A	B
B	A	B	A
B	A	B	B
B	B	A	A
B	B	A	B
B	B	B	A
B	B	B	B

DDC DATA LATENCY

The overall signal path latency from DDC input to output can be expressed in high speed clock cycles. Use the following equation to calculate the latency:

$$T_{latency} = M_{rCIC2}\,(M_{CICS} + 7) + N_{taps} + 26$$

where:

M_{rCIC2} and M_{CIC5} are decimation values for the rCIC2 and CIC5 filters, respectively.

N_{taps} is the number RCF taps chosen.

GAIN SWITCHING

The AD6652 includes circuitry that is useful in applications in which large dynamic range input signals exist. This circuitry allows digital thresholds to be set such that an upper and a lower threshold can be programmed.

One use of this circuitry is to detect when an ADC is about to reach full scale with a particular input condition. The results provide a flag can quickly insert an attenuator to prevent ADC overdrive. If 18 dB (or any arbitrary value) of attenuation (or gain) is switched in, then the signal dynamic range of the system is increased by 18 dB. The process begins when the input signal reaches the upper programmed threshold. In a typical application, this might be set 1 dB (user definable) below full scale. When this input condition is met, the appropriate LI (LIA, $\overline{\text{LIA}}$, LIB or $\overline{\text{LIB}}$) signal associated with either the A or B input port is made active. This can be used to switch the gain or attenuation of the external circuit. The LI line stays active until

the input condition falls below the lower programmed threshold.

To provide hysteresis, a dwell time register (see Table 28) is available to hold off switching of the control line for a predetermined number of clocks. Once the input condition is below the lower threshold, the programmable counter begins counting high speed clocks. As long as the input signal stays below the lower threshold for the number of high speed clock cycles programmed, the attenuator is removed on the terminal count. However, if the input condition goes above the lower threshold with the counter running, it is reset and must fall below the lower threshold again to initiate the process. This prevents unnecessary switching between states.

Threshold settings for LI are illustrated in Figure 47. When the input signal goes above the upper threshold, the appropriate LI signal becomes active. Once the signal falls below the lower threshold, the counter begins counting. If the input condition goes above the lower threshold, the counter is reset and starts again, as shown in the figure. Once the counter has terminated to 0, the LI line goes inactive.

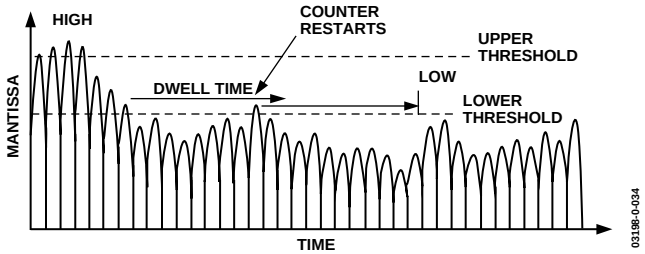


Figure 47. Threshold Settings for LI

The LI line can be used for a variety of functions. It can be used to set the controls of an attenuator, DVGA, or integrated and used with an analog VGA. To simplify the use of this feature, the AD6652 includes two separate gain settings, one when this line is inactive (rCIC2_QUIET[4:0] stored in Bits 9:5 of 0x92 register) and the other when active (rCIC2_LOUD[4:0] stored in Bits 4:0 of 0x92 register). This allows the digital gain to be adjusted to the external changes. In conjunction with the gain setting, a variable hold-off is included to compensate for the pipeline delay of the ADC and the switching time of the gain control element. Together, these two features provide seamless gain switching.

rCIC2_LOUD[4:0] and rCIC2_QUIET[4:0]

These 5-bit registers contain scale values to compensate for the rCIC2 gain and external attenuator gain (if used). If no external attenuator is used, both the rCIC2_QUIET and rCIC2_LOUD registers contain the same value. These 5-bit scale values are stored in the rCIC2 scale register (0x92) and the scaling is applied before the data enters the rCIC2 resampling filter.

Both DDC input ports of the AD6652 have independent gain control circuits, allowing each respective LI pin to be programmed to different set points. Note that the input gain control circuits are wideband and are implemented prior to any filtering elements to minimize loop delays. Any of the four DDC processing channels can be set to monitor either of the DDC input ports.

The chip also provides appropriate scaling of the internal data, based on the attenuation associated with the LI signal. In this manner, data to the DSP maintains a correct scale value throughout the process, making it totally independent. The AD6652 includes a programmable pipeline delay that can be used to compensate for the inherent 7-clock pipeline delay associated with the front-end ADC. This feature promotes smoother switching among gain settings.

NUMERICALLY CONTROLLED OSCILLATOR

FREQUENCY TRANSLATION TO BASEBAND

This processing stage comprises a digital tuner consisting of two multipliers, I and Q, and a 32-bit complex numerically controlled oscillator (NCO). Each channel of the AD6652 has an independent NCO. The NCO serves as a quadrature local oscillator capable of producing an NCO frequency between $_{-CLK}/2$ and $_{+CLK}/2$ with a resolution of $CLK/2^{32}$ in the complex mode. The worst-case spurious signal from the NCO is better than −100 dBc for all output frequencies.

The NCO frequency programmed in Registers 0x85 and 0x86 is interpreted as a 32-bit unsigned integer. Use the following equation to calculate the NCO frequency:

$$NCO_FREQ = 2^{32} \times \left(\frac{f}{CLK} \right)$$

where:

NCO_FREQ is a decimal number equal to the 32-bit binary number to be programmed at 0x85 and 0x86.

f is the desired NCO output frequency in Hz.

CLK is the AD6652 DDC master clock rate (in Hz).

NCO SHADOW REGISTER

A shadow register generally precedes an active register. It holds the next number to be used by the active register whenever that function's hold-off counter causes the active register to be updated with the new value. Active registers are also updated with the contents of a shadow register any time the channel is brought out of sleep mode.

The NCO shadow register is updated during normal programming of the registers through the microport or serial input port. The active frequency register can receive update data only from the NCO shadow register. When software reads back an NCO's frequency, it is reading back the active frequency register and not the shadow register.

NCO FREQUENCY HOLD-OFF REGISTER

When the NCO frequency registers are written, data is actually passed to a shadow register. Data can be moved to the active register by one of two methods: when the channel comes out of sleep mode or when a SYNC hop occurs. As a result of either event, a count-down counter is loaded with an NCO frequency hold-off value. The 16-bit unsigned integer counter (0x84) starts counting down at the DDC CLK rate and, when it reaches one, the new frequency value in the shadow register is written to the active NCO frequency register.

The NCO can be set up to update its frequency immediately upon receipt of a HOP_SYNC or START_SYNC, with no hold-off count, by setting the hold-off count value to 1. Setting the hold-off count to zero prevents any frequency updates.

PHASE OFFSET

The phase offset register (0x87) adds a programmable offset to the phase accumulator of the NCO. This 16-bit register is interpreted as a 16-bit unsigned integer. A 0x0000 in this register corresponds to no offset, and a 0xFFFF corresponds to an offset of 2π radians. This register allows multiple NCOs to be synchronized to produce outputs with constant and known phase differences.

NCO CONTROL REGISTER

Use the NCO control register located at 0x88 to configure the features of the NCO, which are controlled on a per channel basis. These features are described in the following sections.

Bypass

To bypass the NCO of the AD6652, set Bit 0 of 0x88 high. When the NCO is bypassed, down-conversion is not performed, and the AD6652 channel functions simply as a real filter on complex data. This feature is useful for baseband sampling applications, where the A input is connected to the I signal path within the filter and the B input is connected to the Q signal path. Bypassing the NCO might be desired, if the digitized signal has already been converted to baseband in prior analog stages or by other digital preprocessing.

Phase Dither

The AD6652 provides a phase dither option for improving the spurious performance of the NCO. To enable phase dither, set Bit 1 of Register 0x88, which causes discrete spurs due to phase truncation in the NCO to be randomized. The energy from these spurs is spread into the noise floor and spurious free dynamic range is increased at the expense of slight decreases in the SNR. The choice of whether to use phase dither in a system depends ultimately on the system goals. If lower spurs are desired at the expense of a slightly raised noise floor, then phase dither should be employed. If the lowest noise floor is desired and higher spurs can be tolerated or filtered by subsequent stages, then phase dither is not needed.

Amplitude Dither

Amplitude dither can also be used to improve spurious performance of the NCO. To enable amplitude dither, set Bit 2 of 0x88, which causes amplitude quantization errors to be randomized within the angular-to-Cartesian conversion stage of the NCO. This option reduces spurs at the expense of a slightly raised noise floor and slightly reduced SNR. Amplitude dither and phase dither can be used together, separately, or not at all.

Clear Phase Accumulator on Hop

When Bit 3 is logic high, the NCO phase accumulator is cleared (set to all zeros) at the beginning of the next frequency change. This ensures a consistent phase of the NCO on each hop by defeating the phase continuous feature. The NCO phase offset is unaffected by this setting. If phase continuous hopping is desired, this bit should be cleared so that the last phase in the NCO phase register becomes the beginning phase for the new frequency.

Reserved Bits

Bits 4 and 5 are reserved and should be written to Logic 0.

Input Select

Bit 6 of the NCO control register at Address 0x88 controls input port selection. If this bit is set high, then Input Port B is connected to the selected filter channel. If this bit is cleared, then Input Port A is connected to the selected filter channel.

Sync Pin Select

Bits 7 and 8 of the NCO control register determine which external sync pin (if any) is assigned to the channel of interest. The AD6652 has four sync pins: SYNCA, SYNCB, SYNCC, and SYNCD. Any sync pin can be assigned to any or all four receiver channels of the AD6652; however, a channel can have only one sync pin assigned to it. The sync pin(s) must also be enabled in the PIN_SYNC control register at Address 4 of the external memory map. Table 13 shows the bit values used to select a specific external sync pin.

Table 13. Programming Channel Address Register (CAR) Bits to Choose a Sync Pin for a Selected NCO

Address/Bit 0x88:8	Address/Bit 0x88:7	Selected Sync Pin
0	0	SYNCA
0	1	SYNCB
1	0	SYNCC
1	1	SYNCD

SECOND-ORDER rCIC FILTER

The rCIC2 filter is a second-order resampling cascaded integrator comb filter. The resampler is implemented using a unique technique, which does not require the use of a high-speed clock, thus simplifying the design and saving power. The resampler allows for noninteger relationships between the DDC CLK and the output data rate. This allows easier implementation of systems that are either multimode or require a master clock that is not a multiple of the data rate to be used.

Interpolation up to 512 and decimation up to 4096 is allowed in the rCIC2. The resampling factor for the rCIC2 (L) is a 9-bit integer. When combined with the decimation factor M, a 12-bit number, the total rate-change can be any fraction in the form of

$$R_{rCIC2} = \frac{L}{M}$$
$$R_{rCIC2} \leq 1$$

The only constraint is that the ratio *L/M* must be less than or equal to one. This implies that the rCIC2 decimates by 1 or more.

Resampling is implemented by apparently increasing the input sample rate by the factor L, using zero stuffing for the new data samples. Following the resampler is a second-order cascaded integrator comb filter. Filter characteristics are determined only by the fractional rate-change (L/M).

The filter can process signals at the full rate of the input port (65 MHz). The output rate of this stage is given by the following equation:

$$f_{SAMP2} = \frac{L_{rCIC2}\, f_{SAMP}}{M_{rCIC2}}$$

where:

L_{rCIC2} and M_{rCIC2} are unsigned integers.
L_{rCIC2}, the interpolation rate, can be from 1 to 512.
M_{rCIC2}, the decimation, can be between 1 and 4096.

The stage can be bypassed by setting the decimation to 1/1. The frequency response of the rCIC2 filter is given by the following equations:

$$H(z) = \frac{1}{2^{S_{rCIC2}} \times L_{rCIC2}} \times \left(\frac{1 - z\dfrac{M_{rCIC2}}{L_{rCIC2}}}{1 - z^{-1}} \right)^2$$

$$H(f) = \frac{1}{2^{S_{rCIC2}} \times L_{rCIC2}} \times \left(\frac{\sin\left(\pi \dfrac{M_{rCIC2} \times f}{L_{rCIC2} \times f_{SAMP}}\right)}{\sin\left(\pi \dfrac{f}{f_{SAMP}}\right)} \right)^2$$

Use these equations along with the following filter transfer equations to calculate the gain and pass-band droop of the rCIC2. Excessive pass-band droop can be compensated for in the RCF stage by peaking the pass-band by the inverse of the roll-off.

rCIC2 SCALE FACTOR

The scale factor, S_{rCIC2}, is a programmable unsigned 5-bit between 0 and 31, which serves as an attenuator that can reduce the gain of the rCIC2 in 6 dB increments. For the best dynamic range, set S_{rCIC2} to the least attenuation without creating an overflow condition. This can be safely accomplished using the following equation, where *input_level* is the largest fraction of full scale possible at the input to the AD6652 (normally 1). The S_{rCIC2} scale factor is always used whether or not the rCIC2 is bypassed.

The S_{rCIC2} value must be less than 32 or the interpolation and decimation rates must be adjusted to validate this equation. The *ceil* function denotes the next whole integer, and the *floor* function denotes the current whole integer. For example, the *ceil*(4.2) is 5 while the *floor*(4.2) is 4. When S_{rCIC2} has been determined for all channels, it must be programmed at 0x92 [9:5] of each channel address register. The same value should also be programmed at 0x92[4:0] to accommodate a redundant hardware feature.

The gain and pass-band droop of the rCIC2 should be calculated by the previous equations, as well as the rCIC2 filter transfer equations. Excessive pass-band droop can be compensated for in the RCF stage by peaking the pass-band by the inverse of the roll-off.

$$S_{rCIC2} = ceil\left[\log_2 \left(M_{rCIC2} + floor\left(\frac{M_{rCIC2}}{L_{rCIC2}}\right) \times \left(2 \times M_{rCIC2} - L_{rCIC2} \times floor\left(\frac{M_{rCIC2}}{L_{rCIC2}} + 1\right)\right)\right)\right]$$

rCIC2 OUTPUT LEVEL

After the proper scaling factor has been determined, the output level from the rCIC2 stage can be determined using the following equation:

$$OL_{rCIC2} = \frac{\left(M_{rCIC2}{}^{2}\right)}{L_{rCIC2} \times 2^{S_{rCIC2}}} \times input_level$$

where:

input_level is normally full scale (or 1) from the ADC to the rCIC2 stage.
OL_{rCIC2} is the output level from the rCIC2 stage expressed as a fraction of the *input_level*. OL_{rCIC2} is used later in the CIC5 stage-level calculations.

rCIC2 REJECTION

Table 14 illustrates the amount of bandwidth in percentage of the data rate into the rCIC2 stage. The data in this table can be scaled to any other allowable sample rate up to 65 MHz. The table can be used as a tool to decide how to distribute the decimation between rCIC2, CIC5, and the RCF.

Example Calculations:

Goal: Implement a filter with an input sample rate of 10 MHz, requiring 100 dB of alias rejection for a ±7 kHz pass band.

Solution: First determine the percentage of the sample rate that is represented by the pass band, as follows:

$$BW_{fraction} = 100 \times \frac{7\,\text{kHz}}{10\,\text{MHz}} = 0.07$$

Then find the −100 dB column on the right of the table and look down this column for a value greater than or equal to the pass-band percentage of the clock rate. Then look across to the extreme left column and find the corresponding rate change factor (M_{rCIC2}/L_{rCIC2}). Referring to the table, notice that for a M_{rCIC2}/L_{rCIC2} of 4, the frequency having −100 dB of alias rejection is 0.071%, which is slightly greater than the 0.07% calculated. Therefore, for this example, the maximum bound on rCIC2 rate change is 4. A higher chosen M_{rCIC2}/L_{rCIC2} means less alias rejection than the 100 dB required.

An M_{rCIC2}/L_{rCIC2} of less than 4 would still yield the required rejection; however, power consumption can be minimized by decimating as much as possible in this rCIC2 stage. Decimation in rCIC2 lowers the data rate, and, therefore, reduces power consumed in subsequent stages. It should also be noted that there is more than one way to get the decimation by 4. A decimation of 4 is the same as an L/M ratio of 0.25. Thus, any integer combination of L/M that yields 0.25 works (1/4, 2/8, or 4/16). However, for the best dynamic range, use the simplest ratio. For example, 1/4 gives better performance than 4/16.

Table 14. SSB rCIC2 Alias Rejection Table (f_{SAMP} = 1) Bandwidth Shown in Percentage of f_{SAMP}

M_{rCIC2}/L_{rCIC2}	−50 dB	−60 dB	−70 dB	−80 dB	−90 dB	−100 dB
2	1.79	1.007	0.566	0.318	0.179	0.101
3	1.508	0.858	0.486	0.274	0.155	0.087
4	1.217	0.696	0.395	0.223	0.126	0.071
5	1.006	0.577	0.328	0.186	0.105	0.059
6	0.853	0.49	0.279	0.158	0.089	0.05
7	0.739	0.425	0.242	0.137	0.077	0.044
8	0.651	0.374	0.213	0.121	0.068	0.038
9	0.581	0.334	0.19	0.108	0.061	0.034
10	0.525	0.302	0.172	0.097	0.055	0.031
11	0.478	0.275	0.157	0.089	0.05	0.028
12	0.439	0.253	0.144	0.082	0.046	0.026
13	0.406	0.234	0.133	0.075	0.043	0.024
14	0.378	0.217	0.124	0.07	0.04	0.022
15	0.353	0.203	0.116	0.066	0.037	0.021
16	0.331	0.19	0.109	0.061	0.035	0.02

DECIMATION AND INTERPOLATION REGISTERS

rCIC2 decimation values are stored in Register 0x90. This 12-bit register contains the decimation value minus 1. The interpolation portion is stored in Register 0x91. This 9-bit value holds the interpolation value minus one.

rCIC2 SCALE REGISTER

Register 0x92 contains the scaling information for the rCIC2. The primary function is to store the scale value computed in the previous sections.

Bits 4–0 of this register should be written with the same values as those written to Bits 9–5 to accommodate a redundant internal hardware feature.

Bits 9–5 (S_{rCIC2}) contain the 5-bit scaling factor for rCIC2.

Bits 11–10 are reserved and must be written low.

In applications that do not require the features of the rCIC2, bypass it by setting the L/M ratio to 1/1. This effectively bypasses all circuitry of the rCIC2 except the scaling, which is still effectual.

FIFTH-ORDER CIC FILTER

The fourth signal processing stage, CIC5, implements a sharper fixed-coefficient, decimating filter than rCIC2. The input rate to this filter is f_{SAMP2}. The maximum input rate is given by the following equation. N_{CH} equals two for diversity channel real input mode; otherwise, N_{CH} equals one. To satisfy this equation, increase M_{rCIC2} or reduce N_{CH}.

$$f_{SAMP2} \leq \frac{f_{CLK}}{N_{CH}}$$

The decimation ratio, M_{CIC5}, can be programmed from 2 to 32 (all integer values). The frequency response of the filter is given by the following equations. Use these equations to calculate the gain and pass-band droop of CIC5. Both parameters can be compensated for in the RCF stage.

$$H(z) = \frac{1}{2^{S_{CIC5}+5}} \times \left(\frac{1 - z^{-M_{CIC5}}}{1 - z^{-1}} \right)^5$$

$$H(f) = \frac{1}{2^{S_{CIC5}+5}} \times \left(\frac{\sin\left(\pi \frac{M_{CIC5} \times f}{f_{SAMP2}} \right)}{\sin\left(\pi \frac{f}{f_{SAMP2}} \right)} \right)^5$$

The scale factor, S_{CIC5}, is a programmable unsigned integer between 0 and 20. It serves to control the attenuation of the data into the CIC5 stage in 6 dB increments. For the best dynamic range, set S_{CIC5} to the least attenuation without creating an overflow condition. This can be safely accomplished using the following equation, where OL_{rCIC2} is the largest fraction of full scale possible at the input to this filter stage. This value is output from the rCIC2 stage, then pipelined into the CIC5.

$$S_{CIC5} = ceil\left(\log_2\left(M_{CIC5}{}^5 \times OL_{rCIC2}\right)\right) - 5$$

$$OL_{CIC5} = \frac{\left(M_{CIC5}{}^5\right)}{2^{S_{CIC5}+5}} \times OL_{rCIC2}$$

The output rate of this stage is given by the following equation:

$$f_{SAMP5} = \frac{f_{SAMP2}}{M_{CIC5}}$$

CIC5 REJECTION

Table 15 lists the amount of bandwidth in percentage of the input rate that can be protected with various decimation rates and alias rejection specifications. The maximum input rate into the CIC5 is 65 MHz when the rCIC2 decimates by 1. As in the previous rCIC2 table (Table 14), these are the single-sideband bandwidth characteristics of the CIC5.

The CIC5 stage can protect a much wider band to any given rejection than rCIC2.

Given the desired filter characteristics, Table 15 can help in the calculation of an upper bound on decimation, M_{CIC5}.

Table 15. SSB CIC5 Alias Rejection Table (f_{SAMP2} = 1)

M_{CIC5}	−50 dB	−60 dB	−70 dB	−80 dB	−90 dB	−100 dB
2	10.277	8.078	6.393	5.066	4.008	3.183
3	7.924	6.367	5.11	4.107	3.297	2.642
4	6.213	5.022	4.057	3.271	2.636	2.121
5	5.068	4.107	3.326	2.687	2.17	1.748
6	4.267	3.463	2.808	2.27	1.836	1.48
7	3.68	2.989	2.425	1.962	1.588	1.281
8	3.233	2.627	2.133	1.726	1.397	1.128
9	2.881	2.342	1.902	1.54	1.247	1.007
10	2.598	2.113	1.716	1.39	1.125	0.909
11	2.365	1.924	1.563	1.266	1.025	0.828
12	2.17	1.765	1.435	1.162	0.941	0.76
13	2.005	1.631	1.326	1.074	0.87	0.703
14	1.863	1.516	1.232	0.998	0.809	0.653
15	1.74	1.416	1.151	0.932	0.755	0.61
16	1.632	1.328	1.079	0.874	0.708	0.572
17	1.536	1.25	1.016	0.823	0.667	0.539
18	1.451	1.181	0.96	0.778	0.63	0.509
19	1.375	1.119	0.91	0.737	0.597	0.483
20	1.307	1.064	0.865	0.701	0.568	0.459
21	1.245	1.013	0.824	0.667	0.541	0.437
22	1.188	0.967	0.786	0.637	0.516	0.417
23	1.137	0.925	0.752	0.61	0.494	0.399
24	1.09	0.887	0.721	0.584	0.474	0.383
25	1.046	0.852	0.692	0.561	0.455	0.367
26	1.006	0.819	0.666	0.54	0.437	0.353
27	0.969	0.789	0.641	0.52	0.421	0.34
28	0.934	0.761	0.618	0.501	0.406	0.328
29	0.902	0.734	0.597	0.484	0.392	0.317
30	0.872	0.71	0.577	0.468	0.379	0.306
31	0.844	0.687	0.559	0.453	0.367	0.297
32	0.818	0.666	0.541	0.439	0.355	0.287

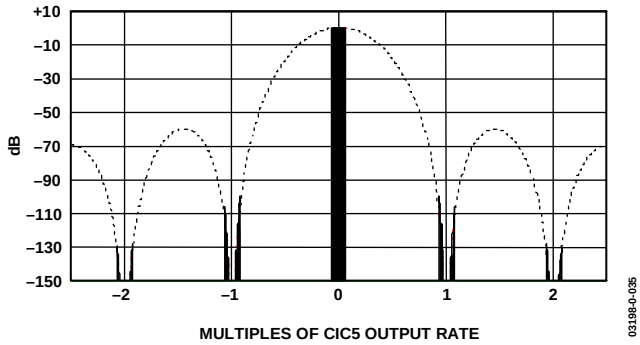


Figure 48. Double Side-Band Graph Showing CIC5 Filter Response and Alias Rejection of –100 dB

RAM COEFFICIENT FILTER

The final signal processing stage is a sum-of-products decimating filter with programmable coefficients. A simplified block diagram is shown in Figure 49. The data memories I-RAM and Q-RAM store the 160 most recent complex samples from the previous filter stage with 20-bit resolution. The coefficient memory, CMEM, stores up to 256 coefficients with 20-bit resolution. On every CLK cycle, one tap for I and one tap for Q are calculated using the same coefficients. The RCF output consists of 24 bits of I data and 24 bits of Q data.

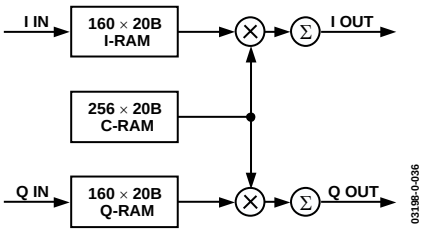


Figure 49. RAM Coefficient Filter Block Diagram

RCF DECIMATION REGISTER

Use each RCF channel to decimate the data rate. The decimation register is an 8-bit register that can decimate from 1 to 256. The RCF decimation is stored in 0xA0 in the form of $M_{RCF} - 1$. The input rate to the RCF is f_{SAMP5}.

RCF DECIMATION PHASE

Use the RCF decimation phase to synchronize multiple filters within a chip. This is useful when using multiple channels within the AD6652 to implement a polyphase filter, requiring that the resources of several filters be paralleled. In such an application, two RCF filters would be processing the same data from the CIC5. However, each filter is delayed by one-half the decimation rate, thus creating a 180° phase difference between the two halves. The AD6652 filter channel uses the value stored in this register to preload the RCF counter. Therefore, instead of starting from 0, the counter is loaded with this value, thus creating an offset in the processing that should be equivalent to the required processing delay. This data is stored in 0xA1 as an 8-bit number.

RCF FILTER LENGTH

The maximum number of taps this filter can calculate, N_{taps}, is given by the following equation. The value $N_{taps} - 1$ is written to the channel register within the AD6652 at address 0xA2.

$$N_{taps} \leq \min\left(\frac{f_{CLK} \times M_{RCF}}{f_{SAMP5}}, 160\right)$$

where *min* indicates that N_{taps} is the lesser of the two values, separated by the comma, that appear within the brackets.

The RCF coefficients are located in addresses 0x00 to 0x7F and are interpreted as 20-bit twos complement numbers. When writing the coefficient RAM, the lower addresses are multiplied by relatively older data from the CIC5, and the higher coefficient addresses are multiplied by relatively newer data from the CIC5. The coefficients need not be symmetric, and the coefficient length, N_{taps}, can be even or odd. If the coefficients are symmetric, then both sides of the impulse response must be written into the coefficient RAM.

Although the base memory for coefficients is only 128 words long, the actual length is 256 words long. There are two pages, each of 128 words long. The page is selected by Bit 8 of 0xA4. Although this data must be written in pages, the internal core handles filters that exceed the length of 128 taps. Therefore, the full length of the data RAM can be used as the filter length (160 taps).

The RCF stores the data from the CIC5 into a 160 × 40 RAM. 160 × 20 is assigned to I data and 160 × 20 is assigned to Q data. The RCF uses the RAM as a circular buffer, so that it is difficult to know in which address a particular data element is stored.

When the RCF calculates a filter output, it starts by multiplying the oldest value in the data RAM by the first coefficient, which is pointed to by the RCF coefficient offset register (0xA3). This value is accumulated with the products of newer data words multiplied by the subsequent locations in the coefficient RAM until the coefficient address $RCF_{OFF} + N_{taps} - 1$ is reached.

Table 16. Three-Tap Filter

Coefficient Address	Impulse Response	Data
0	h(0)	N(0) oldest
1	h(1)	N(1)
2 = (N_{taps} − 1)	h(2)	N(2) newest

The RCF coefficient offset register has two purposes. The main purpose of this register is for rapid filter changes, by allowing multiple filters to be loaded into memory and then selected simply by changing the offset as a pointer. The other use of this register is to form part of symbol timing adjustment. If the desired filter length is padded with zeros on the ends, then the starting point can be adjusted to form slight delays in when the filter is computed with reference to the high speed clock. This allows for vernier adjustment of the symbol timing. Course adjustments can be made with the RCF decimation phase.

The output rate of this filter is determined by the output rate of the CIC5 stage and M_{RCF}, as follows:

$$f_{SAMPR} = \frac{f_{SAMP5}}{M_{RCF}}$$

RCF OUTPUT SCALE FACTOR AND CONTROL REGISTER

Register 0xA4 is a compound register used to configure several aspects of the RCF register. Use Bits 3–0 to set the scale of the fixed-point output mode. This scale value can also be used to set the floating-point outputs in conjunction with Bit 6 of this register.

Bits 4 and 5 determine the output mode. Mode 00 sets the chip up in fixed-point mode. The number of bits is determined by the serial port configuration.

Mode 01 selects floating-point mode 8 + 4. In this mode, an 8-bit mantissa is followed by a 4-bit exponent. In mode 1x (x is don't care), the mode is 12 + 4, or 12-bit mantissa and 4-bit exponent.

Table 17. Output Mode Formats

Format	Value
Floating Point 12 + 4	1x
Floating Point 8 + 4	01
Fixed Point	00

Normally, the AD6652 determines the exponent value that optimizes numerical accuracy. However, if Bit 6 is set, the value stored in Bits 3–0 is used to scale the output. This ensures consistent scaling and accuracy during conditions that might warrant predictable output ranges. If Bits 3–0 are represented by RCF scale, the scaling factor in dB is given by

$$Scaling\ Factor = (RCF\ Scale - 3) \times 20\log_{10}(2)\ \text{dB}$$

For an RCF scale of 0, the scaling factor is equal to −18.06 dB, and for a maximum RCF scale of 15, the scaling factor is equal to +72.25 dB.

If Bit 7 is set, the same exponent is used for both the real and imaginary (I and Q) outputs. The exponent used is the one that prevents numeric overflow at the expense of small signal accuracy. However, this is seldom a problem, because small numbers would represent 0 regardless of the exponent used.

Bit 8 is the RCF bank select bit used to program the register. When this bit is 0, the lowest block of 128 is selected (taps 0 to 127). When high, the highest block is selected (taps 128 to 255). It should be noted that while the chip is computing filters, Tap 127 is adjacent to Tap 128 and there are no paging issues.

Bit 9 selects where the input to each RCF originates. If Bit 9 is clear, then the RCF input comes from the CIC5 normally associated with the RCF. However, if the bit is set, then the input comes from CIC5 Channel 1. The only exception is Channel 1, which uses the output of CIC5 Channel 0 as its alternate. Using this feature, each RCF can either operate on its own channel data or be paired with the RCF of Channel 1. The RCF of Channel 1 can also be paired with Channel 0. This control bit is used with polyphase distributed filtering.

If Bit 10 is clear, the AD6652 channel operates in normal mode. However, if Bit 10 is set, then the RCF is bypassed to Channel BIST. See the User-Configurable Built-In Self-Test (BIST) section for more details.

INTERPOLATING HALF-BAND FILTERS

The AD6652 has two interpolating half-band FIR filters that immediately precede the two digital AGCs and follow the four RCF channel outputs. Each interpolating half-band takes 16-bit I and 16-bit Q data from the preceding RCF and outputs 16-bit I and 16-bit Q to the AGC. The half-band and AGC operate independently of each other, so the AGC can be bypassed, in which case the output of the half-band is sent directly to the output data port. The half-band filters also operate independently of each other—either one can be enabled or disabled. The control register for Half-Band A is at Address 0x08 and for Half-Band B is at Address 0x09.

Half-band filters also perform the function of interleaving data from various RCF channel outputs prior to the actual function of interpolation. Interleaving of data is allowed even when the half-band filter is bypassed. This allows the implementation of a polyphase filter by combining the processing power of multiple channels to act upon a single carrier. This is accomplished by appropriate phasing of the processing channels using one of the following methods:

- RCF phase decimation
- Start hold-off counter

For example, if two channels of the AD6652 are used to process one CDMA2000 carrier, RCF filters for both the channels should be 180° out of phase. This can be done using RCF phase decimation or an appropriate start hold-off counter followed by appropriate NCO phase offsets.

Half-band A can listen to all four channels: Channels 0, 1, 2, and 3; Channel 0 and 1; or only Channel 0. Half-band B can listen to Channels 2 and 3, or only Channel 2. Each half-band interleaves the channels specified in its control register and interpolates by two on the combined data from those channels. For one channel running at twice the chip rate, the half-band can be used to output channel data at four times the chip rate. The frequency response of the interpolating half-band FIR is shown in Figure 50.

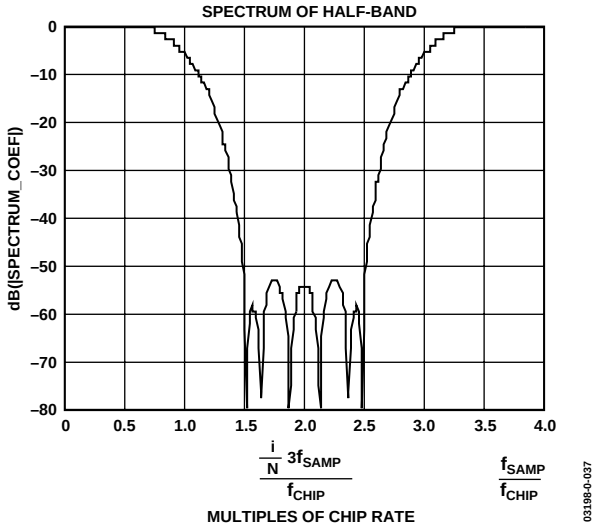


Figure 50. Interpolating Half-Band Frequency Response

The SNR of the interpolating half-band is around −149.6 dB. The highest error spurs due to fixed-point arithmetic are around −172.9 dB. The coefficients of the 13-tap interpolating half-band FIR are given in Table 18.

Table 18. Half-Band Coefficients

0	14	0	−66	0	309	512	309	0	−66	0	14	0

AUTOMATIC GAIN CONTROL

The AD6652 is equipped with two independent automatic gain control (AGC) loops for direct interface with a Rake receiver. Each AGC circuit has 96 dB of range. It is important that the decimating filters of the AD6652 preceding the AGC reject undesired signals, so that each AGC loop is operating on only the carrier of interest and carriers at other frequencies do not affect the ranging of the loop.

The AGC compresses the 23-bit complex output from the interpolating half-band filter into a programmable word size of 4 to 8, 10, 12, or 16 bits. Because the small signals from the lower bits are pushed into higher bits by adding gain, the clipping of the lower bits does not compromise the SNR of the signal of interest. The AGC strives to maintain a constant mean output power despite input signal fluctuations. This permits operation in environments where the dynamic range of the signal exceeds the dynamic range of the output resolution.

The AGCs and the interpolation filters need not be linked together. Either can be selected without the other. The AGC section can be bypassed, if desired, by setting Bit 0 of the AGC control word. When bypassed, the I/Q data is still clipped to a desired number of bits, and a constant gain can be provided through the AGC gain multiplier.

Three sources of error can be introduced by the AGC function: underflow, overflow, and modulation. Underflow is caused by truncation of bits below the output range. Overflow is caused by clipping errors when the output signal exceeds the output range. Modulation error occurs when the output gain varies during the reception of data.

Set the desired signal level based on the probability-density function of the signal, so that the errors due to underflow and overflow are balanced. Set the gain and damping values of the loop filter so that the AGC is fast enough to track long-term amplitude variations of the signal that might cause excessive underflow or overflow, but slow enough to avoid excessive loss of amplitude information due to the modulation of the signal.

AGC LOOP

The AGC loop is implemented using a log-linear architecture. It performs four basic operations: power calculation, error calculation, loop filtering, and gain multiplication. The AGC can be configured to operate in one of the following modes:

- Desired signal level mode
- Desired clipping level mode as set by Bit 4 of AGC control word (0x0A, 0x12)

The AGC adjusts the gain of the incoming data according to how far its level is from the desired signal level or desired clipping level, depending on the mode of operation selected.

Two datapaths to the AGC loop are provided: one before the clipping circuitry and one after the clipping circuitry, as shown in Figure 51. For desired signal level mode, only the I/Q path before the clipping is used. For desired clipping level mode, the difference of the I/Q signals before and after the clipping circuitry is used.

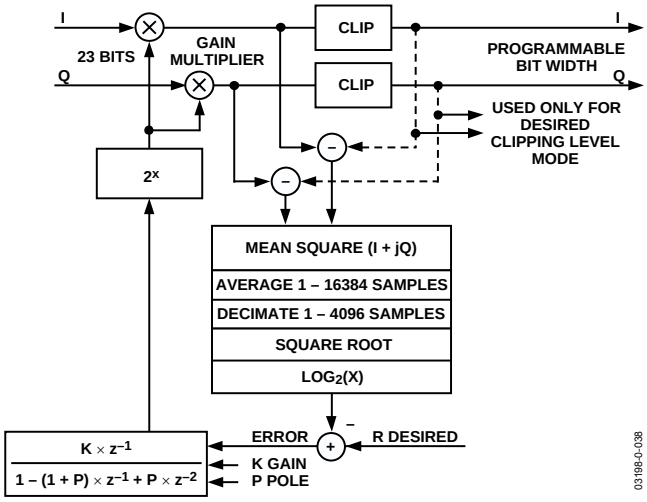


Figure 51. Block Diagram of the AGC

DESIRED SIGNAL LEVEL MODE

In this mode of operation, the AGC strives to maintain the output signal at a programmable set level. This mode of operation is selected by writing AGC control word (0x0A:4, and 0x12:4) to Logic 0. First, the loop finds the square (or power) of the incoming complex data signal by squaring I and Q and adding them. This operation is implemented in exponential domain using 2^x.

The AGC loop has average and decimate blocks that operate on power samples before the square root operation, as shown in Figure 51. The average block can be programmed to average 1 to 16,384 power samples, and the decimate block can be programmed to update the AGC once every 1 to 4096 samples. The limitations on the averaging operation are that the number of averaged power samples must be an integer multiple of the decimation value, and the only allowable multiple values are 1, 2, 3, or 4.

The averaging and decimation effectively mean that the AGC can operate over averaged power of 1 to 16,384 output samples. The choice of updating the AGC once every 1 to 4096 samples and operating on average power facilitates the implementation of a loop filter with slow time constants, where the AGC error converges slowly and makes infrequent gain adjustments. It would also be useful where the user wants to keep the gain scaling constant over a frame of data (or a stream of symbols).

Because the number of average samples must be an integer multiple of the decimation value, only the multiple number 1, 2, 3, or 4 is programmed. This number is programmed in Output Port Control Registers 0x10:1–0 and 0x18:1–0. These averaged samples are then decimated with decimation ratios programmable from 1 to 4096. This 12-bit decimation ratio is defined in Registers 0x11 and 0x19.

The average and decimate operations are linked together and implemented using a first-order CIC filter and FIFO registers. The gain and bit growth associated with CIC filters depends on the decimation ratio. To compensate for the gain associated with these operations, attenuation scaling is provided before the CIC filter.

This scaling operation accounts for the division associated with the averaging operation as well as the traditional bit growth in CIC filters. Because this scaling is implemented as a bit shift operation, only coarse scaling is possible. Fine scaling is implemented as an offset in the request level, explained later in this section. The attenuation scaling, S_{CIC}, is programmable from 0 to 14 using four bits of 0x10 and 0x18 of the output port control registers, and is given by

$$S_{CIC} = ceil[\log_2 (M_{CIC} \times N_{avg})]$$

where:

M_{CIC} is the decimation ratio (1 to 4096).
N_{avg} is the number of averaged samples programmed as a multiple of decimation ratio (1, 2, 3, or 4).
Ceil is MathCad-speak for rounding up to the next whole number.

For example, if a decimation ratio M_{CIC} is 1000 and N_{avg} is selected to be 3 (decimation of 1000 and averaging of 3000 samples), then the actual gain due to averaging and decimation is 3000 or 69.54 dB (= $\log_2(3000)$). Because attenuation is implemented as a bit shift operation, only multiples of 6.02 dB attenuations are possible. S_{CIC}, in this case, is 12 corresponding to 72.24 dB. This way, S_{CIC} scaling always attenuates more than is sufficient to compensate for the gain changes in average and decimate sections and, therefore, prevents overflows in the AGC loop. But it is also evident that the CIC scaling is inducing a gain error (difference between gain due to CIC and attenuation provided) of up to 6.02 dB. This error should be compensated for in the request signal level, as explained below.

Logarithm to the Base 2 is applied to the output from the average and decimate section. These decimated power samples (in logarithmic domain) are converted to rms signal samples by applying a square root. This square root is implemented using a simple shift operation. The rms samples so obtained are subtracted from the request signal level, *R*, specified in Registers (0x0B, 0x14), leaving an error term to be processed by the loop filter, *G(z)*.

Set this programmable request signal level, *R*, according to the output signal level desired. The request signal level *R* is programmable from 0 to −23.99 dB in steps of 0.094 dB. The request signal level should also compensate for error, if any, due to the CIC scaling, as explained previously. Therefore, the request signal level is offset by the amount of error induced in CIC, given by

$$Offset = 20 \times \log_{10}(M_{CIC} \times N_{avg}) - S_{CIC} \times 6.02$$

where the offset is in dB.

Continuing with the previous example, this offset is given by

$$Offset = 72.24 - 69.54 = 2.7 \text{ dB}$$

So the request signal level is given by

$$R = ceil\left[\frac{(DSL - Offset)}{0.094}\right] \times 0.094$$

where:

R is the request signal level.
DSL (desired signal level) is the output signal level that the user desires.

Therefore, in the previous example, if the desired signal level is −13.8 dB, the request signal level, *R*, is programmed to be −16.54 dB.

The AGC provides a programmable second-order loop filter. The programmable parameters, gain *K* and pole *P*, completely define the loop filter characteristics. The error term after subtracting the request signal level is processed by the loop filter, *G(z)*. The open loop poles of the second-order loop filter are 1 and *P*, respectively. The loop filter parameters, pole P and gain *K*, allow adjustment of the filter time constant, which determines the window for calculating the peak-to-average ratio.

The open loop transfer function for the filter, including the gain parameter is as follows:

$$G(z) = \frac{Kz^{-1}}{1-(1+P)z^{-1}+Pz^{-2}}$$

If the AGC is properly configured (in terms of offset in request level), then there are no gains except the filter gain K. Under these circumstances, a closed loop expression for the AGC loop is possible and is given by

$$G_{closed}(z) = \frac{G(z)}{1+G(z)} = \frac{Kz^{-1}}{1+(K-1-P)z^{-1}+Pz^{-2}}$$

The gain parameter *K* and pole *P* are programmable through registers (0x0E and 0x0F, respectively, for AGC Channel A and Channel B) from 0 to 0.996 in steps of 0.0039 using 8-bit

representation. Though the user defines the open loop pole P and gain K, they directly impact the placement of the closed loop poles and filter characteristics. These closed loop poles P_1, P_2 are the roots of the denominator of the above closed loop transfer function and are given by

$$P_1, P_2 = \frac{(1+P-K)+\sqrt{(1+P-K)^2-4P}}{2}$$

Typically the AGC loop performance is defined in terms of its time constant or settling time. In such a case, set the closed loop poles to meet the time constants required by the AGC loop. The following relation between time constant and closed loop poles can be used for this purpose:

$$P_{1,2} = \exp\left[\frac{M_{CIC}}{sample\,rate \times \tau_{1,2}}\right]$$

where:

$\tau_{1,2}$ are the time constants corresponding to the poles $P_{1,2}$.
exp denotes the inverse of the natural log.

The time constants can also be derived from settling times as follows:

$$\tau = \frac{2\%\,settling\,time}{4}\ or\ \frac{5\%\,settling\,time}{3}$$

where:

M_{CIC} (CIC decimation) is from 1 to 4096.
settling time or *time constant* is chosen by the user.
sample rate is the combined sample rate of all the interleaved channels coming into the AGC/half-band interpolated filters.

If two channels are being used to process one carrier of UMTS at 2× chip rate, then each channel works at 3.84 MHz and the combined sample rate coming into the half-band interpolated filters is 7.68 MSPS. Use this rate in the calculation of poles in the previous equation, if half-band interpolating filters are bypassed.

The loop filter output corresponds to the signal gain that is updated by the AGC. Because all computation of the samples in the loop filter is done in logarithmic domain (to the base 2), the signal gain is generated using the exponent (power of 2) of the loop filter output.

The gain multiplier gives the product of the signal gain with both the I and Q data entering the AGC section. This signal gain is applied as a coarse 4-bit scaling and then a fine scale 8-bit multiplier. Therefore, the applied signal gain is between 0 dB and 96.296 dB in steps of 0.024 dB. Initial value for signal gain is programmable using Register 0x0D for AGC A and Register 0x15 for AGC B.

The products of the gain multiplier are the AGC scaled outputs, which have 19-bit representation. These are in turn used as I and Q for calculating the power and AGC error and loop filtered to produce signal gain for the next set of samples. These AGC scaled outputs can be programmed to have 4-, 5-, 6-, 7-, 8-, 10-, 12-, or 16-bit widths using the AGC control word (0x0A, 0x12). The AGC scaled outputs are truncated to the required bit widths using the clipping circuitry shown in Figure 51.

Open Loop Gain Setting

If filter gain K occupies only one LSB or 0.0039, then, during the multiplication with error term, errors of up to 6.02 dB could be truncated. This truncation is due to the lower bit widths available in the AGC loop. If filter gain K is the maximum value, truncated errors are less than 0.094 dB (equivalent to 1 LSB of error term representation). Generally, a small filter gain is used to achieve a large time constant loop (or slow loops), but, in this case, it would cause large errors to go undetected. Due to this peculiarity, the designers recommend that, if a user wants slow AGC loops, they should use fairly high values for filter gain K and then use CIC decimation to achieve a slow loop. In this way, the AGC loop makes large infrequent gain changes compared to small frequent gain changes, as in the case of a normal small-gain loop filter. However, though the AGC loop makes large infrequent gain changes, a slow time constant is still achieved and there is less truncation of errors.

Average Samples Setting

Though it is complicated to express the exact effect of the number of averaging samples, thinking intuitively, it has a smoothing effect on the way the AGC loop attacks a sudden increase or a spike in the signal level. If averaging of four samples is used, the AGC attacks a sudden increase in signal level more slowly compared to no averaging. The same applies to the manner in which the AGC attacks a sudden decrease in the signal level.

Desired Clipping Level Mode

As noted previously, each AGC can be configured so that the loop locks onto a desired clipping level or a desired signal level. Select desired clipping level mode by setting Bit 4 of the individual AGC control words (0x0A, 0x12). For signals that tend to exceed the bounds of the peak-to-average ratio, the desired clipping level option provides a way to keep from truncating those signals and still provide an AGC that attacks quickly and settles to the desired output level. The signal path for this mode of operation is shown with broken arrows in Figure 51, and the operation is similar to the desired signal level mode.

First, the data from the gain multiplier is truncated to a lower resolution (4, 5, 6, 7, 8, 10, 12, or 16 bits) as set by the AGC control word. An error term (both I and Q) is generated that is the difference between the signals before and after truncation. This term is passed to the complex squared magnitude block,

for averaging and decimating the update samples and taking their square root to find rms samples, as in desired signal level mode. In place of the request desired signal level, a desired clipping level is subtracted, leaving an error term to be processed by the second-order loop filter. The rest of the loop operates the same way as the desired signal level mode. This way, the truncation error is calculated and the AGC loop operates to maintain a constant truncation error level.

Apart from Bit 4 of the AGC control words, the only register setting changes compared to the desired signal level mode is that the desired clipping level is stored in the AGC desired level registers (0x0C, 0x15) instead of the request signal level (as in desired signal level mode).

SYNCHRONIZATION

In instances where the AGC output is connected to a Rake receiver, a signal from the Rake receiver can synchronize the average-and-update section of the AD6652 to update the average power for AGC error calculation and loop filtering. This external signal synchronizes the AGC changes to the Rake receiver and makes sure that the AGC gain word does not change over a symbol period and, therefore, more accurate estimation. The external synchronization signal is connected to one or more of the pin sync pins (A, B, C, or D).

Pin synchronization requires the use of an AGC hold-off counter. The hold-off counter of AGC A shares the pin sync that the user has assigned to DDC processing Channel 0. Therefore, the user must attach the external sync signal to the pin sync chosen for DDC Channel 0. Likewise, the hold-off counter of AGC B shares the pin synch that the user has assigned to DDC processing Channel 2. Therefore, the user must attach the external sync signal to the pin sync that will be assigned to DDC Channel 2.

The hold-off counter register, 0x0B and 0x13 for AGC A and AGC B, respectively, must be programmed with a 16-bit number that corresponds to the number of CLK cycles that will be counted (a known delay) before a new CIC decimated value is updated. Writing a logic high to the proper pin sync pin triggers the AGC hold-off counter with a one-shot pulse every time the pin is written high. Once triggered, the counter counts down to a value of one and then causes a start of decimation for a new update sample.

Note: Setting the hold-off count to zero disables the hold-off counter. Setting the hold-off count to one provides the smallest delay.

If the user chooses not to use pin sync signals, the user can use the *Sync Now* command through the microport. Each AGC control register has a sync now bit in Registers 0x0A:3 and 0x12:3 that, when written high, performs an immediate start of decimation for a new update sample. This bit has a one-shot characteristic and does not need to be reset in order to respond to a new logic high being written to it. Use of the sync now bit bypasses the AGC hold-off counters and performs sync functions without delay.

Each *Pin Sync logic high* initiates a new trigger event for the hold-off counter unless *First Sync Only* of the AGC's control register (Bit 1) is set to logic high. When high, only the first sync signal is recognized and any others disregarded until *First Sync Only* is reset.

Along with updating a new decimation value, the CIC filter accumulator can be reset if the *Init on Sync* bit (Bit 2) of the AGC control register is set. *Init on Sync* is triggered by either sync signal, pin sync, or sync now.

Addresses 0x0A to 0x11 have been reserved for configuring AGC A, and Addresses 0x12 to 0x19 have been reserved for configuring AGC B. The register specifications are detailed in Table 29.

USER-CONFIGURABLE BUILT-IN SELF-TEST (BIST)

The AD6652 includes two built-in test features to test the integrity of each channel. The first is a RAM BIST (built-in self-test), which is intended to test the integrity of the high speed random access memory within the AD6652. The second is channel BIST, which is designed to test the integrity of the main signal paths of the AD6652. The BIST functions are independent of each other and can be operated simultaneously.

RAM BIST

Use the RAM BIST to validate functionality of the on-chip RAM. This feature provides a simple pass/fail test, which gives confidence that the channel RAM is operational. Follow these steps to perform this test:

1. Put the channels to be tested into sleep mode via the External Address Register 0x01.
2. Program the RAM BIST enable bit in the RCF Register 0xA8 of the channel address registers to logic high. Wait at least 1600 clock cycles, then perform Step 3.
3. Read back Register 0xA8 (see Table 19). If Bit 0 is high, the test is not yet complete. If Bit 0 is low, the test is complete and Bits 1 and 2 indicate the condition of the internal RAM. If Bit 1 is high, then CMEM is bad. If Bit 2 is high, then DMEM is bad.

Table 19. BIST Register 0xA8

3-Bit Data	Coefficient MEM	Data MEM
xx1	Test incomplete	Test incomplete
000	PASS	PASS
010	FAIL	PASS
100	PASS	FAIL
110	FAIL	FAIL

CHANNEL BIST

The channel BIST is a thorough test of the selected AD6652 signal path. With this test mode enabled, it is possible to use externally supplied test vectors or an internal pseudonoise (PN) data generator. An error signature register in the RCF monitors the output data of the channel and is used to determine if the proper data exits the RCF. If errors are detected, then each internal block can be bypassed and another test can be run to debug the fault. The I and Q paths are tested independently. Follow these steps to perform this test:

1. Place the channel(s) to be programmed in sleep mode at External Address 3:3–0. Set the appropriate bits high. Example 3:0 = 1 places Channel 0 in sleep mode.
2. Configure the channels to be tested as required for the application. This might require setting the NCO parameters, the decimation rates, scalars, and RCF coefficients.
3. Program the start hold-off counter, 0x83, to a value of 1 in the channel address registers of the channels to be tested.
4. Program Channel Address Registers 0xA5 and 0xA6 to all 0s for the channels to be tested.
5. Enable the channel BIST located at 0xA7 by programming Bits 19–0 to the number of RCF outputs to observe.
6. For External Address Register 5:3–0, program the desired SYNC CH bits to logic high to select which channels will receive a start soft-sync signal.
7. External Address Register 5:4 should be programmed high to emit a one-shot soft sync pulse for the start function.
8. Reset External Address Register 5:6 to 0 to allow user-provided test vectors. The internal pseudorandom number generator can also be selected to generate a PN data input sequence by setting Bit 7 high.
9. For External Address Register 5, an internal negative full-scale sine wave is output at the NCO frequency, when Bit 6 is set to 1 and Bit 7 is cleared.
10. When the SOFT_SYNC control register is written with the above parameters, the selected channels become active with the programmed attributes.
11. If the user is providing external vectors, then the chip can be brought out of sleep mode by one of the other methods.
12. After a sufficient amount of time, the channel BIST Signature Registers 0xA5 and 0xA6 contain a numeric value that can be compared to the expected value for a known good AD6652 with the exact same configuration. If the values are the same, then there is a very low probability of an error in the channel.

Note: To better visualize these instructions, see Figure 53, Sync Control Block Diagram; Table 22, the External Memory Map; and Table 24, the Channel Address Registers Memory Map.

CHANNEL/CHIP SYNCHRONIZATION

The AD6652 has been designed to easily synchronize two common functions: *Start* and *Hop*. While the AGC stage can also be synchronized, it is not accommodated using the versatile soft-sync and pin-sync signals normally associated with AD6652 synchronization. *Start* and *Hop* functions are described in detail in the following sections. The synchronization is accomplished with the use of a shadow register and a hold-off counter. See Figure 52 for a simplified schematic of the NCO shadow register and NCO frequency hold-off counter to understand basic operation. Triggering of the hold-off counter can occur with either a Soft_Sync (via the microport), or a Pin_Sync (via any of the four AD6652 SYNC pins A, B, C, and D). Figure 53 details how synchronization signals are managed for a single receive processing channel.

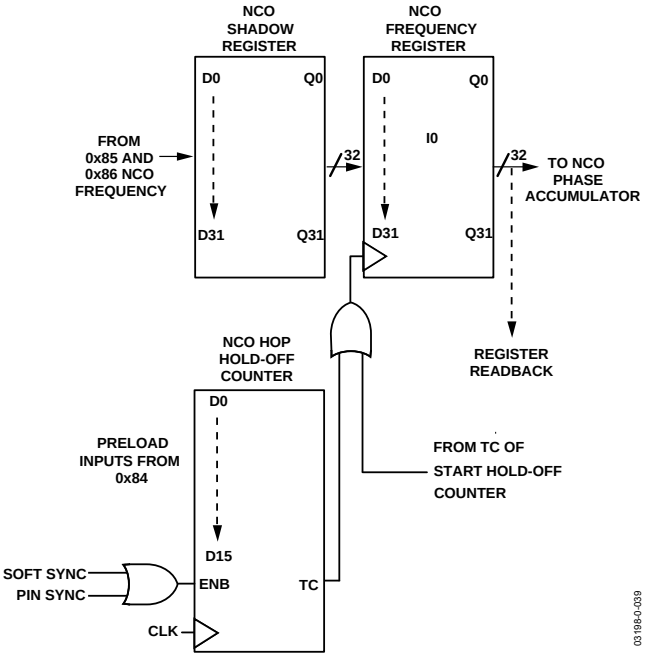


Figure 52. NCO Shadow Register and Hold-Off Counter

There are two types of synchronization stimuli to choose from: *Soft_Sync* and *Pin_Sync*. The first method is initiated over the microport or serial programming port using a software routine. The second method relies on an external stimulus that is attached to one of the four synchronization input pins (SYNC A, B, C, and D). In both cases, a logic high triggers the synchronization process. Both methods can be used simultaneously by setting the appropriate qualifiers.

START

Start refers to the startup of an individual channel or chip, or multiple chips. If a channel is not used, it should be placed in sleep mode to reduce power dissipation. Following a hard reset (low pulse on the AD6652 $\overline{\text{RESET}}$ pin), all channels are placed in sleep mode. Channels can also be manually placed in sleep mode by writing to the register controlling the sleep function, External Address 3:3–0.

Before and after a start command is received by one or more channels, the following occurs:

1. Just before the start command is issued, *while the channel is in sleep mode,* any or all control registers, including filter coefficients, can be safely reprogrammed without crashing the AD6652 or creating unwanted output.

2. When a *Start_Sync* pulse is received, it transfers the contents of the channel's start hold-off register, 0x83, to the counter's preload inputs and commences counting. When the count reaches a value of one, *the channel is awakened* and initialized with the information from each applicable register for a proper channel startup. However, if the start preload value is 0, this defeats the start function, and the channel remains dormant.

Note that start does *not* affect the AGC hold-off counter. The counter can be triggered only by setting the sync now bit or by pin sync signals (see the Automatic Gain Control section).

What happens if a *Start_Sync* pulse is received while the channel is awake (actively processing data)? This can actually be a very useful tool to dynamically adjust the RCF phase or timing to allow synchronization of multiple AD6652 ICs. Refer to the discussions of Registers 0x83 and 0xA1 in the Channel Address Register (CAR) section for further explanation.

Start with No Sync

If no synchronization is needed to start multiple channels or multiple AD6652s, use the following method to initialize the device:

1. To program a channel, put it in sleep mode (bit high, External Address 3:3–0), then load all appropriate control and memory registers to set up the proper channel configuration.

2. Load the start hold-off counter (0x83) with a 16-bit value from 1 to $2^{16} - 1$.

3. Set the channel's sleep bit low (External Address 3:3–0). Awakening from sleep involves an internally generated start command that performs the same functions as a software-generated sync pulse. This activates the channel after the hold-off counter reaches a value of one with the newly programmed or previous parameters.

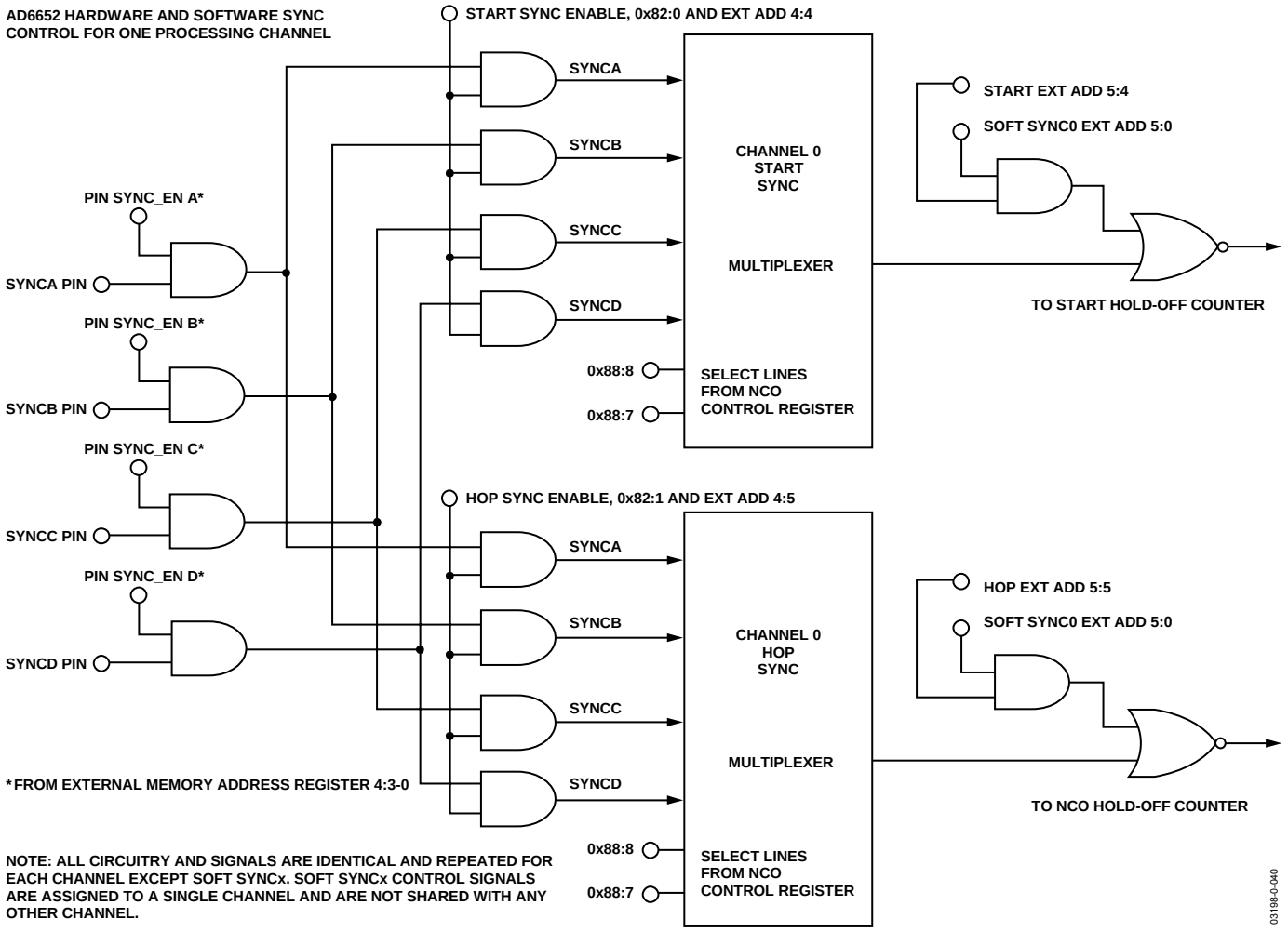


Figure 53. Synchronizing Signal Routing Example, Channel 0 ; Note that Multiple Qualifiers Are Required to Enable either a Pin_Sync or a Soft_Sync Signal to Be Routed to a Hop or Start Hold-Off Counter

Start with Soft Sync

The AD6652 includes the ability to synchronize channels or chips using the microport. One action to synchronize is the start of channels or chips. The start update hold-off counter (0x83) in conjunction with the start bit and sync bit (External Address 5) allows this synchronization. The start update hold-off counter delays the start of a channel by the 16-bit value programmed at 0x83 (number of AD6652 CLK periods). Use the following method to synchronize the start of multiple channels via microprocessor control:

1. Place the channels in sleep mode (a hard reset to the AD6652 $\overline{\text{RESET}}$ pin forces all four DDC processing channels into sleep mode).
2. Write the start hold-off counter(s) (0x83) to a value from 1 to $2^{16} - 1$. If the chip or channels have not been completely programmed, write all other registers now.
3. Write the start bit and the applicable channel sync bit(s) high at External Address 5. This triggers the start hold-off counters to begin their count. The counters are clocked with the AD6652 CLK signal. When it reaches a count of one, the sleep bits of the selected channels are set low to turn on the channel with the new or existing operating parameters.

Note: Each channel has a redundant soft-sync control register at Address 0x81. This register mimics the programming as set in the External Memory Address 5:5–4. The user can control the soft-sync function of a DDC channel by writing to the 0x81 register, if it is advantageous to do so in the application.

The time from when the $\overline{\text{DTACK}}$ pin goes high (which acknowledges the receipt of the soft sync command data) to when the DDC channel begins processing data is equal to the time period set up by the start hold-off counter value at 0x83 plus six CLK cycles.

Start with Pin Sync

The AD6652 provides four SYNC pins. A, B, C, and D, which are used for very accurate channel synchronization. Each DDC channel can be programmed to respond to any or all four sync pins. Synchronization of start with one of the external sync pins is accomplished with the following method. Refer to Figure 53 to assist in following this process.

1. Place the channels to be programmed in sleep mode. The AD6652 $\overline{\text{RESET}}$ pin places all four DDC processing channels in sleep mode when toggled low momentarily.
2. Write the start hold-off counter(s) (0x83) to a value from 1 to $2^{16} - 1$. If the chip or channels have not been completely programmed, write all other registers now.
3. Set the Start_En bit high (External Address 4:4) and choose which Pin Sync_En bits (External Address 4:3–0) are to be used. Write the bit high to enable it.
4. Set the sync input select bits *for each active channel*. This is done at Address 0x88:8–7. Table 20 is the truth table for these bits.

Table 20. Truth Table

0x88:8	0x88:7	Sync Pin Selected
0	0	A
0	1	B
1	0	C
1	1	D

After programming is complete and when the external signal attached to the selected sync pin goes high, this triggers the start hold-off counter of the chosen channel(s). The hold-off counter begins counting using the AD6652 CLK signal. When it reaches a count of 1, the sleep bit of the selected channel(s) is set low to awaken the channel(s). Each *Pin Sync logic high* initiates a new trigger event for the hold-off counter unless *First Sync Only*, External Address 4:6 is set to logic high. When high, only the first sync signal is recognized and any others are disregarded until *First Sync Only* is reset.

Note: Each channel has a redundant pin-sync control register at Address 0x82. This register mimics the programming as set in External Memory Address 4:6–4. The user can control the pin sync function of a DDC channel by writing to Registers 0x82 and 0x88:8–7, if it is advantageous to do so in the application.

The time from when the pin sync goes high to when the DDC channel resumes processing is equal to the time period set up by the start hold-off counter value at 0x83 plus 3 CLK cycles.

HOP

Hop is a change from one NCO frequency to a new NCO frequency. This can apply to a single channel or multiple channels and can be synchronized via microprocessor control (soft sync) or an external sync signal (pin sync), as described in the following sections. Awakening the channel from sleep mode generates an internal start command that performs both hop and start functions as if a soft-sync or pin-sync had been received.

Hop with Soft Sync

The AD6652 includes the ability to synchronize a change in NCO frequency of multiple channels or chips using the microport. The NCO frequency hold-off counter (0x84) in conjunction with the hop bit and the sync bit (External Address 4) allows this synchronization. Basically, the NCO frequency hold-off counter delays the new frequency from being loaded into the NCO by its value (number of AD6652 CLKs). Use the following method to synchronize a hop in frequency of multiple channels via microprocessor control:

1. Write the NCO frequency hold-off counter (0x84) to the appropriate value (greater than 0 and less then 2^{16}).
2. Write the NCO Frequency Register(s), 0x85 and 0x86, to the new desired frequency.
3. Write the hop bit and the applicable channel sync bit(s) high at External Address 5.

This triggers the frequency hold-off counter(s) to begin their count. The counters are clocked with the AD6652 CLK signal. When it reaches a count of 1, the new frequency data is transferred from the shadow register to the working register of the NCO. Unlike the start function, the channels do not need to be placed in sleep mode to achieve a frequency hop.

Note: Each channel has a redundant soft-sync control register at Address 0x81. This register mimics the programming as set in the External Memory Address 5:5–4. The user can control the soft-sync function of a DDC channel by writing to the 0x81 register, if it is advantageous to do so in the application.

The time from when the $\overline{\text{DTACK}}$ pin goes high (which acknowledges the receipt of the soft sync command data) to when the DDC channel begins processing data is equal to the time period set up by the frequency or hop hold-off counter value at 0x84 plus 7 CLK cycles.

Hop with Pin Sync

Just as in the start function, the AD6652 provides four SYNC pins, A, B, C, and D, which are used for very accurate channel synchronization. Each DDC channel can be programmed to respond to any or all four SYNC pins.

Synchronization of hop with one of the external SYNC pins is described as follows:

1. Write the NCO frequency hold-off counter(s) (0x84) to the appropriate value (greater than 0 and less than 2^{16}).
2. Write the NCO Frequency Register(s), 0x85 and 0x86, to the new desired frequency.
3. Set the hop on pin sync bit high and the appropriate sync pin enable high at External Address 4.
4. Set the sync input select bits *for each active channel*. This is done at Address 0x88:8–7. The truth table for these bits is the same as for the start with pin sync, in Table 20.

When the selected sync pin is sampled high by the AD6652 CLK, this enables the count-down of the NCO frequency hold-off counter. The counter is clocked with the AD6652 CLK signal. When it reaches a count of 1, the new frequency is loaded into the NCO. Each *Pin Sync logic high* initiates a new trigger event for the hold-off counter unless *First Sync Only,* External Address 4:6 is set to logic high. When high, only the first sync signal is recognized and any others are disregarded until *First Sync Only* is reset. Unlike the start function, the channels do not need to be placed in sleep mode to achieve a frequency hop.

Note: Each channel has a redundant pin-sync control register at Address 0x82. This register mimics the programming as set in External Memory Address 4:6–4. The user can control the pin sync function of a DDC channel by writing to the 0x82 and 0x88:8–7 registers, if it is advantageous to do so in the application.

The time from when the external signal on the SYNC input pin goes high to when the NCO begins processing data is equal to the time period set up by the NCO frequency hold-off counter (0x84) plus five master clock cycles.

PARALLEL OUTPUT PORTS

The AD6652 incorporates two independent 16-bit parallel ports for output data transfer. To minimize package ball count, the eight LSBs of each 16-bit port are shared with their respective DSP link port data bits (see Figure 54). This means that an output port can transmit 16-bit parallel data or 8-bit link port data, but not both. Transmitting both link and parallel data simultaneously requires that the second AD6652 output port be configured for that purpose.

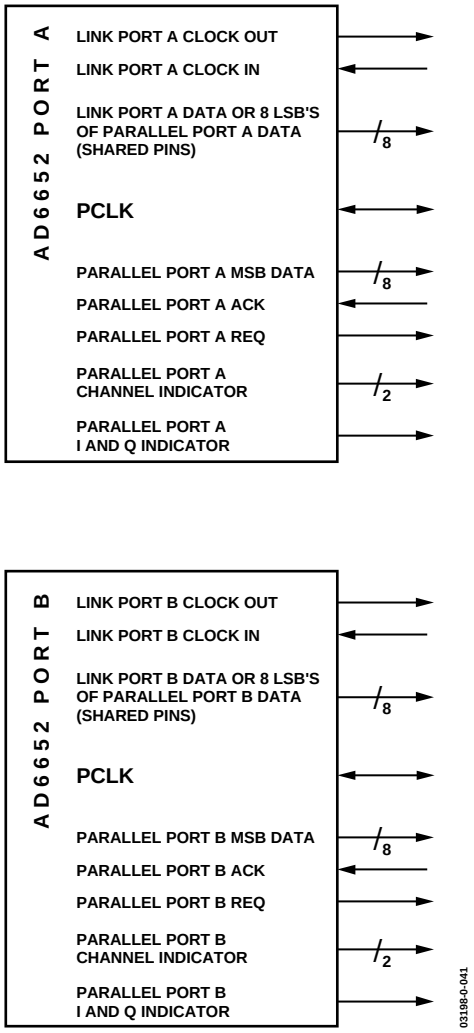


Figure 54. Output Port Configuration

Each parallel output port has six data sources routed to it (see the Functional Block Diagram in Figure 1):

- Noninterpolated RAM coefficient FIR filter output data from Channels 1, 2, 3, and 4
- Interpolated, interleaved, and/or AGC modified Channel A data
- Interpolated, interleaved, and/or AGC modified Channel B data

Any of the six sources can be output on any port(s). A port can be configured to output parallel data or DSP link data. Output port control registers (Table 29) perform these multiplexing and selection tasks.

Parallel port configuration is specified by accessing Port Control Register Addresses 0x1A and 0x1C for Parallel Ports A and B, respectively. Port clock master/slave mode (described in the Master/Slave PCLK Modes section) is configured using the port clock control register at Address 0x1E. Note that to access these registers, Bit 5 (access port control registers) of External Address 3 (sleep register) must be set. The address is then selected by programming the CAR register at External Address 6.

The parallel ports are enabled by setting Bit 7 of the link control registers at Addresses 0x1B and 0x1D for Ports A and B, respectively. Each parallel port is capable of operating in either channel mode or AGC mode. These modes are described in detail in the following sections.

CHANNEL MODE

Parallel port channel mode is selected by setting Bit 0 of Addresses 0x1B and 0x1D for Parallel Ports A and B, respectively. In channel mode, I and Q words from each channel are directed to the parallel port, bypassing the AGC. The specific channels output by the port are selected by setting Bits 1–4 of Parallel Port Control Register 0x1A (Port A) and 0x1C (Port B).

Channel mode provides two data formats. Each format requires a different number of parallel port clock (PCLK) cycles to complete the transfer of data. In each case, each data element is transferred during one PCLK cycle. See Figure 55 and Figure 56, which present channel mode parallel port timing.

The 16-bit interleaved format provides I and Q data for each output sample on back-to-back PCLK cycles. Both I and Q words consist of the full port width of 16 bits. Data output is triggered on the rising edge of PCLK when both REQ and ACK are asserted. I data is output during the first PCLK cycle; the PAIQ and PBIQ output indicator pins are set high to indicate that I data is on the bus. Q data is output during the subsequent PCLK cycle; the PAIQ and PBIQ output indicator pins are low during this cycle.

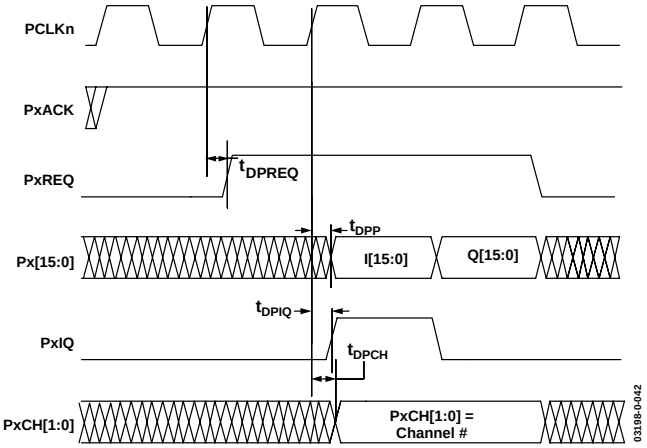


Figure 55. Channel Mode Interleaved Format

The 8-bit concurrent format provides 8 bits of I data and 8 bits of Q data simultaneously during one PCLK cycle, also triggered on the rising edge of PCLK. The I byte occupies the most significant byte of the port, while the Q byte occupies the least significant byte. The PAIQ and PBIQ output indicator pins are set high during the PCLK cycle. Note that if data from multiple channels is output consecutively, the PAIQ and PBIQ output indicator pins remain high until data from all channels has been output.

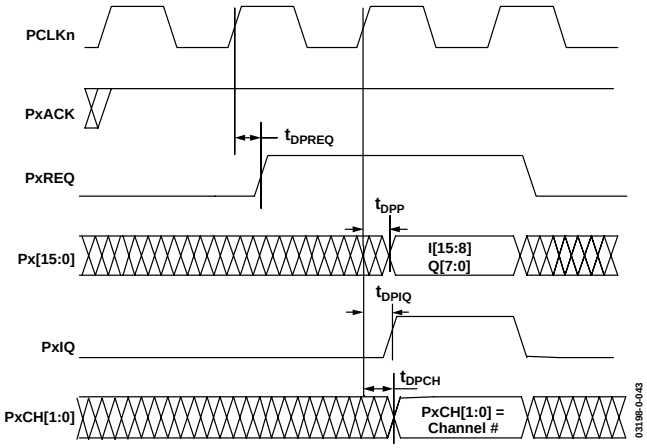


Figure 56. Channel Mode 8I/8Q Parallel Format

The PACH[1:0] and PBCH[1:0] pins provide a 2-bit binary value indicating the source channel of the data currently being output.

Care should be taken to read data from the port as soon as possible. If not, the sample will be overwritten when the next new data sample arrives. This occurs on a per-channel basis; that is, a Channel 0 sample is overwritten only by a new Channel 0 sample, and so on.

The order of data output is dependent on when data arrived at the port, which is a function of total decimation rate, start hold-off values, and so on. Priority order is, from highest to lowest, Channels 0, 1, 2, and 3.

AGC MODE

Parallel port channel mode is selected by clearing Bit 0 of Addresses 0x1A and 0x1C for Parallel Ports A and B, respectively. I and Q data output in AGC mode are output from the AGC, not the individual channels. AGC A accepts data from Channel 0 to Channel 3, while AGC B accepts data from Channel 2 and Channel 3. Each pair of channels is required to be configured such that the generation of output samples from the channels is out of phase (by typically 180°). Each parallel port can provide data from either one or both AGCs. Bit 1 and Bit 2 of Register Addresses 0x1A (Port A) and 0x1C (Port B) control the inclusion of data from AGCs A and B, respectively.

AGC mode provides only one I&Q format, which is similar to the 16-bit interleaved format of channel mode. When both REQ and ACK are asserted, the next rising edge of PCLK triggers the output of a 16-bit AGC I word for one PCLK cycle. The PAIQ and PBIQ output indicator pins are high during this cycle, and are low otherwise. A 16-bit AGC Q word is provided during the subsequent PCLK cycle. If the AGC gain word has been updated since the last sample, a 12-bit RSSI word is provided during the PCLK cycle following the Q word of 12 MSBs of the parallel port data pins. This RSSI word is the bit-inverse of the signal gain word used in the gain multiplier of the AGC.

The data provided by the PACH[1:0] and PBCH[1:0] pins in AGC mode is different than that provided in channel mode. In AGC mode, PACH[0] and PBCH[0] indicate the AGC source of the data currently being output (0 = AGC A, 1 = AGC B). PACH[1] and PBCH[1] indicate whether the current data is an I/Q word or an AGC RSSI word (0 = I/Q word, 1 = AGC RSSI word). The two different AGC outputs are shown in Figure 57 and Figure 58.

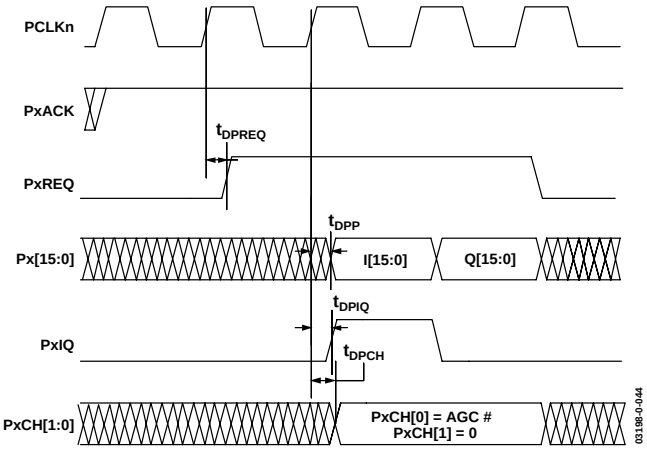


Figure 57. AGC with No RSSI Word

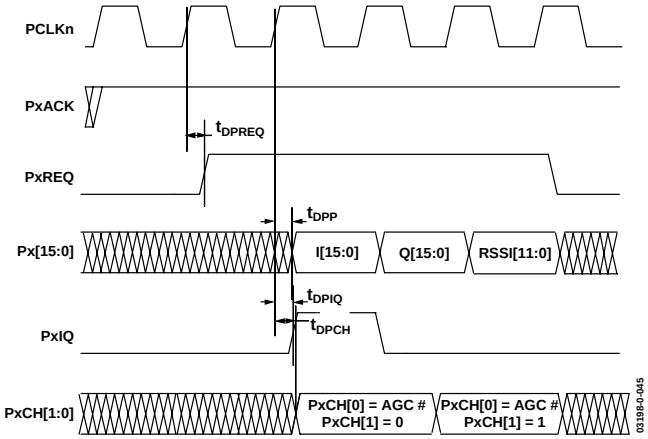


Figure 58. AGC with RSSI Word

MASTER/SLAVE PCLK MODES

The parallel ports operate in either master or slave mode. The mode is set via the port clock control register (Address 0x1E). The parallel ports power up in slave mode to avoid possible contentions on the PCLK pin.

In master mode, PCLK is an output whose frequency is the AD6652 clock frequency divided by the PCLK divisor. Because values for PCLK_divisor[2:1] can range from 0 to 3, integer divisors of 1, 2, 4,or 8, respectively, can be obtained. Because the maximum clock rate of the AD6652 is 65 MHz, the highest PLCK rate in master mode is also 65 MHz. Master mode is selected by setting Bit 0 of Address 0x1E.

In slave mode, external circuitry provides the PCLK signal. Slave-mode PCLK signals can be either synchronous or asynchronous. The maximum slave-mode PCLK frequency is 100 MHz.

PARALLEL PORT PIN FUNCTIONS

PCLK

Input/output. As an output (master mode), the maximum frequency is CLK/*n*, where CLK is the AD6652 clock and *n* is an integer divisor 1, 2, 4 or 8. As an input (slave mode), it might be asynchronous relative to the AD6652 CLK. This pin powers up as an input to avoid possible contentions. Other port outputs change on the rising edge of PCLK.

REQ

Active high output, synchronous to PCLK. A logic high on this pin indicates that data is available to be shifted out of the port. A logic high value remains high until all pending data has been shifted out.

PxACK

Active high asynchronous input. Applying a logic low on this pin inhibits parallel port data shifting. Applying a logic high to this pin when REQ is high causes the parallel port to shift out data according to the programmed data mode. PxACK is sampled on the falling edge of PCLK. Data is shifted out on the next rising edge of PCLK after PxACK is sampled. PxACK can be held high continuously. In this case, when data becomes available, shifting begins 1 PCLK cycle after the assertion of REQ (see Figure 55 to Figure 58).

PAIQ, PBIQ

High whenever I data is present on the port output, otherwise low.

PACH[1:0], PBCH[1:0]

These pins serve to identify data in both data modes. In channel mode, these pins form a 2-bit binary number identifying the source channel of the current data word. In AGC mode, [0] indicates the AGC source (0 = AGC A, 1 = AGC B), and [1] indicates whether the current data word is I/Q data (0) or a gain word (1).

PA[15:0], PB[15:0]

Parallel output data ports. Contents and format are mode-dependent.

LINK PORT

The AD6652 has two configurable link ports that provide a seamless data interface with the TigerSHARC TS-101 series DSP. Each link port allows the AD6652 to write output data to the receive DMA channel in the TigerSHARC for transfer to memory. Because they operate independently of each other, each link port can be connected to a different TigerSHARC or different link ports on the same TigerSHARC. Figure 59 shows how to connect one of the two AD6652 link ports to one of the four TigerSHARC link ports. Link Port A is configured through Register 0x1B and Link Port B is configured through Register 0x1D.

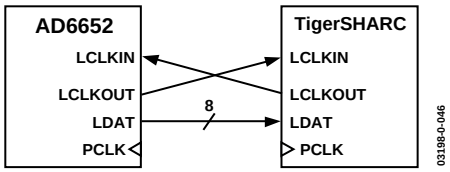


Figure 59. Link Port Connection between AD6652 and TigerSHARC

LINK PORT DATA FORMAT

Each link port can output data to the TigerSHARC in five different formats: 2-channel, 4-channel, dedicated AGC, redundant AGC with receive signal strength indicator (RSSI) word, and redundant AGC without RSSI word. Each format outputs two bytes of I data and two bytes of Q data to form a 4-byte IQ pair. Because the TigerSHARC link port transfers data in quad-word (16-byte) blocks, four IQ pairs can make up one quad-word. If the channel data is selected (Bit 0 = 0 of 0x1B/0x1D), then 4-byte IQ words of the four channels can be output in succession, or alternating channel pair IQ words can be output. Figure 60 and Figure 61 show the quad-word transmitted for each case with corresponding register values for configuring each link port.

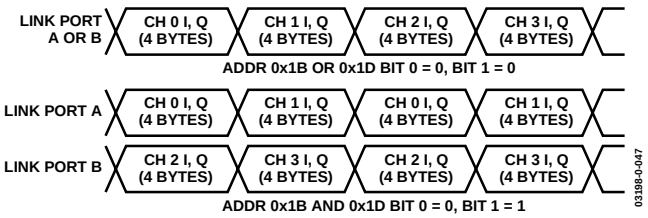


Figure 60. Link Port Data from RCF

If AGC output is selected (Bit 0 = 1), then RSSI information can be sent with the IQ pair from each AGC. Each link port can be configured to output data from one AGC, or both link ports can output data from the same AGC. If both link ports are transmitting the same data, then RSSI information must be sent with the IQ words (Bit 2 = 0). Note that the actual RSSI word is only two bytes (12 bits appended with 4 0s), so the link port sends two bytes of 0s immediately after each RSSI word to make a full 16-byte quad-word.

Note that Bit 0 = 1, Bit 1 = 0, and Bit 2 = 1 is not a valid configuration. Bit 2 must be set to 0, to output AGC A IQ and RSSI words on Link Port A and AGC B IQ and RSSI words on Link Port B.

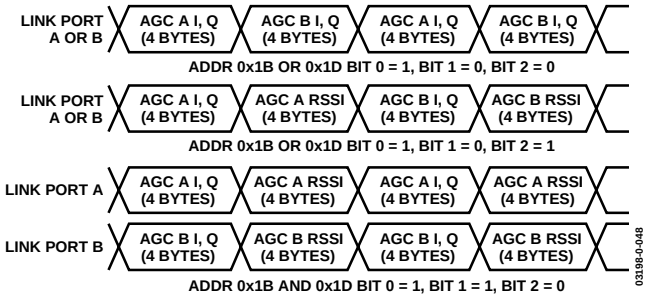


Figure 61. Link Port Data from AGC

LINK PORT TIMING

Both link ports run off of PCLK, which can be externally provided to the chip (Address 0x1E Bit 0 = 0) or generated from the master clock of the AD6652 (Address 0x1E Bit 0 = 1). This register boots to 0 (slave mode) and allows the user to control the data rate coming from the AD6652. PCLK can be run as fast as 100 MHz in slave mode.

The link port provides 1-byte data words (LA[7:0], LB[7:0] pins) and output clocks (LACLKOUT, LBCLKOUT pins) in response to a ready signal (LACLKIN, LBCLKIN pins) from the receiver. Each link port transmits 8 bits on each edge of LCLKOUT, requiring 8 LCLKOUT cycles to complete transmission of the full 16 bytes of a TigerSHARC quad-word.

Due to the TigerSHARC link port protocol, the AD6652 must wait at least 6 PCLK cycles after the TigerSHARC is ready to receive data, as indicated by the TigerSHARC setting the respective AD6652 LCLKIN pin high. Once the AD6652 link port has waited the appropriate number of PCLK cycles and has begun transmitting data, the TigerSHARC does a connectivity check by sending the AD6652 LCLKIN low and then high while the data is being transmitted. This tells the AD6652 link port that the TigerSHARC's DMA is ready to receive the next quad-word after completion of the current quad-word. Because the connectivity check is done in parallel to the data transmission, the AD6652 can stream uninterrupted data to the TigerSHARC.

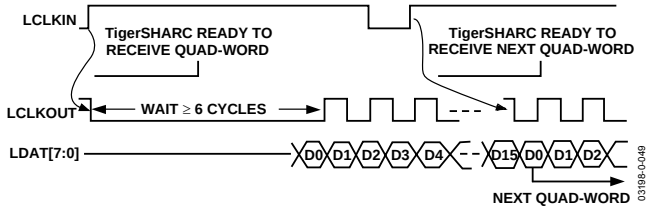


Figure 62. Link Port Data Transfer

The length of the wait before data transmission is a 4-bit programmable value in the link port control registers (0x1B and 0x1D Bits 6–3). This value allows the AD6652 PCLK and the TigerSHARC PCLK to be run at different rates and out of phase.

$$WAIT \geq ciel\left(6 \times \frac{f_{LCLK_AD6652}}{f_{LCLK_TSHARC}}\right)$$

WAIT ensures that the amount of time the AD6652 needs to wait to begin data transmission is at least equal to the minimum amount of time the TigerSHARC is expecting it to wait. If the PCLK of the AD6652 is out of phase with the PCLK of the TigerSHARC and the argument to the ceil() function is an integer, then WAIT must be strictly greater than the value given in the above formula.

If the LCLKs are in phase, then the maximum output data rate is

$$f_{LCLK_AD6652} \leq \frac{15}{6} \times f_{LCLK_TSHARC}$$

Otherwise, it is

$$f_{LCLK_AD6652} \leq \frac{14}{6} \times f_{LCLK_TSHARC}$$

TIGERSHARC CONFIGURATION

Because the AD6652 is always the transmitter in this link and the TigerSHARC is always the receiver, the following values can be programmed into the LCTL register for the link port used to receive AD6652 output data.

Table 21. TigerSHARC LCTLx Register Configuration

Register	Value
VERE	0
SPD	User[1]
LTEN	0
PSIZE	1
TTOE	0
CERE	0
LREN	1
RTOE	1

[1] The term *User* means that the actual register value depends on the user's application.

EXTERNAL MEMORY MAP

The external memory map is the *only* way to gain access to the four channel address register pages and the output port control register page. This set of eight registers is shown in Table 22. These registers are collectively referred to as the external memory map registers, because they control all accesses to the channel address space as well as output control registers.

The use of each of these individual registers is described in detail in the following sections. It should be noted that the serial control interface has the same memory map as the microport interface and can carry out exactly the same functions, although at a slower rate.

Table 22. External Memory Map

Address	Name	Comment	
7	Access Control Register (ACR)	7:	Auto increment
		6:	Broadcast
		5–2:	Instruction[3:0]
		1–0:	A[9:8]
6	Channel Address Registers (CAR)	7–0:	A[7:0]
5	SOFT_SYNC Control Register (Write Only)	7:	PN_EN
		6:	Test_MUX_Select
		5:	Hop
		4:	Start
		3:	SYNC CH3
		2:	SYNC CH2
		1:	SYNC CH1
		0:	SYNC CH0
4	PIN_SYNC Control Register (Write Only)	7:	Reserved write to logic low
		6:	First SYNC only
		5:	Hop_En
		4:	Start_En
		3:	PIN SYNC_EN D
		2:	PIN SYNC_EN C
		1:	PIN SYNC_EN B
		0:	PIN SYNC_EN A
3	SLEEP (Write Only)	7–6:	Reserved write to logic low
		5:	Access output port control registers
		4:	Reserved low
		3:	SLEEP CH3
		2:	SLEEP CH2
		1:	SLEEP CH1
		0:	SLEEP CH 0
2	Data Register 2 (DR2)	7–4:	Reserved
		3–0:	D[19:16]
1	Data Register 1 (DR1)	15–8:	D[15:8]
0	Data Register 0 (DR0)	7–0:	D[7:0]

ACCESS CONTROL REGISTER (ACR)
External Address 7

The ACR specifies certain programming characteristics such as autoincrement or broadcast, which are to be applied to the incoming instructions, and selects which channel(s) are to be programmed by the microport or serial port.

Bit 7 of this register is the autoincrement bit. If this bit is a 1, then the CAR register, described in the Channel Address Register (CAR) section, increments its value after every access to the channel. This allows blocks of address space such as coefficient memory to be initialized more efficiently.

Bit 6 of the register is the broadcast bit, which determines how Bits 5–2 are interpreted. If broadcast is 0 then Bits 5–2, which are referred to as instruction bits (Instruction[3:0]), are compared with the CHIP_ID[3:0] pins. The instruction that matches the CHIP_ID[3:0] pins determines the access. This allows up to 16 chips to be connected to the same port and memory mapped without external logic. This also allows the same serial port of a host processor to configure up to 16 chips.

If the broadcast bit is high, the Instruction[3:0] word allows multiple AD6652 channels and/or chips to be configured simultaneously independent of the CHIP_ID[3:0] pins. The 10 possible instructions are defined in Table 23. This is useful for smart antenna systems, where multiple channels listening to a single antenna or carrier can be configured simultaneously. The x's in the comment portion of the table represent "don't cares" in the digital decoding. When broadcast is enabled (Bit 6 set high) readback is not valid because of the potential for internal bus contention. Therefore, if readback is subsequently desired, the broadcast bit should be set low.

Bits 1–0 of the ACR are address bits that decode which of the four channels are being accessed. If the instruction bits decode an access to multiple channels, then these bits are ignored. If the instruction decodes an access to a subset of chips, then the A[9:8] bits otherwise determine the channel being accessed.

Table 23. Microport Instructions, 7:5–2

Instruction	Comment
0000	All chips and all channels have access.
0001	Channels 0, 1, 2 of all chips have access.
0010	Channels 1, 2, 3 of all chips have access.
0100	All chips get the access.[1]
1000	All chips with Chip_ID[3:0] = xxx0 have access.[1]
1001	All chips with Chip_ID[3:0] = xxx1 have access.[1]
1100	All chips with Chip_ID[3:0] = xx00 have access.[1]
1101	All chips with Chip_ID[3:0] = xx01 have access.[1]
1110	All chips with Chip_ID[3:0] = xx10 have access.[1]
1111	All chips with Chip_ID[3:0] = xx11 have access.[1]

[1] A[9:8] bits control which channel is decoded for access.

CHANNEL ADDRESS REGISTER (CAR)
External Address 6

The user writes the 8-bit internal address of a channel register to be programmed in the CAR. If the autoincrement bit of the ACR is 1, then this value is incremented after every access to the DR0 register, which in turn accesses the location pointed to by this address. The channel address register cannot be read back while the broadcast bit is set high.

SOFT_SYNC CONTROL REGISTER
External Address 5

The SOFT_SYNC control register is write only. The register name is somewhat deceiving in that this register also contains BIST (built-in self-test) commands that turn internal test signals off or on, namely, pseudonoise and negative full-scale sine wave, at Bits 7 and 6, explained below.

Bits 0–3 of this register are the SOFT_SYNC channel enable bits for each of the four DDC channels. Writing a logic high to one or all of these bits simply selects the indicated channel(s) to be recipients of a soft_sync synchronizing pulse—whenever such signal is generated by Bits 4 and 5 of this register as described below. A pin-sync signal can be used in addition to a soft-sync signal, if desired.

Bit 4 is the start software synchronizing pulse. Writing this bit to logic high initiates a one-shot-type pulse to trigger the start hold-off counter of the selected DDC channels according to Bits 3–0 above. See the Channel/Chip Synchronization section for further information. Programming this bit also programs Channel Address Register 0x82 of each channel.

Bit 5 is the hop software synchronizing pulse. Writing this bit to logic high initiates a one-shot-type pulse to trigger the hop frequency hold-off counter of the selected DDC channels according to Bits 3–0 above. See the Channel/Chip Synchronization section. Programming this bit also programs the Channel Address Register 0x82 of each channel.

Bit 6 configures how the internal input data bus is configured. If this bit is low, then the ADCs (analog–to-digital converters) are connected to the DDC NCOs according to the user's choice—this is normal operation. If this bit is logic high, then the internal test signals are connected to all DDC NCOs for BIST purposes and this overrides any NCO programmed input choice. The internal test signals are configured in Bit 7 of this register.

If Bit 7 is logic low, a negative full-scale signal is generated and made available to the internal data bus. If this bit is high, then the internal pseudorandom noise generator is enabled and this data is available to the internal input data bus. The combined functions of Bits 6 and 7 facilitate BIST functions. Also, in conjunction with the MISR registers, this allows for detailed in-system chip testing.

PIN_SYNC CONTROL REGISTER
External Address 4

This is the write-only PIN_SYNC control register.

Bits 3–0 of this register are the PIN SYNC_EN control bits. These bits can be written to by the controller to select any or all of the external pin sync inputs: A, B, C, and/or D. One pin can be assigned to all channels, one pin can be assigned to one channel, or any combination in between. This register is fully configurable at the channel level (in the channel address register memory map, 0x88) as to which pin-sync signal is selected. A pin-sync signal can be used in addition to a soft-sync signal, if desired. See Figure 53.

Bit 4 is the start enable bit. Writing this bit to logic high enables or facilitates the routing of the external pin-sync signal to *all* the DDC channels. This bit enables any pin-sync signals that were selected by Bits 3–0 above, to be routed to a 4-to-1 multiplexer and ultimately chosen to be the channel's pin-sync signal that controls the start function. See Figure 53. Programming this bit also programs the Channel Address Register 0x82 of each channel.

Bit 5 is the hop enable bit. Writing this bit to logic high enables or facilitates the routing of the external pin-sync signal to *all* the DDC channels. This bit enables any pin-sync signals that were selected by Bits 3–0 above to be routed to a 4-to-1 multiplexer and ultimately chosen to be the channel's pin-sync signal that controls the Hop function. See Figure 53. Programming this bit also programs the Channel Address Register 0x82 of each channel.

Bit 6 is used to ignore repetitive synchronization signals. If this bit is clear, each PIN_SYNC restarts or frequency hops the channel. If this bit is set, then only the first occurrence causes the action to occur. Programming this bit also programs the Channel Address Register 0x82 of each channel.

Bit 7 is reserved; the bits should be written to Logic 0.

SLEEP CONTROL REGISTER
External Address 3

In addition to sleep mode control, this register also provides access to the output port control register's memory map.

Bits 3–0 control the sleep mode of the indicated channel. If the bit is low, the channel operates normally. If the bit is high, the indicated channel enters a low-power sleep mode. Programming this bit also programs the Channel Address Register 0x82 of each channel.

Bit 4 is reserved and should be written to Logic 0.

Bit 5 allows access to the output control port registers. When this bit is low, the channel address registers are accessed. However, when this bit is set high, it allows access to the output port control registers. When this bit is set high, the value in External Address 6 (CAR) points to the memory map for the output control port registers instead of the normal channel address register memory map. See Table 29 in the Output Port Control Registers section.

Bit 6–7 are reserved and should be written low.

DATA ADDRESS REGISTERS
External Address 2–0

These registers form the data registers DR2, DR1, and DR0, respectively. All internal data-words have widths that are equal to or less than 20 bits. When External Address 0 is written to, it triggers an internal access to the AD6652 based on the address indicated in the ACR and CAR. Thus, during writes to the internal registers, External Address [0] DR0 must be written last. At this point, data is transferred to the internal memory indicated in A[9:0]. Reads are performed in the opposite direction. Once the address is set, External Address [0] DR0 must be the first data register read to initiate an internal access. DR2 is only 4 bits wide. Data written to the upper 4 bits of this register are ignored. Likewise, reading from this register produces only 4 LSBs.

Figure 63 is a block diagram of the memory structure.

CHANNEL ADDRESS REGISTERS (CAR)
0x00–0x7F: Coefficient Memory (CMEM)

This register is the coefficient memory (CMEM) used by the RCF. It is memory mapped as 128 words by 20 bits. A second 128 words of RAM can be accessed via this same location by writing Bit 8 of the RCF control register high at Channel Address 0xA4. The filter calculated always uses the same coefficients for I and Q. By using memory from both of these 128 blocks, a filter of up to 160 taps can be calculated. Multiple filters can be loaded and selected with a single internal access to the coefficient offset register at Channel Address 0xA3.

0x80: Channel Sleep Register

This register contains the sleep bit for the channel. It mimics the programming of Bits 0–3 at External Address 3. External Address 3 provides simultaneous sleep mode control for all four DDC channels. The user can overwrite the data in 0x80, if desired. Sleep mode is selected when this bit is written logic high.

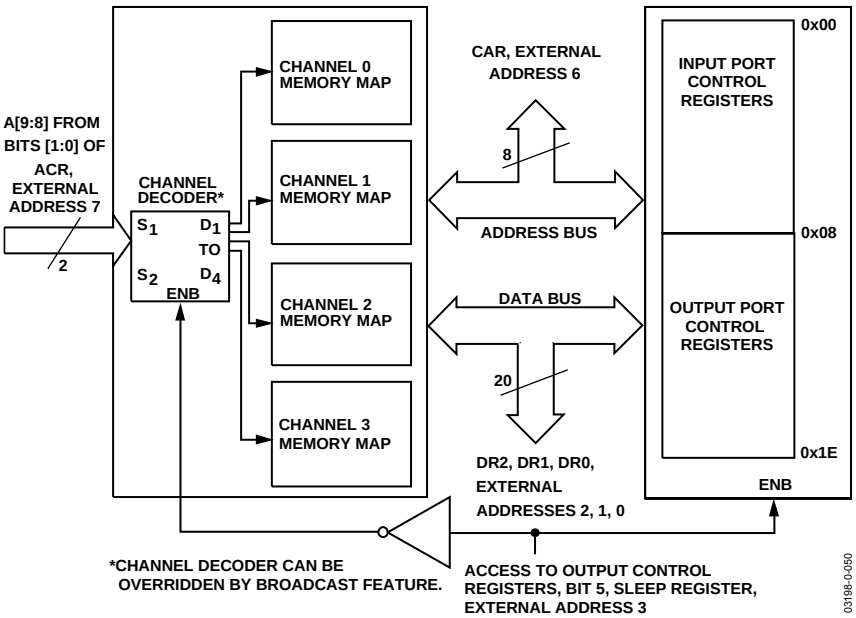


Figure 63. Block Diagram of the AD6652 Internal Memory Maps and Controls

0x81: Soft_SYNC Register

This register is used to initiate software-generated SYNC events through the microport. It mimics the programming of Bits 4 and 5 at External Address 5. If the hop bit is written high, then the hop hold-off counter at Address 0x84 is loaded and begins to count down. When the count reaches a value of 1, the channel's NCO frequency accumulator is loaded with the data from Channel Addresses 0x85 and 0x86. When the start bit is written high, the start hold-off counter is loaded with the value at Address 0x83 and begins to count down. When the count reaches a value of 1, the sleep bit in Address 0x80 is written low and the channel is started.

0x82: Pin_SYNC Register

This register mimics Bits 4, 5, and 6 of External Memory Map Address 4. Because the programming at External Memory Address 4 applies to all four channels, the user can customize a particular channel by overwriting the data in 0x82.If the initial programming provided by External Address 4 is satisfactory, the user does not need to reprogram the elements of this register.

Unlike the two bits in 0x81 above, setting the Hop_En or the Start_En (Bits 1 and 0) of this register does *not* trigger anything. These bits simply allow, or enable, an external synchronizing signal to be routed to the channel's start and/or hop multiplexers. Even though a signal has been enabled to reach the multiplexer, it still needs to be selected. This job is accomplished by Bits 8 and 7 of 0x88, as discussed below. The schematic diagram of Figure 53 is helpful in understanding the Pin_SYNC enabling and selection bits of the involved registers.

Bit 2 of 0x82 engages the first sync only function for the channel. This bit is a copy of External Address 4, Bit 6, but can be overwritten to change the programming of a particular channel. If this bit is clear, each PIN_SYNC restarts or rehops the channel. If this bit is set, then only the first sync pulse causes the action to occur.

0x83: Start Hold-Off Counter

The start hold-off counter is loaded with the 16-bit value written to this address. When the Start function is triggered by either a Soft_SYNC or Pin_SYNC, the hold-off counter begins decrementing. When the count reaches a value of one, the channel is brought out of sleep mode and begins processing data. *If the channel is already running, the phase of the filter(s) is adjusted such that multiple AD6652s can be synchronized.*

A periodic pulse on the SYNC pin can be used in this way to adjust the timing of the filters with the resolution of the ADC sample clock. See the 0xA1 register description for further information about filter phase adjustment. If this register is written to Logic 1, then the start occurs immediately after the SYNC pulse arrives. If it is written to Logic 0, then the counter does not respond to a SYNC pulse.

0x84: Hop or Frequency Hold-Off Counter

The NCO frequency hold-off counter is loaded with the 16-bit value written to this address upon receipt of either a Soft_SYNC or Pin_SYNC. The counter begins counting, and when the count reaches a value of 1, the 32-bit NCO frequency word is updated with the values at 0x85 and 0x86. This is known as a hop or Hop_SYNC. Writing this register to a value of 1 causes the NCO frequency to be updated immediately when the SYNC comes into the channel. If it is written to a 0, then no Hop occurs. NCO hops can be either phase-continuous or non-phase-continuous, depending upon the state of Bit 3 of the

NCO control register at Channel Address 0x88. When this bit is low, then the phase accumulator of the NCO is not cleared, but starts to add the new NCO frequency word to the accumulator as soon as the SYNC occurs. If this bit is high, then the phase accumulator of the NCO is cleared to 0, and the new word is then accumulated.

0x85: NCO Frequency Register 0

This register represents the 16 LSBs of the NCO frequency word. These bits are shadowed and are not updated to the working register until the channel is either brought out of sleep mode, or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases, the register is updated when the frequency hold-off counter count reaches a value of 1. If the frequency hold-off counter value is set to a value of 1, then the register is updated as soon as the shadow is written.

0x86: NCO Frequency Register 1

This register represents the 16 MSBs of the NCO frequency word. These bits are shadowed and are not updated to the working register until the channel is either brought out of sleep mode, or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases, the register is updated only when the frequency hold-off counter count reaches a value of 1. If the frequency hold-off counter is set to a value of 1, then the register is updated as soon as the shadow is written.

Table 24. Channel Address Memory Map

Channel Address	Register	Bit Width	Comments
00–7F	Coefficient Memory (CMEM)	20	128 x 20-bit memory
80	CHANNEL SLEEP	1	0: Sleep bit from EXT_ADDRESS 3
81	Soft_Sync Control Register	2	1: Hop 0: Start
82	Pin_SYNC Control Register	3	2: First SYNC only 1: Hop_En 0: Start_En
83	Start Hold-Off Counter	16	Start hold-off value
84	NCO Frequency Hold-Off Counter	16	NCO_FREQ hold-off value
85	NCO Frequency Register 0	16	NCO_FREQ[15:0]
86	NCO Frequency Register 1	16	NCO_FREQ[31:16]
87	NCO Phase Offset Register	16	NCO_PHASE[15:0]
88	NCO Control Register	9	8-7: SYNC input select[1:0] 00 = A, 01 = B, 10 = C, 11 = D 6: Input port select B or A, 0 = A, 1 = B 5-4: Reserved, write both bits logic low 3: Clear phase accumulator on hop 2: Amplitude dither 1: Phase dither 0: Bypass (A-input -> I-path, B -> Q)
89–8F	Unused		
90	rCIC2 Decimation – 1	12	$M_{rCIC2} - 1$
91	rCIC2 Interpolation – 1	9	$L_{rCIC2} - 1$
92	rCIC2 Scale	12	11: Reserved, write to logic low 10: Reserved, write to logic low 9-5: rCIC2 _QUIET [4:0] 4-0: rCIC2_LOUD [4:0]
93	Reserved	8	Reserved (must be written low)
94	CIC5 Decimation – 1	8	$M_{CIC5} - 1$
95	CIC5 Scale	5	4-0: CIC5_SCALE[4:0]
96	Reserved	8	Reserved (must be written low)
97–9F	Unused		
A0	RCF Decimation – 1	8	$M_{RCF} - 1$
A1	RCF Decimation Phase	8	P_{RCF}
A2	RCF Number of Taps – 1	8	$N_{Taps} - 1$
A3	RCF Coefficient Offset	8	CO_{RCF}

Channel Address	Register	Bit Width	Comments
A4	RCF Control Register	11	10: RCF bypass BIST 9: RCF input select (own 0, other 1) 8: Program RAM bank 1/0 7: Use common exponent 6: Force output scale 5-4: Output format 1x: Floating point 12 + 4 01: Floating point 8 + 4 00: Fixed point 3-0: Output scale
A5	BIST Signature for I Path	16	BIST-I
A6	BIST Signature for Q Path	16	BIST-Q
A7	BIST Outputs to Accumulate	20	19-0: Number of outputs (counter value read)
A8	RAM BIST Control Register	3	2: D-RAM fail/pass 1: C-RAM fail/pass 0: RAM BIST enable
A9	Output Control Register	10	9: Map RCF data to BIST registers 5: Output format 1: 16-bit I and 16-bit Q 0: 12-bit I and 12-bit Q 4-0: Reserved, write to Logic 0

0x87: NCO Phase Offset Register

This register represents a 16-bit phase offset to the NCO. It can be interpreted as values ranging from 0 to just under 2π. The 16-bit phase offset is added to the 16 MSBs of the 32-bit NCO phase accumulator to arrive at the final phase angle number used to compute the amplitude value.

0x88: NCO Control Register

This 9-bit register controls features of the NCO and the channel. The bits are defined in this section. For details, see the Numerically Controlled Oscillator section.

Bits 8–7 of this register choose which one of the four Pin_SYNC pins (A, B, C, or D) is used by the channel to initiate channel start and frequency hop functions. These bits can also be used to make timing adjustments to a channel.

Table 25 shows the bit logic state needed to select a particular Pin_Sync.

Table 25. Bit Logic States for Sync Pins

0x88:8	0x88:7	Sync Pin Selected
0	0	A
0	1	B
1	0	C
1	1	D

Bit 6 of this register defines which ADC channel, A or B, is used by the DDC channel being programmed. If this bit is low, then Input Port A selected; if this bit is high, Input Port B is selected.

Bits 5–4 are reserved and must be written logic low.

Bit 3 determines whether or not the phase accumulator of the NCO is cleared when a hop occurs. The hop can originate from either Pin_SYNC or Soft_SYNC. When this bit is set to 0, the hop is phase-continuous and the accumulator is not cleared. When this bit is set to 1, the accumulator is cleared to 0 before it begins accumulating the new frequency word. This is appropriate when multiple channels are hopping from different frequencies to a common frequency.

Bits 2–1 control whether or not the phase and amplitude dither functions of the NCO are activated. The use of these features is determined by the system constraints. See the Numerically Controlled Oscillator section for more information on the use of dither. As usual, a logic high activates the function.

Bit 0 of this register allows the NCO frequency translation stage to be bypassed. When this occurs, the data from Input Port A is passed down the I path of the channel and the data from Input Port B is passed down the Q path of the channel. This allows a real filter to be performed on baseband I and Q data.

0x89–0x8F: Unused

Unused.

0x90: rCIC2 Decimation – 1 (M_{rCIC2} – 1)

This register sets the decimation in the rCIC2 filter. The value written to this register is the decimation minus one. The rCIC2 decimation can range from 1 to 4096, depending upon the interpolation of the channel. The decimation must always be greater than the interpolation.

M_{rCIC2} must be chosen larger than L_{rCIC2}, and both must be chosen such that a suitable rCIC2 scalar can be chosen. For details, see the Second-Order RCIC Filter section.

0x91: rCIC2 Interpolation – 1 (L_{rCIC2} – 1)

This register is used to set the interpolation in the rCIC2 filter. The value written to this register is the interpolation minus 1. The rCIC2 interpolation can range from 1 to 512, depending upon the decimation of the rCIC2. There is no timing error associated with this interpolation. For details, see the Second-Order RCIC Filter section.

0x92: rCIC2 Scale

The rCIC2 scale register is used to provide attenuation to compensate for the gain of the rCIC2 and to adjust the linearization of the data from the floating-point input. The use of this scale register is influenced by the rCIC2 growth. For details, see the Second-Order RCIC Filter section.

Bit 11 is reserved. Write all bits to Logic 0.

Bit 10 is reserved. Write all bits to Logic 0.

Bits 9–5 are the actual scale value used when the level indicator, LI pin associated with this channel, is active (Logic 1).

Bits 4–0 are the actual scale value used when the level indicator, LI pin associated with this channel, is inactive (Logic 0).

0x93: Reserved

Eight bits, reserved (must be written low).

0x94: CIC5 Decimation – 1 (M_{CIC5} – 1)

This register is used to set the decimation in the CIC5 filter. The 8-bit value written to this register is the decimation minus 1.

0x95: CIC5 Scale

The 5-bit CIC5 scale factor is used to compensate for the growth of the CIC5 filter. For details, see the Fifth-Order CIC Filter section.

0x96: Reserved

Reserved (must be written low).

0x97–0x9F: Unused

Unused.

0xA0: RCF Decimation – 1 (M_{RCF} – 1)

This register is used to set the decimation of the RCF stage. The value written to this register is the desired decimation minus one. Although this is an 8-bit register that allows decimation up to 256, most filter designs should be limited to between 1 and 32. Higher decimations are allowed, but the alias rejection of the RCF might not be acceptable for some applications.

0xA1: RCF Decimation Phase (P_{RCF})

This register allows any one of the M_{RCF} phases of the filter to be used and can be adjusted dynamically. Each time a filter is started, this phase is updated. When a channel is synchronized, it retains the phase setting chosen here. This can be used as part of a timing recovery loop with an external processor or can allow multiple RCFs to work together while using a single RCF pair. For details, see the RAM Coefficient Filter section.

0xA2: RCF Number of Tap – 1 (N_{RCF} – 1)

The number of taps for the RCF filter minus 1 is written to this register.

0xA3: RCF Coefficient Offset (CO_{RCF})

This register is used to specify which section of the 256-word coefficient memory is used for a filter. It can be used to select among multiple filters that are loaded into memory and referenced by this pointer.

This register is shadowed, and the filter pointer is updated (from the shadow register) on every new filter output sample. This allows the coefficient offset to be written without disturbing operation, even while a filter is being computed. The next sample that comes out of the RCF is with the new filter.

0xA4: RCF Control Register

The RCF control register is an 11-bit register that controls the general features of the RCF as well as output formatting. The bits of this register and their functions are described below.

Bit 10 bypasses the RCF filter and sends the CIC5 output data to the BIST-I and BIST-Q registers. The 16 MSBs of the CIC5 data can be accessed from this register, if Bit 9 of the output control register at Channel Address 0xA9 is set.

Bit 9 of this register controls the source of the input data to the RCF. If this bit is 0, then the RCF processes the output data of its own channel. If this bit is 1, then it processes the data from the CIC5 of another channel. The CIC5 channels that the RCF can be connected to when this bit is 1 are shown in the Table 26. These can be used to allow multiple RCFs to be used together to process wider bandwidth channels.

Table 26. RCF Input Configurations

Channel	RCF Input Source when Bit 9 Is 1
0	1
1	0
2	1
3	1

Bit 8 is used as an extra address to allow a second block of 128 words of CMEM to be addressed by the channel addresses at 0x00–0x7F. If this bit is 0, then the first 128 words are written; if this bit is 1, then the next 128 words are written. This bit is used to program only the coefficient memory so that filters longer than 128 taps can be realized.

Bit 7 is used to control the output formatting of the AD6652's RCF data. This bit is used only when the 8 + 4 or 12 + 4 floating-point modes are chosen. These modes are enabled by Bits 5 and 4 of this register. When this bit is 0, then the I and Q output exponents are determined separately based on their

individual magnitudes. When this bit is 1, then the I and Q data is a complex floating-point number, where I and Q use a single exponent that is determined based on the maximum magnitude of I or Q.

Bit 6 is used to force the output scale factor in Bits 3–0 of this register to be used to scale the data even when one of the floating-point output modes is used. If the number is too large to represent with the output scale chosen, then the mantissas of the I and Q data clip do not overflow.

Normally, the AD6652 determines the exponent value that optimizes numerical accuracy. However, if Bit 6 is set, the value stored in Bits 3–0 is used to scale the output. This ensures consistent scaling and accuracy during conditions that warrant predictable output ranges.

Bits 5 and 4 choose the output formatting option used by the RCF data. The options are defined in the Table 27 and are discussed further in the Output Port Control Registers section.

Table 27. Output Formats

Bit Value	Output Formatting Option
1x	12-bit mantissa and 4-bit exponent (12 + 4)
01	8-bit mantissa and 4-bit exponent (8 + 4)
00	Fixed point mode

Bits 3–0 of this register represent the output scale factor of the RCF. The scale factor is used to scale the data when the output format is in fixed-point mode or when the force exponent bit is high. If Bits 3–0 are represented by RCF scale, the scaling factor in dB is given by

$$Scaling\ \ Factor = (RCF\ Scale\ -\ 3) \times 20\log_{10}\ (2)\,dB$$

For an RCF scale of 0, the scaling factor is equal to −18.06 dB; for a maximum RCF scale of 15, the scaling factor is equal to +72.25 dB.

0xA5: BIST Register for I

This register serves two purposes. The first is to allow the complete functionality of the I datapath in the channel to be tested in the system. See the User-Configurable Built-In Self-Test (BIST) section for details. The second function is to provide access to the I output data through the microport. To accomplish this, the Map RCF Data to BIST bit in the RCF Control Register 2, 0xA9, should be set high. Then 16 bits of I data can be read through the microport in either the 8 + 4, 12 + 4, 12-bit linear, or 16-bit linear output modes. This data can come from either the formatted RCF output or the CIC5 output.

0xA6: BIST Register for Q

This register serves two purposes. The first is to allow the complete functionality of the Q data path in the channel to be tested in the system. See the User-Configurable Built-In Self-Test (BIST) section for further details. The second function is to provide access to the Q output data through the microport. To accomplish this, the Map RCF Data to BIST bit in the RCF Control Register 2, 0xA9, should be set high. Then 16 bits of Q data can be read through the microport in either the 8 + 4, 12 + 4, 12-bit linear, or 16-bit linear output modes. This data can come from either the formatted RCF output or the CIC5 output.

0xA7: BIST Outputs to Accumulate

This 20-bit register controls the number of outputs of the RCF or CIC filter that are observed when a BIST test is performed. The BIST signature registers at Addresses 0xA5 and 0xA6 observe this number of outputs and then terminate. The loading of this register also starts the BIST engine running. For details on utilizing the BIST circuitry, see the User-Configurable Built-In Self-Test (BIST) section.

0xA8: RAM BIST Control Register

This 3-bit register is used to test the memories of the AD6652, if a failure is suspected. Bit 0 of this register is written with a 1 when the channel is in sleep mode. The user waits for 1600 CLKs, and then polls the bits. If Bit 1 is high, then the CMEM failed the test; if Bit 2 is high, then the data memory used by the RCF failed the test.

0xA9: Output Control Register

Bit 9 of this register allows the RCF or CIC5 data to be mapped to the BIST registers at Addresses 0xA5 and 0xA6. When this bit is 0, then the BIST register is in signature mode and ready for a self-test to be run. When this bit is 1, then the output data from the RCF (after formatting) or from CIC5 data is mapped to these registers and can be read through the microport.

Bit 5 determines the word length used by the parallel port. If this bit is 0, then the parallel port uses 12-bit words for I and Q. If this bit is 1, then the parallel port uses 16-bit words for I and Q. When the fixed-point output option is chosen from the RCF control register, then these bits also set the rounding correctly in the output formatter of the RCF.

Bits 4–0 are reserved and should be written low when programming.

INPUT PORT CONTROL REGISTERS

The input port control registers enable various input-related features used primarily for level control. Depending on the mode of operation, up to four different signal paths can be monitored with these registers. These features are accessed by setting Bit 5 of External Address 3 (sleep register) and then using the CAR (External Address 6) to address the eight locations available. Response to these settings is directed to the LIA, $\overline{\text{LIA}}$, LIB, and $\overline{\text{LIB}}$ pins.

To access the input port registers, the program gain control bit should be written high. The CAR is then written with the address to the correct input port register.

0x00: Lower Threshold A

This word is 10 bits wide and maps to the 10 MSB of the mantissa. If the upper 10 bits of Input Port A are less than or equal to this value, then the lower threshold has been met. In normal chip operation, this starts the dwell time counter. If the input signal increases above this value, then the counter is reloaded and awaits the input to drop back to this level.

0x01: Upper Threshold A

This word is 10 bits wide and maps to the 10 MSB of the mantissa. If the upper 10 bits of Input Port A are greater than or equal to this value, then the upper threshold has been met. In normal chip operation, this causes the appropriate LI pin (LIA or $\overline{\text{LIA}}$) to become active.

0x02: Dwell Time A

This word sets the time that the input signal must be at or below the lower threshold before the LI pin is deactivated. For the input level detector to work, the dwell time must be set to at least 1. If set to 0, the LI functions are disabled. This is a 20-bit register. When the lower threshold is met following an excursion into the upper threshold, the dwell time counter is loaded and begins to count high speed clock cycles as long as the input is at or below the lower threshold. If the signal increases above the lower threshold, the counter is reloaded and waits for the signal to fall below the lower threshold again.

0x03: Gain Range A Control Register

Bit 4 determines the polarity of LIA and $\overline{\text{LIA}}$. If this bit is clear, then the LI signal is high when the upper threshold has been exceeded. However, if this bit is set, the LI pin is low when active. This allows maximum flexibility when using this function.

Bit 3 = 0 (Reserved).

Bit 2–0 determines the internal latency of the gain detect function. When the LIA, $\overline{\text{LIA}}$ pins are made active, they are typically used to change an attenuator or gain stage. Because this is prior to the ADC, there is a latency associated with the ADC and with the settling of the gain change. This register allows the internal delay of the LIA, $\overline{\text{LIA}}$ signal to be programmed.

0x04: Lower Threshold B

This word is 10 bits wide and maps to the 10 MSB of the mantissa. If the upper 10 bits of Input Port B are less than or equal to this value, then the lower threshold has been met. In normal chip operation, this starts the dwell time counter. If the input signal increases above this value, then the counter is reloaded and awaits the input to drop back to this level.

0x05: Upper Threshold B

This word is 10 bits wide and maps to the 10 MSB of the mantissa. If the upper 10 bits of Input Port B are greater than or equal to this value, then the upper threshold has been met. In normal chip operation, this causes the appropriate LI pin (LIB or $\overline{\text{LIB}}$) to become active

0x06: Dwell Time B

This word sets the time that the input signal must be at or below the lower threshold before the LI pin is deactivated. For the input level detector to work, the dwell time must be set to at least 1. If set to 0, the LI functions are disabled. This is a 20-bit register. When the lower threshold is met following an excursion into the upper threshold, the dwell time counter is loaded and begins to count high speed clock cycles as long as the input is at or below the lower threshold. If the signal increases above the lower threshold, the counter is reloaded and waits for the signal to fall below the lower threshold again.

0x0: Gain Range B Control Register

Bit 4 determines the polarity of LIB and $\overline{\text{LIB}}$. If this bit is clear, then the LI signal is high when the upper threshold has been exceeded. However, if this bit is set, the LI pin is low when active. This allows maximum flexibility when using this function.

Bit 3 = 0 (Reserved.

Bit 2–0 determines the internal latency of the gain detect function. When the LIB, $\overline{\text{LIB}}$ pins are made active, they are typically used to change an attenuator or gain stage. Because this is prior to the ADC, there is a latency associated with the ADC and with the settling of the gain change. This register allows the internal delay of the LIB, $\overline{\text{LIB}}$ signal to be programmed.

Table 28. Memory Map for Input Port Control Registers

Channel Address	Register	Bit Width	Comments	
00	Lower Threshold A	10	9–0:	Lower threshold for Input A
01	Upper Threshold A	10	9–0:	Upper threshold for Input A
02	Dwell Time A	20	19–0:	Minimum time below Lower Threshold A
03	Gain Range A Control Register	5	4:	Output polarity LIA and $\overline{\text{LIA}}$
			3:	(0) Reserved
			2–0:	Linearization hold-off register
04	Lower Threshold B	10	9–0:	Lower threshold for Input B
05	Upper Threshold B	10	9–0:	Upper threshold for Input B
06	Dwell Time B	20	19–0:	Minimum time below Lower Threshold B
07	Gain Range B Control Register	5	4:	Output polarity LIB and $\overline{\text{LIB}}$
			3:	(0) Reserved
			2–0:	Linearization hold-off register

OUTPUT PORT CONTROL REGISTERS

This group of registers is dedicated to data management after individual channels have processed the incoming data. They manage data interleaving, 2× interpolation, AGC functions, output port assignment, and output port setup. Because there are two output ports, A and B, the data must be funneled from four channels down to two. These registers are responsible for guiding the data directly to the proper output port(s) or detouring the data through other post-filtering stages (AGC, and so on) before the output port is selected.

To access the output port registers for Output Ports A and B, Bit 5 of External Address 3 (the sleep register) must be written logic high. The channel address register (CAR) is then written with the address to the correct output port register. See Table 29 for a complete listing and brief description of all registers.

0x00–0x07: Reserved

Reserved. All bits should be written logic low.

0x08: LHB A Control Register

LHB is the acronym for interpolating half-band, with L being a widely accepted symbol for interpolation. This register includes the interleaving stage as well as the half-band filter stage, as shown in Figure 64. These two stages are controlled separately from the final AGC stage, so that they do not get lost among the numerous AGC control elements.

Bit 3, the LHB A enable bit, acts as an on/off switch for the interleave stage, half-band filter, and the AGC stage. See Figure 64. If Bit 3 is low, the interleave stage is shut down and prevents any further propagation of data to the remaining stages. This condition is desirable when the three stages are not needed and power conservation is desired. When Bit 3 is high, the interleave stage is active and works to interleave the data of up to four DDC channels according to the truth table of Bit 2 and Bit 1. The data is then propagated to the LHB and AGC stages with bypass opportunities included.

Bits 2 and 1 choose which channels are interleaved. The truth table for these bits is shown in Table 29.

Bit 0, the bypass bit, when high, directs data from the interleave stage to bypass the half-band filter stage and proceed directly to the AGC stage without interpolation. The channel data streams are still interleaved, but they are not filtered or interpolated. The maximum data rate from this configuration is two times the chip rate.

When Bit 0 is low, data from the interleave stage is passed through the half-band filter and undergoes a 2× interpolation rate. The maximum output data rate of the half-band is four times the chip rate.

0x09: LHB B Control Register

Same as LHB A, except that only two channels can be interleaved. Channels are selected using only Bit 1; Bit 2 is the LHB B enable bit.

0x0A: AGC A Control Register

Bits 7–5 define the output word length of the AGC. The output word can be 4 to 8, 10, 12, or 16 bits wide. The truth table to obtain different output word lengths is given in the Table 29 memory map, 0x0A.

Bit 4 of this register sets the mode of operation for the AGC. When this bit is 0, the AGC tracks to maintain the output signal level; when this bit is 1, the AGC tracks to maintain a constant clipping error. See the Automatic Gain Control section for details about these two modes.

Bits 3–1 are used to configure the synchronization of the AGC. The CIC decimator filter in the AGC can be directly synchronized to an externally generated signal. When synchronized, the AGC outputs an update sample for the AGC error calculation and filtering. This way, the AGC gain changes can be synchronized to a Rake receiver.

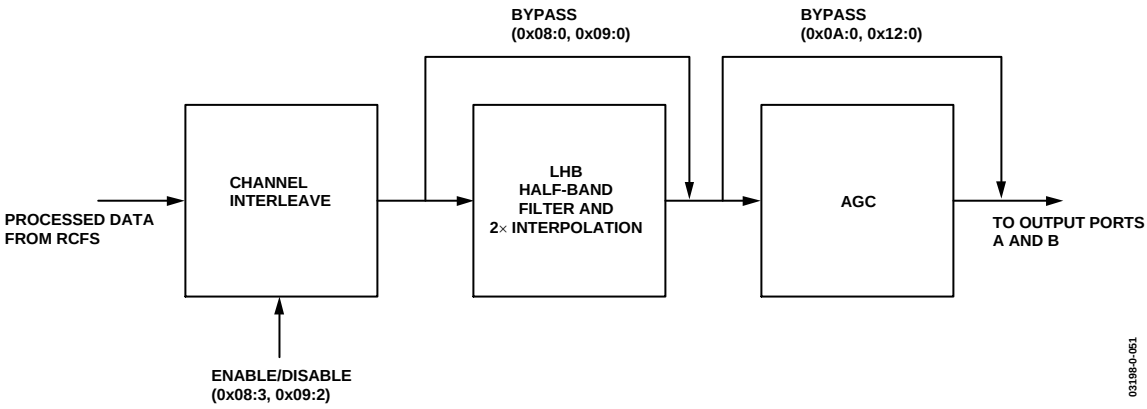


Figure 64. Block Diagram of an AGC Stage Showing the Components and Signal Routing Options

Note: The hold-off counter of AGC A shares the PIN SYNC assigned to DDC processing Channel 0. Therefore, if the user intends to use the AGC A's hold-off counter, the user must attach the external sync signal to the pin sync that is assigned to DDC Channel 0. The hold-off counter register at Address 0x0B for AGC A must be programmed with a 16-bit number that corresponds to the desired delay before a new CIC decimated value is updated. Writing a logic high to the proper pin sync pin triggers the AGC hold-off counter with a retriggerable one-shot pulse every time the pin is written high.

Bit 3 is the sync now bit. If the user chooses not to use pin sync signals, the user can use the *Sync Now* command by programming this bit high. This performs an immediate start of decimation for a new update sample and initializes the AGC, if Bit 2 is set. This bit has a one-shot characteristic and does not need to be reset in order to respond to a new logic high being written to it. Use of the sync now bit bypasses the AGC hold-off counters; therefore, the name *Sync Now*.

Bit 2 is used to determine whether the AGC should initialize on a *Sync Now* or not. When this bit is set, the CIC filter is cleared and new values for CIC decimation, number of averaging samples, CIC scale, signal gain Gs, gain K, and pole parameter P are loaded. When Bit 2 = 0, the above-mentioned parameters are not updated and the CIC filter is not cleared. In both cases, an AGC update sample is output from the CIC filter and the decimator starts operating towards the next output sample whenever a *Sync Now* occurs.

Bit 1 is used to ignore repetitive Pin_Sync signals. In some applications, the synchronization signal might occur periodically. If this bit is clear, each Pin_Sync resynchronizes the AGC. If this bit is set, only the first sync high is recognized and succeeding sync events are ignored until Bit 1 is reset.

Bit 0 is used to bypass the AGC section, when it is set. The data from the interpolating half-band filters is still reduced to a lower bit width representation as set by Bits 7–5 of the AGC A control register. A truncation at the output of the AGC accomplishes this task.

0x0B: AGC A Hold-Off Counter

The AGC A hold-off counter is loaded with the 16-bit value written to this address when *Sync Now* is written high or a Pin_Sync is received. If this register is written to a 0, the AGC cannot be synchronized.

Note: The hold-off counter of AGC A shares the pin sync assigned to DDC processing Channel 0. Therefore, if the user intends to use AGC A's hold-off counter, the user must either attach the external sync signal to the pin sync that is assigned to DDC Channel 0 or use the software-controlled *Sync Now* function of Bit 3 at 0x0A.

The hold-off counter must be programmed with a 16-bit number that corresponds to the desired delay before a new CIC decimated value is updated. Writing a logic high to the proper pin sync pin triggers the AGC hold-off counter with a retriggerable one-shot pulse every time the pin is written high.

0x0C: AGC A Desired Level

This 8-bit register contains the desired output power level or desired clipping level, depending on the mode of operation. This desired request R level can be set in dB from 0 to −23.99 dB, in steps of 0.094 dB. An 8-bit binary floating-point representation is used with a 2-bit exponent followed by the 6-bit mantissa. The mantissa is in steps of 0.094 dB and the exponent is in 6.02 dB steps. For example: 10'100101 represents $2 \times 6.02 + 37 \times 0.094 = 15.518$ dB.

0x0D: AGC A Signal Gain

This register is used to set the initial value for a signal gain used in the gain multiplier. This 12-bit value sets the initial signal gain between 0 and 96.296 dB in steps of 0.024 dB. A 12-bit binary floating-point representation is used with a 4-bit exponent followed by the 8-bit mantissa. For example: 0111'10001001 represents $7 \times 6.02 + 137 \times 0.024 = 45.428$ dB.

Table 29. Memory Map for Output Port Control Registers

Address	Register	Bit Width	Comments
08	LHB A Control Register	4	3: LHB A enable[1] 2–1: LHB A signal interleaving 11 All 4 channels 10 Channels 0, 1, 2 01 Channels 0, 1 00 Channel 0 0: Bypass LHB A[1]
09	LHB B Control Register	3	2: LHB B enable[1] 1: LHB B signal interleaving 1: Channels 2, 3 0: Channel 2 0: Bypass LHB B[1]
0A	AGC A Control Register	8	7–5: Output word length 111 4 bits 110 5 bits 101 6 bits 100 7 bits 011 8 bits 010 10 bits 001 12 bits 000 16 bits 4: Clipping error 1: Maintain level of clipping error 0: Maintain output signal level 3: Sync now 2: Init on sync 1: First sync only 0: Bypass
0B	AGC A Hold-Off Counter	16	15–0: Hold-off value
0C	AGC A Desired Level	8	7–0: Desired output power level or clipping energy (R parameter)
0D	AGC A Signal Gain	12	11–0: Gs parameter
0E	AGC A Loop Gain	8	7–0: K parameter
0F	AGC A Pole Location	8	7–-0: P parameter
10	AGC A Average Samples	6	5–2: Scale for CIC decimator 1–0: Number of averaging samples
11	AGC A Update Decimation	12	11–0: CIC decimation ratio
12	AGC B Control Register	8	7–5: Output word length 111 4 bits 110 5 bits 101 6 bits 100 7 bits 011 8 bits 010 10 bits 001 12 bits 000 16 bits 4: Clipping error 1: Maintain level of clipping error 0: Maintain output signal level

Address	Register	Bit Width	Comments
			3: Sync now 2: Init on Sync 1: First sync only
			0: Bypass
13	AGC B Hold-Off Counter	16	15–0: Hold-off value
14	AGC B Desired Level	8	7–0: Desired output power level or clipping energy (R parameter)
15	AGC B Signal Gain	12	11–0: Gs parameter
16	AGC B Loop Gain	8	7–0: K parameter
17	AGC B Pole Location	8	7–0: P parameter
18	AGC B Average Samples	6	5–2: Scale for CIC decimator 1–0: Number of averaging samples
19	AGC B Update Decimation	12	11–0: CIC decimation
1A	Parallel A Control	8	7–6: Reserved 5: Parallel port data format 1: 8-bit parallel I, Q 0: 16-bit interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1/AGC B enable 1: Channel 0/AGC A enable 0: AGC_CH select 1: Data comes from AGCs 0: Data comes from channels
1B	Link A Control	8	7: Link Port A enable 6–3: Wait 2: No RSSI word 1: Don't output RSSI word 0: Output RSSI word 1: Channel data interleaved 1: 2-channel mode/separate AB 0: 4-channel mode/AB same port 0: AGC_CH select 1: Data comes from AGCs 0: Data comes from channels
1C	Parallel B Control	8	7–6: Reserved 5: Parallel port data format 1: 8-bit parallel I, Q 0: 16-bit interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1/AGC B enable 1: Channel 0/AGC A enable 0: AGC_CH select 1: Data comes from AGCs 0: Data comes from channels
1D	Link B Control	8	7: Link Port B enable 6–3: Wait 2: No RSSI word 1: Do not output RSSI word 0: Output RSSI word

Address	Register	Bit Width	Comments
			1: Channel data interleaved 1: 2-channel mode/separate AB 0: 4-channel mode/AB same port 0: AGC_CH select 1: Data comes from AGCs 0: Data comes from channels
1E	Port Clock Control	3	2–1: PCLK divisor 0: PCLK master/slave[2] 0: Slave 1: Master

[1] Set the LHB A and/or LHB B enable bits to logic low only when the entire block functions (LHB signal interleaving, LHB filtering, and AGC functions) are to be shut down.
[2] PCLK boots as a slave.

0x0E: AGC A Loop Gain

This 8-bit register defines the open loop gain K. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of K is updated in the AGC loop each time the AGC is initialized.

0x0F: AGC A Pole Location

This 8-bit register defines the open loop filter pole location P. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of P is updated in the AGC loop each time the AGC is initialized. This open loop pole location directly impacts the closed loop pole locations. See the Automatic Gain Control section.

0x10: AGC A Average Samples

This 6-bit register contains the scale used for the CIC filter and the number of power samples to be averaged before being fed to the CIC filter.

Bits 5–2 define the scale used for the CIC filter.

Bits 1–0 define the number of samples to be averaged before they are sent to the CIC decimating filter. This number can be set between 1 and 4 with 00 meaning one sample and 11 meaning four samples.

0x11: AGC A Update Decimation

This 12-bit register sets the AGC decimation ratio from 1 to 4096. Set an appropriate scaling factor to avoid loss of bits.

0x12: AGC B Control Register

Bits 7–5 define the output word length of the AGC. The output word can be 4 to 8, 10, 12, or 16 bits wide. The control register bit representation to obtain different output word lengths is given in Table 29.

Bit 4 of this register sets the mode of operation for the AGC. When this bit is 0, the AGC tracks to maintain the output signal level; when this bit is 1, the AGC tracks to maintain a constant clipping error. See the Automatic Gain Control section for details about these two modes.

Bits 3–1 are used to configure the synchronization of the AGC. The CIC decimator filter in the AGC can be indirectly synchronized to an externally generated signal. When synchronized, the AGC outputs an update sample for the AGC error calculation and filtering. This way, the AGC gain changes can be synchronized to a Rake receiver or other external block.

Note: The hold-off counter of AGC B shares the pin sync assigned to DDC processing Channel 2. Therefore, if the user intends to use the AGC B's hold-off counter, the user must attach the external sync signal to the pin sync that will be assigned to DDC Channel 2. The hold-off counter must be programmed with a 16-bit number that corresponds to the desired delay before a new CIC decimated value is updated. Writing a logic high to the proper pin sync pin triggers the AGC hold-off counter with a retriggerable one-shot pulse every time the pin is written high.

Bit 3 is the sync now bit. If the user chooses not to use pin sync signals, the user can use the *Sync Now* command by programming this bit high. This performs an immediate start of decimation for a new update sample and initializes the AGC, if Bit 2 is set. This bit has a one-shot characteristic and does not need to be reset in order to respond to a new logic high being written to it. Use of the sync now bit bypasses the AGC hold-off counters; therefore, the name *Sync Now*.

Bit 2 is used to determine whether the AGC should initialize on a *Sync Now* or not. When this bit is set, the CIC filter is cleared and new values for CIC decimation, number of averaging samples, CIC scale, signal gain Gs, gain K, and pole parameter P are loaded. When Bit 2 = 0, the above-mentioned parameters are not updated and the CIC filter is not cleared. In both cases, an AGC update sample is output from the CIC filter and the decimator starts operating towards the next output sample whenever a *Sync Now* occurs.

Bit 1 is used to ignore repetitive Pin_Sync signals. In some applications, the synchronization signal might occur periodically. If this bit is clear, each Pin_Sync resynchronizes the AGC.

If this bit is set, only the first sync high is recognized and succeeding sync events are ignored until Bit 1 is reset.

Bit 0 is used to bypass the AGC section, when it is set. When the AGC is bypassed, the output data is the 16 MSBs of the 24-bit input data from the half-band filter.

0x13: AGC B Hold-Off Counter

The AGC B hold-off counter is loaded with the 16-bit value written to this address when *Sync Now* is written high or a Pin_Sync signal is received. If this register is written to 0, the AGC cannot be synchronized.

Note: The hold-off counter of AGC B shares the pin sync assigned to DDC processing Channel 2. Therefore, if the user intends to use AGC A's hold-off counter, the user must either attach the external sync signal to the pin sync that is assigned to DDC Channel 2, or use the software-controlled sync now function of Bit 3 at 0x12.

The hold-off counter must be programmed with a 16-bit number that corresponds to the desired delay before a new CIC decimated value is updated. Writing a logic high to the proper pin sync pin triggers the AGC hold-off counter with a retriggerable one-shot pulse every time the pin is written high.

0x14: AGC B Desired Level

This 8-bit register contains the desired output power level or desired clipping level, depending on the mode of operation. This desired request R level can be set from 0 dB to −23.99 dB in steps of 0.094 dB. An 8-bit binary floating-point representation is used with a 2-bit exponent followed by the 6-bit mantissa. The mantissa is in steps of 0.094 dB and the exponent is in 6.02 dB steps. For example: 10'100101 represents 2 × 6.02 + 37 × 0.094 = 15.518 dB.

0x15: AGC B Signal Gain

This register is used to set the initial value for a signal gain used in the gain multiplier. This 12-bit value sets the initial signal gain between 0 dB and 96.296 dB in steps of 0.024 dB. A 12-bit binary floating-point representation is used with a 4-bit exponent followed by the 8-bit mantissa. For example: 0111'10001001 represents 7 × 6.02 + 137 × 0.024 = 45.428 dB.

0x16: AGC B Loop Gain

This 8-bit register is used to define the open loop gain K. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of K is updated in the AGC loop each time the AGC is initialized.

0x17: AGC B Pole Location

This 8-bit register is used to define the open loop filter pole location P. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of P is updated in the AGC loop each time the AGC is initialized. This open loop pole location directly impacts the closed loop pole locations as explained in the Automatic Gain Control section.

0x18: AGC B Average Samples

This 6-bit register contains the scale used for the CIC filter and the number of power samples to be averaged before being fed to the CIC filter.

Bits 5–2 define the scale used for the CIC filter.

Bits 1–0 define the number of samples to be averaged before they are sent to the CIC decimating filter. This number can be set between 1 and 4 with bit representation 00 meaning one sample and bit representation 11 meaning four samples.

0x19: AGC B Update Decimation

This 12-bit register sets the AGC decimation ratio from 1 to 4096. Set an appropriate scaling factor to avoid loss of bits.

0x1A: Parallel Port Control A

Data is output through either a parallel port interface or a link port interface. When 0x1B, Bit 7 = 0, the use of Link Port A is disabled and the use of Parallel Port A is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on Parallel Port A. When Bit 0 = 0, Parallel Port A outputs data from the RCF according to the format specified by Bits 1–4. When Bit 0 = 1, Parallel Port A outputs the data from the AGCs according to the format specified by Bits 1 and 2.

In AGC mode, Bit 0 = 1 and Bit 1 determines if Parallel Port A can output data from AGC A. Bit 2 determines if Parallel Port A can output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, Bit 0 = 0 and Bits 1–4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data words. When Bit 5 = 0, Parallel Port A outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved, and the IQ indicator pin determines whether data on the port is I data or Q data. When Bit 5 = 1, Parallel Port A is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins are high.

0x1B: Link Port Control A

Data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6652 and a TigerSHARC DSP and can be enabled by setting 0x1D, Bit 7 = 1.

Bit 0 selects which data is output on Link Port A. When Bit 0 = 0, Link Port A outputs data from the RCF according to the format specified by Bit 1. When Bit 0 = 1, Link Port A outputs the data from the AGCs according to the format specified by Bits 1 and 2.

Bit 1 has two different meanings, depending on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (Bit 0 = 0), Bit 1 selects between two and four channel data mode. Bit 1 = 1 indicates that Link Port A transmits RCF IQ words alternately from Channels 0 and 1. When Bit 1 = 1, Link Port A outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, 3. However, when AGC data is selected (Bit 0 = 1), Bit 1 selects the AGC data output mode. In this mode, when Bit 1 = 1, Link Port A outputs AGC A IQ and gain words. With this mode, gain words must be included by setting Bit 2 = 0. However, if Bit 0 = Bit 1 = 0, then AGC A and AGC B are alternately output on Link Port A and the inclusion or exclusion of the gain words is determined by Bit 2.

Bit 2 determines if RSSI words are included or not in the data output. If Bit 1 = 1, Bit 2 = 0. Because the RSSI words are only two bytes long and the IQ words are four bytes long, the RSSI words are padded with zeros to give a full 16-byte TigerSHARC quad-word. If AGC output is not selected (Bit 0 = 0), then this bit can be any value.

Bits 6–3 specify the programmable delay value for Link Port A between the time the link port receives a data ready from the receiver and the time it transmits the first data-word. The link port must wait at least 6 cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6652 link port and the TigerSHARC link port. For details on the limitations and relationship of these clocks, see the Link Port section.

0x1C: Parallel Port Control B

Data is output through either a parallel port interface or a link port interface. When 0x1D, Bit 7 = 0, the use of Link Port B is disabled and the use of Parallel Port B is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on Parallel Port B. When Bit 0 = 0, Parallel Port B outputs data from the RCF according to the format specified by Bits 1–4. When Bit 0 = 1, Parallel Port B outputs the data from the AGCs according to the format specified by Bits 1 and 2.

In AGC mode, Bit 0 = 1 and Bit 1 determines if Parallel Port B is able to output data from AGC A. Bit 2 determines if Parallel Port B is able to output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, Bit 0 = 0 and Bits 1–4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data words. When Bit 5 = 0, Parallel Port B outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved and the IQ indicator pin determines whether data on the port is I data or Q data. When Bit 5 = 1, Parallel Port B is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins are high.

0x1D: Link Port Control B

Data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6652 and a TigerSHARC DSP and can be enabled by setting 0x1D, Bit 7 = 1.

Bit 0 selects which data is output on Link Port B. When Bit 0 = 0, Link Port B outputs data from the RCF according to the format specified by Bit 1. When Bit 0 = 1, Link Port B outputs the data from the AGCs according to the format specified by Bits 1 and 2.

Bit 1 has two different meanings that depend on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (Bit 0 = 0), Bit 1 selects between two and four channel data mode. Bit 1 = 1 indicates that Link Port A transmits RCF IQ words alternately from Channels 0 and 1. When Bit 1 = 1, Link Port B outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, 3. However, when AGC data is selected (Bit 0 = 1), Bit 1 selects the AGC data output mode. In this mode, when Bit 1 = 1, Link Port B outputs AGC B IQ and gain words. With this mode, gain words must be included by setting Bit 2 = 0. However, if Bit 0 = Bit 1 = 0, then AGC A and B are alternately output on Link Port B and the inclusion or exclusion of the gain words is determined by Bit 2.

Bit 2 determines whether gain words are included in the data output. If Bit 1 = 1, Bit 2 = 0. Because the gain words are only two bytes long and the IQ words are four bytes long, the gain words are padded with zeros to give a full 16-byte TigerSHARC quad-word. If AGC output is not selected (Bit 0 = 0), then this bit can be any value.

Bits 6–3 specify the programmable delay value for Link Port B between the time the link port receives a data ready from the receiver and the time it transmits the first data-word. The link port must wait at least six cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6652 link port and the TigerSHARC link port. For details on the limitations and relationship of these clocks, see the Link Port section.

0x1E: Port Clock Control

Bit 0 determines whether PCLK is supplied externally by the user or derived internally in the AD6652. If PCLK is derived internally from CLK (Bit 0 = 1), it is output through the PCLK pin as a master clock. For most applications, PCLK is provided by the user as an input to the AD6652 via the PCLK pin.

Bits 2 and 1 allow the user to divide CLK by an integer value to generate PCLK (00 = 1, 01 = 2, 10 = 4, 11 = 8).

MICROPORT CONTROL

The AD6652 has an 8-bit microprocessor port or *microport*. The microport interface is a multimode interface that is designed to give flexibility when dealing with the host processor. There are two modes of bus operation: Intel nonmultiplexed mode (INM), and Motorola nonmultiplexed mode (MNM). The mode is selected based on the host processor and which mode is best suited to that processor. The microport has an 8-bit data bus (D[7:0]), 3-bit address bus (A[2:0]), 3 control pin lines ($\overline{CS}$, $\overline{DS}$, or $\overline{RD}$, R/$\overline{W}$ or $\overline{WR}$), and one status pin ($\overline{DTACK}$ or RDY). The functionality of the control signals and status line changes slightly depending upon the mode that is chosen.

Write Sequencing

Writing to an internal location is achieved by first writing the upper two bits of the address to Bits 1–0 of the ACR (Access Control Register, External Address 7). Bits 7:2 can be set to select the channel, as indicated above. The CAR is then written with the lower eight bits of the internal address (the CAR can be written before the ACR, as long as both are written before the internal access). Data Register 2 (DR2) and Data Register 1 (DR1) must be written first, because the write to Data Register DR0 triggers the internal access. Data Register DR0 must always be the last register written to initiate the internal write.

Read Sequencing

Reading from the microport is accomplished in the same manner. The internal address is set up the same way as the write. A read from Data Register DR0 activates the internal read; thus, Register DR0 must always be read first to initiate an internal read followed by DR1and DR2. This provides the 8 LSBs of the internal read through the microport (D[7:0]). Additional data registers can be read to read the balance of the internal memory.

Read/Write Chaining

The microport of the AD6652 allows for multiple accesses while $\overline{CS}$ is held low. ($\overline{CS}$ can be tied permanently low, if the microport is not shared with additional devices.) The user can access multiple locations by pulsing the $\overline{WR}$ or $\overline{RD}$ line and changing the contents of the external 3-bit address bus. External access to the external registers of Table 22 is accomplished in one of two modes using the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and MODE inputs. The access modes are Intel nonmultiplexed mode and Motorola nonmultiplexed mode. These modes are controlled by the MODE input (MODE = 0 for INM, MODE = 1 for MNM). $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control the access type for each mode.

Intel Nonmultiplexed Mode (INM)

MODE must be tied low to operate the AD6652 microprocessor in INM mode. The access type is controlled by the user with the $\overline{CS}$, $\overline{RD}$ ($\overline{DS}$), and $\overline{WR}$ (R/$\overline{W}$) inputs. The RDY ($\overline{DTACK}$) signal is produced by the microport to communicate to the user that an access has been completed. RDY ($\overline{DTACK}$) goes low at the start of the access and is released when the internal cycle is complete. See the timing diagrams for both the read and write modes in the DDC Timing Diagrams section.

Motorola Nonmultiplexed Mode (MNM)

MODE must be tied high to operate the AD6652 microprocessor in MNM mode. The access type is controlled by the user with the $\overline{CS}$, $\overline{DS}$ ($\overline{RD}$), and R/$\overline{W}$ ($\overline{WR}$) inputs. The $\overline{DTACK}$ (RDY) signal is produced by the microport to communicate to the user that an access has been completed. $\overline{DTACK}$ (RDY) goes low when an internal access is complete and then returns high after $\overline{DS}$ ($\overline{RD}$) is deasserted. See the timing diagrams for both the read and write modes in the DDC Timing Diagrams section.

Microport Programming Overview

The AD6652 uses an indirect addressing scheme. The external memory map (or external registers) is used to access the internal memory maps that are made up of a channel memory map and an output port memory map. The 4-channel memory pages are decoded using A[9:8] given in the External Memory Register 7 of the access control register (ACR). The output port register memory map is selected using Bit 5 of External Address 3 (sleep register). When this bit is written with a 0, the channel memory map is selected; when this bit is 1, the output port memory map is selected.

Internal Write Access

Up to 20 bits of data (as needed) can be written by the following process. Any high order bytes that are needed are written to the corresponding data registers defined in the external memory map 3-bit address space. The least significant byte is then written to DR0 at Address (000). When a write to DR0 is detected, the internal microprocessor port state machine then moves the data in DR2–DR0 to the internal address pointed to by the address in the channel address register (CAR) and access control register (ACR).

```
Write Pseudocode
void write_micro(ext_address, int data);
main();

{
/* This code shows the programming of the NCO
phase offset register using the write_micro
function as defined above. The variable address is
the External Address A[2:0] and data is the value
to be placed in the external interface register.
Internal Address = 0x087
 */
// holding registers for NCO phase byte wide
access data
int d1, d0;
// NCO frequency word (16 bits wide)
NCO_PHASE = 0xCBEF;
// write ACR
write_micro(7, 0x03 );
// write CAR
write_micro(6, 0x87);
// write DR1 with D[15:8]
d1 = (NCO_PHASE & 0xFF00) >> 8;
write_micro(1, d1);
// write DR0 with D[7:0]
// On this write all data is transferred to the
internal address
d0 = NCO_FREQ & 0xFF;
write_micro(0, d0);
} // end of main
```

Internal Read Access

A read is performed by first writing the channel address register (CAR) and ACR as with a write. The data registers (DR2–DR0) are then read in the reverse order that they were written. First, the least significant byte of the data (D[7:0]) is read from DR0.

On this transaction, the high bytes of the data are moved from the internal address pointed to by the CAR and ACR into the remaining data registers (DR2–DR1). This data can then be read from the data registers using the appropriate 3-bit addresses. The number of data registers used depends solely on the amount of data to be read or written. Any unused bit in a data register should be masked out for a read.

```
Read Pseudocode
int read_micro(ext_address);

main();
{
/* This code shows the reading of the first RCF
coefficient using the read_micro function as
defined above. The variable address is the
External Address A[2..0].
Internal Address = 0x000
 */
// holding registers for the coefficient
int d2, d1, d0;
// coefficient (20-bits wide)
long coefficient;
// write ACR
write_micro(7, 0x00 );
// write CAR
write_micro(6, 0x00);
/* read D[7:0] from DR0, All data is moved from
the internal registers to the interface registers
on this access */
d0 = read_micro(0) & 0xFF;
// read D[15:8] from DR1
d1 = read_micro(1) & 0xFF;
// read D[23:16] from DR2
d2 = read_micro(2) & 0x0F;
coefficient = d0 + (d1 << 8) + (d2 << 16);
} // end of main
```

APPLICATIONS

AD6652 RECEIVER APPLICATIONS

One CDMA2000 IF Carrier with No External Analog Filtering

Code Division Multiple Access depends upon a unique code sequence that modulates the IF carrier along with the payload data. This permits multiple signals to be transmitted on the same carrier frequency and successfully separated at the receiver. This technique spreads the spectrum of the initial digital bit stream over a much wider bandwidth. The wideband nature and stringent adjacent channel-filtering requirements of CDMA2000 allow the AD6652 to process only one CDMA2000 channel. To do this requires the processing power of all four channels operating at maximum speed.

Two CDMA2000 IF Carriers with External Analog Saw Filtering

If two CDMA2000 carriers are to be processed by the AD6652, prefiltering of the analog signal(s) going to the AD6652 is required. Surface acoustic wave (SAW) filters are commonly used to reduce the digital signal processing required of the AD6652 filters. This combination permits adequate reduction of the adjacent channel interference as specified for that medium and permits two CDMA2000 carriers to be processed using only two DDC channels per carrier.

Two UMTS or WCDMA IF Carriers with No External Analog Saw Filtering

Due to less stringent filter requirements of wideband CDMA and UMTS, the AD6652 can receive two WCDMA carriers using the processing power of two channels for each carrier without the use of external analog filters.

Baseband I and Q Processor

This application calls for baseband I and Q analog signals to be routed individually to the two AD6652 ADC inputs. The 12-bit ADCs digitize the signals and send the data to all four receive processing channels for decimation and filtering. Therefore, each channel is processing the same 12 bits of I data and 12 bits of Q data simultaneously. The user can shut down unused channels as desired.

Processing baseband I and Q data requires that each active channel's NCO and quadrature mixer be bypassed by programming of the NCO control registers.

DESIGN GUIDELINES

When designing the AD6652 into a system, it is recommended that, before starting design and layout, the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements required for certain pins.

1. The following power-up sequence is recommended for the AD6652. First, ensure that $\overline{\text{RESET}}$ is held logic low. Apply AVDD (3.0 V) and VDD (2.5 V), allowing them both to settle to nominal values before applying VDDIO (3.3 V). Once VDDIO (3.3 V) has settled to nominal value, bring $\overline{\text{RESET}}$ logic high. Last, apply a logic low $\overline{\text{RESET}}$ pulse for 30 ns to reset the AD6652 into a known state ready for programming.

2. $\overline{\text{RESET}}$ pin: The $\overline{\text{RESET}}$ pin must be held logic low during power-up sequencing to ensure that the internal logic starts in a known state. Certain registers, noted in the datasheet, are cleared after hardware reset. Failure to ensure hardware reset during power-up might result in invalid output until a valid reset is applied.

3. The number format used in this part is twos complement. All input ports and output ports use twos complement data format. The formats for individual internal registers are given in the memory map description of these registers.

4. To enhance microport programming, the $\overline{\text{DTACK}}$ (RDY) pin should be pulled high (to VDDIO) externally using a pull-up resister. The recommended value for the pull-up resistor is between 1 kΩ and 5 kΩ.

5. $\overline{\text{CS}}$ pin is used as chip select for programming with the microport. It is recommended that the designer not tie this pin low at all times. This pin should ideally be pulled high using a pull-up resistor, and the user can pull it low whenever microport control is required.

6. The output parallel port has one clock cycle overhead for every output sample. So, if data from two AGCs with the same data rate are output on one output port in 16-bit interleaved I/Q mode along with the AGC word, then four clock cycles are required for one sample from each channel/AGC: one blank clock cycle, and one clock cycle each for I data, Q data, and gain data.

7. Serial port control and serial data output are not available on this part.
8. Broadcast and programming multiple AD6652 parts using the same microport control/data signals does not work for input/output port control registers (Addresses 0x00 to 0x1E). If two AD6652 parts have different values for input/output control registers, they cannot share the microport bus (see the Microport Control section).
9. To optimize ADC performance, decouple any system-induced noise from the sensitive ADC reference nodes. Place the 0.010 μF, 0.1 μF, and 10 μF external decoupling capacitors as close as possible to the AD6652 device's VREF, REFTA/REFBA, and REFTB/REFBB pins. See the ADC Voltage Reference section of the data sheet and the evaluation board schematics, which are available on the AD6652 product page at www.analog.com.

AD6652 EVALUATION BOARD AND SOFTWARE

The AD6652 evaluation board kit contains a fully populated AD6652 PCB, schematic diagrams, operating software, comprehensive instruction manual, and digital filter design software.

Users can preview the evaluation board schematic, the software, and the instruction manual on the product Web page of the Analog Devices website. A block diagram of the basic components is shown in Figure 65.

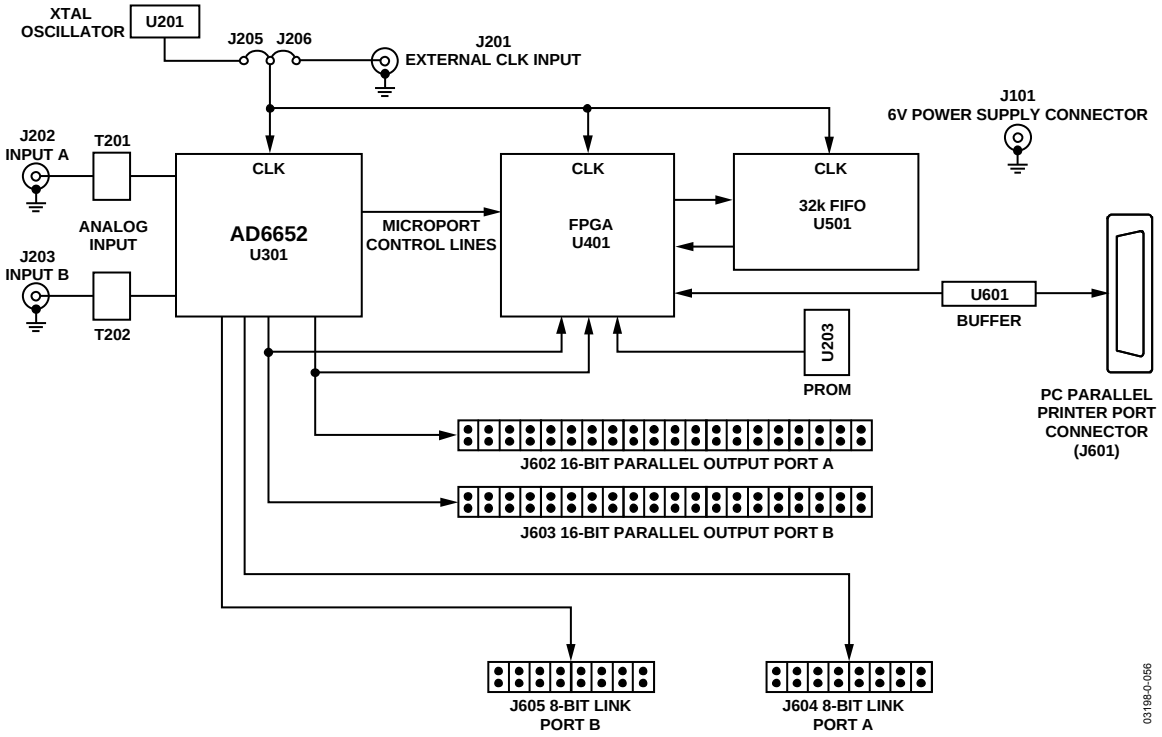


Figure 65. Simplified Block Diagram of AD6652 PCB

OUTLINE DIMENSIONS

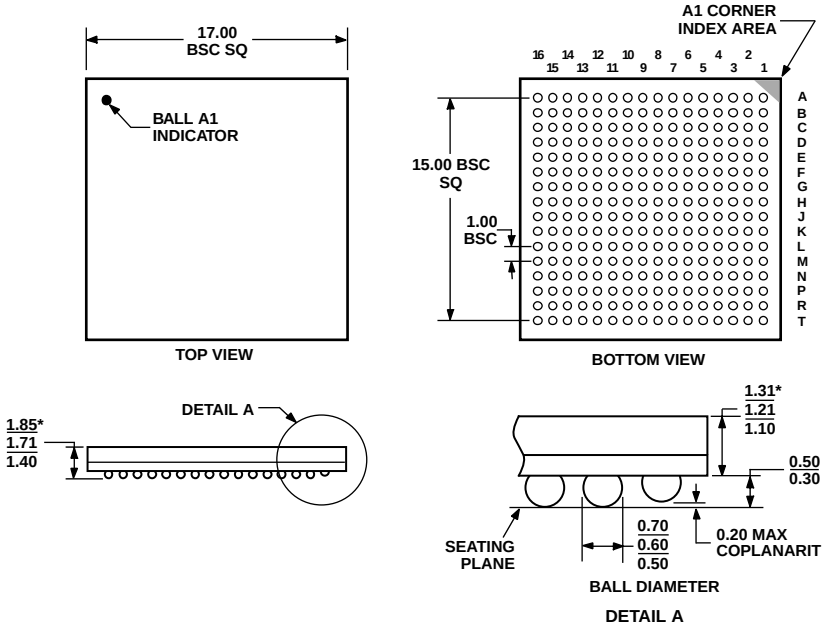


Figure 66. 256-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-256-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6652BBC	−40°C to +85°C	256-Lead CSPBGA (Chip Scale Ball Grid Array)	BC-256-2
AD6652BC/PCB		Evaluation Board with AD6652 and Software	

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