SAM L10/L11 Family

Silicon Errata and Data Sheet Clarification

SAM L10/L11 Family

The SAM L10/L11 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001513D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Silicon Issue Summary.

The errata described in this document will be addressed in future revisions of the SAM L10/L11 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 3. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM L10 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML10E16A	0x2084xx00	0x1
SAML10E15A	0x2084xx01	
SAML10E14A	0x2084xx02	
SAML10D16A	0x2084xx03	
SAML10D15A	0x2084xx04	
SAML10D14A	0x2084xx05	

Table 2. SAM L11 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML11E16A	0x2083xx00	0x1
SAML11E15A	0x2083xx01	
SAML11E14A	0x2083xx02	
SAML11D16A	0x2083xx03	
SAML11D15A	0x2083xx04	
SAML11D14A	0x2083xx05	

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001513D) for detailed information on Device Identification and Revision IDs for your specific device.

Table of Contents

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
ADC	Reference Buffer Offset Compensation	2.1.1	First ADC conversions are incorrect when using Reference Buffer Offset Compensation.	SAM L10	X
				SAM L11	X
CCL	PAC protection	2.2.1	Writing the Software Reset bit in the Control A register will trigger a PAC protection error.	SAM L10	X
				SAM L11	X
CCL	Enable-protected Registers	2.2.2	The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit.	SAM L10	X
				SAM L11	X
CCL	Sequential logic	2.2.3	LUT Output is corrupted after enabling CCL when sequential logic is used.	SAM L10	X
				SAM L11	X
Device	Temperature sensor	2.3.1	Temperature sensor is not functional.	SAM L10	X
				SAM L11	X
DMAC	Linked descriptors	2.4.1	When using concurrent channel triggers, DMA write-back descriptors may get corrupted.	SAM L10	X
				SAM L11	X
EIC	PAC protection	2.5.1	EIC reads/writes on the reserved area between the CONFIG and the DEBOUNCEN registers do not generate a PAC protection error.	SAM L10	X
				SAM L11	X
FREQM	PAC protection	2.6.1	FREQM reads on the Control B register generate a PAC protection error.	SAM L10	X
				SAM L11	X
MCLK	PAC protection	2.7.1	Writes to the MCLK Control A register do not generate a PAC protection error even if this register has been write-protected using the PAC.	SAM L10	X
				SAM L11	X
MCLK	DFLLULP clock	2.7.2	Hardfault exception after having selected DFLLULP clock as main clock.	SAM L10	X
				SAM L11	X
OPAMP	Reference buffer	2.8.1	The internal reference REFBUF is not generated when the voltage doubler is disabled.	SAM L10	X
				SAM L11	X
OPAMP	High Gain Instrumentation Amplifier	2.8.2	High Gain Instrumentation Amplifier is not functional.	SAM L10	X
				SAM L11	X
RTC	Tamper detection	2.9.1	Tamper detection limitation when CTRLB.SEPTO = 0.	SAM L10	X
				SAM L11	X
RTC	Event generation	2.9.2	Periodic Daily Event (PERD) Event Generator never occurs in Clock/Calendar mode.	SAM L10	X
				SAM L11	X
RTC	Write corruption	2.9.3	RTC COUNT and CLOCK registers write corruption.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection Timestamp	2.9.4	If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.	SAM L10	X
				SAM L11	X
RTC	Prescaler	2.9.5	When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER=0).	SAM L10	X
				SAM L11	X

.....continued

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
RTC	Active Layer Protection	2.9.6	Active Layer Protection feature is limited to one tamper channel n (i.e. one RTC INn/OUTn pair).	SAM L10	X
				SAM L11	X
RTC	Tamper Detection Timestamp	2.9.7	The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.	SAM L10	X
				SAM L11	X
RTC	Tamper Detection Timestamp	2.9.8	A wrong timestamp value can be returned if more than one CPU and DMA accesses to the TIMESTAMP register are performed upon a INTFLAG.TAMPER assertion.	SAM L10	X
				SAM L11	X
SERCOM I^2C	High-speed mode	2.10.1	When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated start	2.10.2	Bus error is generated during a Repeated Start (when QCEN = 1 and SCLSM = 1).	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / Master mode 10-bit	2.10.3	Repeated Start in 10-bit addressing mode for Master Write operations does not work.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / Master mode 10-bit	2.10.4	Repeated Start is not supported for High-Speed mode Master Read operations.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Repeated Start / High-Speed mode	2.10.5	Repeated Start is not supported for High-Speed mode Master Write operations.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Slave Mode with DMA	2.10.6	Character lost in I^2C Slave mode with DMA when a NACK occurs.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Slave mode 10-bit	2.10.7	I^2C Slave 10-bit addressing mode is not functional.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Status Flag	2.10.8	BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR Status register bits are not automatically cleared.	SAM L10	X
				SAM L11	X
SERCOM I^2C	Status Flag	2.10.9	The CLKHOLD Status bit is not read only.	SAM L10	X
				SAM L11	X
SERCOM SPI	Data Preload	2.11.1	Data lost in SPI Slave mode with Data Preload Enabled.	SAM L10	X
				SAM L11	X
SERCOM USART	Inverted Bits	2.12.1	The TXINV and RXINV bits in the CTRLA register have inverted functionality.	SAM L10	X
				SAM L11	X
SERCOM USART	ISO7816 Mode	2.12.2	In ISO7816 mode, the SERCOM bus clock continues to run in Stand-by Sleep mode causing an extra power consumption.	SAM L10	X
				SAM L11	X
SERCOM USART	Debug Mode	2.12.3	Debug mode is not functional.	SAM L10	X
				SAM L11	X
SERCOM USART	Collision Detection	2.12.4	Collision Detection does not stop Data Transfer.	SAM L10	X
				SAM L11	X
SERCOM USART	Wakeup	2.14.5	The USART does not wake up the device on Error (INTFLAG.ERROR=1) interrupt.	SAM L10	X
				SAM L11	X

.....continued

Module	Feature	Errata Number	Summary	Device	Affected Silicon Revisions
					B
TC	Flags Synchronization	2.13.1	The SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.	SAM L10	X
				SAM L11	X
TC	Capture mode / Over consumption	2.13.2	Over consumption in Capture mode when entering Standby mode.	SAM L10	X
				SAM L11	X
TRNG	Over consumption	2.14.1	When TRNG is disabled, some internal logic could continue to operate causing an over consumption.	SAM L10	X
				SAM L11	X
SUPC	Buck Converter Mode	2.15.1	Digital Phase-Locked Loop FDPLL96M cannot be used with main voltage regulator in Buck Converter mode.	SAM L10	X
				SAM L11	X
OSC32KCTRL	External 32.768KHz Crystal Oscillator	2.16.1	External 32.768KHz crystal oscillator operation is not supported over the full temperature range of -40°C to +125°C.	SAM L10	X
				SAM L11	X
Boot ROM	GCM API	2.17.1	GCM API does not follow the Procedure Call Standard for the ARM Architecture (AAPCS)	SAM L10	
				SAM L11	X

2. SAM L10/L11 Errata Issues

The following issues apply to the SAM L10/L11 Family devices.

2.1 ADC

2.1.1 Reference Buffer Offset Compensation Reference:CHIP003-247

TUE of the ADC conversion result is out of specification when,

- Using the reference source as REFCTRL.REFSEL ≠ VDDANA
  and
- Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1)

Workaround

The first five conversions after enabling ADC must be ignored. All further ADC conversions are within the specification.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2 Configurable Custom Logic (CCL)

2.2.1 PAC Protection Reference: CLA100-6

Writing the Software Reset bit in the Control A register (CTRLA.SWRST) will trigger a PAC protection error.

Workaround

Clear the CCL PAC error each time a CCL software reset is executed.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.2 Enable Protected Registers Reference: CLA100-33

The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit whereas they should be enable-protected by the LUTCTRL0/1.ENABLE bits.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.3 Sequential Logic Reference: CLA100-32

LUT Output is corrupted after enabling CCL when sequential logic is used.

Workaround
Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.3 DEVICE

2.3.1 Temperature Sensor Reference: CHIP003-299

Temperature Sensor is not functional.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.4 Direct Memory Access Controller (DMAC)

2.4.1 Linked Descriptors Reference: DMA100-17

When using concurrent channels triggers, DMAC write-back descriptors may get corrupted.

Workaround
Multiple transfers must only be sequenced using linked descriptors on a single channel.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.5 External Interrupt Controller (EIC)

2.5.1 PAC Protection Reference: INT103-3

EIC reads/writes on the reserved area between the CONFIG and the DEBOUNCEN registers do not generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.6 Frequency Meter (FREQM)

2.6.1 PAC Protection Reference: CLK101-9

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7 Main Clock (MCLK)

2.7.1 PAC Protection Reference: CLK107-7

Writes to the MCLK Control A register (MCLK.CTRLA) do not generate a PAC protection error even if this register has been write-protected using the PAC.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7.2 DFLLULP Clock Reference: CLK107-8

A Hard fault exception can occur after selecting the DFLLULP clock as main clock source (CTRLA.CKSEL = 1).

Workaround
Add 6 NOP instructions after writing the CTRAL.CKSEL bit.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.8 Operational Amplifier Controller (OPAMP)

2.8.1 Reference Buffer Reference: OPAMP100-4

The internal reference REFBUF is not generated when the voltage doubler is disabled (CTRLA.LPMUX = 1).

Workaround
Enable the voltage doubler (CTRLA.LPMUX = 0) when the internal REFBUF is used.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						

.....continued

Device Family	B						
SAM L11	X						

2.8.2 High Gain Instrumentation Amplifier Reference: OPAMP100-7

High Gain Instrumentation Amplifier is not functional.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9 RTC

2.9.1 Tamper Detection Reference: TMR102-44

When the RTC Separate Tamper Outputs (SEPTO) bit of the CTRLB register is cleared (CTRLB.SEPTO=0) and the Active layer protection 0 (ALSI0) bit of the TAMPCTRLB register is set (TAMCTRLB.ALSI0=1), the RTC pseudo random pattern is only generated on the TrustRAM Active layer.

Workaround

Set the CTRLB.SEPTO bit to '1' if Tamper Detection is required on the RTC Tamper pins.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.2 Event Generation Reference: TMR102-45

In RTC Clock mode or Calendar mode (CTRLA.MODE = 2), the Periodic Daily Event (PERD) is not generated.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.3 Write Corruption Reference: TMR102-46

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

Workaround

Write the registers with:

- A 32-bit write access for:
  - COUNT register in COUNT32 mode
  - CLOCK register in CLOCK mode
- A 16-bit write access for:
  - COUNT register in COUNT16 mode

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.4 Tamper Detection Timestamp Reference: TMR102-48

If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.

Workaround

Enable RTC tamper interrupt and copy the timestamp from the RTC CLOCK register to one of the following locations:

- SRAM
- GPx register in RTC

Affected Silicon Revisions

Device Family	B						
SAM L10	X						

.....continued

Device Family	B						
SAM L11	X						

2.9.5 Prescaler Reference: TMR102-52

When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER=0).

Workaround

When the prescaler is OFF (CTRLA.PRESCALER=0), clear the Periodic Interval n Event Output Enable bits (EVCTRL.PEREOn [n = 7...0]) and the respective Periodic Interval n Interrupt Enable (INTENCLR.PERn [n = 7...0]) bits.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.6 Active Layer Protection Reference: TMR102-66

Active Layer Protection feature is limited to one tamper channel n (i.e. one RTC INn/OUTn pair). Any other tamper channels can be used either in Wake mode or Capture mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.7 Tamper Detection Timestamp Reference: TMR102-67

The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.

Workaround

Clear the INTFLAG.TAMPER bit by writing a ‘1’ to this bit when the Timestamp value has been read from the TIMESTAMP register.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.8 Tamper Detection Timestamp Reference: TMR102-60

A wrong timestamp value can be returned if more than one CPU and DMA accesses to the TIMESTAMP register are performed upon a INTFLAG.TAMPER assertion.

Workaround

The timestamp value captured in the TIMESTAMP register must be retrieved as described below:

- If RTC can trigger a DMA request when the timestamp value is available (CTRLB.DMAEN=1):
  - Wait for DMA transfer completion to read the timestamp value from the DMA buffers
  - Clear the INTFLAG.TAMPER bit.

Note: Do not read the timestamp value from the TIMESTAMP register.

- If RTC cannot trigger a DMA request when the timestamp value is available (CTRLB.DMAEN=0):
  - Wait for the INTFLAG.TAMPER bit to read the timestamp value from the TIMESTAMP register
  - Clear the INTFLAG.TAMPER bit

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10 Serial Communication Interface Inter-Integrated Circuit (SERCOM I^2C)

2.10.1 High-Speed Mode Reference: CHIP003-145

When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.

Workaround

When reflection is observed, a 100 ohm serial resistor can be added on the impacted line.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.2 Repeated Start Reference: COM100-84

When Quick command is enabled (CTRLB.QCEN = 1), the software can issue a Repeated Start by either writing the CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = 1, a bus error will be generated.

Workaround

Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.3 Repeated Start Reference: COM100-128

For Master Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue correctly a Repeated Start command.

Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate properly a Repeated Start.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.4 Repeated Start Reference: COM100-123

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.5 Repeated Start Reference: COM100-122

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.6 Slave Mode with DMA Reference: COM100-94

In I^2C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Since a NACK was received, the transfer on the I^2C bus will not occur causing the loss of this data.

Workaround

Configure the DMA transfer size to the number of data to be received by the I^2C master. DMA cannot be used if the number of data to be received by the master is not known.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.7 Slave Mode 10-bit Reference: COM100-101

I^2C slave 10-bit addressing mode is not functional.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.8 Status Flags Reference: COM100-102

In Slave mode, the BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.

Workaround

Clear the STATUS register bits, BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR, by writing these STATUS bits to '1' when INTFLAG.AMATCH is cleared.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.9 Status Flags Reference: COM100-114

The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.

Workaround

Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11 Serial Communication Serial Peripheral Interface (SERCOM SPI)

2.11.1 Data Preload Reference: COM100-83

In SPI Slave mode with Slave Data Preload Enabled (CTRLB.PLOADEN = 1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select pin low until the end of transmission.

Workaround

In SPI Slave mode, the Slave Select (SS) pin must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12 Serial Communication Interface USART (SERCOM USART)

2.12.1 Inverted Bits Reference: COM100-61

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

Workaround

In software, interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.2 ISO7816 Mode Reference: COM100-55

When the SERCOM USART is in ISO7816 mode, the SERCOM bus clock continues to run in Standby Sleep mode causing extra power consumption.

Workaround

Disable the USART before entering Standby Sleep mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.3 Debug Mode Reference: COM100-80

In USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted when entering Debug mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.4 Collision Detection Reference: COM100-75

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB clock is lower than the SERCOM generic clock.

Workaround

The SERCOM APB clock must always be higher than the SERCOM generic clock to support collision detection.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.5 Wakeup Reference: COM100-41

The USART does not wake up the device on Error Interrupt (INTFLAG.ERROR=1).

Workaround

Configure the USART to wake up the device on the RX Complete Interrupt (INTENSET.RXC=1) to check the PERR/FERR status (STATUS.PERR=1 or STATUS.FERR=1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13 Timer Counter (TC)

2.13.1 Flags Synchronization Reference: TMR100-12

When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.

Workaround

Successively, clear the STATUS.PERBUFV/STATUS.CCBUFVx flags twice to ensure that the PERBUF/CCBUFx registers value is properly restored before updating it.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						

.....continued

Device Family	B						
SAM L11	X						

2.13.2 Capture Mode / Over consumption Reference: TMR100-8

If the Time Counter x (TCx) is in Capture mode (TC.CTRLA.CAPTENx=1) and TC.CTRLA.RUNSTBY=0, the clock source driving GCLK_TCx can be kept running in Standby mode causing extra power consumption.

Workaround

Disable the Time Counter x (TCx) (TC.CTRLA.ENABLE=0) which has a channel configured in Capture mode before going to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.14 True Random Number Generator (TRNG)

2.14.1 Over consumption Reference: MATH100-7

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

Workaround

Disable the TRNG module twice:

- TRNG > CTRLA.reg = 0;
- TRNG > CTRLA.reg = 0;

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.15 Supply Controller (SUPC)

2.15.1 Buck Converter Mode Reference: CHIP003-311

Buck Converter mode is not supported when using FDPLL96M. As a result, the data provided in Tables 46-8 and 47-2 “Active Current Consumption for Buck converter mode with FDPLL96M at Performance Level 2 (PL2) setting” is not valid and must be disregarded.

Workaround
Use the LDO Regulator mode when using FDPLL96M.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.16 OSC32KCTRL

2.16.1 External 32.768KHz Crystal Oscillator Reference: UANA163-1

External 32.768 KHz crystal oscillator operation is not supported over the full temperature range of -40°C to +125°C.

Workaround
Limit external 32.768 KHz crystal oscillator operation temperature range from 0°C to 125°C with a crystal ESR <70kΩ.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.17 Boot ROM

2.17.1 GCM API Reference: BROM100-18

The GCM API function crya_gf_mult128_t does not save and restore the core register r8 on return, thereby violating the Procedure Call Standard for the ARM® Architecture (AAPCS).

Workaround
The ARM core register r8 must be saved before calling the crya_gf_mult128_t function and must be restored when returning from it.

Affected Silicon Revisions

Device Family	B						
SAM L10							
SAM L11	X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001513D):

Note: Corrections in tables, registers, and texts are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

- Table 46-8 Active Current Consumption was updated:

Table 3-1. Active Current Consumption

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	COREMARK/ FIBONACCI	LDO	PL0	DFLLULP at 8MHz	1.8V	Max at 85°C Typ at 25°	64.1	82	µA/Mhz
					3.3V		64.4	84	
				OSC 8MHz	1.8V		66.6	81	
					3.3V		70.3	83	
				OSC 4MHz	1.8V		74.1	102	
					3.3V		77.8	106	
			PL2	FDPLL96M at 32MHz	1.8V		82.0	89	
					3.3V		82.5	89	
				DFLLULP at 32MHz	1.8V		75.8	99	
					3.3V		75.8	96	
		BUCK	PL0	**DFLLULP at 4.88MHz**	1.8V		**44**	**60**	
					3.3V		**29.9**	**41**	
				OSC 8MHz	1.8V		43.8	53	
					3.3V		32.1	39	
				OSC 4MHz	1.8V		50.3	68	
					3.3V		38.9	52	
			PL2	FDPLL96M at 32MHz	1.8V	Max at 85°C Typ at 25°	59.9	66	
					3.3V		35.3	39	
				DFLLULP at 26.78MHz	1.8V		**55.8**	**70**	
					3.3V		**33.7**	**42**	
	WHILE1	LDO	PL0	DFLLULP at 8MHz	1.8V		44.3	61	
					3.3V		44.4	62	
				OSC 8MHz	1.8V		47.6	60	
					3.3V		50.1	63	
				OSC 4MHz	1.8V		54.6	83	
					3.3V		57.7	86	
			PL2	FDPLL96M at 32MHz	1.8V		56.9	61	
					3.3V		57.2	62	
				DFLLULP at 32MHz	1.8V		50.8	66	
					3.3V		51.0	64	

.....continued

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	WHILE1	BUCK	PL0	**DFLLULP at 4.88MHz**	1.8V	Max at 85°C Typ at 25°	**32.4**	**49**	µA/Mhz
					3.3V		**22.8**	**34**	
				OSC 8MHz	1.8V		32.2	41	
					3.3V		25.3	32	
				OSC 4MHz	1.8V		38.4	57	
					3.3V		31.9	45	
			PL2	FDPLL96M at 32MHz	1.8V		41.5	46	
					3.3V		24.6	28	
				DFLLULP at 26.78MHz	1.8V		**38.3**	**48**	
					3.3V		**23.1**	**29**	
IDLE	-	LDO	PL0	DFLLULP at 8MHz	1.8V		16.0	32	
					3.3V		16.2	33	
				OSC 8MHz	1.8V		19.8	33	
					3.3V		22.0	36	
				OSC 4MHz	1.8V		26.2	55	
					3.3V		29.2	59	
			PL2	FDPLL96M at 32MHz	1.8V		20.3	25	
					3.3V		20.4	26	
				DFLLULP at 32MHz	1.8V		14.3	19	
					3.3V		14.4	19	
		BUCK	PL0	**DFLLULP at 4.88MHz**	1.8V		**15.1**	**32**	
					3.3V		**12.3**	**24**	
				OSC 8MHz	1.8V		15.5	24	
					3.3V		15.2	21	
				OSC 4MHz	1.8V		21.3	39	
					3.3V		21.6	35	
			PL2	FDPLL96M at 32MHz	1.8V		14.9	19	
					3.3V		9.1	12	
				DFLLULP at 26.7MHz	1.8V		**11.2**	**16**	
					3.3V		**7.2**	**10**	

- Table 46-54 is a new table which was added to the SAM L10/L11 Data Sheet.

Table 3-2. Digital Frequency Locked Loop Characteristics (Buck Converter mode only)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
FIN	Input Clock Frequency		32		33	KHz
FOUT	Output Clock Frequency	PL0	-	-	4.88	MHz
		PL2	-	-	26.78	

.....continued

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
FOUT drift	Output Clock Frequency drift (2)	PL0, FIN = 32KHz, FOUT = 4.88MHz	-16.3		38.9	%
		PL2, FIN = 32KHz, FOUT = 26.78MHz	-8.7		16.3	
Jp	Period Jitter(2) (cycle to cycle jitter)	PL0, FIN = 32KHz, FOUT = 4.88MHz	-7.8	-	8.1	%
		PL2, FIN = 32KHz, FOUT = 26.78MHz	-5.0	-	4.6	
tLOCK	Lock Time	After startup, time to get lock signal FIN = 32KHz, FOUT = 4.88MHz, PL0 Binary Search mode enabled	-	362	-	µs
		After startup, time to get lock signal FIN = 32KHz, FOUT = 26.78MHz, PL2 Binary Search mode enabled	-	362	-	µs
Duty	Duty Cycle (1)		40	50	60	%

Note:

1. These characteristics are only applicable in Buck Converter mode.

- Table 47-2 was updated to reflect a new data:

Table 3-3. Active Current Consumption

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	COREMARK / FIBONACCI	LDO	PL0	DFLLUP at 8 MHz	1.8V	Max at 125°C Typ at 25°C	64.1	129	uA/MHz
					3.3V		64.4	131	
				OSC 8 MHz	1.8V		66.6	130	
					3.3V		70.3	132	
				OSC 4 MHz	1.8V		74.1	203	
					3.3V		77.8	206	
			PL2	FDPLL96 at 32 MHz	1.8V		82.0	98	
					3.3V		82.5	99	
				DFLLULP at 32 MHz	1.8V		75.8	109	
					3.3V		75.8	107	
		BUCK	PL0	**DFLLUP at 4.88 MHz**	1.8V		**44**	**103**	
					3.3V		**29.9**	**69**	
				OSC 8 MHz	1.8V		43.8	84	
					3.3V		32.1	58	
				OSC 4 MHz	1.8V		50.3	131	
					3.3V		38.9	92	
			PL2	FDPLL96 at 32 MHz	1.8V		59.9	70	
					3.3V		35.3	43	
				DFLLULP at 26.78 MHz	1.8V		**55.8**	**80**	
					3.3V		**33.7**	**48**	
	WHILE1	LDO	PL0	DFLLUP at 8 MHz	1.8V		44.3	110	
					3.3V		44.4	111	
				OSC 8 MHz	1.8V		47.6	111	
					3.3V		50.1	113	
				OSC 4 MHz	1.8V		54.6	184	
					3.3V		57.7	187	
			PL2	FDPLL96 at 32 MHz	1.8V		56.9	79	
					3.3V		57.2	80	
				DFLLULP at 32 MHz	1.8V		50.8	72	
					3.3V		51.0	72	

.....continued

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
ACTIVE	WHILE1	BUCK	PL0	**DFLLUP at 4.88 MHz**	1.8V	Max at 125°C Typ at 25°C	**32.4**	**90**	uA/MHz
					3.3V		**22.8**	**62**	
				OSC 8 MHz	1.8V		32.2	73	
					3.3V		25.3	51	
				OSC 4 MHz	1.8V		38.4	121	
					3.3V		31.9	86	
			PL2	FDPLL96 at 32 MHz	1.8V		41.5	55	
					3.3V		24.6	34	
				DFLLULP at 26.78 MHz	1.8V		**38.3**	**58**	
					3.3V		**23.1**	**36**	
IDLE	-	LDO	PL0	DFLLUP at 8 MHz	1.8V		16.0	81	
					3.3V		16.2	82	
				OSC 8 MHz	1.8V		19.8	82	
					3.3V		22.0	85	
				OSC 4 MHz	1.8V		26.2	152	
					3.3V		29.2	157	
			PL2	FDPLL96 at 32 MHz	1.8V		20.3	54	
					3.3V		20.4	54	
				DFLLULP at 32 MHz	1.8V		14.3	32	
					3.3V		14.4	33	
		BUCK	PL0	**DFLLUP at 4.88 MHz**	1.8V		**15.1**	**68**	
					3.3V		**12.3**	**48**	
				OSC 8 MHz	1.8V		15.5	55	
					3.3V		15.2	40	
				OSC 4 MHz	1.8V		21.3	100	
					3.3V		21.6	73	
			PL2	FDPLL96 at 32 MHz	1.8V		14.9	30	
					3.3V		9.1	19	
				DFLLULP at 26.78 MHz	1.8V		**11.2**	**26**	
					3.3V		**7.2**	**17**	

4. Revision History

Revision C - 05/2019

The following new errata were added:

- RTC:
  - 2.9.5 Prescaler Reference: TMR102-52
  - 2.9.6 Active Layer Protection Reference: TMR102-66
  - 2.9.7 Tamper Detection Timestamp Reference: TMR102-67
  - 2.9.8 Tamper Detection Timestamp Reference: TMR102-60
- SERCOM USART:
  - 2.12.5 Wakeup Reference: COM100-41

Revision B - 02/2019

The following new errata were added:

- RTC: 2.9.4 Tamper Detection Timestamp Reference: TMR102-48
- SUPC: 2.15.1 Buck Converter Mode Reference: CHIP003-311
- OSC32KCTRL: 2.16.1 External 32.768KHz Crystal Oscillator Reference: UANA163-1
- Boot ROM: 2.17.1 GCM API Reference: BROM100-18

The following errata is updated:

- ADC: 2.1.1 Reference Buffer Offset Compensation Reference:CHIP003-247

The following Data Sheet clarifications were added:

- Updates to Electrical Specifications Tables:
  - Table 46-8
  - Table 46-54
  - Table 47-2

Revision A - 5/2018

This is the initial release of this document.

The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at http://www.microchip.com/. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Trademarks

ISBN: 978-1-5224-4501-2

Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Asia Pacific Office** Suites 3707-14, 37th Floor Tower 6, The Gateway Harbour City, Kowloon **Hong Kong** Tel: 852-2943-5100 Fax: 852-2401-3431 **Australia - Sydney** Tel: 61-2-9868-6733 Fax: 61-2-9868-6755 **China - Beijing** Tel: 86-10-8569-7000 Fax: 86-10-8528-2104 **China - Chengdu** Tel: 86-28-8665-5511 Fax: 86-28-8665-7889 **China - Chongqing** Tel: 86-23-8980-9588 Fax: 86-23-8980-9500 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 Fax: 86-571-8792-8116 **China - Hong Kong SAR** Tel: 852-2943-5100 Fax: 852-2401-3431 **China - Nanjing** Tel: 86-25-8473-2460 Fax: 86-25-8473-2470 **China - Qingdao** Tel: 86-532-8502-7355 Fax: 86-532-8502-7205 **China - Shanghai** Tel: 86-21-3326-8000 Fax: 86-21-3326-8021 **China - Shenyang** Tel: 86-24-2334-2829 Fax: 86-24-2334-2393 **China - Shenzhen** Tel: 86-755-8864-2200 Fax: 86-755-8203-1760 **China - Wuhan** Tel: 86-27-5980-5300 Fax: 86-27-5980-5118 **China - Xian** Tel: 86-29-8833-7252 Fax: 86-29-8833-7256	**China - Xiamen** Tel: 86-592-2388138 Fax: 86-592-2388130 **China - Zhuhai** Tel: 86-756-3210040 Fax: 86-756-3210049 **India - Bangalore** Tel: 91-80-3090-4444 Fax: 91-80-3090-4123 **India - New Delhi** Tel: 91-11-4160-8631 Fax: 91-11-4160-8632 **India - Pune** Tel: 91-20-3019-1500 **Japan - Osaka** Tel: 81-6-6152-7160 Fax: 81-6-6152-9310 **Japan - Tokyo** Tel: 81-3-6880- 3770 Fax: 81-3-6880-3771 **Korea - Daegu** Tel: 82-53-744-4301 Fax: 82-53-744-4302 **Korea - Seoul** Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934 **Malaysia - Kuala Lumpur** Tel: 60-3-6201-9857 Fax: 60-3-6201-9859 **Malaysia - Penang** Tel: 60-4-227-8870 Fax: 60-4-227-4068 **Philippines - Manila** Tel: 63-2-634-9065 Fax: 63-2-634-9069 **Singapore** Tel: 65-6334-8870 Fax: 65-6334-8850 **Taiwan - Hsin Chu** Tel: 886-3-5778-366 Fax: 886-3-5770-955 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 Fax: 886-2-2508-0102 **Thailand - Bangkok** Tel: 66-2-694-1351 Fax: 66-2-694-1350	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4450-2828 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **France - Saint Cloud** Tel: 33-1-30-60-70-00 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-67-3636 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-7289-7561 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820