EVALSPEAr300 - evaluation board for the SPEAr300

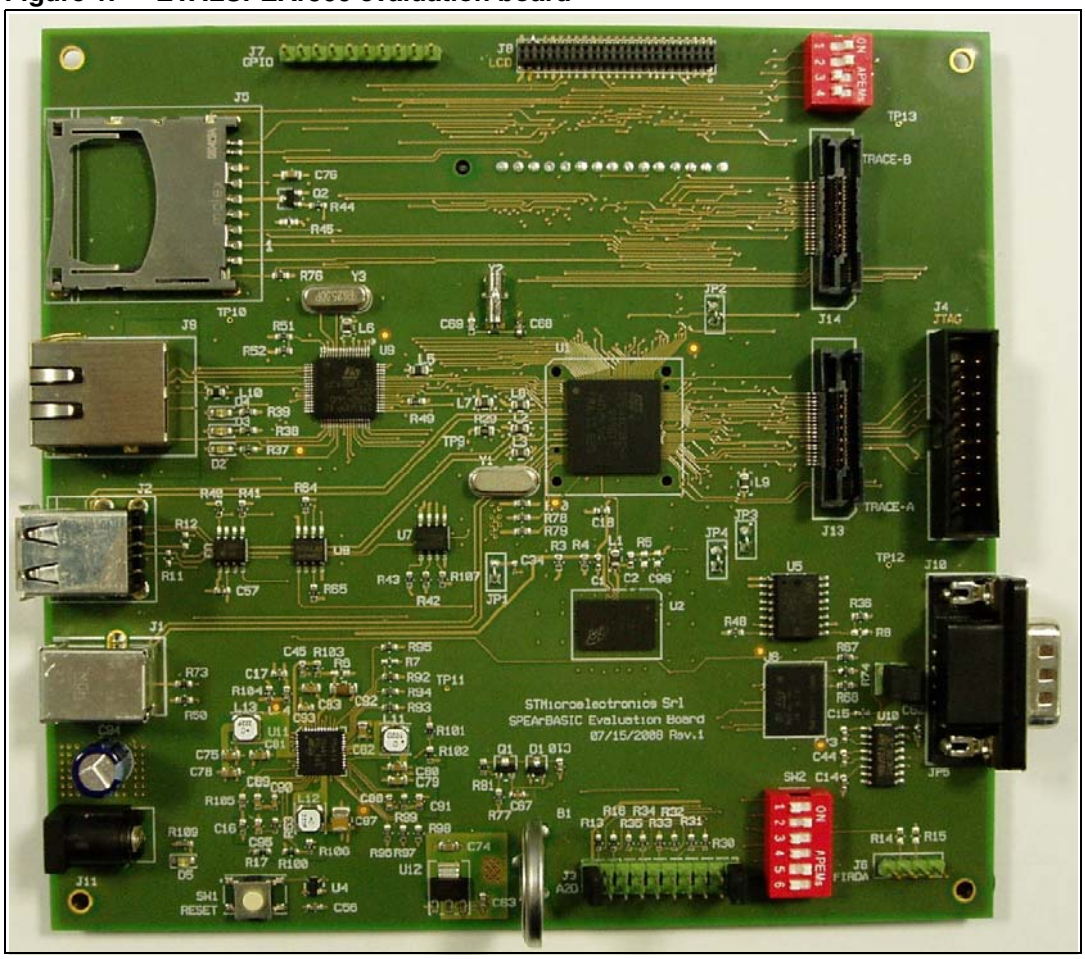
1 Description

The EVALSPEAr300 evaluation board for SPEAr300 is intended to be used for three main purposes:

- To allow you to quickly evaluate and debug software for the SPEAr300
- Act as a learning tool to rapidly get familiar with the SPEAr300 features
- Provide a starting point for the development of the final application board

It is equipped with most of the interfacRev 2es offered by the SPEAr300.

Figure 1. EVALSPEAr300 evaluation board



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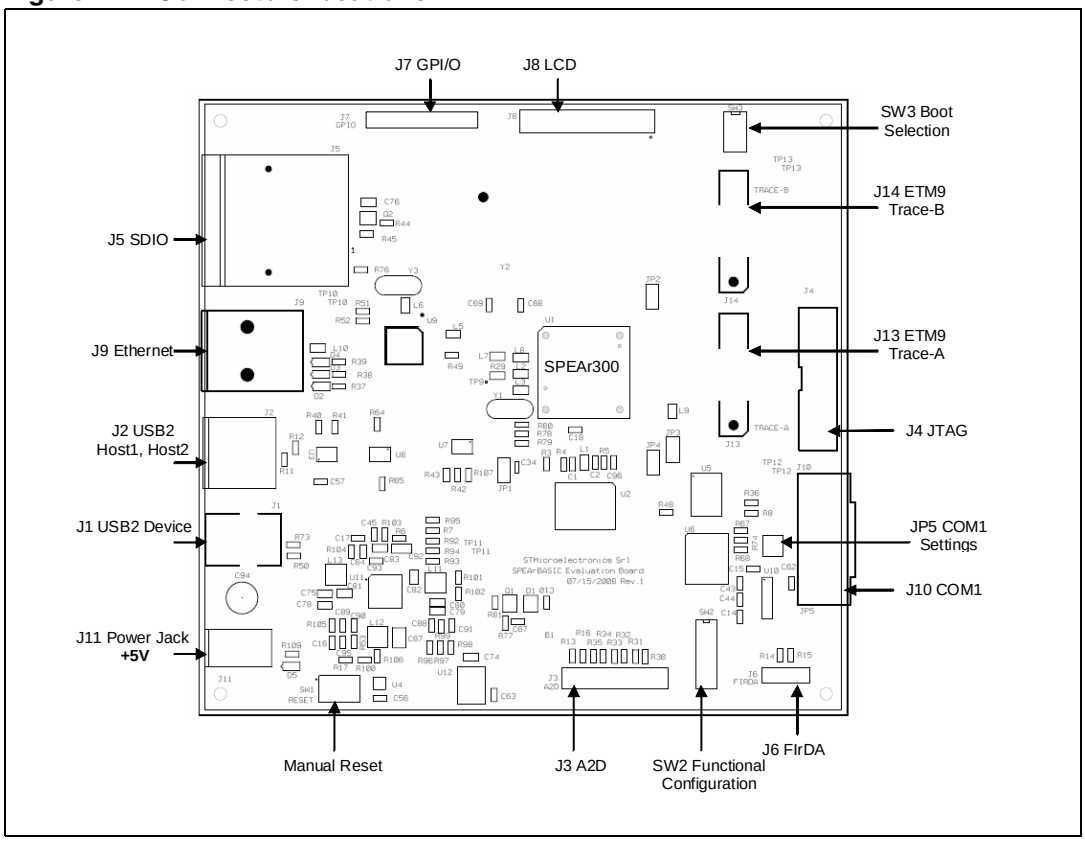
2 Contents of the kit

The EVALSPEAr300 evaluation board kit contains:

- SPEAr300 evaluation board
- AC/adapter (output voltage 5 V)
- 2 Plug Adapter (USA/Europe)
- User manual documentation

3 Connectors locations

Figure 2. Connectors locations



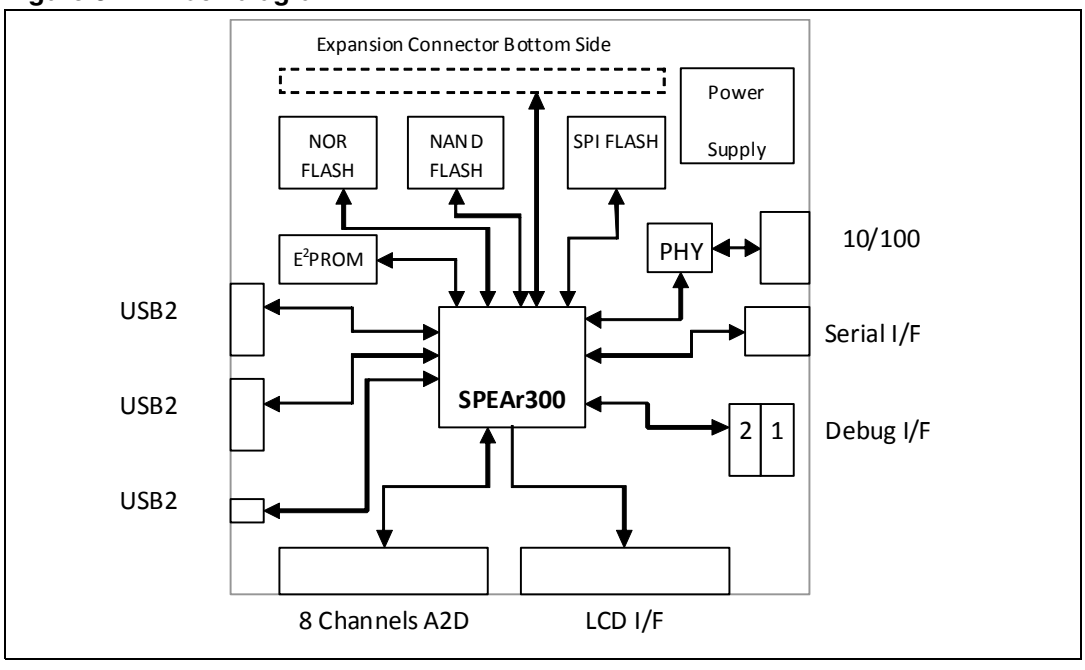
4 Features and block diagram

4.1 Features

- SPEAr300 embedded MPU
- Up to 2 Gb DDR2 333 MHz (std 128 MB)
- Up to 16 MB Serial Flash memory (std 8 MB)
- Up to 2 Gb NAND Flash memory (std 64 MB)
- 4 Kb Serial I^2C
- 4 Mb SPI Flash memory
- Two USB 2.0 full Host port channels
- One USB 2.0 HS Device
- 10/100 Ethernet port
- One serial port (up to 115 Kbaud)
- Debug ports (JTAG + ETM9)
- 8 ADC channels (10 bit, 1 Msamples)
- 8 GPIOs
- LCD I/F up to 24 bits-per-pixel (bpp)
- SD Card interface

4.2 Block diagram

Figure 3. Block diagram



5 Start up

5.1 Unpacking

ELECTROSTATIC WARNING:
The EVALSPEAr300 Evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. General practices for working with static sensitive devices should be applied when working with this board.

- **Wear an anti-static wristband** - Wearing a simple anti-static wristband can help to prevent ESD from damaging the Spear300 evaluation board.
- **Self-grounding** - Touch a grounded conducting material before handling and periodically while handling the Spear300 evaluation board.
- **Use an anti-static pad** - When configuring the Spear300 evaluation board, place it on an antic-static pad to reduce the possibility of ESD damage.
- **Only handle the board edges** - When handling the Spear300 evaluation board.

5.2 Connection

- Connect a serial cable (RS232 on J4) to a host PC (see Figure 4).
- On a host PC running Windows or Linux, start the Terminal program.
- Connect the AC Adapter to a power outlet.
- Power ON the board (plug the jack of the AC/Adapter on J11). A sequence of boot messages is displayed, followed by the Linux console prompt.

For more information, refer to the *SPEAr300 evaluation board software getting started user manual* available on www.st.com/spear.

5.3 Booting procedure

The SPEAr300 Board is able to boot a Linux kernel pre-installed in the serial NOR Flash.

At power on, the serial port outputs a brief header message with some uBoot information (uBoot version, SDK version, and some internal hardware information). At this point you can choose to:

1. **Stop the system directly in uBoot**: For this you have to press the spacebar on the host computer keyboard before the boot delay time expires (default is 3 seconds).
2. **Boot Linux**: The system logs you in automatically as super user and the Linux shell prompt is displayed on the screen.

6 Block descriptions

6.1 Dynamic memory subsystem

The Dynamic memory subsystem is composed of three major parts:

6.1.1 Memory chip

The memory used is a Micron DDR2 device and its part number is: MT47H64M16HR-3. Its size is 128 Mb x 8 (16 Mb x 8 x 8 banks).

6.1.2 Local power supply

It is based on a Monolithic Voltage regulator for the chip set and DDR2/3 (PM6641). It is generated locally in order to minimize the layout impact and also to avoid any noise injection between different subsystems.

6.1.3 Signal termination

A parallel termination is added on the clock lines to compensate, if needed, the layout dissymmetry. Two 100 Ohm resistors are used for each line in order to obtain an impedance of 50 ohm. All the other terminations are directly inside the pads (both on the SPEAr300 and the memory sides).

6.2 Static memory subsystem

6.2.1 Serial Flash memory

This block is based on an M25P64 ST Serial Flash memory device. The size of this chip is 8 MB.

A resistor (R8) is also provided to protect the Flash memory from any unwanted write access.

6.2.2 Serial I^2C EEPROM

This block is based on the M24C04W ST Serial I^2C EEPROM. The size of this chip is 4 Kb.

A resistor (R107) is also provided to protect the EEPROM from any unwanted write access.

6.2.3 NAND Flash memory

This block is based on Nand512W3A2CZA6 ST NAND Flash memory. The size of this chip is 512 Mbit.

6.2.4 SPI Flash memory

This block is based on the M25P40 ST Serial Flash memory. The size of this chip is 4 Mb.

A resistor (R64) is also provided to protect the Flash memory from any unwanted write access.

6.3 Ethernet subsystem

This subsystem is based on the Ethernet PHY STE100P (U9) and a connector (J9) that also includes also all the required magnetics (Line transformer ratio 1:1).

Several LEDs are present to indicate the status of the line:

- The green LED in the connector is driven on continuously when 100 Mb/s network operating speed is detected.
- The yellow LED in the connector blinks when there is TX or RX activity. This LED is driven on continuously when the Link test detects a good link condition.
- The yellow LED (D4) is driven on continuously when a full duplex configuration is detected. This LED blinks at a 20 Hz frequency when a collision status is detected in the half duplex configuration.
- The yellow LED (D3) blinks at a 10 Hz frequency when ongoing receiving or transmitting is detected.
- The yellow LED (D2) is driven on continuously when 10 Mb/s network operating speed is detected.

6.4 USB 2.0 subsystem

6.4.1 Host ports

The board has two host ports (J2) that are fully compliant with the USB 2.0 specification (two controllers with one port each). This means that the two hosts can work in concurrent mode with the maximum possible bandwidth. Each host has also full control of the VBUS supplied by the ST2052 power switch that also provides overcurrent protection in case of a short circuit in the USB cable.

6.4.2 Device port

A USB 2.0 device port is also provided (J1).

6.5 Debug interface

Two debug interfaces are provided:

1. The JTAG interface can be used for "static" debug. This means that it is possible to set a breakpoint and, when the system stops, to verify the contents of the memory and/or registers and modify them if needed.
2. The ETM9 interface can be used for "dynamic" debug. The ETM9 block embedded in the SPEAr300 chip, sends all the information about the AHB transactions during the code execution to the external trace box and the external box stores this information in a local buffer. This makes it possible, by stopping the CPU activity, to analyze the actual program flow. For example, if a particular data abort occurs, you can set a breakpoint on the data abort location and then, when the breakpoint is reached, you can analyze the buffer trace. With this information, it becomes a simple task to identify the event that produced the problem.

The following configurations can be selected by setting SW2 bits [2:1].

Table 1. Switch 2 bits [2:1]

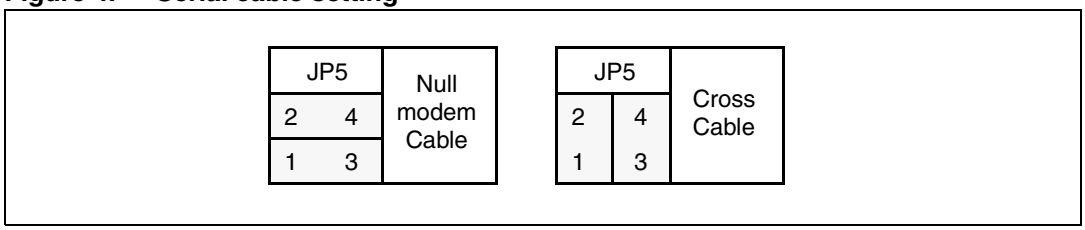
Sw2		Description
2	1	
0	0	No debug features available
0	1	The ARM JTAG is connected to J4
1	0	The ARM ETM bus available on J13 and J14

Please refer to the documentation of the trace box manufacturer for more information on the ETM interface (www.lauterbach.com, www.agilent.com, www.yokogawa.com).

6.6 Serial interface

One serial interface port is available. This typically used as OS monitor, is available on the J10 connector. It is possible to simulate a cross cable by changing the position of the J5 jumpers.

Figure 4. Serial cable setting



6.7 A/D interface

Eight analog input lines are provided on the J3 connector. The connector also allows you to determine the conversion range by setting the conversion limits on pins J3-19 (lower limit) and J3-1 (upper limit). The default setting is to have pins 1-2 and 19-20 shorted by jumpers.

In this way the conversion range is set to the maximum value (0 ~ 2.5V with a granularity of 2.44 mV) but by removing the two jumpers and providing different values on pin 1 and 19 it is possible to reduce the range and thus increase the granularity. For example if you input 1 V on J3-19 and 2 V on J3-1 the range will be 1 V ~ 2 V in steps of less than 1 mV.

In any case the following relationships between the pins should be ensured:

0 V	≤	J3-19	≤	J3 17 ~ 3	≤	J3-1	≤	2.5 V
AGND	≤	Vref_n	≤	ADC_In channels	≤	Vref_p	≤	AVDD

6.8 Real time clock (battery powered)

The real time clock (RTC) is powered with an external battery (3 V) in order to avoid losing its data even if the main power supply is switched off.

6.9 General power supply

From a 5 V external AC/DC regulator power source, this block, generates all the required voltages as follows:

- 1.2 V (Switching regulator PM6641) to supply the internal logic of the SPEAr300
- 1.8 V (Switching regulator PM6641) for the DDR2 memory.
- 2.5 V (LDO regulator) for the analog portion of SPEAr300
- 3.3 V (Switching regulator PM6641) to supply the other interfaces.

A power monitor is also present to provide the general reset of the board.

6.10 General-purpose I/Os

Eight general-purpose I/Os are present on the board. The eight lines are connected to the J7 connector. The same connector also has GND and 3.3V pins available.

Note: For the connector pinout, refer to the schematic drawing available on www.st.com/spear.

6.11 Reset switch

A manual reset switch (SW1) is available on the top side of the board.

6.12 LCD Interface

The J8 connector (p/n SFM-125-02-S-D manufacturer Samtec) is provided to allow you to connect an LCD daughter board. It mates with TFM-125-02-S-D.

The following signals are available on this connector:

- All the LCD interface signals
- Two analog inputs (A/D)
- +5 V
- GND

Note: For the connector pinout, refer to the schematic drawing

6.13 SDIO interface

A standard SDIO connector is also provided on the board (J5).

7 Jumper settings

7.1 Switch 2

Table 2. Switch 2 (SoC functional configuration)

Bit	Description
1	Test0 – see Debug configuration below
2	Test1 – see Debug configuration below
3	Test2 – see Debug configuration below
4	Test3 – see Debug configuration below
5	Test4 – see Debug configuration below
6	BootSel – see Debug configuration below

Table 3. Switch 2 (debug configuration)

Test bit		Debug configuration
2	1	
0	0	Normal Mode (No debug enabled)
0	1	ARM1 JTAG connected to J4
1	0	The ARM ETM bus available on J13 and J14

Table 4. Switch 2 (functional configuration)

Test bit				Functional configuration
6	**5**	**4**	**3**	
1	0	1	1	Configuration 3

Note: When DIP switch SW2-X is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.

Bits 3, 4, and 5 allow you to set the Functional configuration. The default configuration is **Configuration 3**. For the other configurations, please refer to the user manual chapter 6 available on www.st.com/spear.

7.2 Switch 3

Table 5. Switch 3 (strapping options)

Boot from	SW3-1	SW3-2	SW3-3	SW3-4
USB_BOOT	0	0	0	0
ETH (parameter from SPI ROM)	0	0	0	1
ETH (parameter from I2C ROM)	0	0	1	0
Serial NOR (default setting)	0	0	1	1
Parallel NOR 8	0	1	0	0
Parallel NAND 8	0	1	0	1
Parallel NOR 16	0	1	1	0
Parallel NAND 16	0	1	1	1
SPI_BOOT	1	0	0	0
UART_BOOT	1	0	0	1
I2C_BOOT	1	0	1	0

Note: When DIP switch SW3-X is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1

8 Expansion connector

An expansion connector (J12 on bottom side) is provided for a companion board. The manufacturer is Tyco Electronics and the Part Number is 2-5767004-4

The following signals are available on this connector:

- +5 V
- GND
- All the PL_GPIO signals
- The four PL_CLK signals
- Host0_DP and DM

8.1 Board schematic

The board schematic is available on www.st.com/spear.

9 Evaluation board bill of materials (BOM)

Reference: SPEAr300 BOM Board Rev1 (Set. 17 2009)

Table 6. Capacitors

#	Qty	Ref. description	Value	Manufacturer	Manufacturer P/N
1	1	B1		Panasonic	BR/CR2032/1GVF1GV
2	58	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C26, C27, C28, C29, C31, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64	0.1uF	Vitramon	MR-VJ0603Y104KX
3	6	C25, C30, C32, C33, C34, C46	0.1UF	Murata	GRM155R71C104KA88D
4	3	C65, C66, C67	10nF	Kemet Electronics	C0603C103K5RAC
5	4	C68, C69, C70, C71	15pF	Murata	GRM1885C1H150JZ01D
6	2	C72, C73	33pF	Kemet Electronics	C0603C330J5GAC
7	10	C74, C75, C76, C77, C78, C79, C80, C81, C82, C83	10uF	Murata	GRM21BR61A106KE19
8	1	C84	470nF	Kemet Electronics	C0805C474K4RAC
9	2	C85, C86	10pF	Kemet Electronics	C0603C100J5GAC
10	1	C87	47uF	Murata	GRM32ER60J476ME20L
11	3	C88, C89, C90	22nF	Kemet Electronics	C0603C223K5RAC
12	1	C91	470pF	Kemet Electronics	C0603C471K5RAC
13	1	C92	22uF	Murata	GRM31CR60J226KE19
14	1	C93	33nF	Kemet Electronics	C0603C333K5RAC7867
15	1	C94	100uF 25V	Panasonic	ECA1HM101
16	1	C95	2.2nF	Kemet Electronics	C0603C222K5RAC
17	1	D1	BAV70LT1G	On Semiconductor	BAV70LT1G
18	3	D2, D3, D4	LED Yellow	Kingbright	KP-2012SYC
19	1	D5	LED Green	Kingbright	KP-2012SGC

Table 7. Connectors, inductors and transistors

#	Qty	Ref. description	Value	Manufacturer	Manufacturer P/N
20	1	J1	USB_Device	SAMTEC	USB-B-S-F-B-TH
21	1	J2	USB_Host	TYCO Electronics AMP	5787617-1
22	1	J3	A2D Conn.	TYCO Electronics AMP	5-826925-0
23	1	J4	JTAG_Conn. 20	TYCO Electronics AMP	2-1634688-0
24	1	J5	SDIO_CON	MOLEX	67993-8001
25	1	J6		TYCO Electronics AMP	5-826629-0
26	1	J7	GPIO conn.	TYCO Electronics AMP	5-826629-0
27	1	J8	LCD Conn.	SAMTEC	SFM-125-02-S-D
28	1	J9	ETH Conn.	Pulse	J00-0065NL
29	1	J10	Serial Conn.	TYCO Electronics AMP	5747840-2
30	1	J11	JACK 2.1MM	CLIFF Electronics	FC681491
31	1	J12	MICTOR_114	TYCO Electronics AMP	2-5767004-4
32	2	J13, J14	ETM Conn.	TYCO Electronics AMP	5767061-1
33	4	JP1, JP2, JP3, JP4	Jumper	TYCO Electronics AMP	5-826629-0
34	1	JP5	Jumper	TYCO Electronics AMP	5-826925-0
35	1	L1	WE74792023	WURTH Elektronik	742792023
36	9	L2, L3, L4, L5, L6, L7, L8, L9, L10	IND	Murata	BLM21BD601SN1D
37	1	L11	LPS4012-102NL	Coilcraft	LPS4012-102NL
38	2	L12, L13	LPS4012-222ML	Coilcraft	LPS4012-222ML
39	1	Q1	BC848CE6327	Infineon	BC848CE6327
40	1	Q2	BSH205	NXP	BSH205

Table 8. Semiconductors and crystals

#	Qty	Ref. description	Value	Manufacturer	Manufacturer P/N
65	1	U2	MT47H64M16 HR	MICRON	MT47H64M16HR-3E
66	1	U1	SPEAr300	STM	SPEAR300-2 V590BA
67	1	U3	ST2052	STM	ST2052
68	1	U4	STM811	STM	STM811SW16F
69	1	U5	M25P64	STM	M25P64-VMF6P
70	1	U6	NAND512X8	STM	Nand512W3A2CZA6
71	1	U7	M24C04	STM	M24C04-WMN6P

Table 8. Semiconductors and crystals (continued)

#	Qty	Ref. description	Value	Manufacturer	Manufacturer P/N
72	1	U8	M25P40	STM	M25P40-VMN6P
73	1	U9	STE100P	STM	STE100P
74	1	U10	ST3232-SO16	STM	ST3232CDR
75	1	U11	PM6641	STM	PM6641
76	1	U12	LD1117S25TR	STM	LD1117S25TR
77	1	Y1	24MHZ	RAKON	XTAL003325
78	1	Y2	32.768KHZ	FOX Electronics	NC26LF-327
79	1	Y3	25MHZ	FOX Electronics	FOXS/250F-20
80	6		Insulated jumper	WINSLOW Adaptics	W8010T50

Table 9. Resistors and switches

#	Qty	Ref. description	Value	Manufacturer	Manufacturer P/N
41	2	R1, R2	121K	PHYCOMP	P/N 232273461214
42	2	R3, R4	470	TYCO Electronics UK	CRG0603F470R
43	2	R9, R17	0	TYCO Electronics UK	CRG0603ZR
44	11	R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28	100	TYCO Electronics UK	CRG0603F100R
45	1	R29	43,2	TYCO Electronics UK	RN73C2A43R2BTG
46	14	R36, R37, R38, R39, R40, R41, R42, R43, R44, R46, R47, R48, R49, R107	1K	TYCO Electronics UK	CRG0603F1K0
47	17	R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66	10K	TYCO Electronics UK	CRG0603F10K
48	10	R67, R68, R69, R70, R71, R72, R73, R74, R75, R76	4.7K	TYCO Electronics UK	CRG0603F4K7
49	1	R77	390K	TYCO Electronics UK	CRG0603F390K
50	3	R78, R79, R80	10	TYCO Electronics UK	CRG0603F10R
51	4	R82, R83, R84, R85	2.2K	TYCO Electronics UK	CRG0603F2K2
52	1	R86	1M	TYCO Electronics UK	CRG0603F1M0

Table 9. Resistors and switches (continued)

#	Qty	Ref. description	Value	Manufacturer	Manufacturer P/N
53	5	R87, R88, R89, R90, R91	150	TYCO Electronics UK	CRG0603F150R
54	7	R92, R93, R94, R95, R96, R97, R98	68K	TYCO Electronics UK	CRG0603F68K
55	1	R99	27K	TYCO Electronics UK	CRG0603F27K
56	3	R81, R100, R101	150K	TYCO Electronics UK	CRG0603F150K
57	1	R102	47K	TYCO Electronics UK	CRG0603F47K
58	2	R103, R104	4,3	PHYCOMP	p/n 232270464308
59	1	R105	15K	TYCO Electronics UK	CRG0603F15K
60	1	R106	75K	PHYCOMP	p/n 232270467503
61	1	R109	270	TYCO Electronics UK	CRG0603F270R
62	1	SW1		OMRON Electronics	B3S-1000
63	1	SW2		APEM Components	DS06
64	1	SW3		APEM Components	DS04

Appendix A Licence agreements

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10-Nov-2008

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Revision history

Table 10. Document revision history

Date	Revision	Changes
25-Sep-2009	1	Initial release.
25-Feb-2010	2	Updated *Figure 4*. Corrected code names in *Section 6.12: LCD Interface*. Changed the title of *Section 6.13: SDIO interface*. Updated the *Note: on page 13* and *Note: on page 14*. Changed the title of the document. Minor text changes

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