MCP18480

-48V Hot Swap Controller

Features

- Allows safe board removal and insertion from a live backplane
- Accurate (<1.5%) internal voltage reference for fault detection and precision timing
- Programmable foldback current limiting
- Programmable circuit breaker current limiting
- Auto restart option for all faults
- Adjustable Undervoltage lockout thresholds
- Adjustable Overvoltage protection threshold
- Adjustable Power Good delay
- Configurable Power Good output polarity
- Low-side drive of an external N-channel FET

CMOS Technology

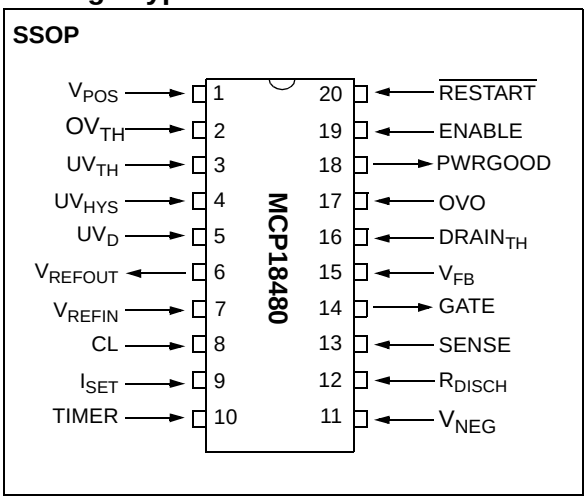
- High-Voltage Operation
- Temperature range: Industrial (I): -40°C to +85°C

Packaging

- 20-lead SSOP

Package Type

SSOP



Description

The MCP18480 is a Hot Swap controller that allows boards to be safely removed or inserted from an active backplane using -48V.

When PCBs are inserted into a live backplane, high-peak or transient currents from the source are generated due to the charging of the bypass capacitors on the supply. The high transient currents can destroy connectors and capacitors. The high inrush current can pull the input voltage BUS down and reset the system.

The MCP18480 solves this problem by controlling the slew rate of the backplane voltage to the board so that these transients are eliminated. This allows boards to be removed and inserted without causing damage to connector pins and input bulk capacitors, in addition to preventing false resets to the other boards on the backplane.

The MCP18480 can be used in applications in several areas including:

- Telecom Line Cards
- Network Switches
- Network Routers and Servers
- Base Station Line Cards
- Power-Over-LAN
- Power-Over-MDI
- IP Phone Switches/Routers
- Mid-Span, Power-Over-MDI

Two forms of current limit are provided in the MCP18480. These are:

- Foldback
- Circuit breaker

The foldback current-limiting circuit uses an external sense resistor and a voltage that is proportional to the external MOSFET's drain voltage. These are used to keep the MOSFET in its Safe Operating Area (SOA).

If the device remains in current limit for a programmed time period, the external N-channel FET is turned off. The option exists to configure the device to automatically restart after a programmed time delay. A programmable catastrophic current limit threshold shuts down the switch (circuit breaker) if excessive current is sensed due to a short-circuit condition.

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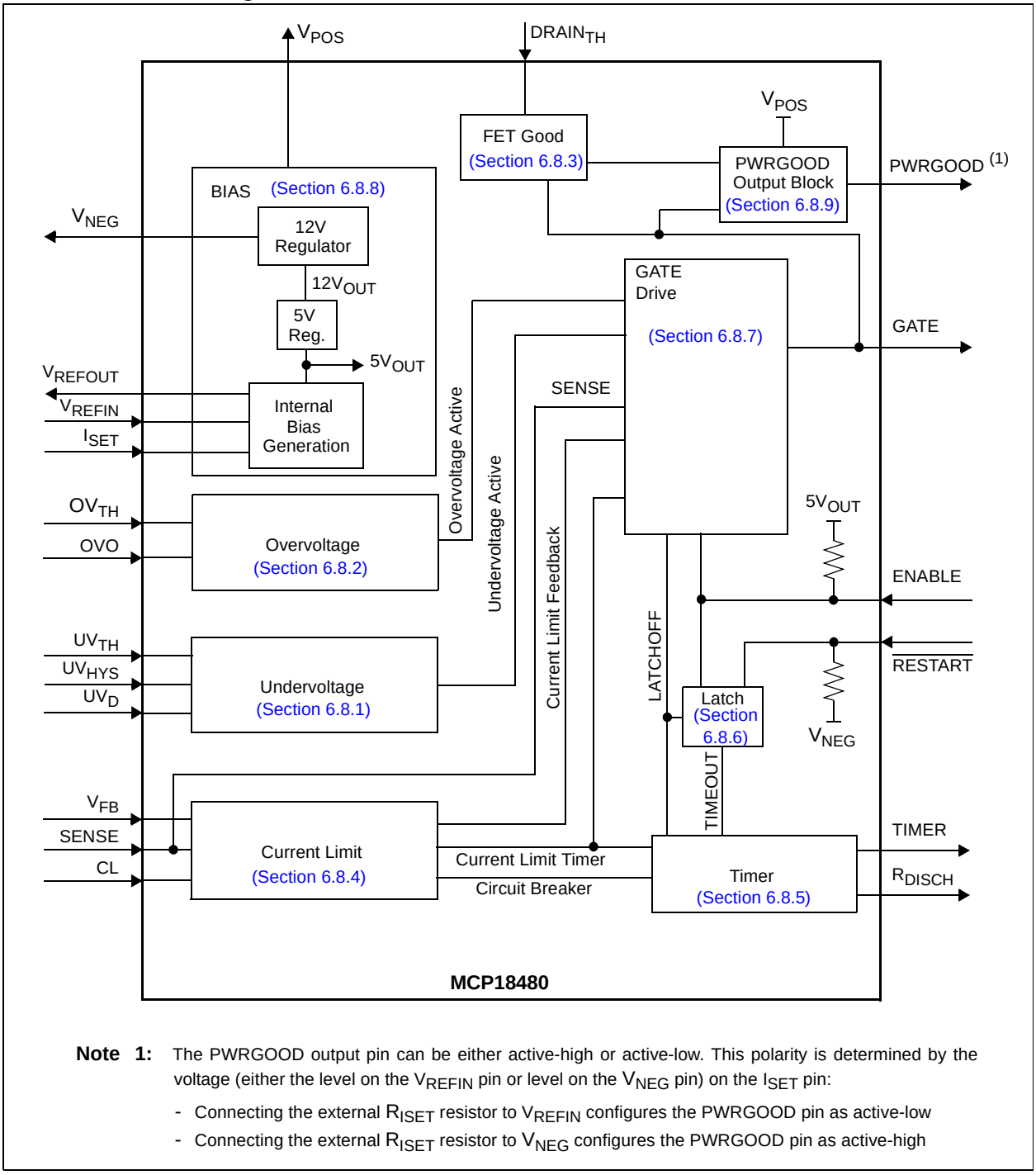
Internal comparators are incorporated to add hysteresis for adjusting the Undervoltage Lockout (UVLO) threshold. The external N-channel MOSFET is turned on when the input is below the user-programmable, Overvoltage threshold and above the user-programmable, Undervoltage threshold.

The PWRGOOD pin indicates the status of the MCP18480 and is active when the device has completed power-up and the system is not in an Undervoltage, Overvoltage or current-limit condition.

PWRGOOD can be externally configured to either active-high or active-low to accommodate external circuitry (power supplies) that have either enabling logic.

A block diagram of the MCP18480 is shown below.

MCP18480 Block Diagram



Note 1: The PWRGOOD output pin can be either active-high or active-low. This polarity is determined by the voltage (either the level on the V_{REFIN} pin or level on the V_{NEG} pin) on the I_{SET} pin:

- Connecting the external R_{ISET} resistor to V_{REFIN} configures the PWRGOOD pin as active-low
- Connecting the external R_{ISET} resistor to V_{NEG} configures the PWRGOOD pin as active-high

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –40°C to +85°C

Storage Temperature ..... –65°C to +150°C

Voltage on V_{POS} with respect to V_{NEG} -0.3V to +15.0V

Voltage on DV_{TH}, UV_{TH}, V_{FB}, OVO and UV_{HYS} pins with respect to V_{NEG} ..... V_{NEG} – 0.3V to (V_{POS} + 0.3V)

Voltage on V_{REFIN}, CL, SENSE, $DRAIN_{TH}$, ENABLE and RESTART pins with respect to V_{NEG} ..... V_{NEG} - 0.3V to 6V.

Total Power Dissipation **(Note 1)** ..... 800 mW

Max. Current out of V_{NEG} pin ..... 80 mA

Max. Current into V_{POS} pin ..... 50 mA

Max. Output Current sunk by Gate pin..... 80 mA

Max. Output Current sunk by V_{REFOUT} pin ..... 5 mA

Max. Output Current sunk by any other Output pin..... 25 mA

Max. Output Current sourced by Gate pin ..... 200 µA

Max. Output Current sourced by V_{REFOUT} pin ..... 5 mA

Max. Output Current sourced by any other Output pin..... 25 mA

Junction to Ambient, Θ_{JA} (20 pin SSOP Package) Derating ..... 108.1°C/W

Junction to Case, Θ_{JC} (20 pin SSOP Package) Derating ..... 32.2°C/W

Lead Temperature, Soldering, 10 seconds ..... 300°C

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power Dissipation is calculated as follows:

$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma\{(V_{DD}-V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, operating temperature: –40°C ≤ T_A ≤ +85°C (Industrial), Supply Current: 5 mA ≤ I_{POS} ≤ 25 mA, R_{ISET} = 125 kΩ, C_{BYP} = 2 µF.

Param. No.	Parameter		Sym	Min	Typ (1)	Max	Units	Conditions
MD001	Current into shunt regulator that produces V_{POS} output voltage that meets MD001A specification		I_{POS1}	5	—	25	mA	ENABLE pin = 5V
				5	—	25		ENABLE pin = V_{NEG}
MD001A	Regulated Output Voltage Differential of V_{POS} to V_{NEG}		V_{POS}	10.4	12.0	13.4	V	See MD001
MD002	V_{REFOUT} pin output voltage		V_{REFOUT}	2.463	2.5	2.538	V	Load = 50 µA
MD010	V_{GATE} pin output voltage		V_{GATE}	V_{POS} - 2	V_{POS} -1	V_{POS}	V	
MD011	Voltage on I_{SET} pin		V_{ISET}	(V_{REFIN}/2) - 0.02	V_{REFIN}/2	(V_{REFIN}/2) +0.02	V	
MD012A	Voltage on SENSE pin to trigger current-limiting		V_{SENSE}	40	50	60	mV	V_{FB} = V_{NEG}
MD012B				25	31.0	40	mV	V_{FB} = V_{NEG} + 0.25V
MD012C				7	12	17	mV	V_{FB} = V_{NEG} + 0.5V
MD013	Undervoltage Threshold		UV_{TH}	V_{REFIN} - 0.03	V_{REFIN}	V_{REFIN} + 0.03	V	
MD014A	Overvoltage Threshold	rising	OV_{TH}	V_{REFIN} - 0.05	V_{REFIN}	V_{REFIN} + 0.05	V	V_{REFIN} = 2.5V
MD014B		falling	OV_{TH}	V_{REFIN} - 0.035	V_{REFIN} - 0.02	V_{REFIN} - 0.005	V	V_{REFIN} = 2.5V
MD015	DRAIN Pin Input Threshold Voltage		V_{DTH}	90	100	130	mV	

Note 1: Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

2: Negative current is defined as current sourced by the pin.

3: All voltages are with respect to the V_{NEG} pin voltage.

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DC Characteristics (Continued)

Electrical Specification: Unless otherwise specified, operating temperature: –40°C ≤ T_A ≤ +85°C (Industrial), Supply Current: 5 mA ≤ I_{POS} ≤ 25 mA, R_{ISET} = 125 kΩ, C_{BYP} = 2 µF

Param. No.	Parameter		Sym	Min	Typ (1)	Max	Units	Conditions
MD020	DRAIN pin current		I_{DRAIN}	—	—	0.1	µA	$DRAIN_{TH}$ pin = V_{NEG}
MD021	SENSE pin current		I_{SENSE}	—	—	0.1	µA	
MD022	GATE pin current	Pull-up	I_{GATE}					SENSE pin = V_{NEG} GATE pin = V_{NEG} +4V
MD022A				-30	-50	-75	µA	V_{FB} = V_{NEG}
MD022B				-9	-17	-33	µA	V_{FB} = V_{NEG} + 500 mV
MD022C		Pull-down	I_{GATE}	31	49	72	mA	Any fault condition
MD023	UV_D pin current		I_{UVD}	-7	-10	-15	µA	UV_{TH} < V_{REFIN}
MD024A	TIMER pin current	Pull-up	I_{TIMER}	-100	-160	-200	µA	R_{ISET} = 125 kΩ, V_{REFIN} = 2.5V
MD024B		Pull-down		52	78	104	nA	R_{ISET} = 125 kΩ, V_{REFIN} = 2.5V R_{DISCH} = 1.6 MΩ
MD025	I_{SET} pin current		I_{ISET}	$V_{ISET(MIN)}$ $R_{ISET(MAX)}$	—	$V_{ISET(MAX)}$ $R_{ISET(MIN)}$	A	**See MD011**

Note 1: Data in the Typical (“Typ”) column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

2: Negative current is defined as current sourced by the pin.

3: All voltages are with respect to the V_{NEG} pin voltage.

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DC Characteristics (Continued)

Electrical Specifications: Unless otherwise specified, operating temperature: –40°C ≤ T_A ≤ +85°C (Industrial), Supply Current: 5 mA ≤ I_{POS} ≤ 25 mA, R_{ISET} = 125 kΩ, C_{BYP} = 2 µF.

Param #	Parameter	Sym	Min	Typ	Max	Units	Conditions
MD030	Input Low Voltage	V_{IL}					
MD031	ENABLE pin		V_{NEG}	—	0.8	V	
MD032	$\overline{\text{RESTART}}$ pin		V_{NEG}	—	0.8		
MD040	Input High Voltage	V_{IH}					
MD041	ENABLE pin		2.0	—	5.0	V	
MD042	$\overline{\text{RESTART}}$ pin		2.0	—	5.0	V	
MD050	Internal Resistance on UV_{HYS} pin	R_{UVHYS}	500	1200	2100	Ω	$V_{UVTH} < V_{REFIN}$, I_{UVHYS} = 30 µA
			50	100	—	MΩ	$V_{UVTH} > V_{REFIN}$, I_{UVHYS} = 30 µA
	Input Leakage Current (Notes 2, 3)						
MD060A	OV_{TH}, UV_{TH}, V_{FB}, OVO and UV_{HYS} pins	I_{IL}	-1	—	+1	µA	$V_{NEG} \le V_{PIN} \le 11V$, Pin at high-impedance
MD060B	V_{REFIN}, CL, SENSE, $DRAIN_{TH}$, ENABLE and RESTART pins		—	—	±1	µA	$V_{NEG} \le V_{PIN} \le 5V$, Pin at hi-impedance
MD070	Minimum current into ENABLE pin to disable MCP18480	I_{EN}	—	10	30	µA	I_{POS} = 5 mA, ENABLE = 0.8V
	Output Low Voltage	V_{OL}					
MD080	PWRGOOD pin		0	—	0.4	V	I_{OL} = 5 mA
	Output High Voltage	V_{OH}		—			
MD090	PWRGOOD pin		0.8 V_{POS}	0.96 V_{POS}	V_{POS}	V	I_{OH} = 2 mA, 7 mA ≤ I_{POS} ≤ 12 mA
MD100	Offset Voltage at the internal comparator input that is connected to the CL pin.	V_{CL}	-15	—	+15	mV	V_{FB} = 0

Note 1: All voltages are with respect to the V_{NEG} pin voltage.

2: The leakage currents on the ENABLE and $\overline{\text{RESTART}}$ pins are strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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1.1 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created using one of the following formats:

1.1.1 TIMING CONDITIONS

The temperature and voltages specified in Table 1-2 apply to all timing specifications, unless otherwise noted. Figure 1-1 specifies the load conditions for the timing specifications.

TABLE 1-1: SYMBOLOGY

1. TppS2ppS

T	
F	Frequency
E	Error

2. TppS

T	Time

Lowercase letters (pp) indicate the device pin.

Uppercase letters and their meanings:

S			
F	Fall	P	Period
FR	Fast Ramp	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

TABLE 1-2: AC TEMPERATURE AND VOLTAGE SPECIFICATIONS

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature: –40°C ≤ T_A ≤ +85°C (industrial) Operating voltage V_{DD} range as described in DC spec Section 1.0.

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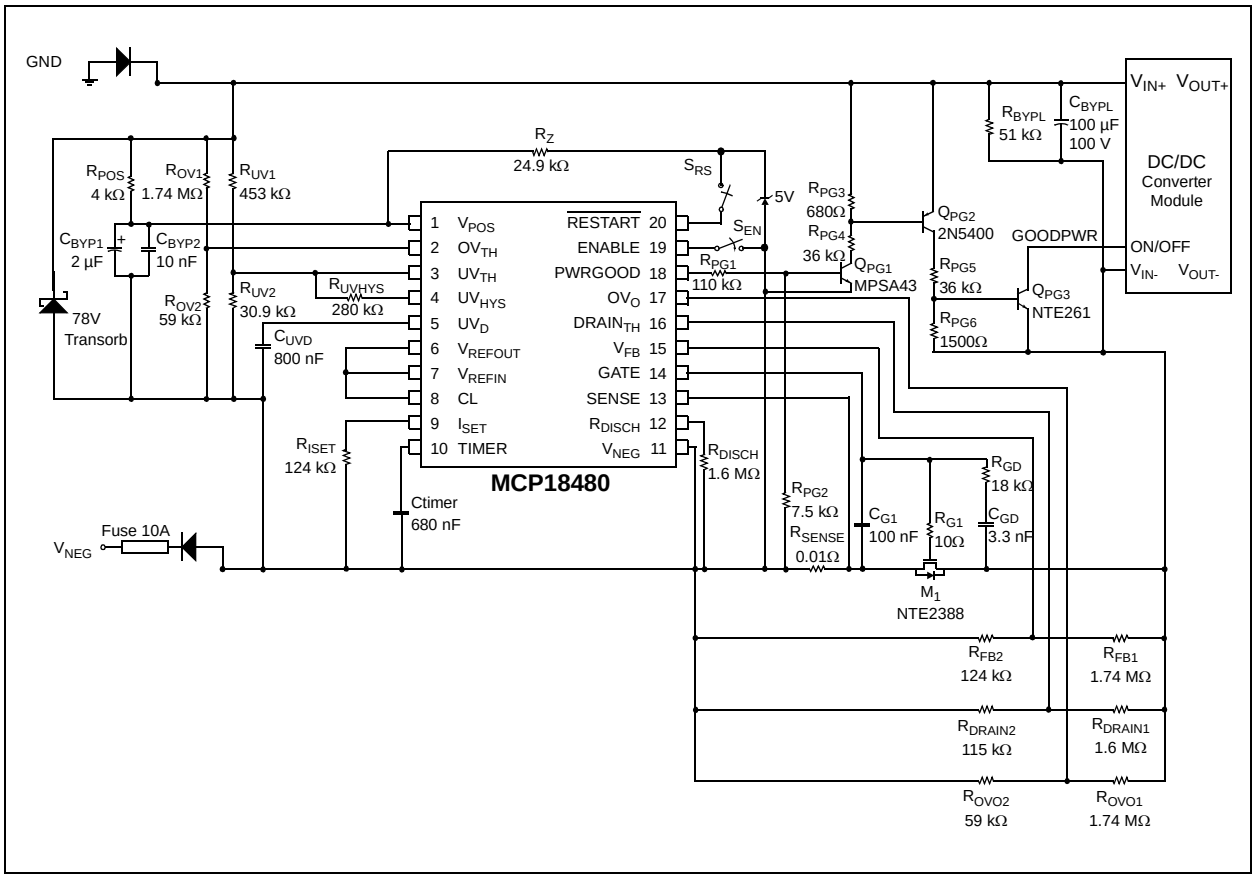
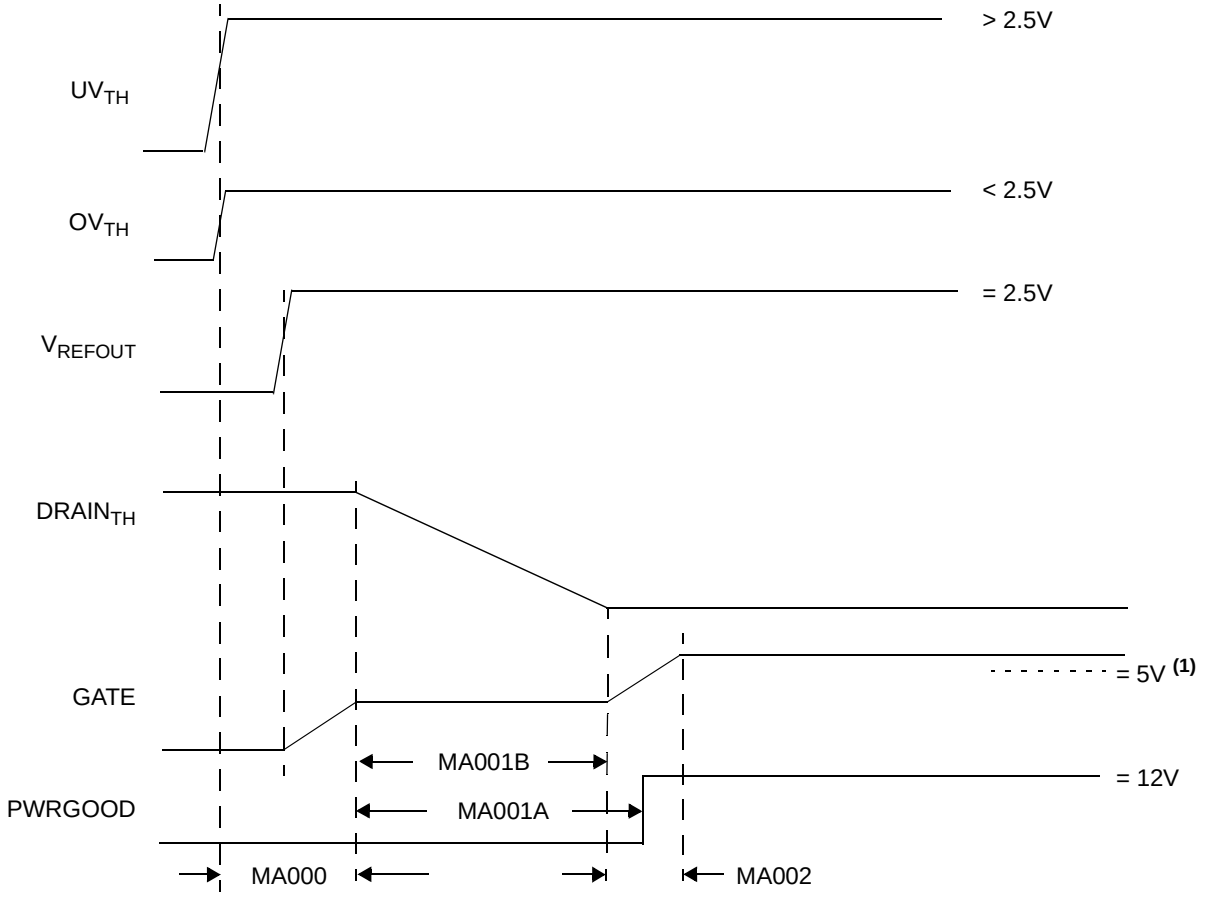


FIGURE 1-1: *Load Conditions for Device Timing Specifications.*

1.2 Timing Diagrams and Specifications



Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

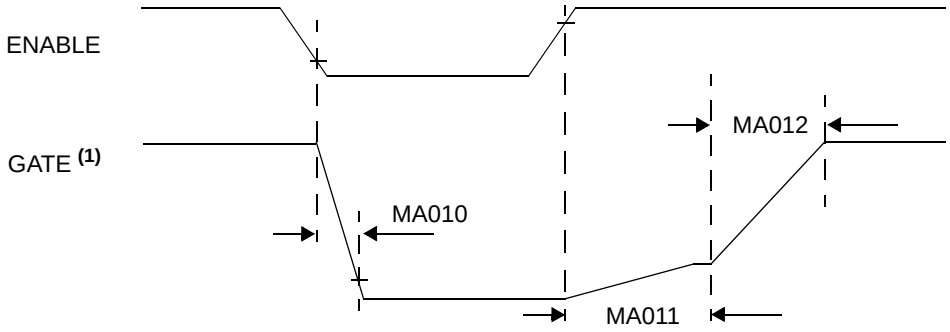
FIGURE 1-2: *Startup Waveforms.*

TABLE 1-3: STARTUP TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA000	UV_{TH}/OV_{TH} High (V_{POS} applied) to $DRAIN_{TH}$ falling	$T_{UVOV}H2_{DTH}F$	—	20.2	—	ms	
MA001A	$DRAIN_{TH}$ falling to PWRGOOD High	$T_{DTH}F2_{GATE}PGH$	—	19.3	—	ms	
MA001B	$DRAIN_{TH}$ falling to GATE Fast Ramp	$T_{DTH}F2_{GATE}FR$	—	13.1	—	ms	
MA002	GATE Fast Ramp to external FET fully enhanced	$T_{GATE}FR2FET_E$	—	16.1	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.

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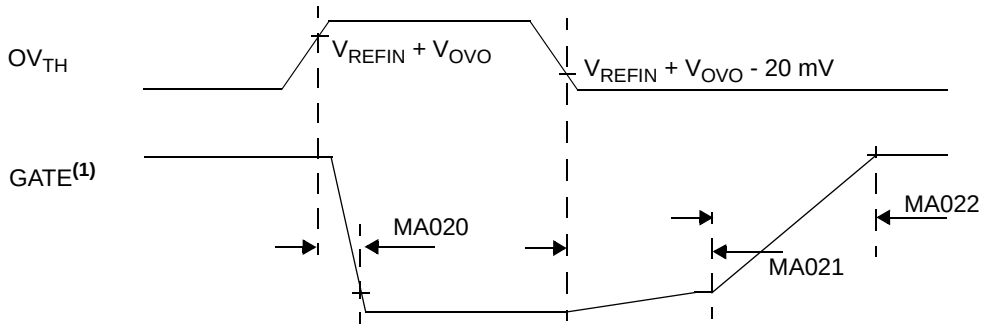
Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

FIGURE 1-3: *ENABLE-to-GATE Waveforms.*

TABLE 1-4: ENABLE-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA010	ENABLE Low to GATE Low	$T_{EN}L2_{GATE}L$	—	23.6	—	µs	
MA011	ENABLE High to GATE Fast Ramp	$T_{EN}H2_{GATE}FR$	—	41	—	ms	
MA012	GATE Fast Ramp to GATE High	$T_{GATE}FR2_{GATE}H$	—	17.8	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.



Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

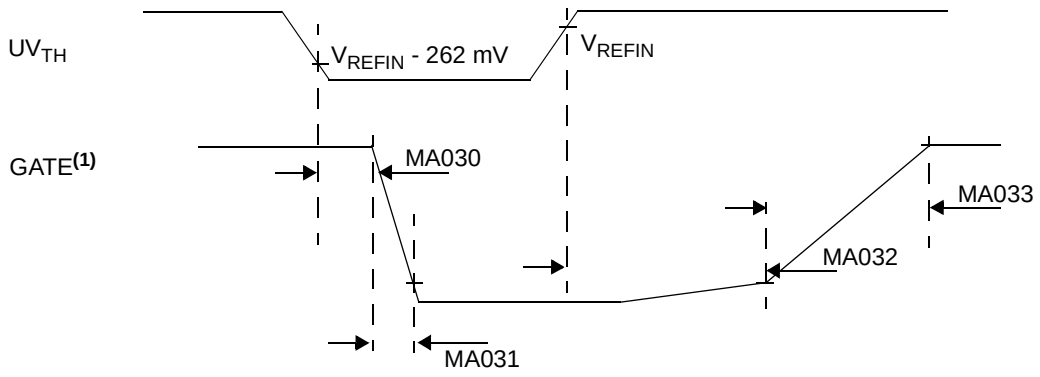
FIGURE 1-4: *OV_{TH}-to-gate Waveform.*

TABLE 1-5: OV_{TH}-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA020	OV_{TH} High to GATE Low	$T_{OV}H2_{GATE}L$	—	58.4	—	µs	
MA021	OV_{TH} Low to GATE Fast Ramp	$T_{OV}L2_{GATE}FR$	—	40.8	—	µs	
MA022	GATE Fast Ramp to GATE High	$T_{GATE}FR2_{GATE}H$	—	17.8	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.

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Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

FIGURE 1-5: *UV_{TH}-to-gate Waveform*

TABLE 1-6: UVTH-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ(1)	Max	Units	Conditions
MA030	UV_{TH} Low to GATE Falling Edge	$T_{UV}L2_{GATE}F$	—	108	—	µs	C_{UVD} = 800 nF
MA031	GATE High to GATE Low	$T_{GATE}H2_{GATE}L$	—	25.8	—	µs	
MA032	ENABLE High to GATE Fast Ramp	$T_{UV}H2_{GATE}FR$	—	40.4	—	ms	
MA033	GATE Fast Ramp to GATE High	$T_{GATE}FR2_{GATE}H$	—	58.4	—	ms	

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C, unless otherwise stated.
2: Minimum and maximum specifications will be provided in future revisions of this data sheet.

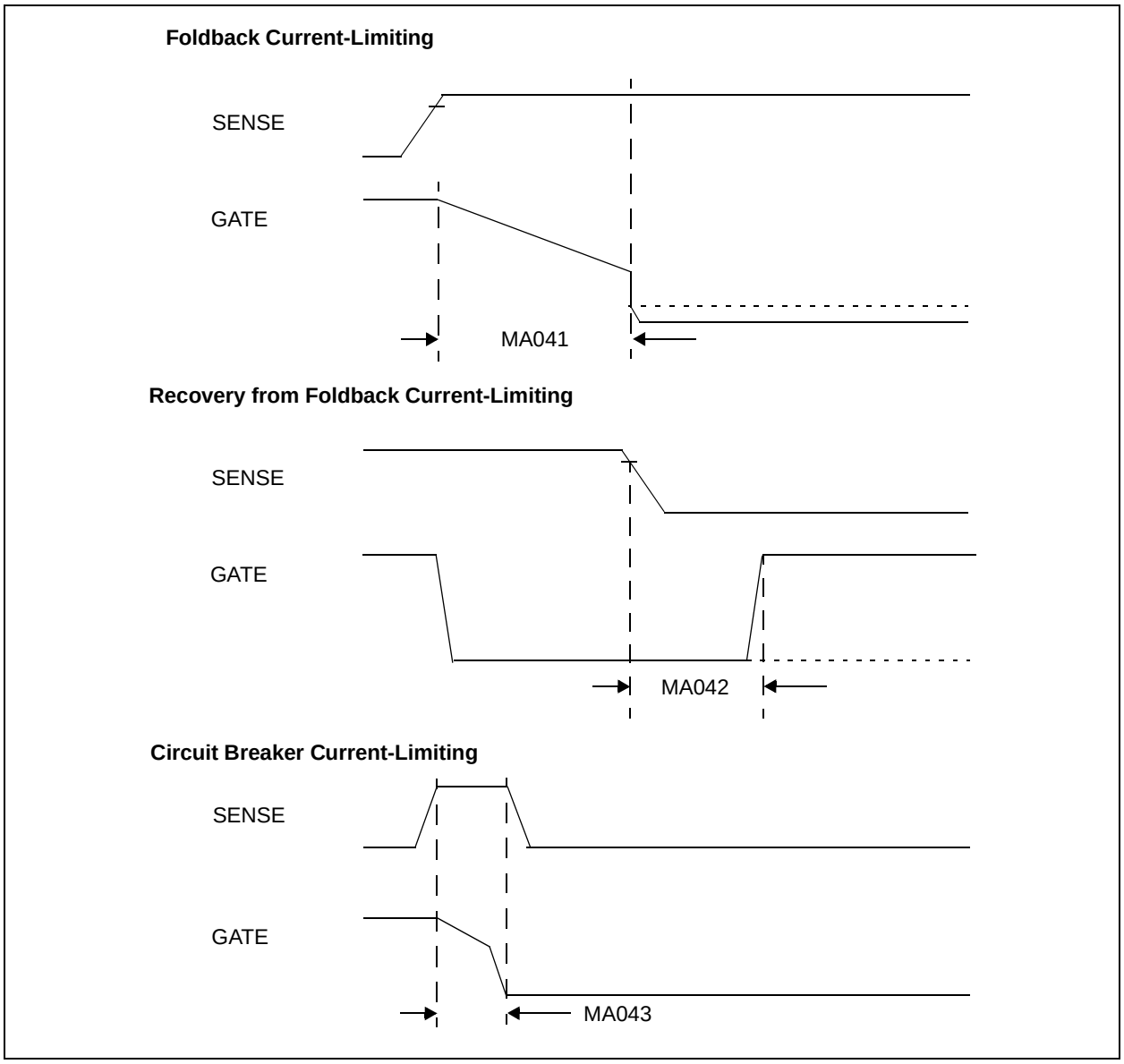


FIGURE 1-6: *Sense-to-gate Waveform.*

TABLE 1-7: SENSE-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA041	GATE Current Limit to GATE Off	$T_{GATE}CL2_{GATE}O$	—	5.5	—	ms	C_{TIMER} = 0.68 µF R_{ISET} = 124 kΩ
MA042	GATE Current Limit Recovery	$T_{GATE}CL$	—	10.2	—	ms	C_{TIMER} = 0.68 µF R_{ISET} = 124 kΩ
MA043	SENSE High to GATE Off	$T_{SENSE}H2_{GATE}O$	—	3.6	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.

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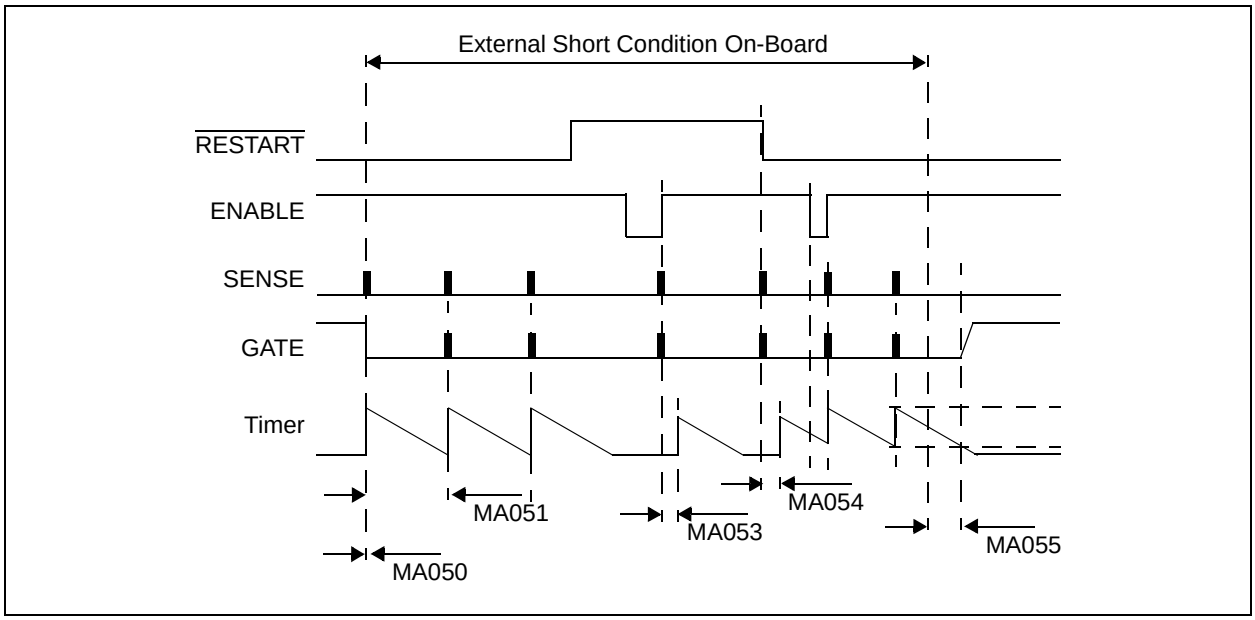


FIGURE 1-7: *Current Limit Waveform.*

TABLE 1-8: CURRENT LIMIT TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA050	External Short to Timer period start	$T_{SHORT}2_{TIMER}S$	—	171	—	mS	
MA051	Timer period	$T_{TIMER}P$	—	5.8	—	sec	C_{TIMER} = 0.68 µF R_{DISCH} = 1.6 MΩ
MA053	ENABLE High to Timer period start	$T_{ENABLE}H2_{TIMER}S$	—	30.5	—	mS	C_{TIMER} = 0.68 µF R_{DISCH} = 1.6 MΩ
MA054	$\overline{\text{RESTART}}$ Low to Timer period start	$T_{\overline{RESTART}}L2_{TIMER}S$	—	30.9	—	mS	C_{TIMER} = 0.68 µF R_{DISCH} = 11.6 MΩ
MA055	External Short removed to Timer off **Note 2**	$T_{NOSHORT}2_{TIMER}O$	—	5.8	—	sec	C_{TIMER} = 0.68 µF R_{DISCH} = 1.6 MΩ

Note 1: Minimum and maximum specifications will be provided in future revisions of this data sheet.

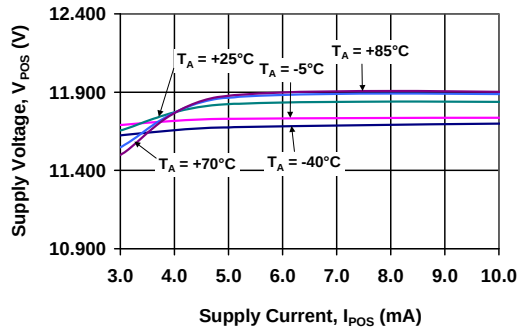
2: This is up to one additional timer period because the external short circuit is removed asynchronously to the timer. The timer must time out before normal operation returns.

NOTES:

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2.0 DC CHARACTERISTIC CURVES

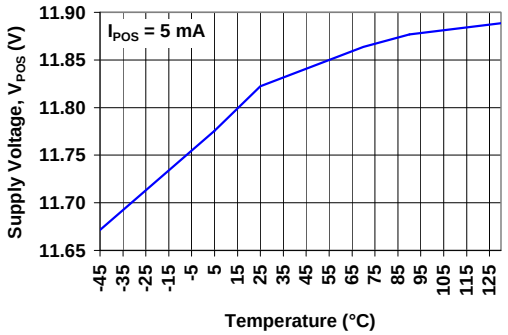
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



Data taken with the minimum following conditions:

V_{REFIN} = 2.5V, I_{SET} = 10 µA

FIGURE 2-1: *Supply Current (I_{POS}) vs. Supply Voltage (V_{POS}).*

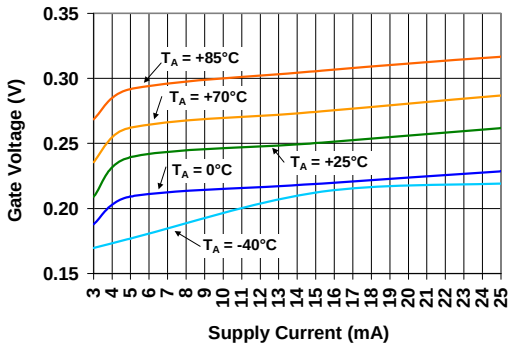


Data taken with the minimum following conditions:

Minimum Supply Current to bring V_{POS} into regulation

V_{REFIN} = 2.5V, I_{SET} = 10 µA

FIGURE 2-2: *Minimum Supply Current vs. Temperature.*



Data taken with the minimum following conditions:

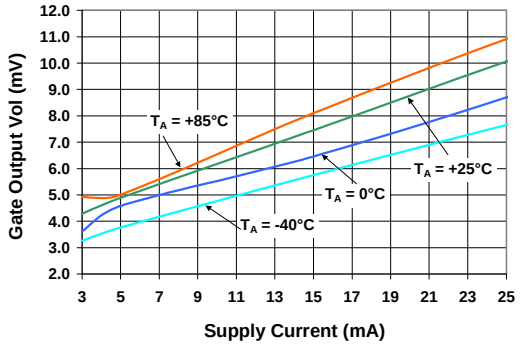
3 mA ≤ I_{POS} ≤ 30 mA

V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-3: *GATE Output High-Voltage (V_{POS}- V_{GATE}) vs. Supply Current (I_{POS}).*



Data taken with the minimum following conditions:

3 mA ≤ I_{POS} ≤ 30 mA

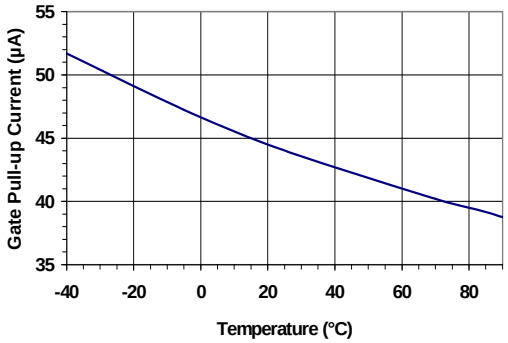
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
$V_{ENABLE} = V_{VNEG}$
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-4: *GATE Output Low-Voltage (V_{GATE} - V_{NEG}) vs. Supply Current (I_{POS}).*

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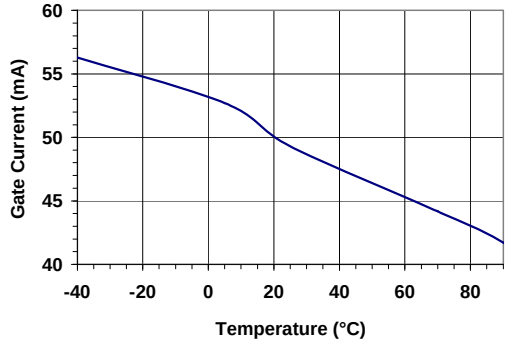
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)

FIGURE 2-5: *GATE Source (Pull-Up) Current vs. Temperature.*



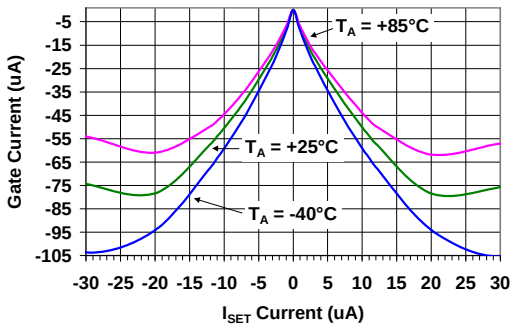
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{GATE} > 0.5V$
$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
$V_{ENABLE} = V_{VNEG}$
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-6: *GATE Sink (Pull-Down) Current vs. Temperature.*



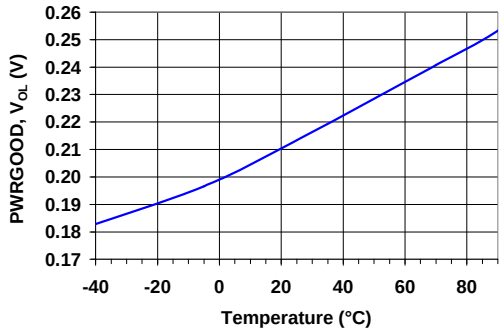
Data taken with the minimum following conditions:

-50 µA µA < I_{ISET} < 50 µA ($I_{ISET} \neq 0$)
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
$_{VREFIN}$ = 2.5V

Note 1:

V_{GATE} > 0.5V
$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-7: *GATE Source Current vs. I_{SET} Pin Current.*



Data taken with the minimum following conditions:

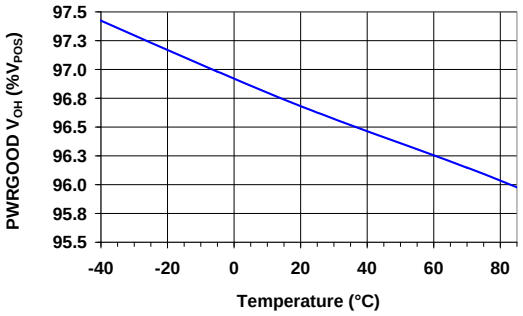
I_{LOAD} = 1 mA
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-8: *PWRGOOD Output Low Voltage (V_{OL}) vs. Temperature.*

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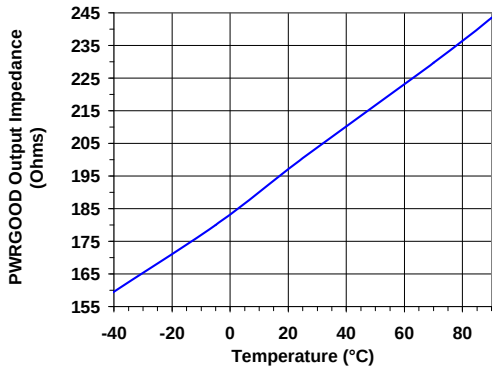
Data taken with the minimum following conditions:

I_{LOAD} = -1 mA
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-9: *PWRGOOD Output High-Voltage (V_{OH}) vs. Temperature.*



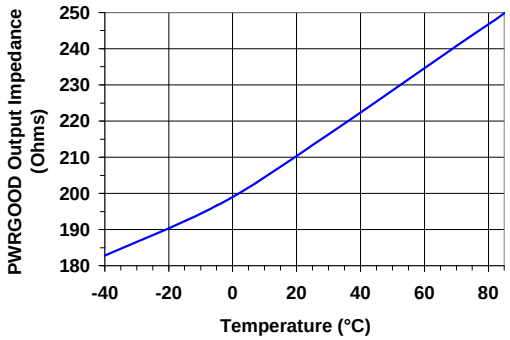
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-10: *PWRGOOD Output High-Impedance vs. Temperature.*



Data taken with the minimum following conditions:

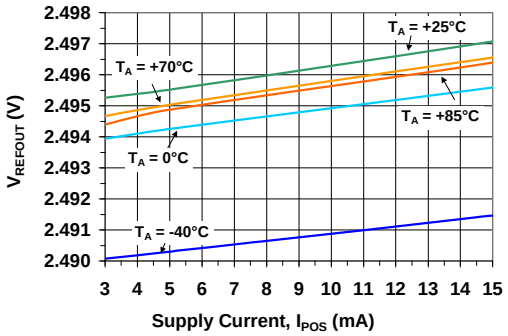
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-11: *PWRGOOD Output Low-Impedance vs. Temperature.*

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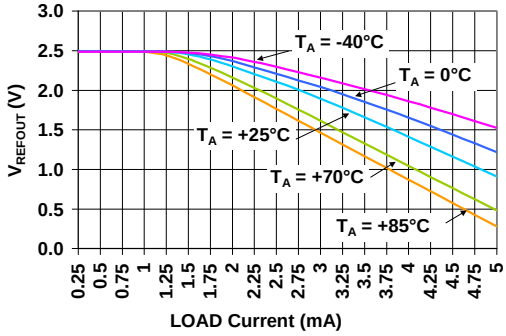


Data taken with the minimum following conditions:

3 mA ≤ I_{POS} ≤ 30 mA

V_{REFIN} = 2.5V, I_{SET} = 10 µA

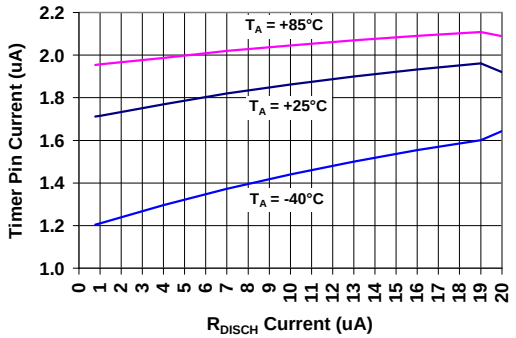
FIGURE 2-12: *V_{REFOUT} vs. Supply Current (I_{POS}).*



Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, Iset = 10 µA

FIGURE 2-13: *V_{REFOUT} vs. LOAD.*



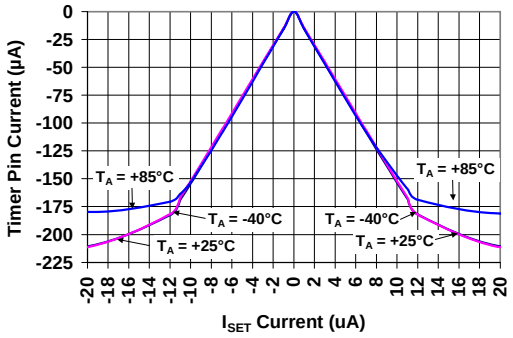
Data taken with the minimum following conditions:

$-50\ \mu A < I_{ISET} < 50\ \mu A$ ($I_{ISET} \neq 0$)
I_{POS} = 5 mA
(V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-14: *TIMER Pin Output Low Current vs. R_{DISCH} Current.*



Data taken with the minimum following conditions:

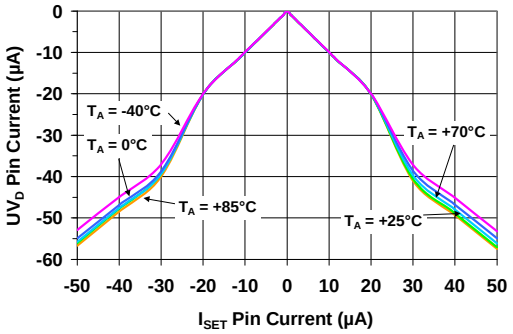
$-50\ \mu A < I_{ISET} < 50\ \mu A$ ($I_{ISET} \neq 0$)
I_{POS} = 5 mA
(V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} \geq 100mV$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-15: *TIMER Pin Output High Current vs. I_{SET} Current.*

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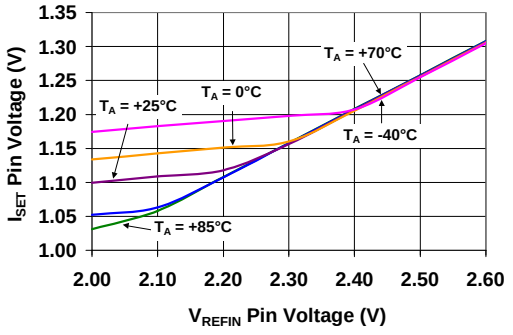
Data taken with the minimum following conditions:

$-50\ \mu A < I_{ISET} < 50\ \mu A\ (I_{ISET} \neq 0)$
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

Note 1:

$V_{UVTH} < V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

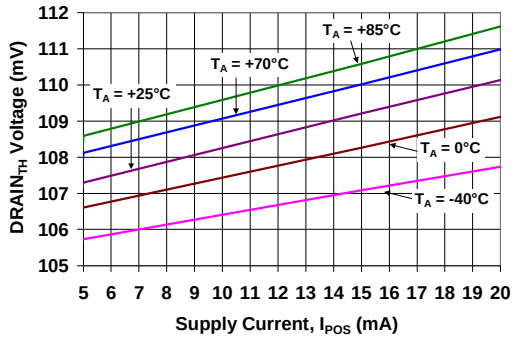
FIGURE 2-16: *UV_D Pin Current vs. I_{SET} Pin Current.*



Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
Iset = 10 µA

FIGURE 2-17: *I_{SET} Pin Voltage vs. V_{REFIN} Pin Voltage.*



Data taken with the minimum following conditions:

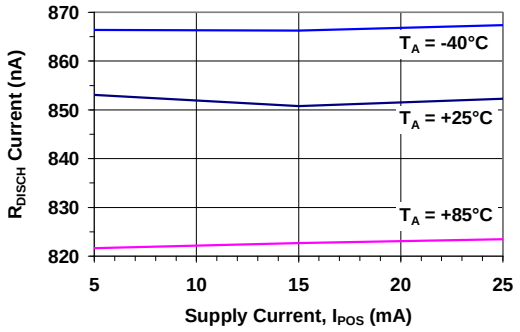
$3\ mA \leq I_{POS} \leq 30\ mA$

V_{REFIN} = 2.5V, I_{SET} = 10 µA
Determined by PWRGOOD signal

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-18: *DRAINTH Threshold Voltage vs. Supply current (I_{POS}).*



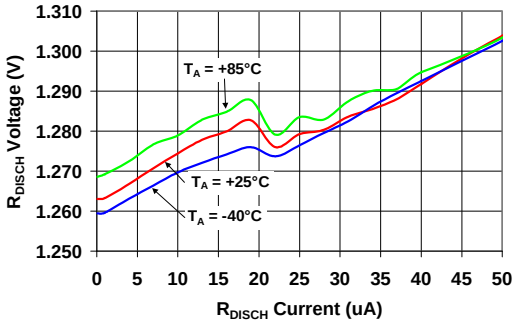
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
R_{DISCH} = 16 MΩ

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-19: *R_{DISCH} Current vs. Supply Current (I_{POS}).*



Data taken with the minimum following conditions:

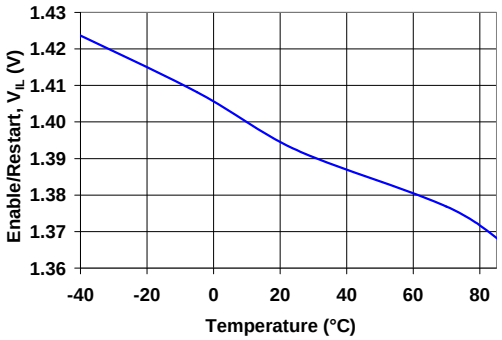
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
I_{RDISCH} from 100 nA to 10 µA (500 nA steps)

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-20: *R_{DISCH} Voltage vs. R_{DISCH} Current.*

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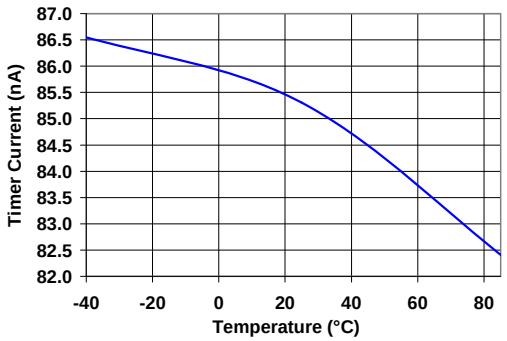
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Determined by GATE voltage

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-21: *ENABLE/$\overline{\text{RESTART}}$ Pin Trip Point Voltage vs. Temperature.*



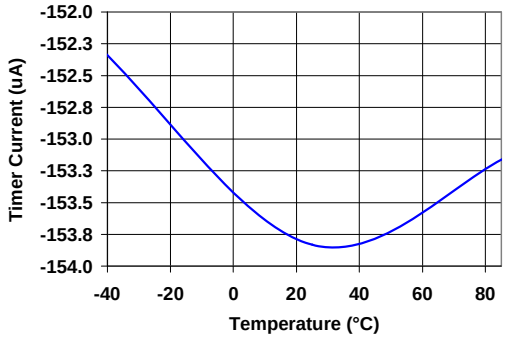
Data taken with the minimum following conditions:

R_{DISCH} = 16 MΩ
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
0.1V ≤ V_{TIMER} ≤ 1.25V

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{NEG}$, I into device
V_{NEG} + 100mV, I out of device
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-22: *TIMER Output Sink Current vs. Temperature.*



Data taken with the minimum following conditions:

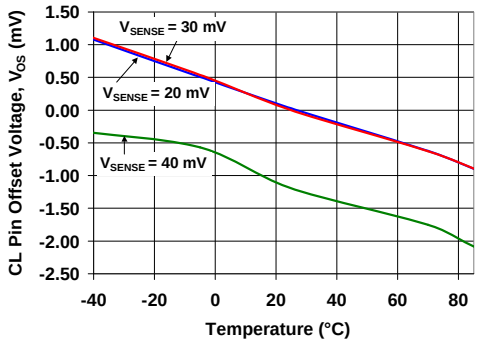
R_{DISCH} = 16 MΩ
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
0.1V ≤ V_{TIMER} ≤ 1.25V

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{NEG}$, I into device
V_{NEG} + 100mV, I out of device
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-23: *TIMER Output Source Current vs. Temperature.*

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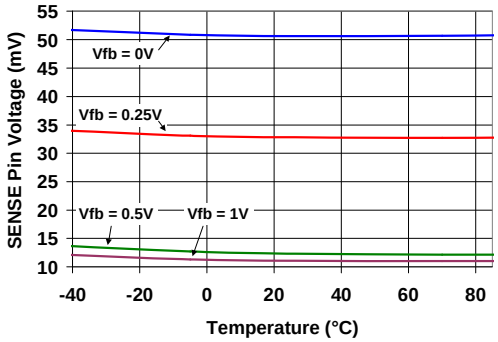
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
V_{SENSE} = 25mV
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-24: *CL pin Input Offset Voltage vs. Temperature.*



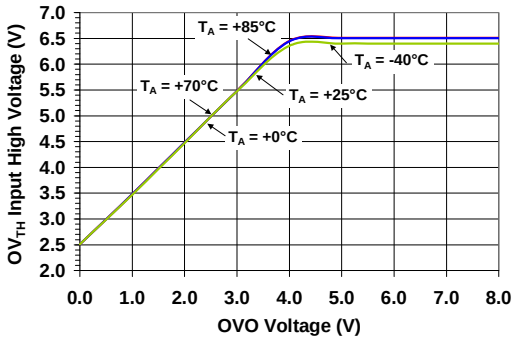
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Use TIMER pin as indicator

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{VFB} = V_{NEG}$, V_{NEG}+ 250mV,
V_{NEG}+500mv, V_{NEG}+1V
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-25: *SENSE Pin Input Threshold vs. Temperature.*



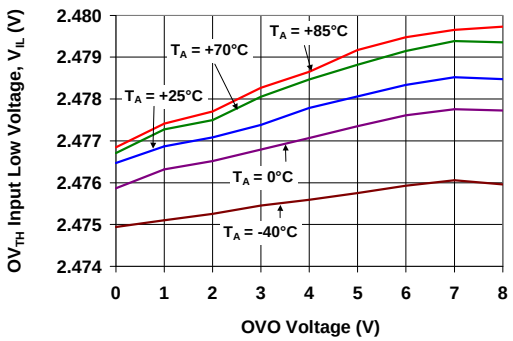
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
OVO = V_{NEG} to 8V
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Use PWRGOOD pin as indicator

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-26: *OV_{TH} Input Rising Threshold vs. OVO Voltage.*



Data taken with the minimum following conditions:

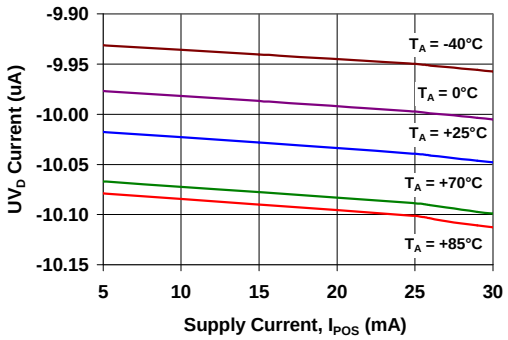
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
OVO = V_{NEG} to 8V
V_{REFIN} = 2.5V, I_{SET}= 10 µA
Use PWRGOOD pin as indicator

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-27: *OV_{TH} Input Falling Threshold vs. OVO Voltage.*

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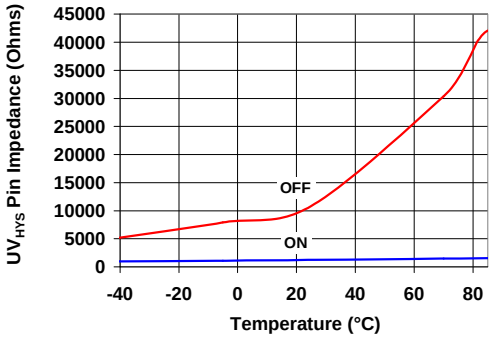
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} < V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-28: *UV_D Current vs. Supply Current (I_{POS}).*



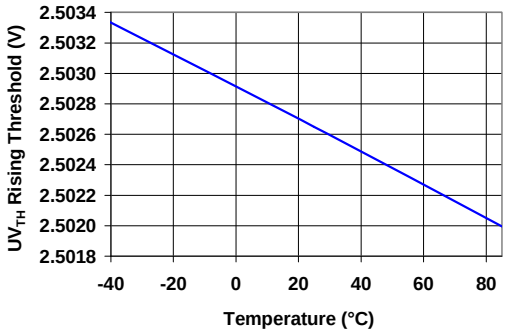
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
$UV_{TH} < V_{REFIN}$, $UV_{TH} > V_{REFIN}$
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-29: *UV_{HYS} Pin Impedance vs. Temperature.*



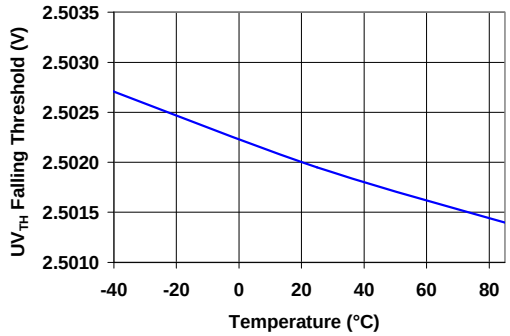
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Use PWRGOOD pin as indicator

Note 1:

$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-30: *UV_{TH} Input Rising Threshold vs. Temperature.*



Data taken with the minimum following conditions:

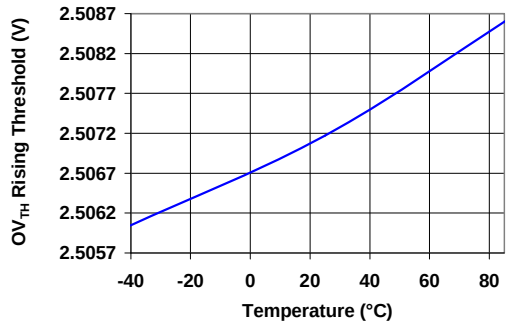
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Use PWRGOOD pin as indicator

Note 1:

$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-31: *UV_{TH} Input Falling Threshold vs. Temperature.*

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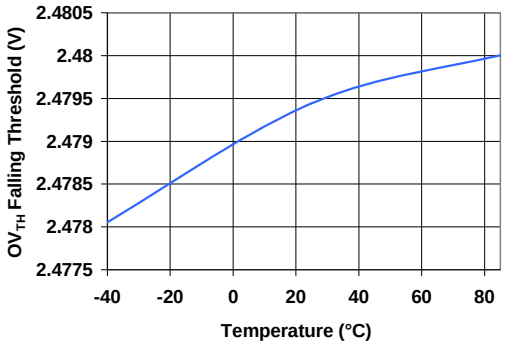
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Use PWRGOOD pin as indicator

Note 1:

$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-32: *OV_{TH} Input Rising Threshold vs. Temperature.*



Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
$V_{UVHYS} = V_{NEG}$
Use PWRGOOD pin as indicator

Note 1:

$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-33: *OV_{TH} Input Falling Threshold vs. Temperature.*

NOTES:

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3.0 PIN DESCRIPTIONS

TABLE 3-1: MCP18480 PIN DESCRIPTIONS

Pin Name	Pin Number	Pin Direction	Buffer Type	Description
	SSOP			
V_{POS}	1	I	P	Positive supply input. Internal Shunt Regulator connected between V_{POS} and V_{NEG} limits the potential to 12V between these two pins. A series resistor must be placed on the V_{POS} pin to limit the current into the device.
OV_{TH}	2	I	A	Overvoltage protection threshold. An external resistor divider network is connected to this input pin to program the overvoltage protection threshold. The selected external resistor values for the OV_{TH} to system ground and OV_{TH} to V_{NEG} resistors should have currents in the 1 mA range. A typical Overvoltage threshold is -76V. Internal hysteresis in the overvoltage input comparator will allow proper operation once V_{NEG} falls below the selected threshold.
UV_{TH}	3	I	A	Undervoltage lockout threshold. An external resistor divider network is connected to this input pin to program the undervoltage lockout threshold. If the voltage on UV_{TH} is less than V_{NEG} + 2.5V, the undervoltage comparator will trip, indicating an Undervoltage condition. An external hysteresis resistor can be used to set the high-to-low (V_{THF}) threshold below the low-to-high (V_{THR}) threshold. For telecom network equipment, it is desirable to have shutdown occur at -38.5V and the startup set at -43.0V.
UV_{HYS}	4	I	A	Undervoltage internal comparator hysteresis. An external resistor is connected between this input to the UV_{TH} input pin to adjust the hysteresis of the internal Undervoltage comparator. Since it is desirable to shut down at -38.5V and restart at -43.0V in telecom switch equipment.
UV_D	5	I/O	A	Undervoltage event delay. An external capacitor is connected to this input pin to set the delay between when the UV_{TH} pin drops below the trip point specified by the voltage on the V_{REFIN} pin and when the system shutdown occurs (causing the PWRGOOD pin to be driven to an inactive level and the GATE pin to be pulled to the V_{NEG} pin voltage level). The UV_D pin sources a current equivalent to the I_{ISET} (in typical applications, the I_{ISET} current equals 10 µA), which charges this external capacitor while an internal comparator compares this voltage on the UV_D pin to $\|V_{REFIN}\|/2$. Typically, for telecom equipment, the system is expected to shut down when the input voltage falls below -38.5V (±1.0V DC) for greater than 100 ms.

Legend: TTL = TTL compatible input
I = Input
P = Power
A = Analog
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS-compatible input
D = Digital

TABLE 3-1: MCP18480 PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Direction	Buffer Type	Description
	SSOP			
V_{REFOUT}	6	O	A	Reference output. Internal reference output voltage (typically 2.5V). Usually tied back to the V_{REFIN} pin unless an external high-precision reference voltage is desired.
V_{REFIN}	7	I	A	Reference input. This pin allows a high-precision reference voltage for the following functions: • Undervoltage Comparator • Overvoltage Comparator • DRAIN Comparator • Current Limit Timer If the precision of the V_{REFOUT} output voltage is acceptable, tie the V_{REFOUT} pin to the V_{REFIN} pin.
CL	8	I	A	Current Limit. Input used to set the maximum current limit threshold allowed by the system via a resistor divider network (with the resistor R_{CL1} between the V_{REFIN} pin and the CL pin and resistor R_{CL} between the V_{NEG} pin and the CL pin). If the voltage across the sense resistor exceeds the voltage on the CL pin, it implies that there is excessive current over the allowed limit and forces the GATE pin to the V_{NEG} pin voltage level without delay.
I_{SET}	9	I	A	Current source set. Establishes the internal I_{SOURCE} for the following: • Undervoltage Delay • Current Limit Timer • GATE Pin Source Current An external resistor R_{ISET} from the I_{SET} pin must be connected to either the V_{NEG} pin or the V_{REFIN} pin to set I_{BIAS}, which will then establish the current sources throughout the device. The I_{BIAS} current is the same for either connection. Connecting the R_{ISET} resistor to the V_{NEG} pin will establish the PWRGOOD pin output polarity to be active-high. Connecting the R_{ISET} resistor to the V_{REFIN} pin will establish the PWRGOOD pin output polarity to be active-low.

Legend: TTL = TTL compatible input
I = Input
P = Power
A = Analog
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS-compatible input
D = Digital

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TABLE 3-1: MCP18480 PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Direction	Buffer Type	Description
	SSOP			
TIMER	10	I	A	Current Limit Timer. The value of the external capacitor (C_{TIMER}) connected to the TIMER pin sets the two time periods used during a current-limit event. These are: • The time that the GATE pin will limit the current through the external FET • The time that the GATE pin will disable the external FET During current limit, a pull-up current source charges up the external capacitor. Until the voltage on the TIMER pin reaches $V_{REFIN}/2$, the GATE pin is driven to maintain a reduced current flow determined by the V_{DS} of the external FET. While the capacitor is being discharged by the pull-down current (pull-up current is off), the GATE pin is at V_{NEG} and the PWRGOOD pin is deasserted. When the TIMER voltage falls below approximately 100 mV, the GATE pin turns on, if the $\overline{\text{RESTART}}$ pin is low, to reset the internal fault latch. If the $\overline{\text{RESTART}}$ pin is high, the GATE pin remains off until the ENABLE pin is forced low. It is then forced high or the $\overline{\text{RESTART}}$ pin is forced low (asserted). The PWRGOOD pin reasserts after the voltages on the $DRAIN_{TH}$ and GATE pins meet the appropriate conditions. The TIMER pin pull-up current is proportioned to the I_{ISET} current (approximately a multiple of 16).
V_{NEG}	11	I	P	Negative supply input. The negative voltage applied to the board by the backplane (typically the most negative voltage in the system).
R_{DISCH}	12	I	A	External MOSFET activation delay. An external resistor (R_{RDISCH}) is connected between the R_{DISCH} pin and the V_{NEG} pin and is used to set the delay between the deactivation and activation of the external pass MOSFET during a current-limit event. The delay is set by the values of the external capacitor (C_{TIMER}) and the external resistor (R_{RDISCH}). The formulas are: $T_{DEACT} = (C_{TIMER} \times R_{ISET}) / 16$ $T_{ACT} = (9.2 \times R_{RDISCH} \times C_{TIMER})$

Legend: TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
I = Input O = Output
P = Power CMOS = CMOS-compatible input
A = Analog D = Digital

TABLE 3-1: MCP18480 PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Direction	Buffer Type	Description
	SSOP			
SENSE	13	I	A	Over-current sense. The voltage on the SENSE input pin is used to detect over-current conditions in the load connected to the external MOSFET. This pin is directly connected to the source of the MOSFET, with an external resistor (R_{SENSE}) (typically a low resistance) connected between the source of the MOSFET and V_{NEG}.
GATE	14	O	A	MOSFET gate driver. The GATE output pin attaches to the gate of the external MOSFET. The voltage on the GATE pin is pulled to the voltage on the V_{NEG} pin whenever the voltage on the UV_{TH} pin is less than the voltage on the V_{REFIN} pin, or the voltage on the OV_{TH} pin is greater than the voltage on the V_{REFIN} pin. The GATE pin is also pulled to the voltage on the V_{NEG} pin when the ENABLE input pin is low. When current limit is reached, the voltage on the GATE pin is adjusted to maintain a constant voltage across the R_{SENSE} resistor while the C_{TIMER} capacitor starts to charge. When the voltage on C_{TIMER} exceeds $V_{REFIN}/2$, the GATE pin is pulled to V_{NEG} to turn off the external MOSFET. A RC network can be added from the GATE pin to the drain of the external MOSFET, along with a capacitor from the GATE pin to the V_{NEG} pin, to control the slew rate of the GATE pin. The GATE pin pull-up current is proportioned to the I_{ISET} current.
V_{FB}	15	I	A	External MOSFET drain monitor. The V_{FB} input pin monitors the voltage at the drain of the external power MOSFET switch with respect to the voltage on the V_{NEG} pin for use by the internal foldback circuitry. An external resistor divider network (R_{FB1} and R_{FB2}) is attached between the drain of this external MOSFET and the V_{NEG} pin (R_{FB1} is connected between the drain of the external MOSFET and the V_{FB} pin, while R_{FB2} is connected between the V_{FB} pin and the V_{NEG} pin). This prevents high-voltage breakdown of the V_{FB} input.
$DRAIN_{TH}$	16	I	A	MOSFET drain comparator threshold. This pin is used during the power-up sequence of the inserted board, and after any fault condition that 'turns off' the GATE pin drive. The voltage on the pin indicates when the external FET is fully enhanced by comparing the pin voltage to an internal reference voltage (approximately 100 mV derived from the internal band gap reference). An external resistor divider network (R_{DRAIN1} and R_{DRAIN2}) is attached between the drain of this external MOSFET and the V_{NEG} pin (R_{DRAIN1} is connected between the drain of the external MOSFET and the $DRAIN_{TH}$ pin while R_{DRAIN2} is connected between the $DRAIN_{TH}$ pin and the V_{NEG} pin).

Legend: TTL = TTL compatible input
I = Input
P = Power
A = Analog
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS-compatible input
D = Digital

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TABLE 3-1: MCP18480 PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number SSOP	Pin Direction	Buffer Type	Description
OVO	17	I	A	Overvoltage detect. Typically for normal operation. This pin is tied to V_{NEG}. This feature allows the overvoltage detection input to monitor an overvoltage condition across the power module. The voltage is sensed at the drain of the external MOSFET. The voltage across the load is internally determined based upon: • The voltage difference between system ground and the voltage on the V_{NEG} pin • The voltage difference between the drain of the external FET and the voltage on the V_{NEG} pin An external resistor divider network (R_{OVO1} and R_{OVO2}) is attached between the drain of the external MOSFET and the V_{NEG} pin (R_{OVO1} is connected between the drain of the external MOSFET and the OVO pin, while R_{OVO2} is connected between the OVO pin and the V_{NEG} pin). When the voltage across the external MOSFET (source-to-drain) equals system ground voltage (- V_{NEG} +), the maximum desired load voltage, the GATE pin is forced to the voltage on the V_{NEG} pin (disabling the external MOSFET). To detect Overvoltage on the board (instead of the load) directly, connect the OVO pin to the V_{NEG} pin.
PWRGOOD	18	O	D	Power Good indicator. This state of the output is determined by four conditions. These are: • Undervoltage • Overvoltage • Current Limit • External FET is fully-enhanced (from $DRAIN_{TH}$ pin on power-up) PWRGOOD is a CMOS logic voltage (V_{NEG} or V_{NEG}+12V). PWRGOOD is active when the device has completed power-up and the system is neither in an Undervoltage or Overvoltage condition. Connecting the R_{ISET} pin to the V_{NEG} pin configures the PWRGOOD pin to be active high. Connecting the R_{ISET} pin to the V_{REF} pin configures the PWRGOOD pin to be active low.
ENABLE	19	I	TTL	Enable Gate driver. Used to enable the GATE pin and assert the PWRGOOD pin. The ENABLE pin is active-high and is internally pulled up to 5V. This pin is pulled low by the user to clear the current limit latch when a current-limit fault occurs with $\overline{\text{RESTART}}$ high, or to disable the GATE pin. H = Enable the GATE and PWRGOOD pins. L = Disables the GATE pin, deasserts the PWRGOOD pin and clears current limit latch. When the ENABLE pin is high, fault conditions will disable the GATE pin and deasserts the PWRGOOD pin.

Legend: TTL = TTL compatible input
I = Input
P = Power
A = Analog
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS-compatible input
D = Digital

TABLE 3-1: MCP18480 PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Direction	Buffer Type	Description
	SSOP			
$\overline{\text{RESTART}}$	20	I	TTL	Auto-restart enable. Enables the auto-restart feature of the device after an over-current fault. L = The internal fault latch is reset and the device attempts to restart with a frequency determined by the values of the external components C_{TIMER} and R_{DISCH}. H = The auto-restart is disabled, allowing the GATE pin to remain at the V_{NEG} pin voltage after an over-current fault. Internally pulled down to the V_{NEG} pin voltage.

Legend: TTL = TTL compatible input
I = Input
P = Power
A = Analog
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS-compatible input
D = Digital

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4.0 APPLICATIONS INFORMATION

The MCP18480 can be programmed to have the PWRGOOD signal be either active-high or active-low via the I_{SET} pin and the connection of the external R_{ISET} resistor (see Section 6.8.8, “Bias Block”). If the R_{ISET} resistor is connected between I_{SET} and V_{NEG}, the PWRGOOD output pin is an active-high signal. If the R_{ISET} resistor is connected between I_{SET} and V_{REFIN}, the PWRGOOD output pin is an active-low signal.

For systems using an active-low-enabled DC/DC converter module, the MCP18480 should be programmed for a high-active PWRGOOD output. Tying the R_{ISET} resistor to the V_{NEG} pin configures the PWRGOOD to be an active-high signal. The active-high PWRGOOD switches on the external NPN and the collector of the external NPN (labeled as GOODPWR) is pulled to V_{NEG}, enabling a low-active GOODPWR and resulting in enabling the DC/DC module.

For active-high DC/DC converter modules, the MCP18480 should be programmed for a low active PWRGOOD output. Connecting R_{ISET} to the V_{REFIN} pin will enable an active-low PWRGOOD output. Refer to Figure 4-1 and Figure 4-2 for schematics.

Figure 4-1 shows a typical telecom application circuit where the DC/DC module is active-high. Figure 4-2 shows a typical telecom application circuit where the DC/DC module is active-low. The polarity of the MCP18480’s PWRGOOD pin (active-high or active-low) is dependant on the state of the I_{SET} pin.

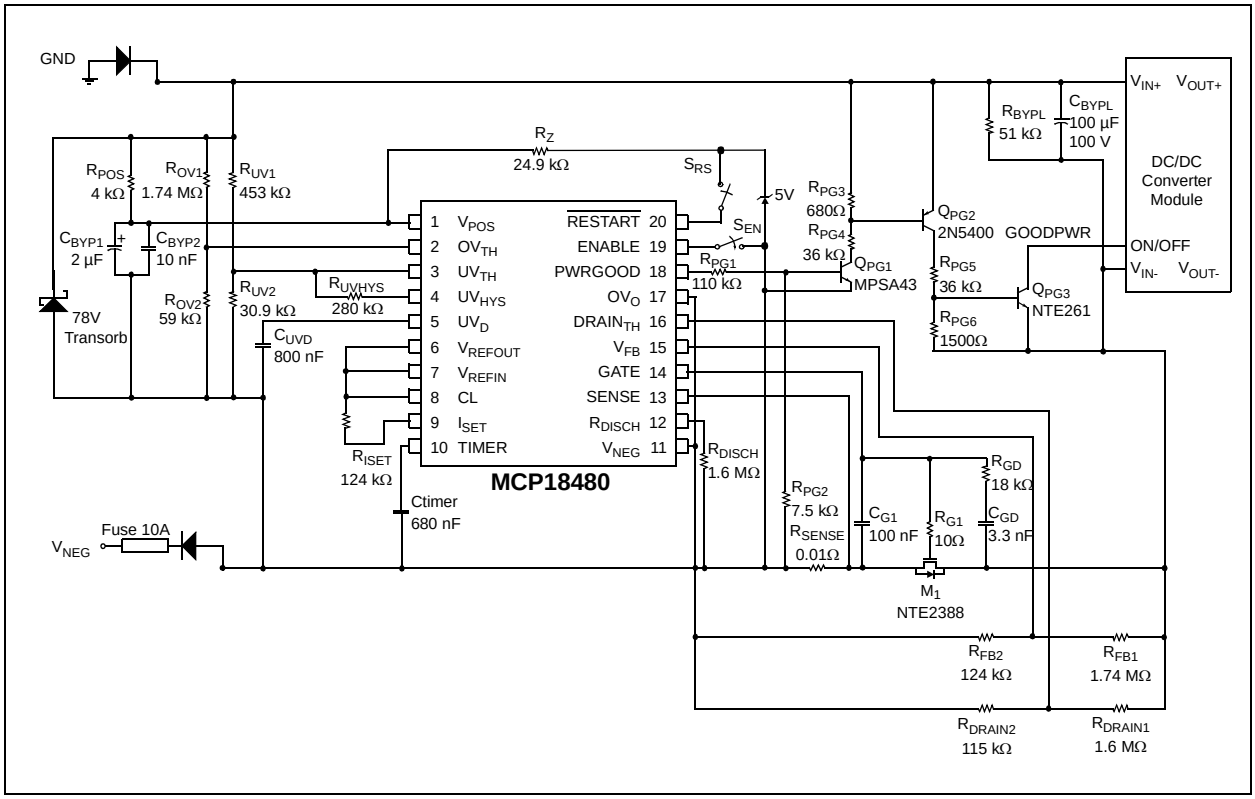


FIGURE 4-1: *Typical Operating Circuit for Telecom Applications with Active-High power Module - foldback current limit enabled.*

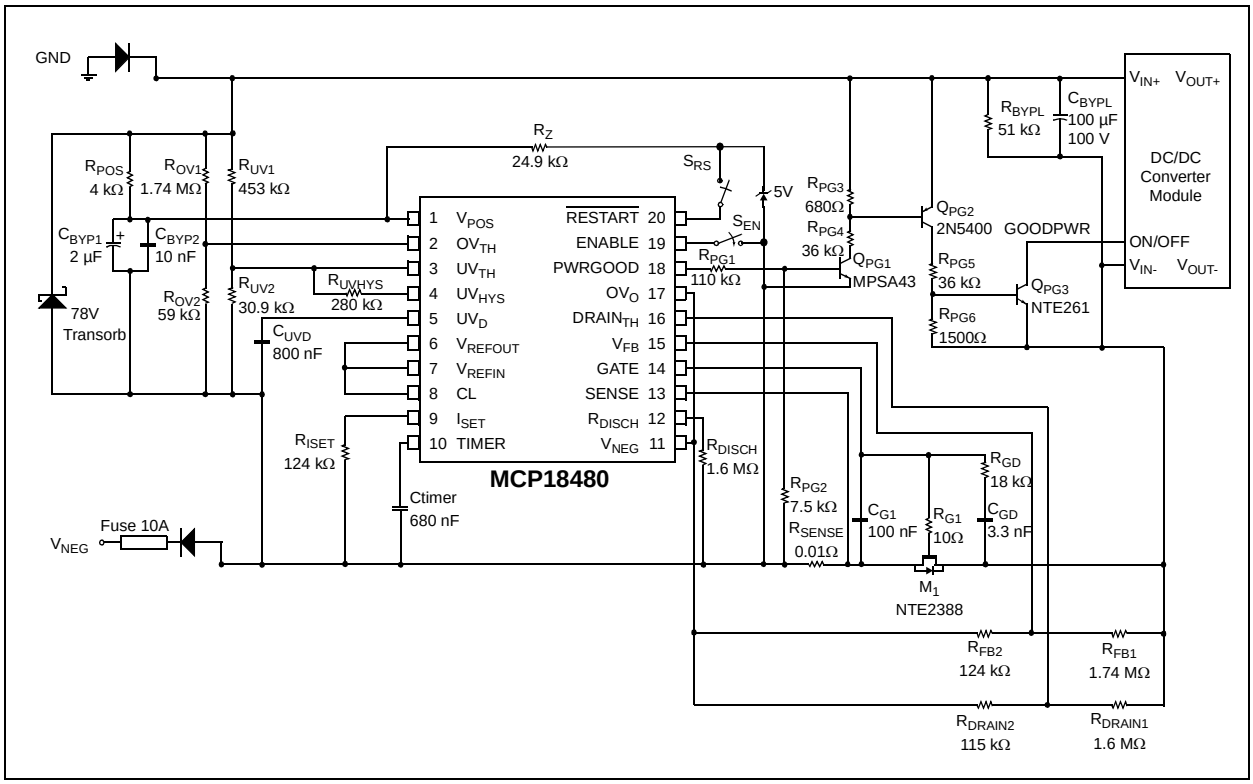


FIGURE 4-2: *Typical operating circuit for telecom applications with Active-Low power Module - foldback current limit enabled.*

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The MCP18480 can typically be implemented in a backplane system in one of two methods. Figure 4-3 shows a system where the backplane integrates the MCP18480 for every slot. Figure 4-4 shows a system where the backplane does not integrate the MCP18480s and each card that will be inserted into any slot is required to integrate the MCP18480.

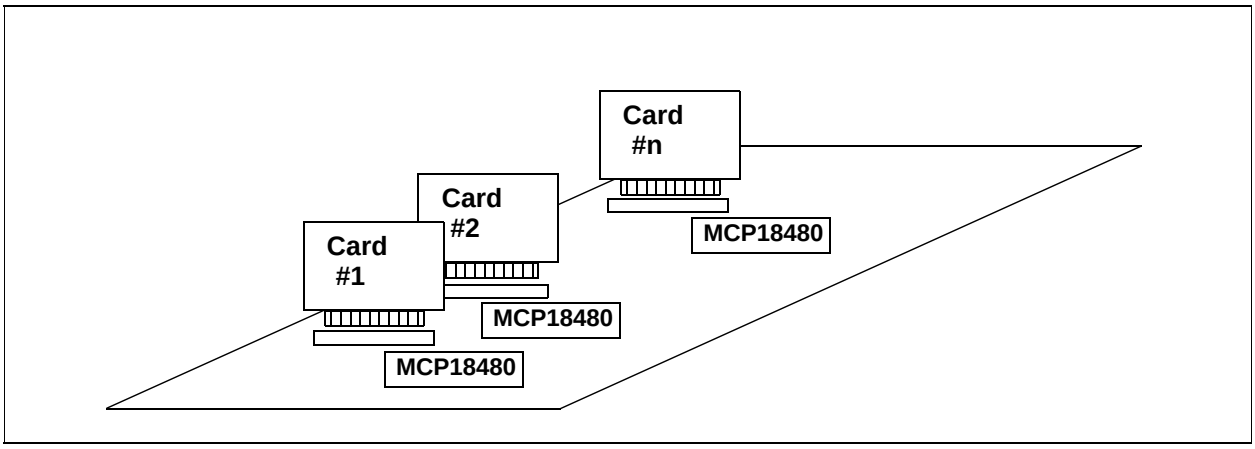


FIGURE 4-3: *Backplane System Block Diagram #1.*

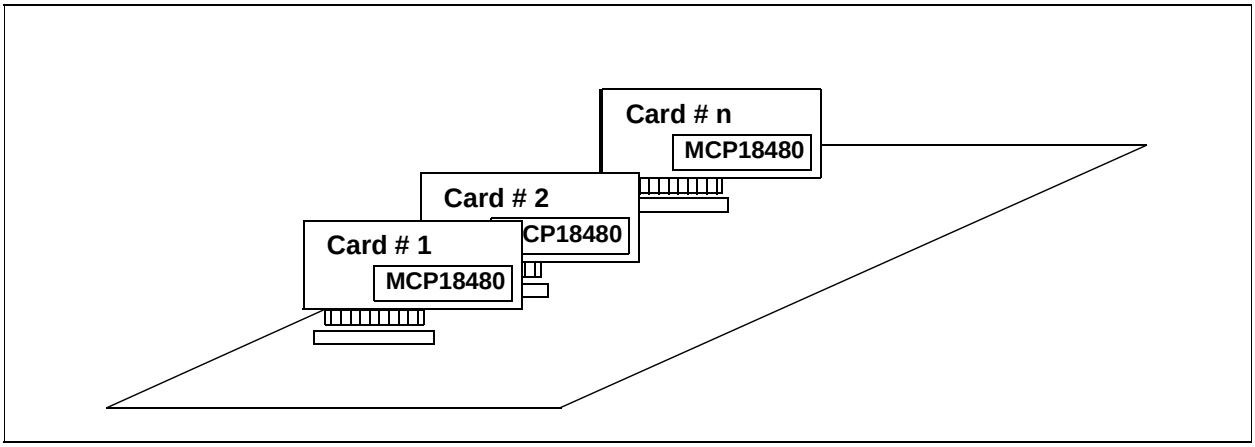


FIGURE 4-4: *Backplane System Block Diagram #2.*

NOTES:

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5.0 POWER-UP

5.1 V_{POS} and V_{NEG} Connection

For proper system operation, it is required that the system ground and the V_{NEG} pin have a solid connection before voltages are applied to any logic on the board.

5.2 The Board Circuitry

After the MCP18480 has "good" voltages on the V_{POS} and V_{NEG} pins, the board may have voltages applied to any of the other signals (a "good" voltage on V_{POS} indicates a "good" voltage on the system ground). The MCP18480 will start to source a small current to the external MOSFET to begin powering the board. This will turn on the MOSFET starting to power the external circuitry (load) of the board. The current from the GATE pin (into the external MOSFET) increases as the V_{DS} of the MOSFET decreases. When the V_{DS} of the MOSFET is below the voltage determined by the two resistors on the $DRAIN_{TH}$ pin (R_{DRAIN1} and R_{DRAIN2}), and the voltage on the GATE pin is greater than 8V, the PWRGOOD pin is active.

6.0 INTERNAL SIGNAL DESCRIPTIONS

The figure on page 2 illustrates a block diagram of the MCP18480. Between the functional blocks, there are some signals that have been named. These signals are briefly explained in Section 6.1 thru Section 6.7.

6.1 Undervoltage Active

A signal that indicates (when low) that System Ground - V_{NEG} is less then the minimum voltage.

6.2 Overvoltage Active

A signal that indicates (when low) that System Ground -V_{NEG} is greater then the maximum voltage.

6.3 LATCHOFF

A signal that controls the GATE pin due to a timeout of the current-limiting timer.

6.4 Current Limit TIMER

A signal that controls the reduction of source current on the GATE pin and starts the voltage ramp of the current limit timer.

6.5 Current Limit Feedback

A voltage that is proportional to the V_{DS} of the external MOSFET to set a trip point for current-limiting.

6.6 TIMEOUT

A signal that indicates the completion of the foldback time and is used to start the latchoff time.

6.7 Circuit Breaker

A signal that immediately causes the GATE pin output to be driven to V_{NEG} upon the detection of excessive current in the external FET.

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6.8 DESCRIPTION OF INTERNAL BLOCKS

The internal blocks shown in the MCP18480 Block Diagram on page 2 are discussed in Section 6.8.1 through Section 6.8.8.

Note:	Voltage levels discussed are with respect to external component values selected in Figure 4-1.

6.8.1 UV (UNDERVOLTAGE) BLOCK

The Undervoltage lockout circuit monitors the input voltage by comparing a centertap voltage on an external resistor divider to a 2.5V reference. The centertap voltage is fed into the UV_{TH} input pin.

If the voltage on the UV_{TH} pin is below the internal 2.5V reference, the absolute magnitude of the supply voltage is too low for proper system operation, resulting in the external MOSFET being turned off. If the voltage on the UV_{TH} pin is greater than V_{NEG} + 2.5V, the supply voltage is above the minimal operating voltage as set by the external resistor divider network.

In telecom network applications, it is common to shut down the DC/DC converter supply when the input voltage falls below -38.5V (tolerance of ±1.0V) for greater than 100 ms. The system will not restart until the voltage exceeds -43.0V (tolerance of ±0.5V). This voltage difference is produced by an open-drain NMOS output (the UV_{HYS} pin) that connects an external resistor in parallel with the lower of the two resistors in the external UV divider network until the supply ramps down to -43V. When the UV_{TH} pin exceeds V_{NEG} + 2.5V, the internal NMOS transistor is turned off, disconnecting the external resistor connected to the UV_{HYS} pin. The voltage at the UV_{TH} pin increases to 2.79V. The supply voltage would have to decrease to -38.5V in order to assert the internal “Undervoltage Active” signal.

An internal 10 µA current source and an external capacitor connected to the UV_D pin adjusts the delay between the input fault and the notification of this fault to the system. This is usually 100 ms for -48V telecom-type equipment. For customized adjustments, the time delay can be expressed as Equation 6-1.

EQUATION 6-1: INPUT FAULT DELAY

$$T_{DELAY} = \frac{\left(\frac{V_{REFIN}}{2}\right) \bullet C_{UVD}}{10\mu A}$$

C_{UV} is the capacitor connected between the UV_D pin and the V_{NEG} pin. A value of 1 µF would provide a delay of about 100 ms.

If the supply voltage dips below the programmed threshold, the input comparator trips the other way. The timing capacitor is released to ramp-up at the previously described rate and the Undervoltage block switches when the capacitor voltage reaches 1.25V. When the input comparator goes to a low level, the hysteresis FET is turned on and the trip point for reassertion of good V_{NEG} reverts to -43V.

While the Undervoltage Active signal is low (includes Undervoltage input filter), the GATE pin driver for the external MOSFET is disabled, the GATE pin is pulled to the voltage of the V_{NEG} pin with a 60 mA current sink and the PWRGOOD output pin is deasserted to indicate that the input voltage is out of range.

EQUATION 6-2: UNDERVOLTAGE HYSTERESIS

$$R_{UVHYS} = \frac{R_{UV1}}{\left(\frac{V_{UVD}}{V_{REFIN}}\right) - \frac{R_{UV1}}{R_{UV2}} - 1}$$

EQUATION 6-3: UNDERVOLTAGE CONDITION

$$V_{REFIN} > \frac{|V_{NEG}| \bullet R_{UV2}}{(R_{UV1} + R_{UV2})}$$

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6.8.2 OV (OVERVOLTAGE) BLOCK

The overvoltage block behaves similarly to the undervoltage block in that it monitors an input voltage by comparing a centertap voltage on an external voltage divider (on the OV_{TH} pin) to the V_{REFIN} pin voltage.

If the centertap voltage is below the reference, the input voltage is not excessive. If the centertap voltage is greater than the V_{NEG} + V_{REFIN} pin voltages, the supply voltage is higher than the programmed acceptable maximum voltage limit. An internal flag is then activated to inform the MCP18480 that the input voltage has exceeded the preset limit.

The “Overvoltage Active” signal deasserts when the input voltage drops back below the threshold determined by the external resistors (R_{OV1} and R_{OV2}).

EQUATION 6-4: OVERVOLTAGE VOLTAGE CONDITION

$$V_{REFIN} < \frac{|V_{NEG}| \bullet R_{OV2}}{(R_{OV1} + R_{OV2})}$$

6.8.3 FET-GOOD BLOCK

The FET-good block monitors the voltage between the drain of the external MOSFET and on the V_{NEG} pin at power-up. It delays assertion of PWRGOOD until the drain-to-source voltage of the external FET is acceptably low and the voltage at the GATE pin is about 8V. The comparator operation is similar to Undervoltage and Overvoltage blocks.

To prevent applying excessive voltages to the gates of the FETs in the Undervoltage circuit, a resistive voltage divider is employed between ground and the V_{NEG} pin. Similarly, the drain of the external MOSFET can be exposed to voltages at around V_{NEG} during normal operation and as high as ground (typically 48V above V_{NEG}).

The FET good block also monitors the GATE pin. When the GATE pin becomes >V_{NEG} +8V and the $DRAIN_{TH}$ pin is within its programmed range, the output of the FET good block is active.

The internal FET good signal goes high and remains active until a fault condition (Undervoltage, Overvoltage or Current Limit) is detected. Any of these conditions hold the PWRGOOD signal deasserted until the fault condition is removed and the external FET gate and drain voltages are acceptable.

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6.8.4 CURRENT LIMIT BLOCK

An excessive current flowing through the external FET is sensed as a voltage across an external resistor connected between the FET's source and V_{NEG}.

The drain voltage is sensed with a resistor divider network, as shown in Figure 4-1 and Figure 4-2. The voltage tap is applied to a circuit whose output is 50 mV above V_{NEG} when the drain of the external FET is at V_{NEG}. The output is 12 mV when the V_{FB} pin is $\geq V_{NEG}$ +0.5V. This output voltage is the Current Limit Feedback (CLFB) signal to the gate driver block for use in the fold-back current-limiting.

The CLFB voltage serves as the reference for a comparator whose other input monitors the voltage across the current limit sense resistor in series with the source of the external FET. When the SENSE pin exceeds the voltage on CLFB, a comparator output goes high to start the timer (see Section 6.8.5). The V_{DS} dependent threshold for the current limit helps keep the FET within its safe operating area.

Another comparator in the current-limiting block watches the SENSE pin for potentially catastrophic over-current conditions, which require immediate termination of conduction in the pass MOSFET. The output of this comparator trips a comparator used in the TIMER block to skip the first part of the timeout cycle and go straight to the "off" period. In some cases, the user may want to program the system to shut off immediately if there is a short-circuit condition that exceeds a desired level. To use this feature, connect a divider between the V_{REFIN} pin and the V_{NEG} pin, with its centertap at the CL input pin. The circuit breaker current that would trigger this mode is given by Equation 6-5.

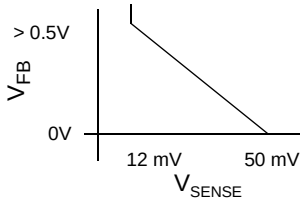
EQUATION 6-5: CIRCUIT BREAKER THRESHOLD

$$I_{CAT} = \frac{\left(\frac{V_{REFIN}}{R_{CL1} + R_{CL2}}\right) \bullet R_{CL2}}{R_{SENSE}}$$

If this function is not needed in a particular application, it can be disabled by connecting the CL pin to the V_{REFIN} pin. Equation 6-6 shows the current of the CL pin during current-limiting.

EQUATION 6-6: CL PIN CURRENT

$$I_{CL} = \frac{V_{SENSE}}{R_{SENSE}}$$



$$V_{SENSE} = 0.76 \times \left(0.05V - \frac{V_{DS} \times R_{FB2}}{R_{FB1} + R_{FB2}}\right) + 0.012V$$

$$for\ V_{FB} > 0.5V,\ V_{SENSE} = 0.012V$$

6.8.5 TIMER BLOCK

Since the external FET can survive brief over-current episodes, it is unnecessary to turn off the FET instantly when the current rises too high (see external FET data sheet). The timer circuit uses the output of the comparator in the current-limiting block to begin charging an external capacitor with 16 • I_{RISET} (typically 160 µA) when an over-current condition is detected. When the voltage on the capacitor ramps up to 1.25V, a comparator output goes high. This output goes to another block that tells the gate driver to turn the external FET off and deassert the PWRGOOD pin. The complementary output of the timer changes the state of a hysteresis circuit that drops the reference input of the comparator to V_{NEG} + 100 mV (± 10 mV).

When the FET is off, the current through it drops to zero, so that the voltage across the current sense resistor also goes to zero and the current limit signal to the timer block goes away. The timer capacitor starts to discharge at a rate set by the external resistor, R_{DISCH}.

Equation 6-7 shows the equations used to calculate the current at the TIMER pin. This current is used for other calculations.

EQUATION 6-7: TIMER PIN CURRENT CALCULATIONS

$$I_{TIMER} = 16 \bullet I_{RISET} \quad Typical$$

$$I_{TIMER} = 10 \bullet I_{RISET} \quad Minimum$$

$$I_{TIMER} = 20 \bullet I_{RISET} \quad Maximum$$

Legend: I_{RISET} is the current through the external R_{ISET} resistor

The delay between the inception of the over-current condition and the deactivation of the FET is given by Equation 6-8.

EQUATION 6-8: OVER-CURRENT FAULT DELAY

$$T_{CLD1} = \frac{C_{TIMER}}{I_{TIMER}} \bullet 1.25$$

The time required to reset the timer and reactivate the gate driver is given by Equation 6-9.

EQUATION 6-9: OVER-CURRENT REACTIVATION DELAY

$$T_{CLD2} = 9.2 \bullet C_{TIMER} \bullet R_{DISCH}$$

As described above, the timer circuit operates as a free-running, multi-vibrator, if $\overline{\text{RESTART}}$ is low.

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6.8.6 LATCH BLOCK

A current limit latch circuit determines whether, following the timeout period resulting from an over-current condition, the external FET should be latched-off until reactivated by an external signal, or be allowed to restart automatically following the timer cycle.

If the $\overline{\text{RESTART}}$ input is low, the part will restart and the gate drive to the external MOSFET will be restored automatically. If the $\overline{\text{RESTART}}$ pin is high, a current limit event will turn the FET off after the programmed delay and maintain an off condition until the ENABLE pin or $\overline{\text{RESTART}}$ pin is pulled low momentarily.

6.8.7 GATE DRIVE BLOCK

The GATE drive block sources a current equal to the voltage at CLFB divided by 1 kΩ to the gate of the external MOSFET. So the current sourced from the GATE pin is determined by the V_{DS} of the external FET. This current, and the external capacitors around the FET, control the slew rate of the drain of the external FET, limiting the current that would otherwise have to be diverted from other boards on the backplane. In the event of a problem (Overvoltage, Undervoltage or current limit), the gate of the external FET is pulled down with 60 mA. During normal operation, the GATE pin ramps up to about 12V, sending the external FET deeply into the triode region. If the drain current becomes excessive while the drain-to-source voltage is high, the inverting input of the op amp is driven to the CLFB voltage by the current-limiting block, causing a reduction in the drive to the external FET to reduce the current through it. This foldback current-limit remains active until the voltage on C_{TIMER} reaches $V_{REFIN}/2$, after which the GATE output pin is pulled to V_{NEG} for the duration of the timeout period, or until ENABLE is cycled low momentarily.

For applications in which it is undesirable to have the drain current track the V_{DS} of the external pass FET in current limit, the user can tie the V_{FB} pin to the V_{REF} or V_{NEG} pin. This will make the MCP18480 try to force the drain current to 12 mV/R_{SENSE} or 50 mV/R_{SENSE}, respectively, until the TIMER block times out. If foldback current-limiting is not desired at all, set the divider associated with the CL pin to detect the desired current in order to shut off the GATE immediately.

A voltage on the GATE pin higher than about 8V is one condition for the PWRGOOD pin to be asserted. Any fault condition that causes the GATE pin voltage to be pulled to V_{NEG} deasserts the PWRGOOD pin. On startup, a NMOS transistor with a resistor pulling its gate up holds the GATE pin down until the MCP18480 is properly biased.

6.8.8 BIAS BLOCK

The internal voltage generation or bias block generates the biasing currents for all internal blocks. It also provides a 2.5V reference voltage that is brought out to the V_{REFOUT} pin. This output pin is usually fed back into the V_{REFIN} pin. However, an externally-generated 2.5V reference voltage may be directly connected to the V_{REFIN} pin, while leaving the V_{REFOUT} pin unconnected. A $V_{REFIN}/2$ voltage is generated within the bias block, which is used as reference in the other blocks.

A internal shunt regulator limits the internal circuitry to 12V. An external current-limiting resistor in series with V_{POS} absorbs the excess voltage. The resulting regulated 12V source is used in the gate drive block and PWRGOOD output circuit.

The 12V source is also stepped-down to generate a 5V regulated source. Most of the other circuitry and blocks operate with the internally-generated 5V.

EQUATION 6-10: EXTERNAL R_{ISET} CURRENT

$$I_{RISET} = \pm\frac{\left(\frac{V_{REFIN}}{2}\right)}{R_{ISET}}$$

Note: The direction of the current is dependant on where the external R_{ISET} resistor is connected (the I_{SET} pin to either the V_{NEG} pin or the V_{REFIN} pin).

6.8.9 POWER GOOD BLOCK

The “power good” block monitors the state of the OV active, the UV active, the current limit circuitry, and output of the FET good block to generate the PWRGOOD output signal.

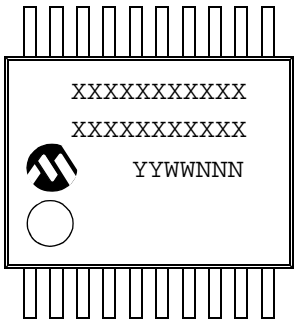
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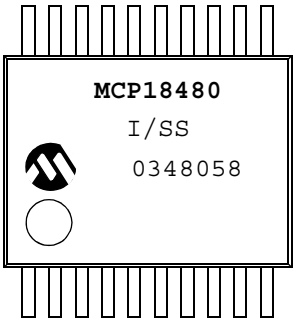
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

20-Lead SSOP



Example:



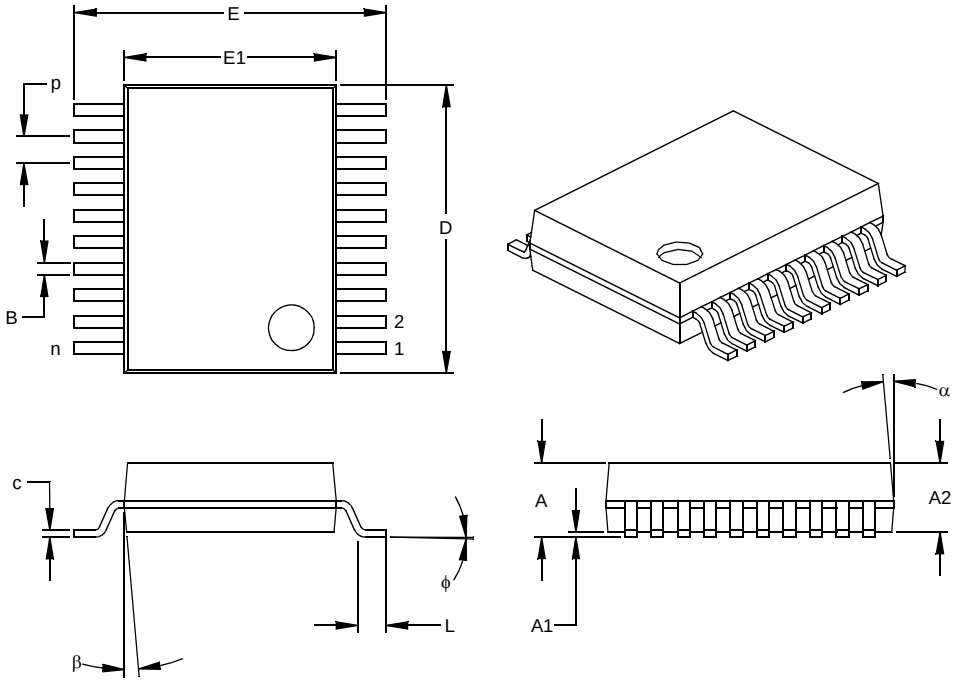
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, and traceability code.

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	ϕ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

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APPENDIX A: REVISION HISTORY

Revision A

This is a new data sheet

Revision B

- Add device characterization information
- Enhanced functional description

Revision C

- Added note to the package outline drawing.

NOTES:

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APPENDIX B: MCP18480 SCHEMATICS

This appendix contains the schematics for the MCP18480 Evaluation Board.

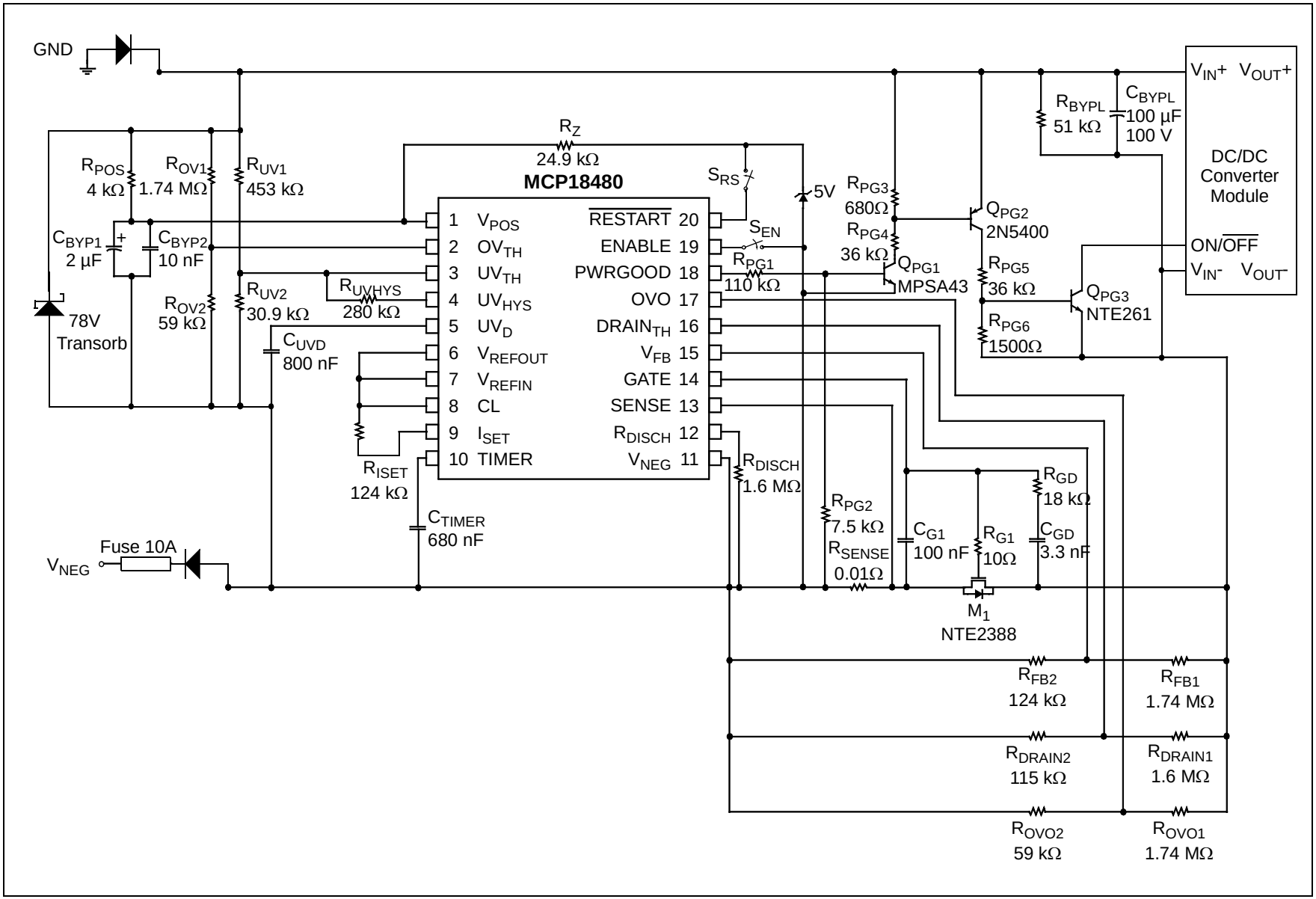


FIGURE B-1: *Typical Operating Circuit for Telcom Applications with Active-High Power Module - Foldback Current Limit Enabled.*

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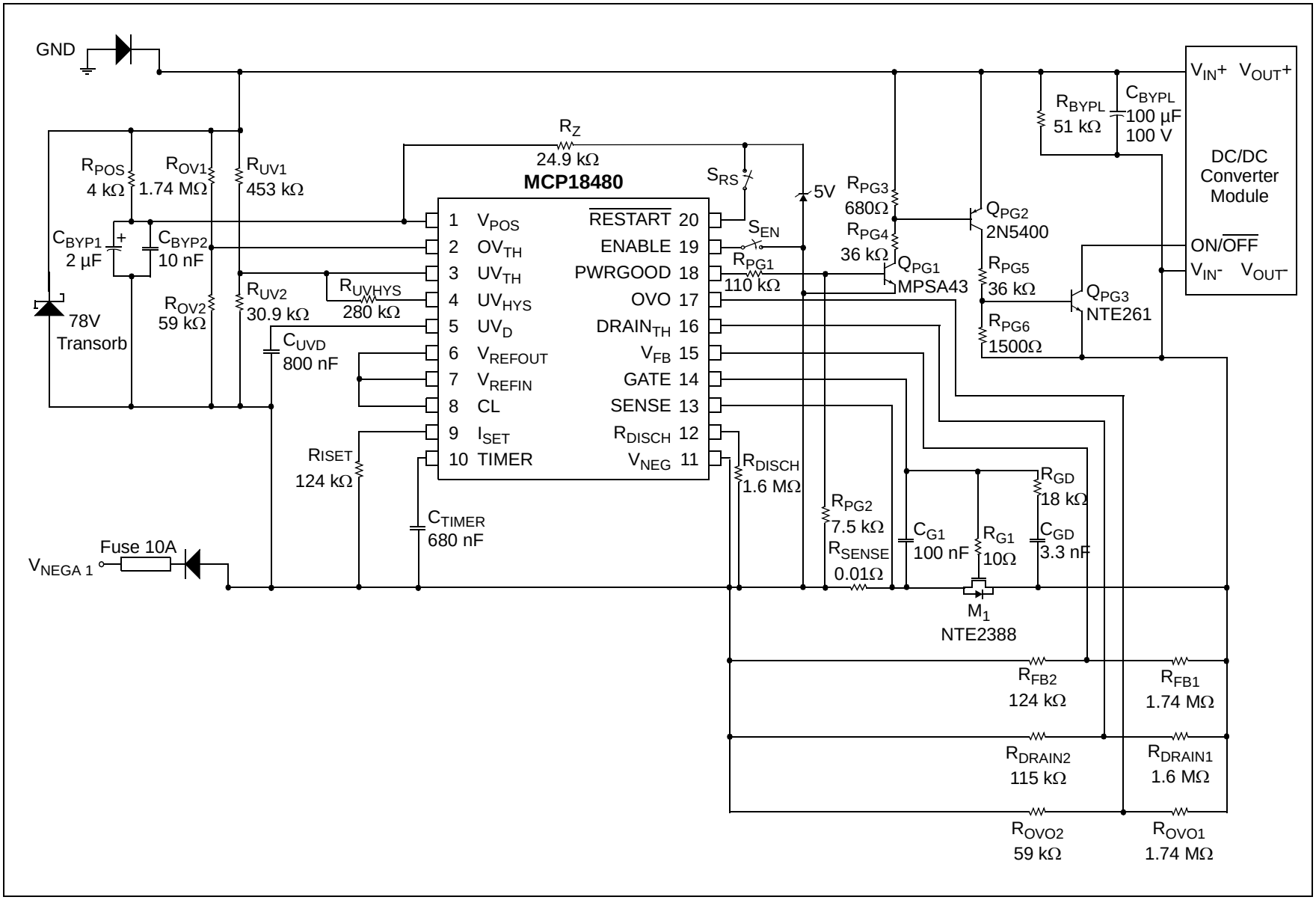


FIGURE B-2: *Typical Operating Circuit for Telcom Applications with Active-Low Power Module - Foldback Current Limit Enabled.*

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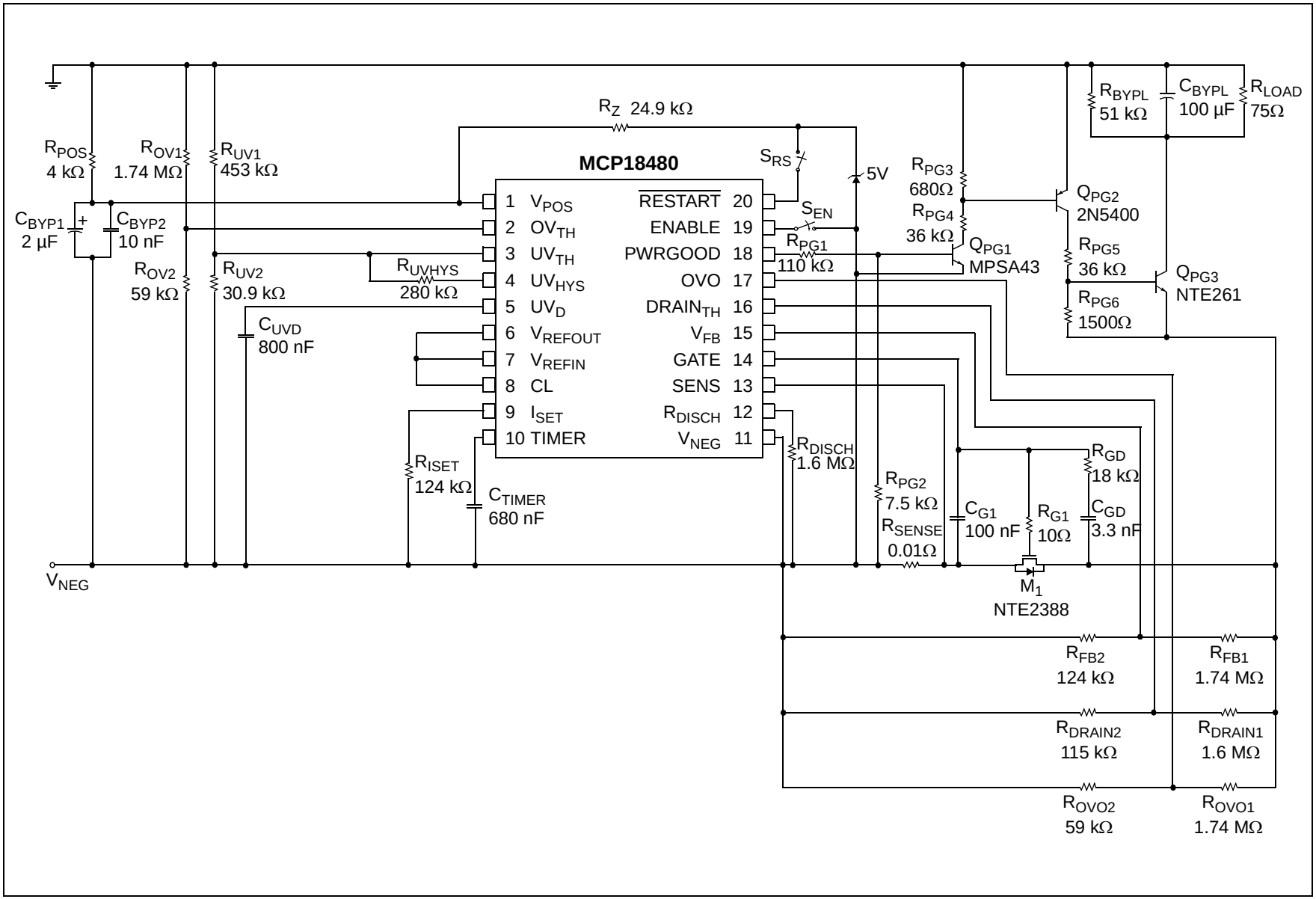


FIGURE B-3: *Evaluation Board Schematic (Active-Low Power Module - Foldback Current Limit Enabled).*

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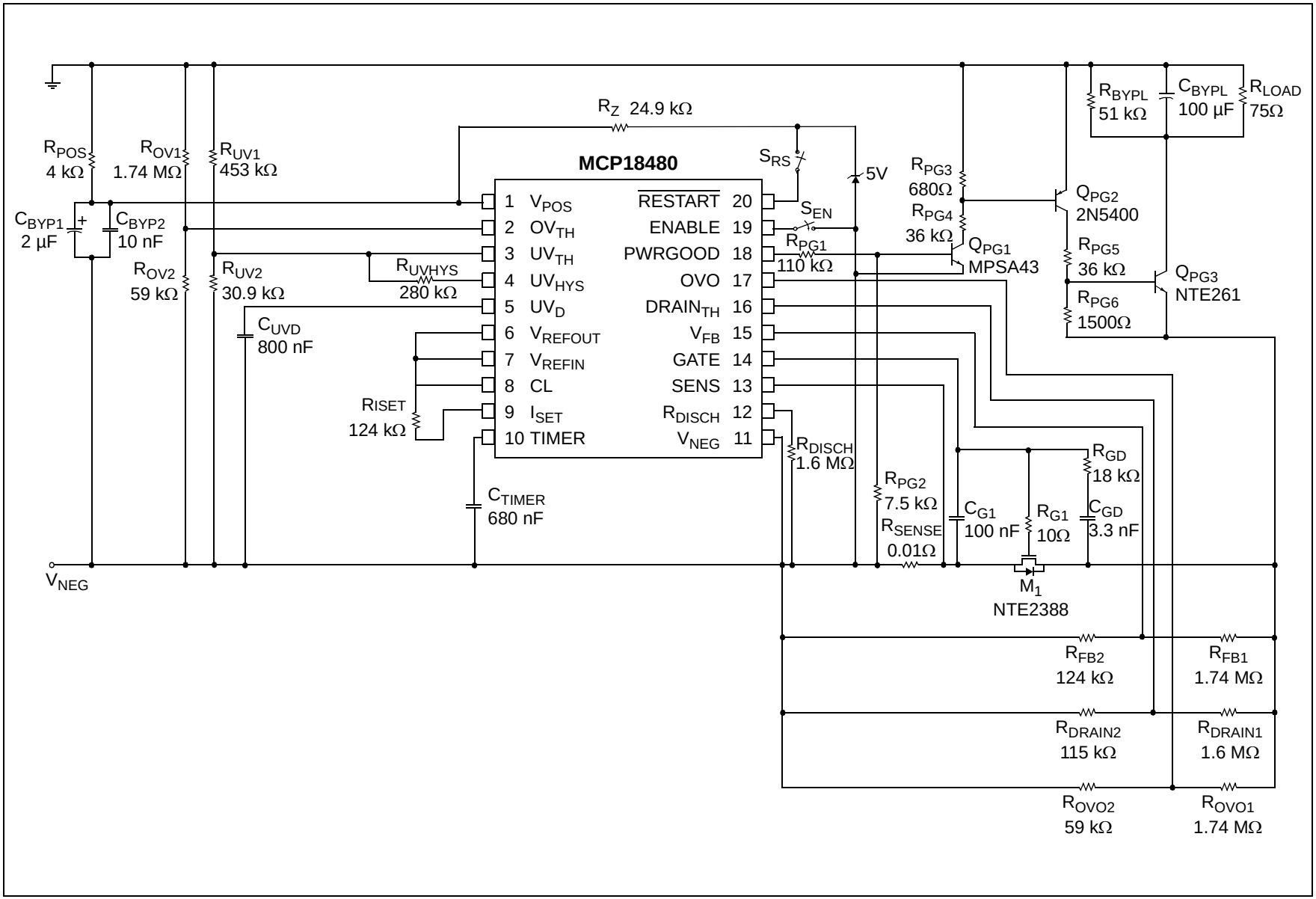


FIGURE B-4: *Evaluation Board Schematic (Active-High Power Module - Foldback Current Limit Enabled).*

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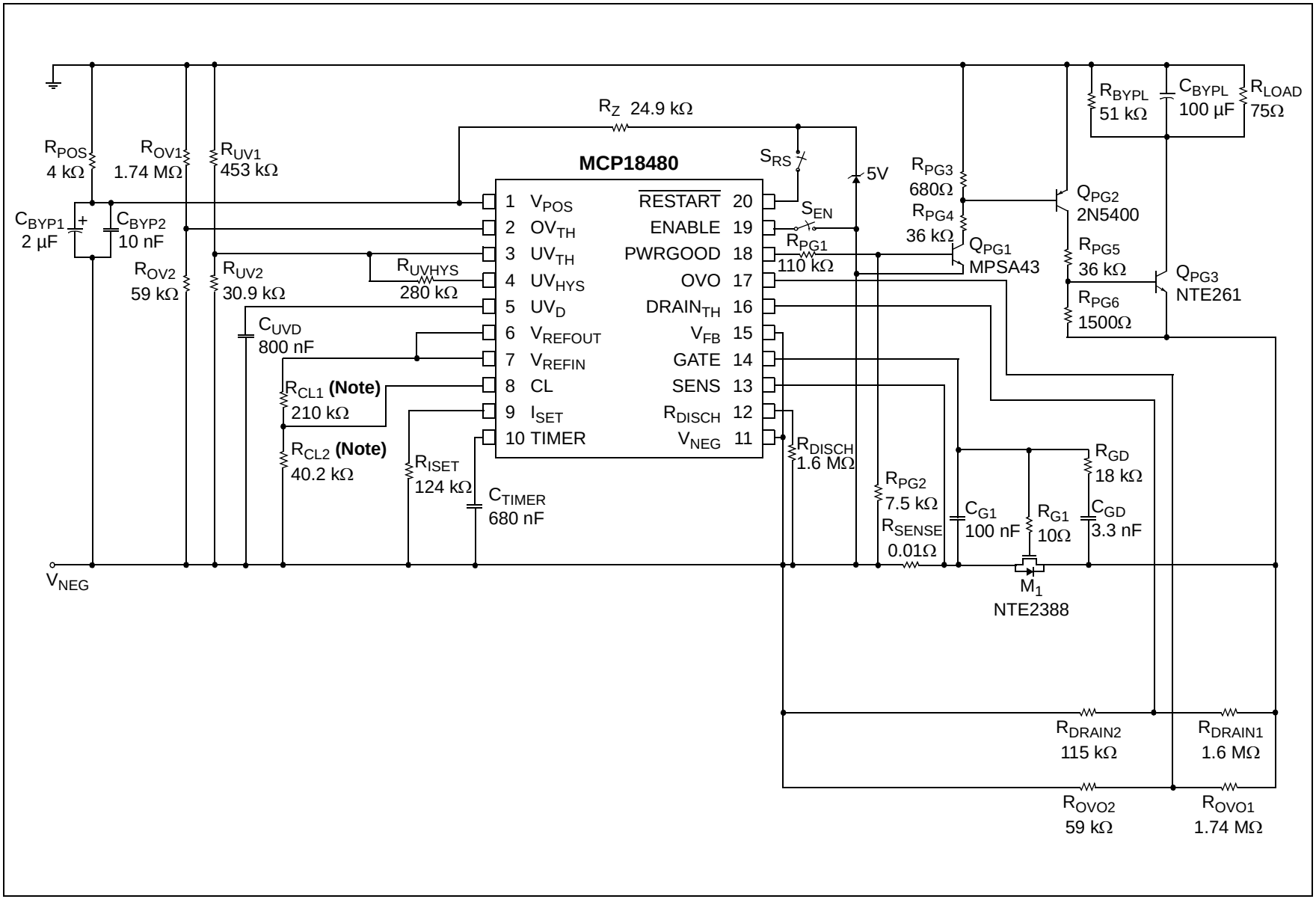


FIGURE B-5: *Evaluation Board Schematic (Active-Low Power Module - Circuit Breaker Current Limit Enabled).*

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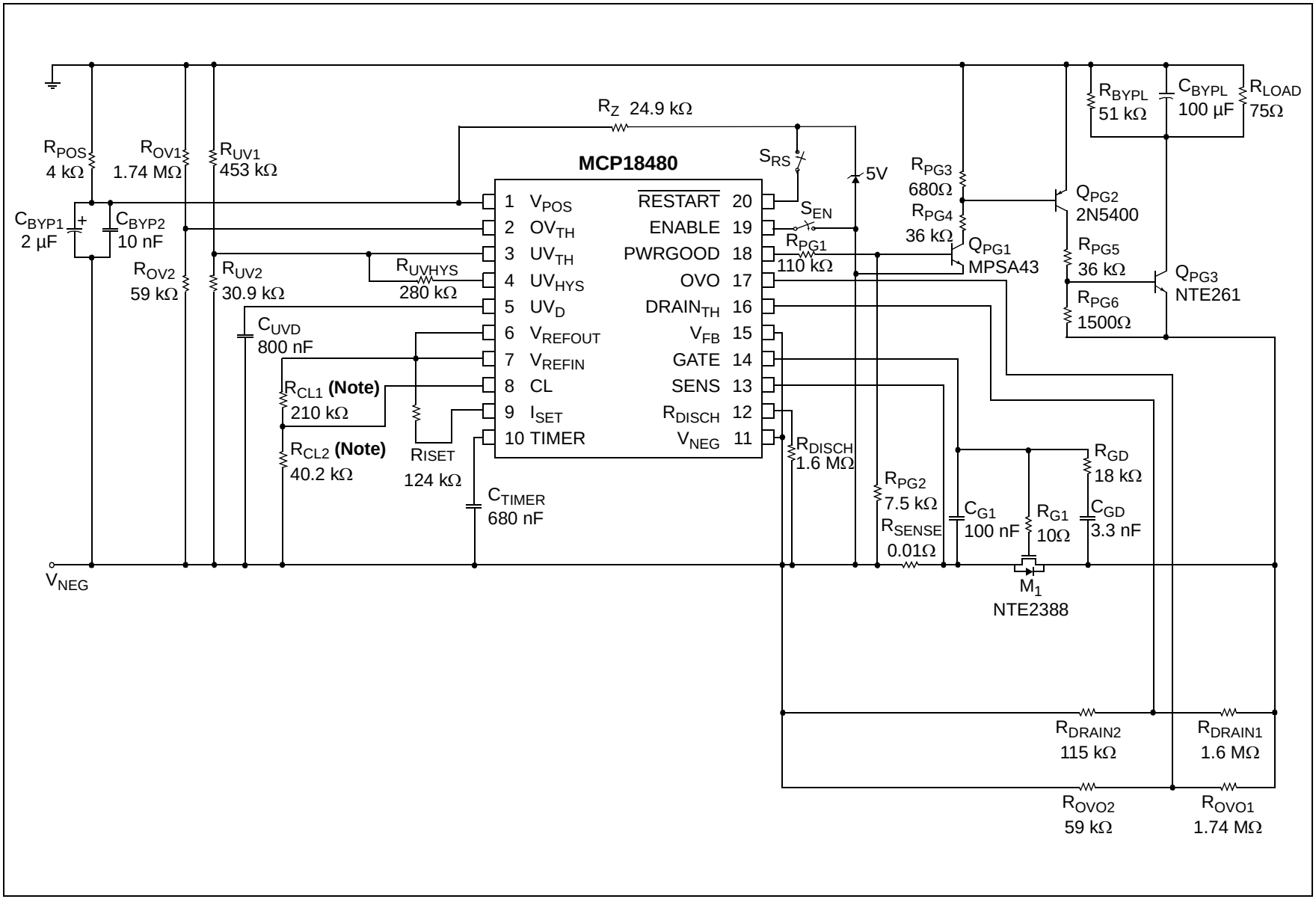


FIGURE B-6: *Evaluation Board Schematic (Active-High Power Module - Circuit Breaker Current Limit Enabled).*

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device	MCP18480:	-48V Hot Swap Controller
	MCP18480T:	-48V Hot Swap Controller (Tape and Reel)
Temperature Range	I =	-40°C to +85°C
Package	SS =	Plastic SSOP (209 mil, Body), 20-lead

Examples:

a) MCP18480-I/SS = Industrial Temp., SSOP package

b) MCP18480T-I/SS = Tape and Reel, Industrial Temp., SSOP package

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