# STw4102

## Dual USB/wall adapter Li-ion battery charger with gas gauge

## Features

- Constant current constant voltage (CCCV) linear charger
- Common or separate USB/wall adapter inputs
- Fast charge current control up to 1 A for wall adapter and up to 500 mA for USB
- Support for currents higher than 1 A using external components
- Programmable charge voltage (4.1 V, 4.2 V, 4.3 V, 4.35 V) with 1% accuracy
- Thermal regulation
- Trickle charge mode at low battery voltage
- Wall adapter voltage up to 16 V
- Battery overvoltage protection at 4.7 V
- Gas gauge with 13-bit AD converter
- Battery voltage monitor with 7-12 bit AD converter
- $I^2C$ interface for device monitoring and control
- Charge status output pin
- Power detection output pin
- Programmable watchdog security timer
- 4.7 V LDO regulator (with external power MOSFET)

## Applications

- Cellular phones (GSM, CDMA, WCDMA), PDA, MP3 players, cordless phones
- Digital camera, USB appliances, bluetooth devices, portable navigation devices

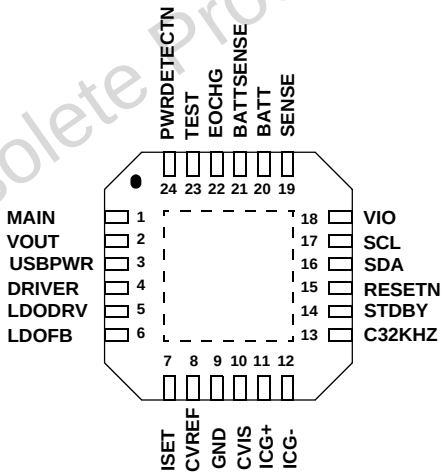
## Description

The STw4102 is a standalone constant current constant voltage (CCCV) linear charger specifically designed for Li-ion batteries.



**QFN 24**
(Plastic micropackage)

**Pin connections**
(top view)




The STw4102 offers dual charging capability using separate inputs for USB cable and wall adapter, or a single input that accepts both.

The STw4102 also offers programmable fast charge current using an external resistor. A thermal regulation circuit limits the charge current against the die high power dissipation or high ambient temperature. An end of charge output pin indicates the charge termination when the fast charge current drops below 10% of the programmed current value.

The STw4102 includes an accurate gas gauge based on a 13-bit AD converter. An external resistor is used between battery and ground to sense a charge/discharge current. With a typical 30 mΩ resistor, current can be up to 2.5 A.

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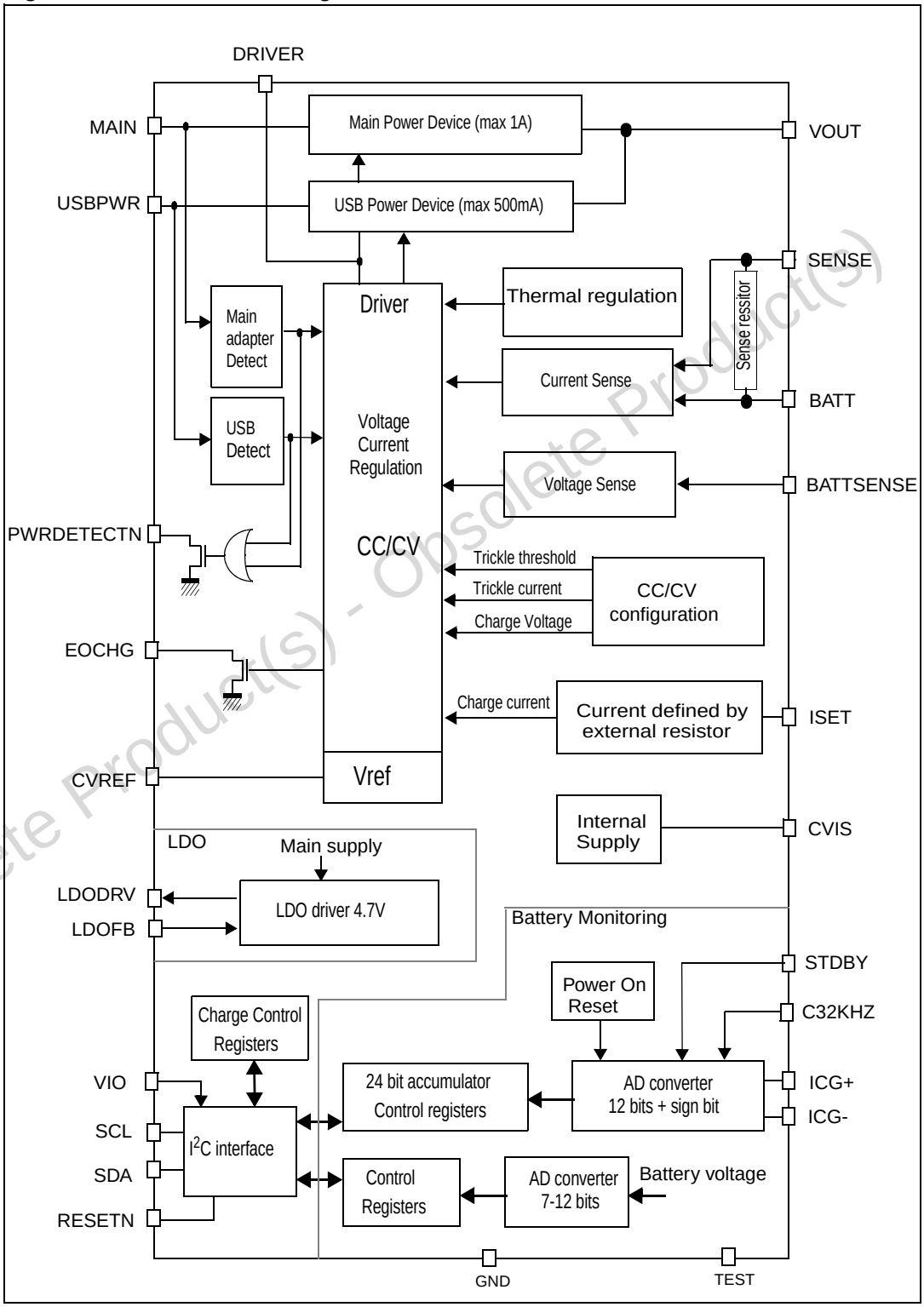
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# 1 Block diagram

**Figure 1. Internal block diagram**




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# 2 Pin assignment

**Table 1. Pin descriptions**

| Pin # | Pin name | Type | Function |
|---|---|---|---|
| 1 | MAIN | Supply | Main power input from wall adapter or USB charger |
| 2 | VOUT | O_A | Power path output |
| 3 | USBPWR | Supply | Power supply from USB cable |
| 4 | DRIVER | O_A | Driver for external power switch (PMOS or PNP) |
| 5 | LDODRV | O_A | LDO power PMOS driver |
| 6 | LDOFB | I_A | LDO feedback regulation |
| 7 | ISET | O_A | Resistor to program the main charge current |
| 8 | CVREF | I_A | Bypass capacitor for internal voltage reference |
| 9 | GND | Ground | Analog and digital ground |
| 10 | CVIS | I_A | Bypass capacitor for internal supply |
| 11 | ICG+ | I_A | Gas gauge sense resistor |
| 12 | ICG- | I_A | Gas gauge sense resistor |
| 13 | C32KHZ | I_D | External 32kHz clock input |
| 14 | STDBY | I_D | Gas gauge standby input (active low) |
| 15 | RESETN | I_D | Digital register reset (active low) |
| 16 | SDA | IO_D | $I^2C$ serial data. |
| 17 | SCL | I_D | $I^2C$ serial clock. |
| 18 | VIO | Supply | Supply for I/O |
| 19 | SENSE | I_A | Sense resistor input to regulate the charge current |
| 20 | BATT | Supply | Battery power voltage |
| 21 | BATTSENSE | I_A | Battery sense voltage |
| 22 | EOCHG | OD | End of charge output status. Pulled low when the fast charge current is above 10% of its programmed maximum value. |
| 23 | TEST | I_D | Reserved pin for factory test. To be connected to ground. |
| 24 | PWRDETECTN | OD | Main or USB plug-in detection. Pulled low when power is detected, open when no power is detected. |

In this table, the following conventions are used:

I: Input
O: Output
I/O: Bidirectional
OD: Open Drain
A: Analog
D: Digital

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# 3 Absolute maximum ratings and operating conditions

**Table 2. Absolute maximum ratings (AMR)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{MAIN}$ | Maximum supply voltage on MAIN input | 20 | V |
| $V_{CC}$ | Voltage on EOCHG, LDODRV, DRIVER pins | -0.3 to $V_{MAIN}$ | V |
| $V_{USB}$ | Maximum supply voltage on USBPWR input | 7 | V |
| $V_{batt}$ | Maximum voltage on BATT, BATTSENSE, PWRDETECTN | 7 | V |
| $V_{IO}$ | Maximum supply voltage on $V_{IO}$ pin | 7 | V |
| $V_{DD}$ | Voltage on I/O pins (SCL, SDA, RESETN, C32KHZ, STDBY) | -0.3 to $V_{IO}$ | V |
| $P_d$ | Power dissipation | self-limited | |
| $I_{sense}$ | Maximum current from SENSE to BATT | 1 | A |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |
| $T_j$ | Maximum junction temperature | 150 | °C |
| $R_{thja}$ | Thermal resistance junction-ambient(1) | 45 | °C/W |
| ESD | Electrostatic discharge (HBM human body model)(2) | 2 | kV |

1. Package's exposed pad is soldered to a copper pad on the PCB with multiple vias to the ground plane.
2. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

**Table 3. Operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{main}$ | Operating supply voltage on MAIN | 4.25 to 16 | V |
| $V_{CC}$ | Maximum voltage on EOCHG | 16 | V |
| $V_{USB}$ | Operating supply voltage on USBPWR | 4.25 to 5.5 | V |
| $V_{IO}$ | Operating supply voltage on VIO | 1.45 to 3.0 | V |
| $V_{batt}$ | Max voltage on BATT, BATTSENSE, PWRDETECTN | 5.0 | V |
| $V_{out}$ | Max voltage on VOUT | BATT +0.7 | V |
| $T_{oper}$ | Operating free air temperature range | -30 to 85 | °C |

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# 4 Electrical characteristics

**Table 4. CC/CV charger - $V_{oper}$= 5V, $V_{batt}$= 3.6V, $T_{amb}$ = -30°C to 85°C (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply ($V_{oper}$ from MAIN or USB)** | | | | | | |
| $I_{charger}$ | Main or USB input operating current | | | 2 | | mA |
| $I_{STBY}$ | USBPWR input standby current | Charge off | | | 40 | µA |
| $I_{batt_sense}$ | BSENSE input current | No charge | | | 1 | µA |
| $I_{batt}$ | BATT input current | No charge | | | 25 | µA |
| POR_IS+ | Power ON reset threshold+ | CVIS internal supply | 2.2 | 2.3 | 2.4 | V |
| POR_IS- | Power ON reset threshold- | CVIS internal supply | 2.1 | 2.2 | 2.3 | V |
| **Voltage regulation** | | | | | | |
| $V_{charge_acc}$ | Output voltage accuracy | $T_{amb}$= 0°C to 85°C | -1 | | +1 | % |
| $R_{power}$ | Power path resistance | MAIN to BATT | | 0.6 | | Ω |
| $Battery_{ovv}$ | Static battery overvoltage detection | | 4.55 | 4.7 | 4.8 | V |
| $Battery_{ovv_hyst}$ | Static battery overvoltage hysteresis | | | 100 | | mV |
| **Current regulation** | | | | | | |
| $I_{trickle}$ | Trickle charge current | $V_{batt}$< $V_{trickle}$<br>Standard configuration<br>Factory OTP option | <br>30<br>60 | <br>60<br>120 | <br>100<br>180 | <br>mA<br>mA |
| $V_{trickle}$ | Trickle to fast charge threshold | Standard configuration | 2.8 | 2.9 | 3.0 | V |
| $V_{trickle_hyst}$ | Trickle to fast charge threshold hysteresis | | | 100 | | mV |
| $I_{charge}$ | Main charge current range | Internal path | 100 | | 1000 | mA |
| $I_{charge_acc}$ | Main charge current accuracy | $I_{charge}$> 500mA | -15 | | +15 | % |
| $I_{USB}$ | USB charge current | REG_CHG0[7..6]:<br>00<br>01<br>10<br>11 | 30 | <br>60<br>200<br>400<br>0 | <br>100<br><br>500 | <br>mA<br>mA<br>mA<br>mA |
| $EOCHG_{ith}$ | End of charge threshold | % of current setting | | 10 | | % |
| $EOCHG_{ith_hys}$ | End of charge threshold hysteresis | % of current setting | | 5 | | % |
| $T_{regulation}$ | Regulated junction temperature | | | 125 | | °C |
| $T_{softstart}$ | Soft start from trickle to fast charge | | | 100 | | µs |

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**Table 4. CC/CV charger - $V_{oper}$= 5V, $V_{batt}$= 3.6V, $T_{amb}$ = -30°C to 85° C (unless otherwise specified) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Watchdog** | | | | | | |
| $t_{watchdog}$ | Watchdog duration | REG_WDOG[2,1]:<br>00<br>01<br>10<br>11 | <br>0.5<br>7.5<br>15<br>30 | <br>1<br>15<br>30<br>60 | <br>1.5<br>22.5<br>45<br>90 | <br>min<br>min<br>min<br>min |
| **Input/output pins** | | | | | | |
| $V_{charger_det}$ | Main charger supply voltage detection | | 2.4 | 2.5 | 2.6 | V |
| $V_{charger_det_hys}$ | Main charger supply voltage detection hysterisis | | | 100 | | mV |
| $V_{USB_det}$ | USB supply voltage detection | | 2.4 | 2.5 | 2.6 | V |
| $V_{USB_det_hys}$ | USB supply voltage detection hysteresis | | | 100 | | mV |
| $Vol_{powerdetect}$ | POWERDETECTN output capability | $I_{sink}$= 10mA | | | 0.45 | V |
| $Vol_{EOCHG}$ | EOCHG output capability | $I_{sink}$= 10mA<br>$I_{sink}$= 20mA | | | 0.5<br>1.1 | V<br>V |
| $I_{drv_sink}$ | Driver sink current | (If option enabled) | 60 | | | mA |

**Table 5. LDO - $V_{main}$= 6V, $T_{amb}$ = -30°C to 85° C (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $LDO_V$ | LDO regulated output voltage | Including line and load regulation (up to 1A), $V_{main}$ > 6V | 4.47 | 4.7 | 4.93 | V |
| $LDO_{power_th}$ | LDO power turn off threshold | | 6.8 | 7.2 | 7.5 | V |
| $LDO_{power_th_hys}$ | LDO power turn off threshold hysterisis | | | 0.7 | | V |
| $LDO_{PSRR}$ | LDO power supply rejection ratio | Up to 20kHz | | 50 | | dB |

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**Table 6. Battery monitor - $V_{batt}$= 3.6V, $T_{amb}$ = -30°C to 85° C (unless otherwise specified)**

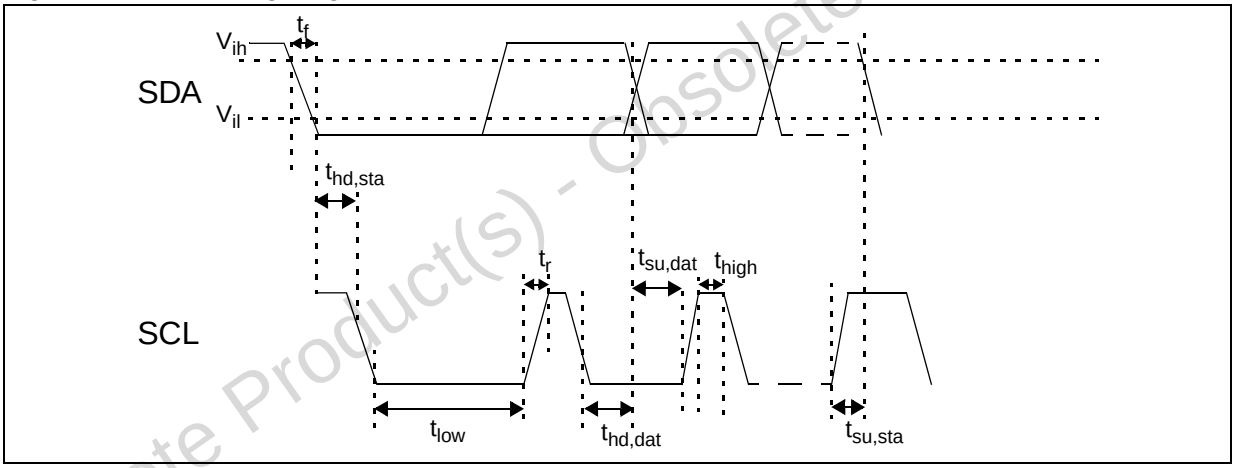
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| POR_IS2+ | Power ON reset threshold+ | CVIS internal supply | 2.6 | 2.7 | 2.8 | V |
| POR_IS2- | Power ON reset threshold- | CVIS internal supply | 2.5 | 2.6 | 2.7 | V |
| **Gas gauge A/D converter** | | | | | | |
| $V_{os_gg}$ | Input offset voltage | | | 40 | | µV |
| $V_{in_gg}$ | Input voltage range | | -80 | | +80 | mV |
| $I_{dd_gg}$ | Current consumption | CG_ENA=1 | | | 90 | µA |
| $I_{pdn_gg}$ | Current consumption in off mode | CG_ENA=0 | | | 1 | µA |
| $I_{in}$ | Input current for ICG+ and ICG- | | | | 500 | nA |
| $LSB_{gg}$ | AD converter granularity (LSB value) | 12 bits + 1 sign bit | | 23.5 | | µV |
| $Acc_{Tamb_gg}$ | Accuracy at ambient temperature | External resistor at 1%<br>No calibration | | 3 | | % |
| **Battery voltage A/D converter** | | | | | | |
| $V_{in_mon}$ | Input voltage range | BATT voltage | 1 | | 5 | V |
| $I_{dd_mon}$ | Current consumption | ADPOWERON=1 | | 190 | | µA |
| $I_{pdn_mon}$ | Current consumption in off mode | ADPOWERON=0 | | | 1 | µA |
| $LSB_{mon}$ | AD converter granularity (LSB value) | 7 bits<br>12 bits | | 45.4<br>1.42 | | mV<br>mV |
| $Acc_{Tamb_mon}$ | Accuracy at ambient temperature | No calibration | | 3 | | % |
| **Digital I/O pins (SCL, SDA, STDBY, C32KHZ, RESETN)** | | | | | | |
| $V_{il}$ | Input pin low voltage | | 0 | | 0.3 x $V_{IO}$ | V |
| $V_{ih}$ | Input pin high voltage | | 0.7 x $V_{IO}$ | | $V_{IO}$ | V |
| $V_{ol}$ | SDA output pin low voltage | $I_{sink}$= 3mA | | | 0.2 x $V_{IO}$ | V |

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**Table 7. $I^2C$ timing - $V_{IO}$= 2.8V, $T_{amb}$ = -30°C to 85° C (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{scl}$ | SCL clock frequency | | | | 400 | kHz |
| $t_{hd,sta}$ | Hold time (repeated) START condition | | 0.6 | | | µs |
| $t_{low}$ | LOW period of the SCL clock | | 1.3 | | | µs |
| $t_{high}$ | HIGH period of the SCL clock | | 0.6 | | | µs |
| $t_{su,dat}$ | Setup time for repeated START condition | | 0.6 | | | µs |
| $t_{hd,dat}$ | Data hold time | | 0 | | 0.9 | us |
| $t_r$ | Rise time of both SDA and SCL signals | | 20+ $0.1C_b$ | | 300 | ns |
| $t_f$ | Fall time of both SDA and SCL signals | | 20+ $0.1C_b$ | | 300 | ns |
| $t_{su,sto}$ | Setup time for STOP condition | | 0.6 | | | µs |
| $C_b$ | Capacitive load for each bus line | | | | 400 | pF |

**Figure 2. $I^2C$ timing diagram**




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# Typical performance curves

**Figure 3. Charger voltage vs. charge current (Main charge, 4.2V and 1A settings)**

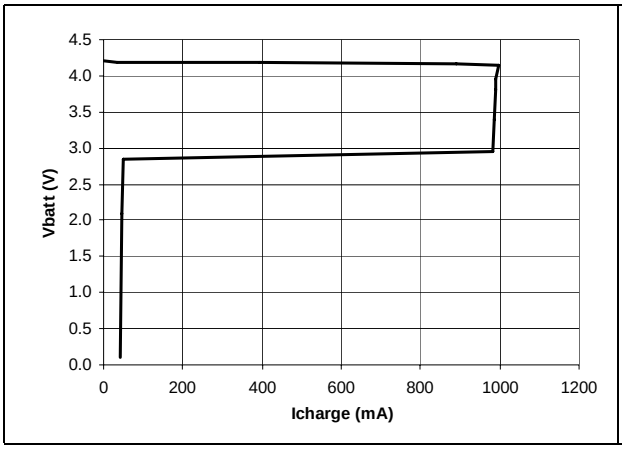



**Figure 4. Charger voltage vs. charge current (USB charge, 4.2V setting)**

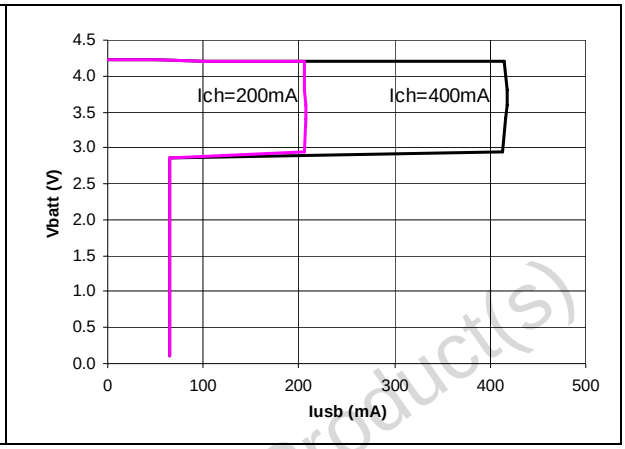



**Figure 5. Charge current vs. temperature (charge from MAIN, 1A setting)**

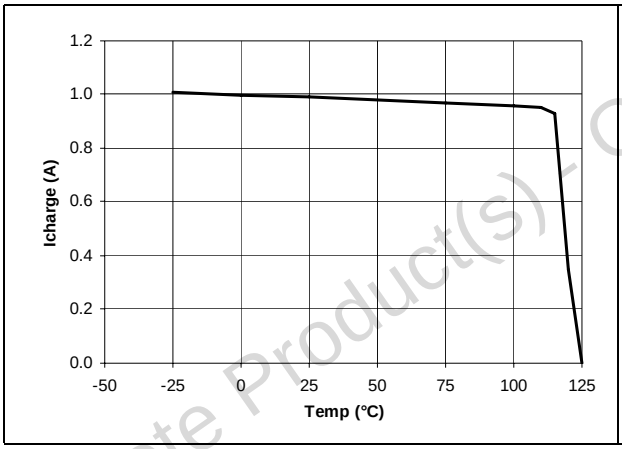



**Figure 6. Charge current vs. temperature (charge from USBPWR)**

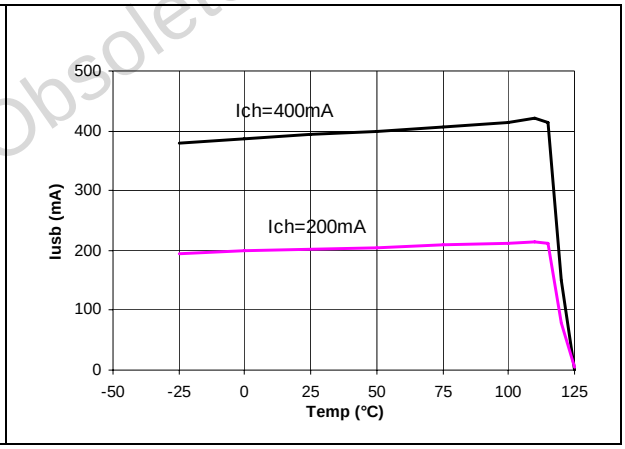
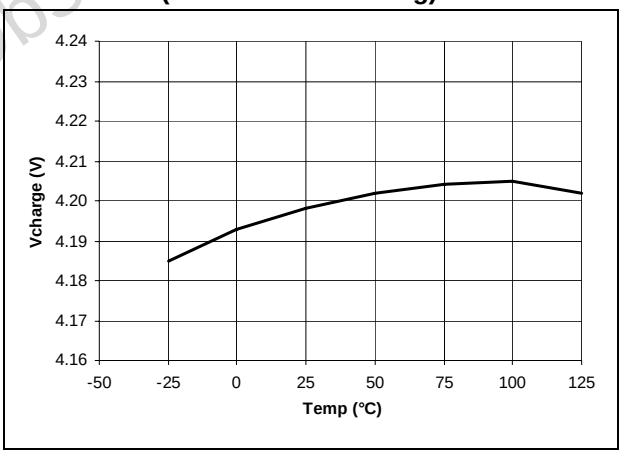



**Figure 7. Charge voltage vs. temperature (4.2V nominal setting)**




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**Figure 8. USB standby input current vs. temperature (charge disabled)**

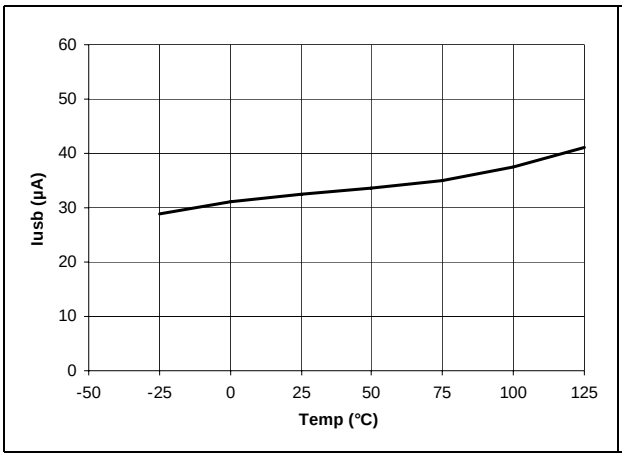



**Figure 9. Battery standby current vs temperature (no MAIN, no USBPWR, gas gauge disabled)**

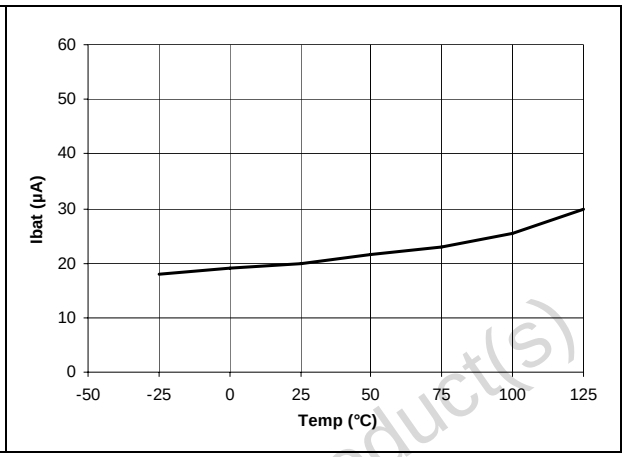



**Figure 10. Watchdog period vs. temperature (normalized to value at 25°C)**

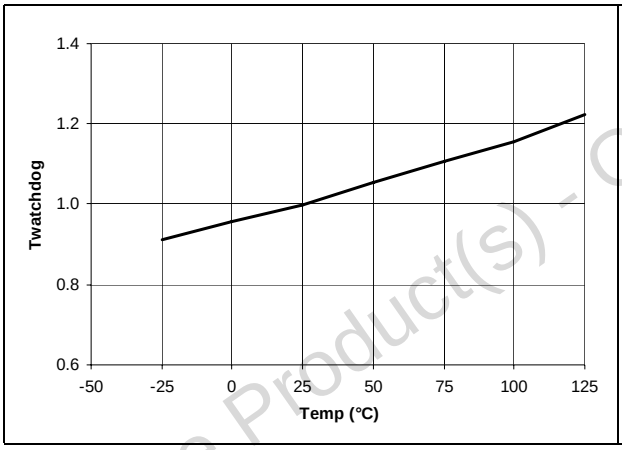



**Figure 11. LDO output voltage vs. temperature (10 mA output current)**

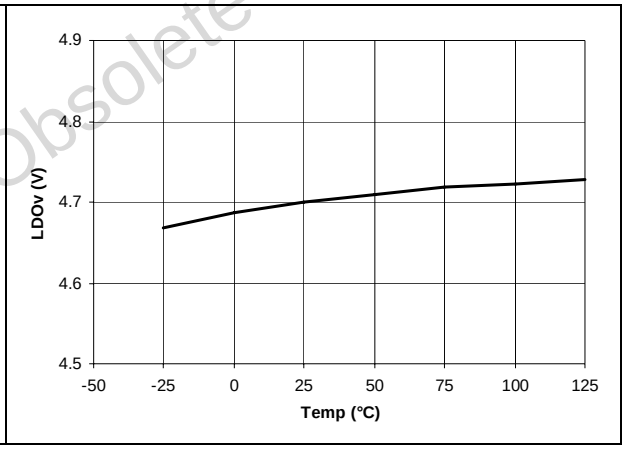
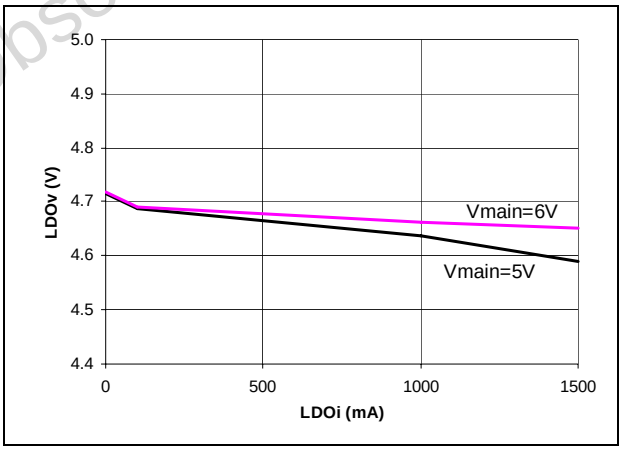



**Figure 12. LDO output voltage vs. output current**




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**Figure 13. Waveforms at USB plug-in**

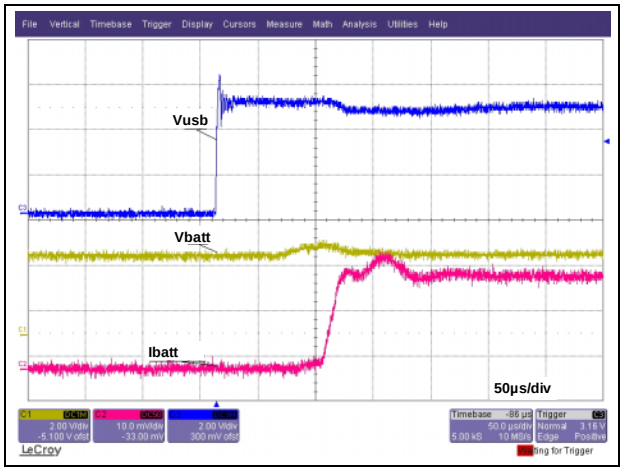



**Figure 14. Switching from USB charge to main charge**

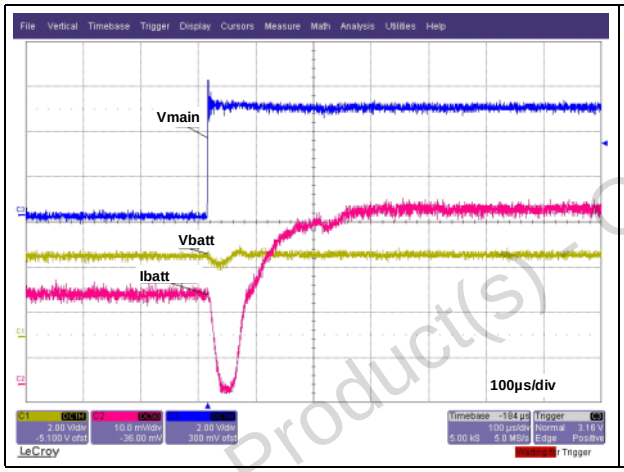
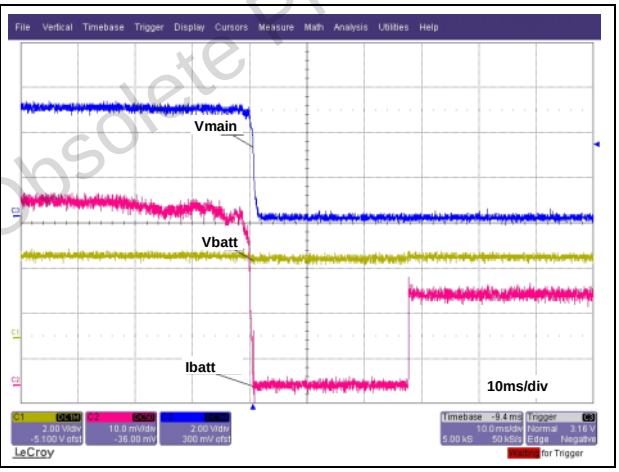



**Figure 15. Switching from main charge to USB charge**



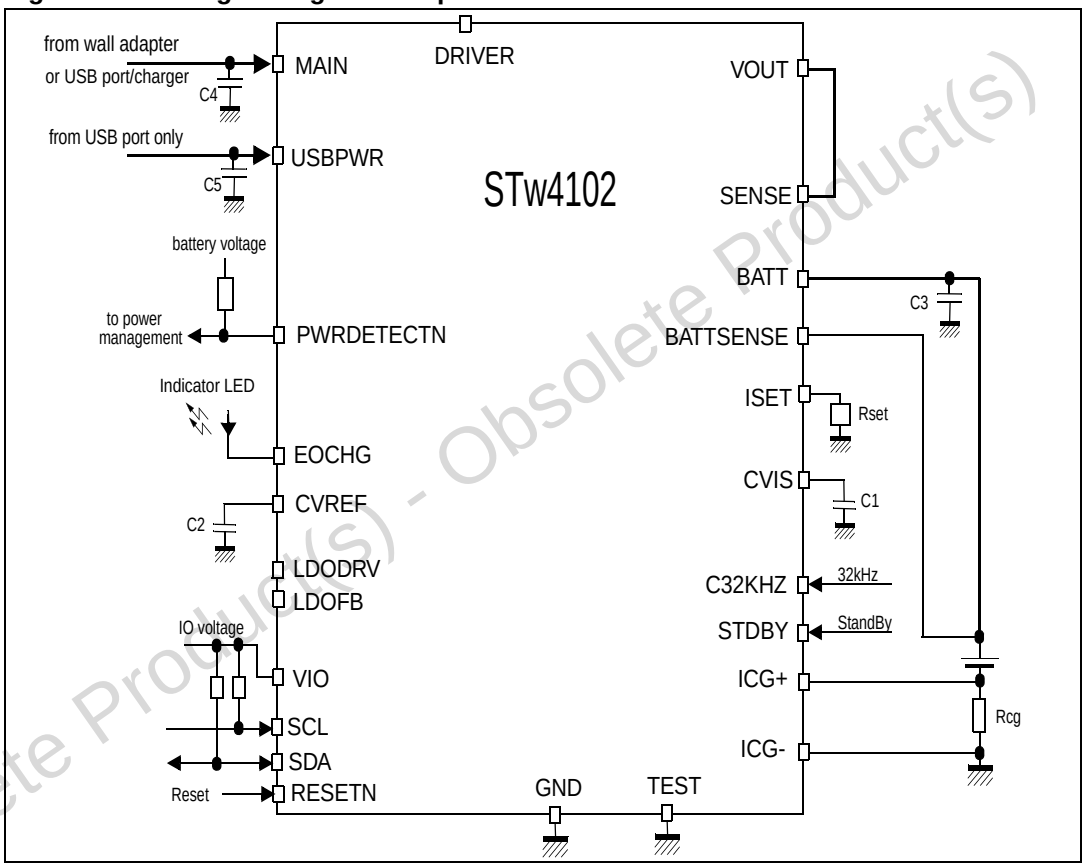

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# 5 Application schematics

## 5.1 Charge from USB or wall adapter

The MAIN input is used with either a wall adapter or a USB charger. The charge current can be programmed to 100 mA or 500 mA max for use with a USB 2.0 port, or programmed to the value set by the $R_{set}$ resistor for use with a wall adapter or a dedicated USB charger. The USBPWR input is used only for charging from a USB port (100 mA or 500 mA max).

**Figure 16. Charge using internal power devices**




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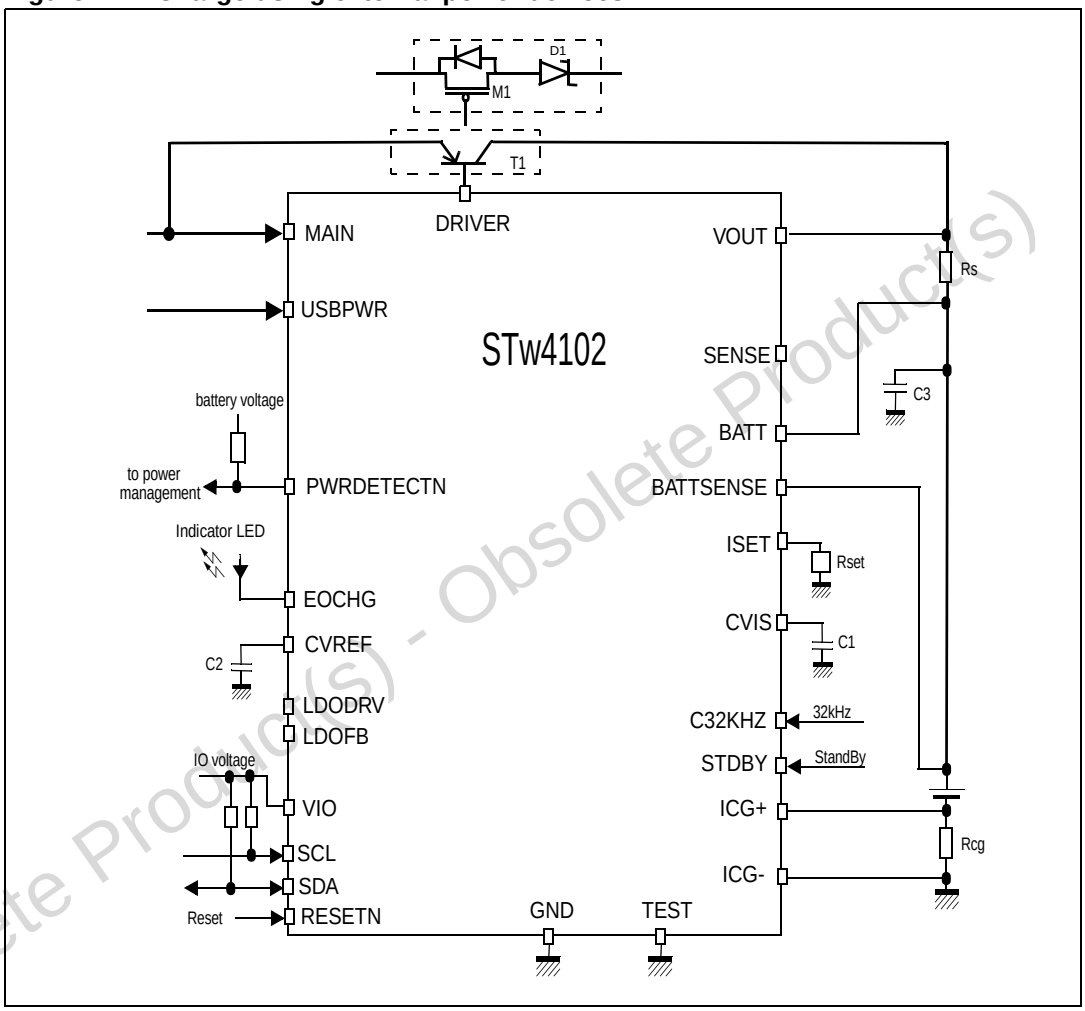
**Table 8. External component list**

| Name | Typ. value | Tolerance | Comments |
|---|---|---|---|
| $R_{set}$ | 12k to 120k | 1% | Main charge current setting |
| $R_{cg}$ | 30mΩ | 1% | Gas gauge sense resistor |
| C1 | 1µF | | Internal supply decoupling capacitor |
| C2 | 1µF | | Internal voltage reference decoupling capacitor |
| C3 | 0.1 to 22µF | | When the battery is removed, a capacitor of at least 15µF is required for low ripple on the battery line. |
| C4 | 0.1 to 1µF | | MAIN input decoupling capacitor |
| C5 | 0.1 to 1µF | | USBPWR input decoupling capacitor |

## 5.2 Charge currents higher than 1 Amp

One-time programming (OTP) options offer the ability to use an external power device or an external sense resistor to handle charge currents higher than 1 A from the wall adapter. These OTP options are set by STMicroelectronics at factory level.

**Figure 17. Charge using external power devices**




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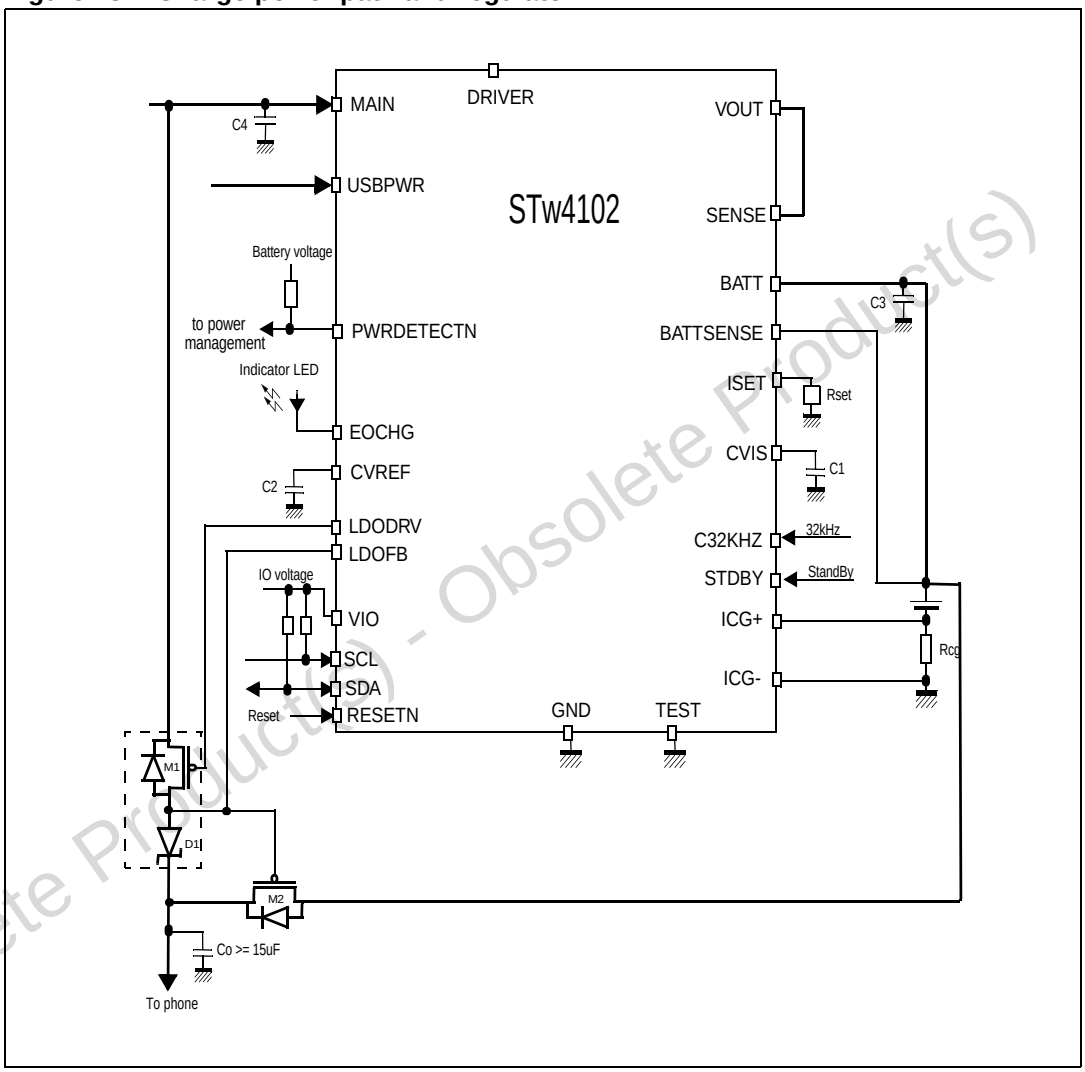
**Table 9. Component list for external power devices**

| Name | Typ. value | Tolerance | Comments |
|---|---|---|---|
| $R_{set}$ | 8k to 12k | 1% | Main charge current setting |
| $R_S$ | 200mΩ | 1% | External current sense resistor |
| T1 or M1 + D1 | STT818B STS2DPFS20V | | PNP transistor PMOS transistor with Schottky diode |

## 5.3 Using LDO regulator to supply telephone from wall adapter

The regulator with external power PMOS (M1) supplies the telephone while the battery is discharged or unplugged. When the charger is unplugged, the phone is supplied by the battery through Power MOS M2. A Schottky diode (D1) avoids reverse current.

**Figure 18. Charge power path and regulator**




Obsolete Product(s) - Obsolete Product(s)

**Table 10. Component list for LDO regulator**

| Name | Typ. value | Tolerance | Comments |
|---|---|---|---|
| M1 + D1 | STS2DPFS20V | | PMOS transistor with Schottky diode |
| M2 | STT5PF20V | | PMOS transistor |
| Co | 10µF to 22µF | | An output capacitor Co of at least 10µF is required. |
| C4 | Co | | An input capacitor C4 equal to or larger than Co is required on MAIN input. |

# 6 Battery charger

## 6.1 Charge cycle

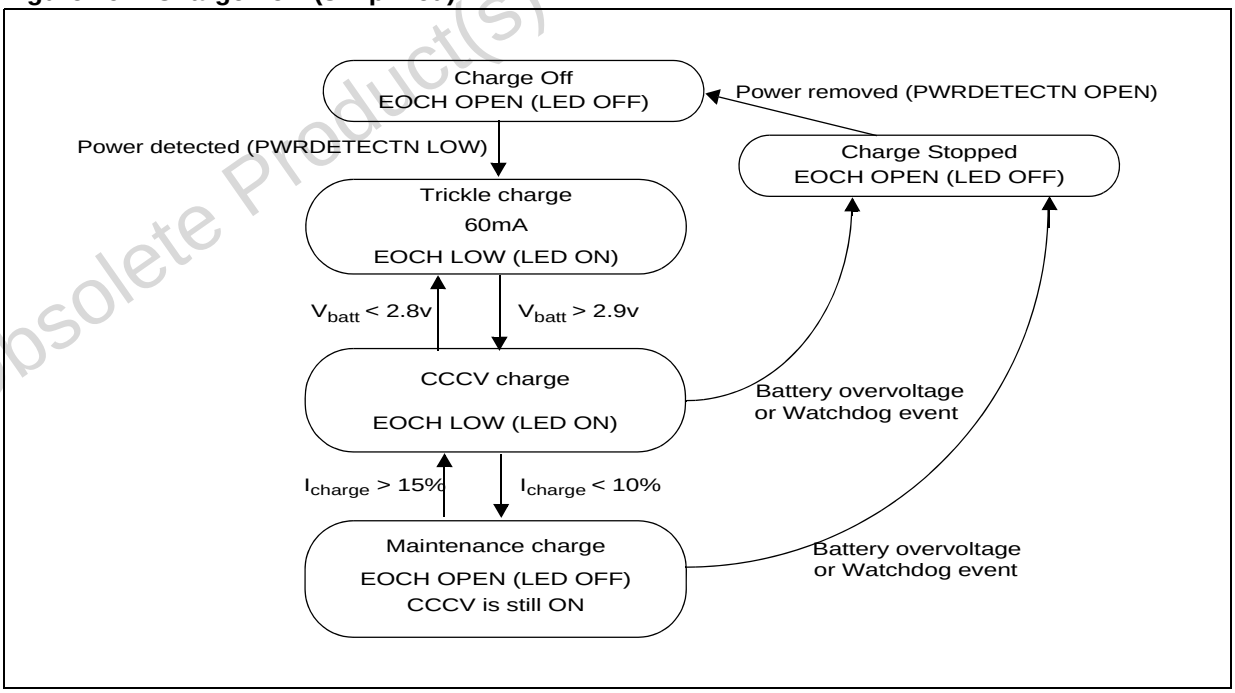
The charge cycle is initiated when the presence of a power source on either the MAIN or USBPWR inputs is detected (the PWRDETECTN pin goes low), while the charger is enabled by the CHG_ENA bit of the REG_CHG1 control register. If both supplies are connected, the MAIN input path is selected.

The EOCHG output pin is driven low as the charge begins. If the battery voltage is lower than the trickle threshold, the charge cycle begins in trickle mode with a low current (default value: 60 mA) until the battery voltage reaches the trickle voltage threshold (default value: 2.9 V). Once the battery voltage rises above this threshold, the charger enters into fast charge mode where the programmed charge current $I_{charge}$ or $I_{USB}$ is supplied to the battery.

When the battery voltage approaches the programmable charge voltage (4.10V, 4.20V, 4.30V or 4.35V), the charger enters into a constant voltage charging mode and the charging current decreases. When the current level reaches the end-of charge level (10% of $I_{charge}$), the EOCHG status pin is switched off (open) to indicate that the battery is almost fully charged, and the charger enters maintenance mode.

In maintenance mode, the charger continues to monitor the battery voltage to maintain the battery voltage level. The maintenance mode lasts until the charge is stopped by clearing the CHG_ENA bit in the REG_CHG1 control register, or by removing the power source (PWRDETECTN is opened).

**Figure 19. Charge flow (simplified)**




Obsolete Product(s) - Obsolete Product(s)

## 6.2 Trickle charge

The trickle charge mode is enabled when the battery voltage $V_{batt}$ is lower than the trickle voltage threshold $V_{trickle}$. An internal current source charges the battery. When $V_{batt}$ is above $V_{trickle}$, the trickle current generator is off and the battery is charged using the constant current method.

The trickle voltage threshold and trickle current are defined by OTP configuration bits and are factory set to 2.9 V and 60 mA by default. Other values are possible, see *Section 9: Factory OTP options on page 24*.

## 6.3 Charging from a wall adapter

The MAIN input is used for charging from a wall adapter or a dedicated USB charger. The SEL_DC_USB bit (bit 5 of register REG_CHG0) must be set to 0. The fast charge current is defined by the external resistor $R_{set}$ connected to the ISET pin, and can be set up to 1 A.

The value of the fast charge current is given by the following formula:

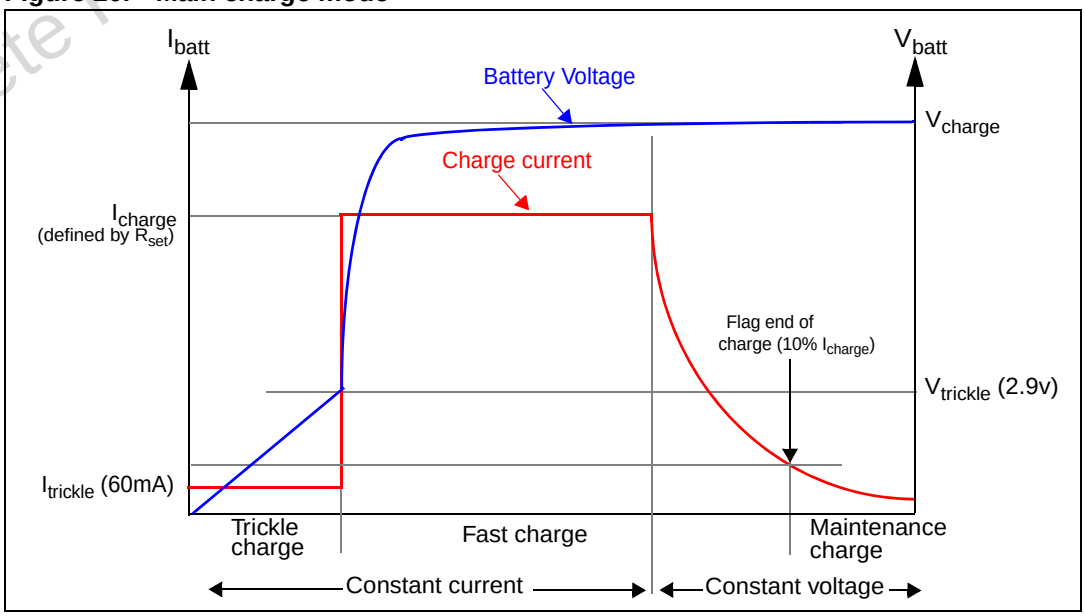
$$I_{charge} = 12000 / R_{set}$$

In the constant voltage mode, the charger output voltage is regulated with 1% accuracy. The charger output voltage is programmable using the REG_CHG0 register, bits 3 and 4 (see *Table 11*).

**Table 11. Charger output voltage**

| REG_CHG0[4] | REG_CHG0[3] | $V_{charge}$ |
|---|---|---|
| 0 | 0 | 4.10V +/-1% |
| 0 | 1 | 4.20V +/-1% |
| 1 | 0 | 4.30V +/-1% |
| 1 | 1 | 4.35V +/-1% |

**Figure 20. Main charge mode**




Obsolete Product(s) - Obsolete Product(s)

## 6.4 Charging from a USB port

The MAIN or USBPWR input can be used to charge from a USB 2.0 port. When using the MAIN input, bit SEL_DC_USB (bit 5 of register REG_CHG0) must be set to 1. Charging from a USB port is similar to charging from a wall adapter, except the fast charge current $I_{USB}$ is set internally and depends on bits 6 and 7 of the control register REG_CHG0.

**Table 12. USB charge current**

| REG_CHG0[7] | REG_CHG0[6] | $I_{USB}$ (typ) |
|---|---|---|
| 0 | 0 | 60mA (100 mA max) |
| 0 | 1 | 200mA |
| 1 | 0 | 400mA (500 mA max) |
| 1 | 1 | off |

## 6.5 Charging using external power devices

To support charge currents higher than 1 A from the main supply adapter, the STw4102 provides the option to use an external power device and sense resistor. This OTP option is factory set.

The STw4102 driver is able to drive an external PNP (STT818B or equivalent) or a PMOS plus Schottky diode (STS2DPFS20V or equivalent). The driver maximum sink current is 60 mA.

The external current sensing device is usually a 200 mΩ shunt resistor. With this resistor value, the trickle and USB charge currents are close to the nominal values.

## 6.6 Charge mode summary

*Table 13* summarizes the different charge modes.

**Table 13. Charge modes**

| $V_{batt}$ | MAIN detected | USBPWR detected | CHG_ENA bit | SEL_DC_USB bit | Charge |
|---|---|---|---|---|---|
| - | x | x | 0 | x | Charge disabled |
| | 0 | 0 | 1 | x | No charge |
| under $V_{trickle}$ | 1 | x | 1 | x | Trickle charge from MAIN |
| | 0 | 1 | | | Trickle charge from USBPWR |
| above $V_{trickle}$ | 1 | x | 1 | 0 | Fast charge from MAIN input, current set by Rset |
| | | | 1 | 1 | Fast charge from MAIN input, current set by USB_ICHG bits |
| | 0 | 1 | 1 | x | Fast charge from USBPWR input, current set by USB_ICHG bits |

Obsolete Product(s) - Obsolete Product(s)

## 6.7 Watchdog timer

When the fast charge is active, a watchdog timer starts to prevent damage on the battery. The system controller refreshes the watchdog periodically in order let the charge continue. When the watchdog time elapses, the charge is stopped.

When the charge starts in trickle mode, to allow the battery to be charged although the system controller is not running, the watchdog is disabled. However, if for any reason the charger goes from fast charge mode to trickle mode, then the watchdog is not disabled to protect against battery failure.

Watchdog timing can be 1 minute, 15 minutes, 30 minutes or 60 minutes. It is programmable through the $I^2C$ interface. The watchdog can be reset by the $I^2C$ interface (bit WDOG_RST) or by unplugging the charger (PWRDETECTN goes to low). The watchdog can also be enabled and disabled through the $I^2C$ interface.

In the standard configuration, the default state at powerup is watchdog enabled and the timing is one minute.

## 6.8 Thermal regulation

A thermal regulation circuit limits the charge current in case of high power dissipation due to high input voltage or high ambient temperature. The charge current is progressively reduced to maintain the die temperature in a safe area. This allows to charge the battery with the highest possible current depending on the operating conditions, and protects the device against any damage.

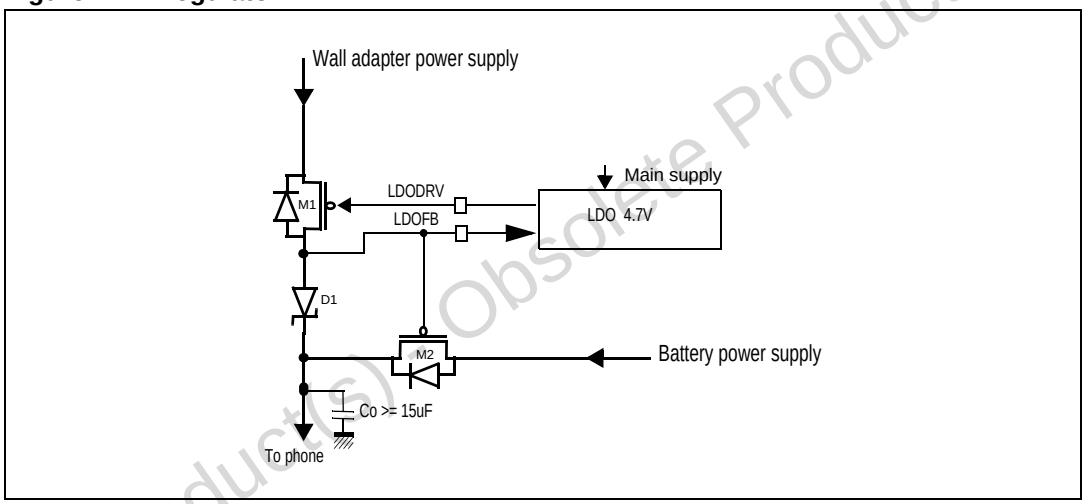
Obsolete Product(s) - Obsolete Product(s)

# 7 Low drop-out regulator

The purpose of the low drop-out regulator (LDO) is to supply the phone directly from the wall adapter when the battery is low or not present. When the wall adapter is present, MOSFET is off and the phone supply is regulated at 4.7 V minus the drop voltage across D1. When the MAIN pin is not connected, MOSFET M2 is on (the gate is pulled down) and the D1 diode avoids any reverse current. The LDO output current is limited by The M1 MOSFET and D1 diode current capabilities. An output capacitor $C_o$ of at least 15 µF is required. The schematics are illustrated in *Figure 21*.

When the battery is fully discharged, the regulator can charge the battery from the main supply and at the same time supply the phone, which avoids waiting for the battery to be charged up to the minimum operating voltage before using the phone.

**Figure 21. Regulator**




When the main supply is above the low dropout threshold $LDO_{power_th}$ (about 7.2 V), then the LDO is turned off to protect the external PMOS against high power dissipation as shown in *Figure 22*. $LDO_{power_th}$ hysteresis is around 0.7 V. By default, this protection feature is enabled, but can be disabled at factory level by OTP.

**Figure 22. Supply voltage**




Obsolete Product(s) - Obsolete Product(s)

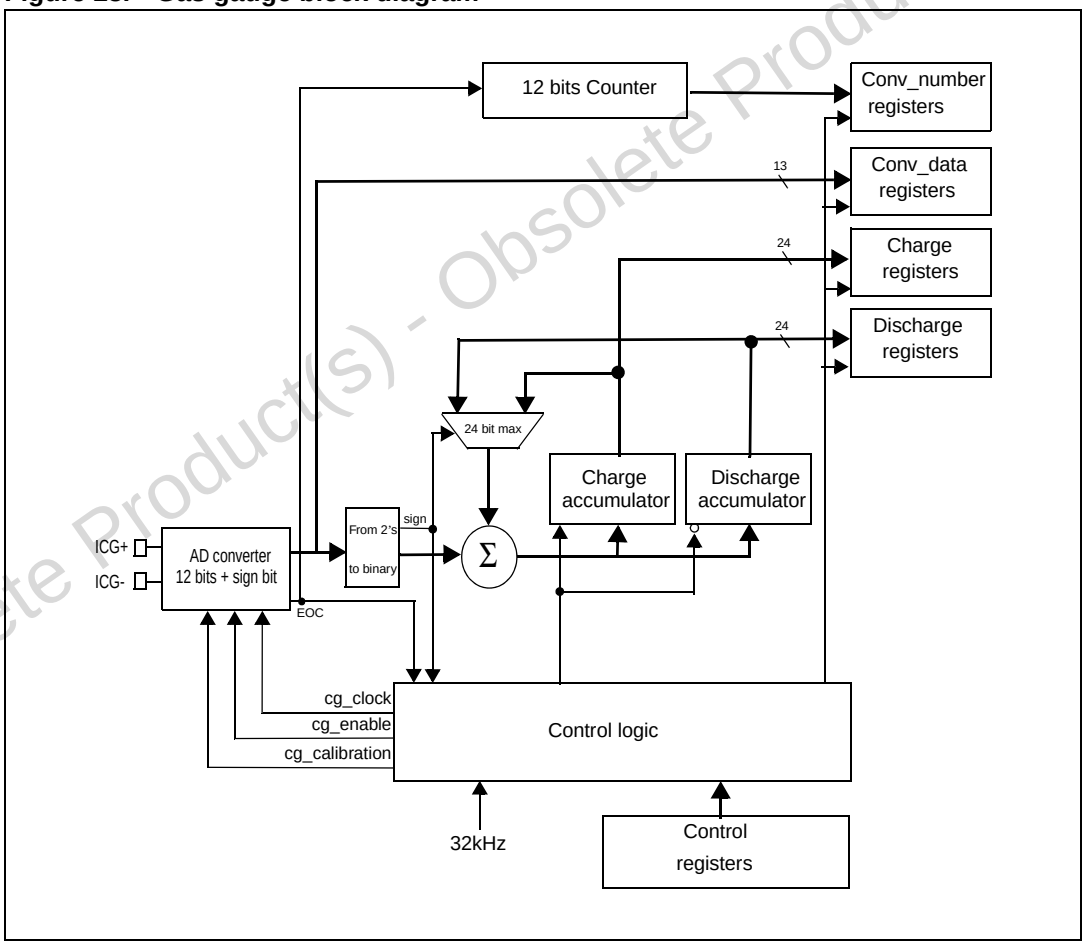
# 8 Battery monitoring

## 8.1 Gas gauge

The gas gauge is designed to monitor the battery capacity. A current sensing resistor (typically of 30 mΩ) is needed between the negative terminal of the battery and the ground. The sensing resistor voltage drop is input to a 13-bit integrating AD converter. When a conversion cycle is completed, depending on the output sign, the result is forwarded to the charge or discharge 24-bit accumulator, and the number of conversions is incremented in a 12-bit counter.

One accumulator accumulates current flowing into the battery during charging and the other accumulates discharge current during system operation. The remaining battery charge is given by the difference between the charge and discharge accumulators.

**Figure 23. Gas gauge block diagram**




Obsolete Product(s) - Obsolete Product(s)

The Digital Base Band (DBB) can control, enable and read gas gauge data through $I^2C$ control registers. The DBB can read the value of the most recent conversion in two's complement format by reading the CONVDATA registers.

The RD_REQ bit enables the transfer of the charge/discharge accumulators and conversion counter register. The transfer can take up to eight 32 kHz cycles, therefore a delay of

approximately 250 microseconds must be respected between the time the RD_REQ bit is set and the actual register reading. The RD_REQ bit is automatically cleared after the transfer.

A high value written to the RST_CHRG, RST_DCHRG or RST_COUNTER bits of the control register resets respectively the charge accumulator, discharge accumulator or conversion counter. If these bits are set together with the RD_REQ bit, then the reset occurs after the transfer to the charge, discharge or conversion counter register respectively. The RST_CHRG, RST_DCHRG or RST_COUNTER bits are automatically cleared after the reset.

The differential inputs are scaled to the full range of the AD converter, introducing a small offset error. A high value written to the CG_CAL bit of the control register connects the inputs of the AD converter together, allowing the DBB to measure the digital offset error. Using this measurement, the gas gauge can be calibrated to reduce the offset error.

The conversion cycle of a 12-bit plus 1 sign-bit AD converter is $2^{13}$ (8192) clock cycles. Using the 32.768kHz RTC clock, the conversion cycle time is 250 ms. The LSB value is 23.54 µV, which corresponds to a current of 784.7 µA with a typical 30 mΩ sense resistor. Given a 250 ms conversion cycle time, this LSB value corresponds to a charge of 54.5 nAh. Under these conditions, the 24-bit accumulator has a capacity of 914 mAh.

The gas gauge system is disabled when the battery voltage is below the Power On Reset threshold (2.7 V), or when the RESETN pin is driven low (CG_ENA bit default value is 0).

During normal operation, either the STDBY pin or the CG_ENA bit can be used to disable the gas gauge function. When the STDBY pin is low, the gas gauge is disabled without waiting for the end of the current conversion. When the CG_ENA bit is low, the current gauge is disabled at the end of the current conversion.

## 8.2 Battery voltage monitoring

The battery voltage can be measured by means of a 7- or 12-bit A/D converter. This function is enabled and configured using the following bits of the ADCTRL register:

- The ADPOWERON bit enables battery voltage monitoring.
- The ADRESOLUTION bit allows to select 7- or 12-bit conversion.
- The ONSTATE bit is set when the ADC converter is ready.
- The ADSTART bit starts a conversion; it is automatically cleared after writing.
- The ADRUN bit indicates that a conversion is in progress. The result is available when the ADRUN bit goes low, and it can be read in the ADDATA registers.

A high value written to the ADCAL bit of the control register connects the input of the A/D converter to ground, allowing the DBB to measure the digital offset error. Using this measurement, the AD converter can be calibrated to reduce the offset error.

The conversion cycle of a 7 (12) bit conversion is $2^8$=256 ($2^{13}$=8192) clock cycles. Using the 32.768kHz RTC clock, the conversion cycle time is 7.8 (250) ms. LSB value is 45 (1.4) mV.

When the battery voltage falls below the Power On Reset threshold, or when the RESETN input is driven low, the battery voltage monitoring function is disabled.

Obsolete Product(s) - Obsolete Product(s)

# 9 Factory OTP options

*Table 14* summarizes the one-time programming (OTP) options offered by STMicroelectronics to customize the STw4102 at factory level.

**Table 14. Factory OTP options**

| Option | Configuration bits | Value |
|---|---|---|
| TRICKLE current (wall adapter charge only) | OTP_TC=0 (default)<br>OTP_TC=1 | 60 mA<br>120 mA |
| TRICKLE threshold voltage | OTP_TV1, OTP_TV0 :<br>00<br>01<br>10<br>11 (default) | <br>2.3 V<br>2.5 V<br>2.7 V<br>2.9 V |
| MAIN input mode at powerup | OTP_SEL_DC_USB=0 (default)<br>OTP_SEL_DC_USB=1 | Wall adapter mode<br>USB mode |
| Watchdog state at powerup | OTP_WD_ENA=0<br>OTP_WD_ENA=1 (default) | Disabled<br>Enabled |
| Watchdog period at powerup | OTP_WD_TIME1, OTP_WD_TIME0 :<br>00 (default)<br>01<br>10<br>11 | <br>1 min<br>15 min<br>30 min<br>60 min |
| Power switch | OPT_IEPD=0 (default)<br>OPT_IEPD=1 | Internal<br>External |
| Sense resistor | OPT_IERSENSE=0 (default)<br>OPT_IERSENSE=1 | Internal<br>External |
| LDO overvoltage protection | OPT_LDOEXT_PRO=0<br>OPT_LDOEXT_PRO=1 (default) | Disabled<br>Enabled |
| $I^2C$ ID address | OTP_ID2, OTP_ID1, OTP_ID0 :<br>000 (default)<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | <br>70h<br>71h<br>72h<br>73h<br>74h<br>75h<br>76h<br>77h |

For any option request other than the standard configuration (default values), contact STMicroelectronics to get a specific order code.

Obsolete Product(s) - Obsolete Product(s)

# 10 I²C interface

## 10.1 Read and write operations

The I²C interface is used to control the charging and the gas gauge system. It is compatible with the I²C specification of Philips (version 2.1). It is a slave serial interface with a serial data line (SDA) and a serial clock line (SCL):

SCL: input clock used to shift data

SDA: input/output bi-directional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity. The bi-directional data line supports transfers up to 400 kbit/s (fast-mode). The data is shifted into and from the chip on the SDA line, MSB first.

The first bit must be high (START), followed by the Device ID and Read/Write control bit (see *Table 15*). The AddrID0 to AddrID2 bits are factory programmable, their default ID value is 70h (AddrID0 = AddrID1 = AddrID2 = 0). Then, the STw4102 sends an acknowledge at the end of the 8-bit transmission.

The next 8 bits correspond to the address register, followed by another acknowledge. *Table 16* shows the address register format.

The data field is sent last. It can be composed of several 8-bit data registers, each followed by an acknowledge. *Table 17* shows the data register format.

The STw4102 supports byte read, word read, block read, and byte write operations. The transmission protocol is summarized in *Figure 24* and *Figure 25*.

Obsolete Product(s) - Obsolete Product(s)

**Table 15. Device ID and R/W bit format**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | AddrID2 | AddrID1 | AddrID0 | R/W |

**Table 16. Address register format**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| RegAddr7 | RegAddr6 | RegAddr5 | RegAddr4 | RegAddr3 | RegAddr2 | RegAddr1 | RegAddr0 |

**Table 17. Data register format**

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| DATA7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |

**Figure 24. Byte, word and block read operation**

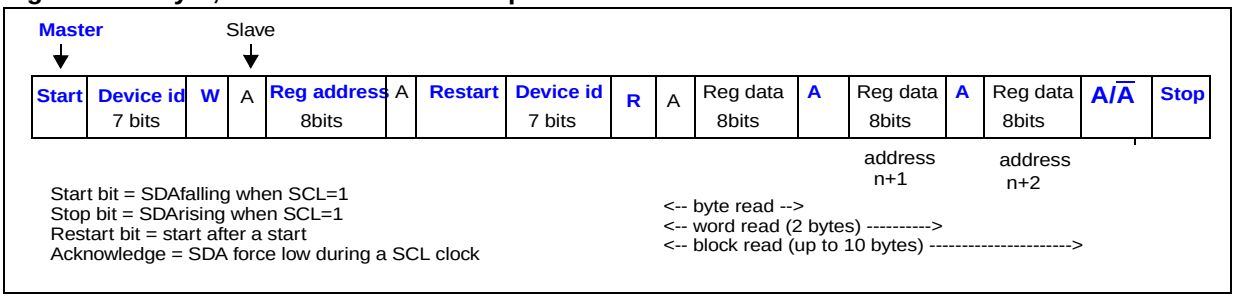
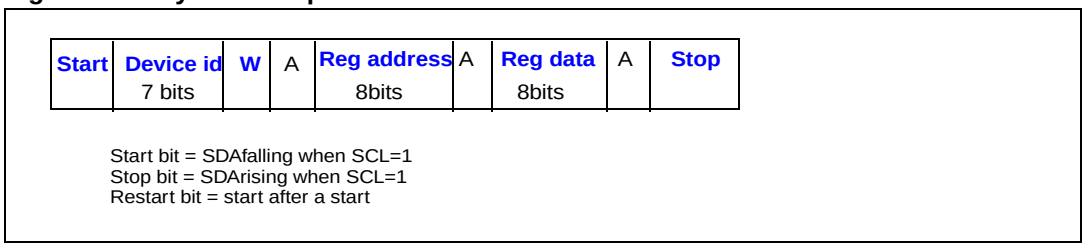


**Figure 25. Byte write operation**




## 10.2 Register mapping

The mapping of all registers is shown in *Table 18*. Individual register descriptions are shown in *Table 19* to *Table 35*. Power-up values are set at power startup, or at reset (RESETN pin falling edge). Charge and discharge internal accumulators are not affected by RESETN.

**Table 18. Register mapping**

| Name | Address (dec.) | Description |
|---|---|---|
| REG_CHG0 | 0 | Charge control and status |
| REG_CHG1 | 1 | Charge enable |
| REG_WDOG | 2 | Watchdog control |
| REG_CG | 3 | Gas gauge control |
| REG_CHARGE_LOW | 4 | Gas gauge charge data, bits 0-7 |
| REG_CHARGE_MID | 5 | Gas gauge charge data, bits 8-15 |
| REG_CHARGE_HIGH | 6 | Gas gauge charge data, bits 16-23 |
| REG_DISCHARGE_LOW | 7 | Gas gauge discharge data, bits 0-7 |
| REG_DISCHARGE_MID | 8 | Gas gauge discharge data, bits 8-15 |
| REG_DISCHARGE_HIGH | 9 | Gas gauge discharge data, bits 16-23 |
| REG_CONVDATA_LOW | 16 | Gas gauge AD converter data, bits 0-7 |
| REG_CONVDATA_HIGH | 17 | Gas gauge AD converter data, bits 8-12 |
| REG_CONVNUMBER_LOW | 18 | Number of conversions, bits 0-7 |
| REG_CONVNUMBER_HIGH | 19 | Number of conversions, bits 8-11 |
| REG_ADCTRL | 20 | Battery voltage monitor control |
| REG_ADDATA_LOW | 21 | Battery voltage monitor AD converter data, bits 0-7 |
| REG_ADDATA_HIGH | 22 | Battery voltage monitor AD converter data, bits 8-10 |

Obsolete Product(s) - Obsolete Product(s)

**Table 19. REG_CHG0. address 0 (00h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| CHARGERUN | 0 | R | 0 | 0: Charge is below 10% of fast charge current.<br>1: Charge is above 10% of fast charge current. |
| MAINDETECT | 1 | R | 0 | Main input voltage detection. |
| USBDETECT | 2 | R | 0 | USB input voltage detection. |
| VCHG | [4,3] | R/W | 00 | Charge voltage<br>00=4.1V, 01=4.2V, 10=4.3V, 11=4.35V. |
| SEL_DC_USB | 5 | R/W | 0 | Wall adapter/USB selection for MAIN input<br>0: charge current set by Rset resistor<br>1: charge current set by USB_ICHG bits |
| USB_ICHG | [7,6] | R/W | 00 | USB charge current<br>00=60mA, 01=200mA, 10=400mA, 11=off. |

**Table 20. REG_CHG1. address 1 (01h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| CHG_ENA | 0 | R/W | 1 | 0: Charger disabled.<br>1: Charger enabled. |
| Reserved | [3,1] | R/W | 0 | Reserved bits, to be set to zero. |
| FORCECHARGERUN | 4 | R/W | 0 | 0: no effect.<br>1: force EOCHG low independently of charge state. |
| SEL_IS | 5 | R/W | 0 | 0: Internal supply from Main or USB input when available and charge enabled.<br>1: Internal supply always from Battery. |
| Unused | [7,6] | R/W | | |

**Table 21. REG_WDOG. address 2 (02h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| WDOG_EN | 0 | R/W | 1 | 0: Watchdog disabled.<br>1: Watchdog enabled. |
| WDOG_TIME | [2,1] | R/W | 00 | 00=1 minute, 01=15 minutes, 10=30 minutes, 11=60 minutes. |
| WDOG_RST | 3 | R/W | 0 | 0: No effect.<br>1: Reset watchdog. Bit clear after watchdog reset. |
| Reserved | [5,4] | R/W | 0 | Reserved bits, to be set to zero |
| WDOG_INT | 6 | R | x | 1: Watchdog is elapsed. |
| Unused | 7 | R/W | | |

Obsolete Product(s) - Obsolete Product(s)

**Table 22. REG_CG. address 3 (03h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| CG_ENA | 0 | R/W | 0 | 0: Gas gauge disabled. Charge/discharge accumulators are reset.<br>1: Gas gauge enabled. |
| RST_CHRG | 1 | R/W | 0 | 0: No effect.<br>1: Resets the charge accumulator. This bit auto clears after the charge register is reset. |
| RST_DCHRG | 2 | R/W | 0 | 0: No effect.<br>1: Resets the discharge accumulator. This bit auto clears after the discharge register is reset. |
| RST_COUNTER | 3 | R/W | 0 | 0: No effect.<br>1: Resets the counter conversion. This bit auto clears after the counter register is reset. |
| RD_REQ | 4 | R/W | 0 | 0: No effect.<br>1: Transfers the 24 bit charge/discharge accumulators and the conversion counter to the charge/discharge and conversion number registers. This bit auto clears after the transfer. |
| CG_CAL | 5 | R/W | 0 | 0: No effect.<br>1: Allows to calibrate AD converter. |
| CG_EOC | 6 | R | 0 | Set high at the end of a conversion. Cleared after read. |
| Unused | 7 | R/W | | |

**Table 23. REG_CHARGE_LOW. address 4 (04h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[7..0] | [7..0] | R | 00 | Current charge data. |

**Table 24. REG_CHARGE_MID. address 5 (05h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[15..8] | [7..0] | R | 00 | Current charge data. |

**Table 25. REG_CHARGE_HIGH. address 6 (06h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[23..16] | [7..0] | R | 00 | Current charge data. |

**Table 26. REG_DISCHARGE_LOW. address 7 (07h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[7..0] | [7..0] | R | 00 | Current discharge data. |

Obsolete Product(s) - Obsolete Product(s)

**Table 27. REG_DISCHARGE_MID. address 8 (08h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[15..8] | [7..0] | R | 00 | Current discharge data. |

**Table 28. REG_DISCHARGE_HIGH. address 9 (09h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[23..16] | [7..0] | R | 00 | Current discharge data. |

**Table 29. REG_CONVDATA_LOW. address 16 (10h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[7..0] | [7..0] | R | 00 | AD converter data. |

**Table 30. REG_CONVDATA_HIGH. address 17 (11h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[12..8] | [4..0] | R | 0 | AD converter data. |
| Not used | [7..5] | R | 0 | |

**Table 31. REG_CONVNUMBER_LOW. address 18 (12h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[7..0] | [7..0] | R | 0 | Number of conversions. |

**Table 32. REG_CONVNUMBER_HIGH. address 19 (13h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[11..8] | [3..0] | R | 0 | Number of conversions. |
| Reserved | [7..4] | R | x | Reserved bits. |

Obsolete Product(s) - Obsolete Product(s)

**Table 33. REG_ADCTRL. address 20 (14h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| ADPOWERON | 0 | R/W | 0 | 0: Allows ADC shutdown.<br>1: Enables ADC operation. |
| ONSTATE | 1 | R | 0 | 0: ADC is not ready for operation.<br>1: ADC is ready for operation. |
| ADSTART | 2 | R/W | 0 | 0: No effect.<br>1: Allows to start a conversion. Cleared upon writing. |
| ADRUN | 3 | R | 0 | 0: An AD conversion is not running.<br>1: An AD conversion is running. |
| ADRESOLUTION | 4 | R/W | 0 | 0: 7 bits.<br>1: 12 bits. |
| ADCAL | 5 | R/W | 0 | 0: No effect.<br>1: Allows to calibrate AD converter. |
| Not used | [7,6] | R | 0 | |

**Table 34. REG_ADDATA_LOW. address 21 (15h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[7..0]<br>DATA[6..0] | [7..0]<br>[6..0] | R | 00 | AD converter data in 12 bit mode.<br>AD converter data in 7 bit mode (bit7=0). |

**Table 35. REG_ADDATA_HIGH. address 22 (16h)**

| Name | Pos. | Type | Power-up | Description |
|---|---|---|---|---|
| DATA[11..8] | [3..0] | R | 0 | AD converter data in 12-bit mode (0 in 7-bit mode). |
| Not used | [7..4] | R | 0 | |

Obsolete Product(s) - Obsolete Product(s)

# 11 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

**Table 36. QFN24 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | 0.80 | 1.00 | | | |
| A1 | | 0.00 | 0.05 | | | |
| A2 | 0.65 | | 0.80 | | | |
| D | 4.00 | | | | | |
| D1 | 3.75 | | | | | |
| E | 4.00 | | | | | |
| E1 | 3.75 | | | | | |
| Θ | | | 12° | | | |
| P | 0.42 | 0.24 | 0.60 | | | |
| R | 0.17 | 0.13 | 0.23 | | | |
| e | 0.50 | | | | | |
| N | 24.00 | | | | | |
| Nd | 6.00 | | | | | |
| Ne | 6.00 | | | | | |
| L | 0.40 | 0.30 | 0.50 | | | |
| b | | 0.18 | 0.30 | | | |
| Q | 0.20 | | 0.45 | | | |
| D2 | 2.10 | 1.95 | 2.25 | | | |
| E2 | 2.10 | 1.95 | 2.25 | | | |

Obsolete Product(s) - Obsolete Product(s)

**Figure 26. QFN24 package mechanical drawing**

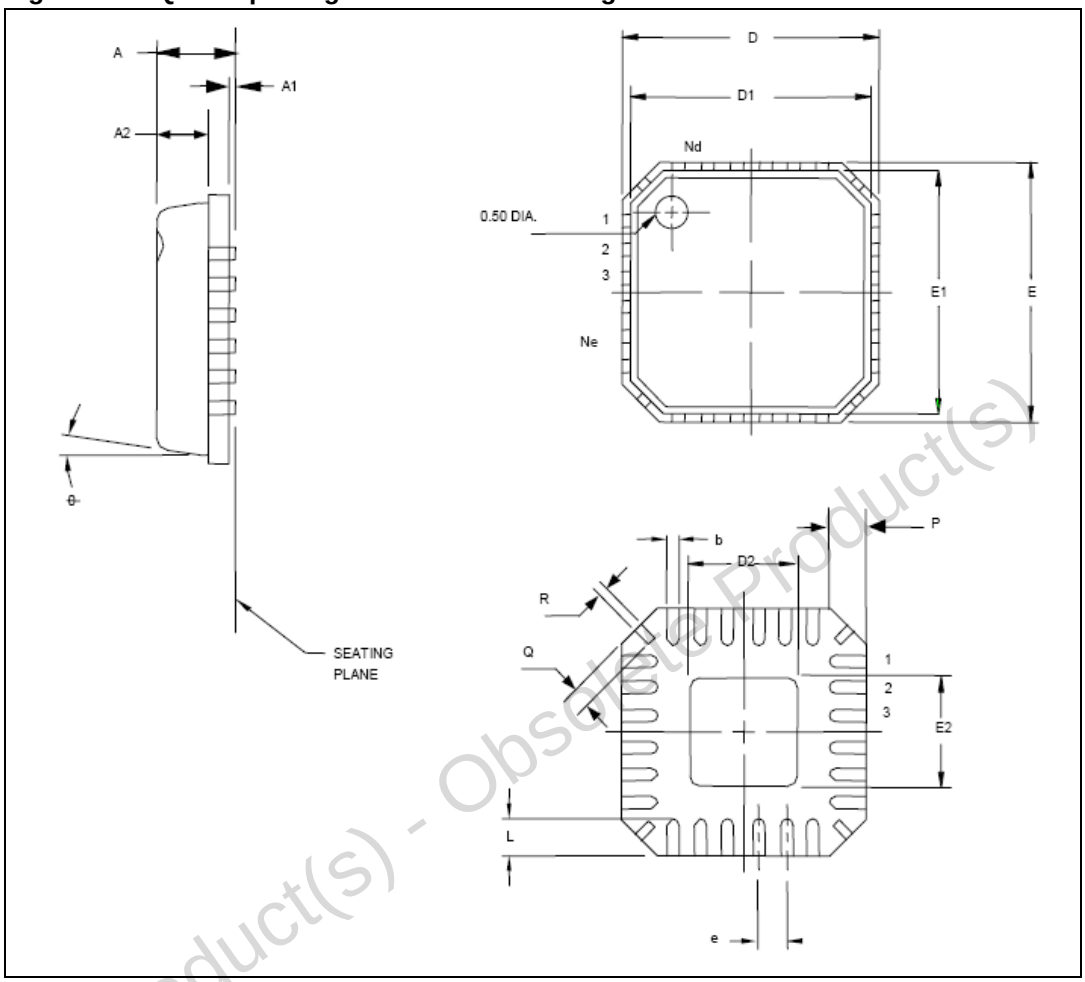
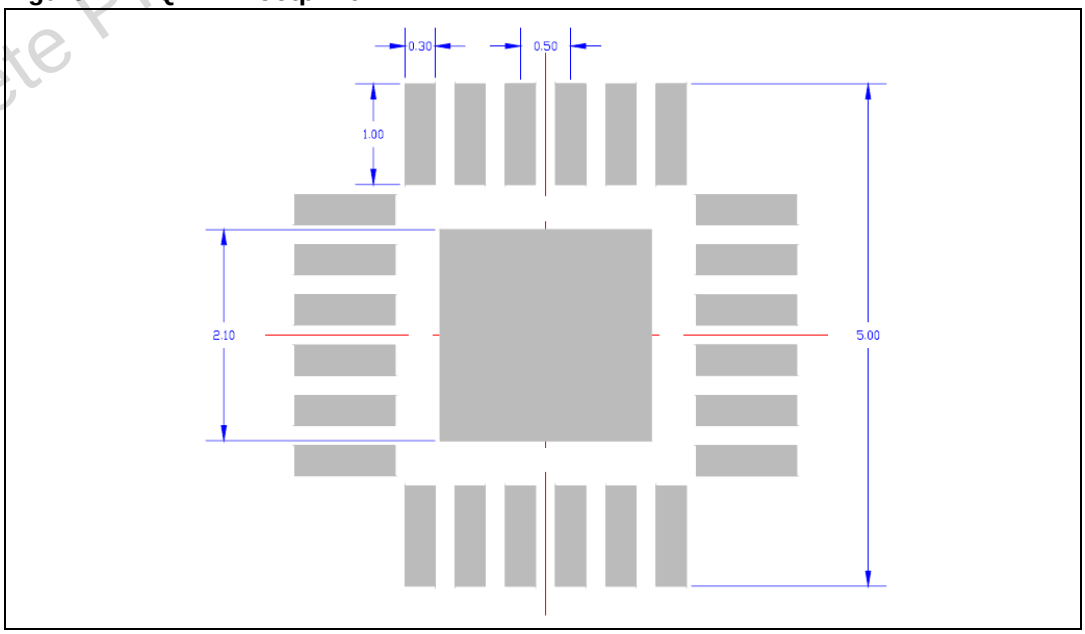



**Figure 27. QFN24 footprint**




Obsolete Product(s) - Obsolete Product(s)

# 12 Ordering information

**Table 37. Order code**

| Order code[1] | Temperature range | Package | Packaging | Marking |
|---|---|---|---|---|
| STw4102IQT | -30° C, +85° C | QFN24 | Tape & reel | W4102I |

1. Order code for parts with standard configuration. Contact STMicroelectronics to get order codes for parts with specific configurations.

# 13 Revision history

**Table 38. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 17-Mar-2008 | 1 | Initial release (preliminary data). |
| 20-Mar-2008 | 2 | Document status promoted from preliminary data to datasheet. |

Obsolete Product(s) - Obsolete Product(s)

Obsolete Product(s) - Obsolete Product(s)

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