MP6526

Hex Half-Bridge Motor Driver with Serial Input Control

DESCRIPTION

The MP6526 is a six-half-bridge, DMOS, output driver with integrated power MOSFETs that can drive up to six different loads.

The six half-bridges can be controlled separately from a standard serial data interface and have various diagnostic functions. The MP6526 has very low quiescent current in standby mode, making it suitable for a wide range of applications.

Full protection features include short-circuit protection (SCP), under-voltage protection (UVP), and thermal shutdown.

The MP6526 requires a minimal number of readily available, standard, external components and is available in SOIC-28, QFN-24 (4mmx4mm), and QFN-24 (5mmx5mm) packages.

FEATURES

- Up to 0.9A Output Current
- Total Max Current 2.4A (All Outputs Combined)
- $R_{DS(ON)}$ (HS + LS) Typically 1.1Ω at 25°C, Maximum 2Ω at 150°C
- Very Low Quiescent Current I_{VS} < 6μA in Standby Mode Versus Total Temperature Range
- Outputs Short-Circuit Protected
- Over-Temperature Protection (OTP) and Pre-Warning
- Under-Voltage Protection (UVP)
- Serial Data Interface
- Various Diagnostic Functions: Shorted Output, Open-Load, Over-Temperature, and Under-Voltage
- Fault Output Flag
- Daisy-Chaining Possible
- Serial Interface Clock Frequency up to 3MHz, 5V Compatible
- Available in SOIC-28, QFN-24 (4mmx4mm) and QFN-24 (5mmx5mm) Packages

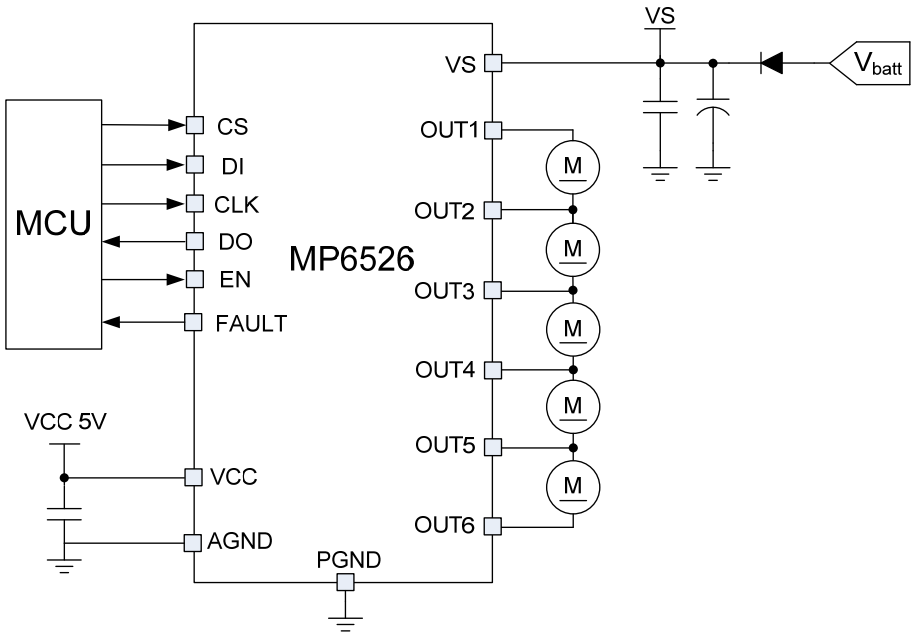
APPLICATIONS

- Drive Various Loads in Automotive and Industrial Applications
- DC Motor

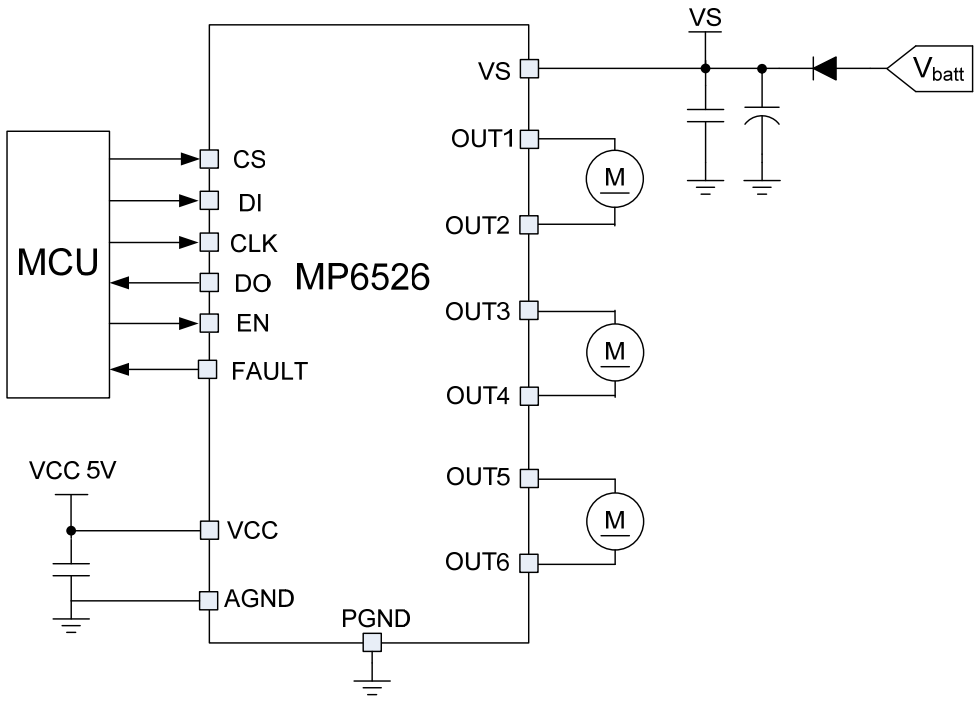
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL APPLICATION



Serial Load Configuration



Parallel Load Configuration (Independent Motor Operation)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6526GY	SOIC-28	*See Below*
MP6526GR	QFN-24 (4mmx4mm)	*See Below*
MP6526GU	QFN-24 (5mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MP6526GY–Z).

TOP MARKING (MP6526GY)

MPSYYWW
MP6526
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6526: Product code of MP6526GY
LLLLLLLLL: Lot number

TOP MARKING (MP6526GR)

MPSYWW
MP6526
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP6526: Product code of MP6526GR
LLLLLL: Lot number

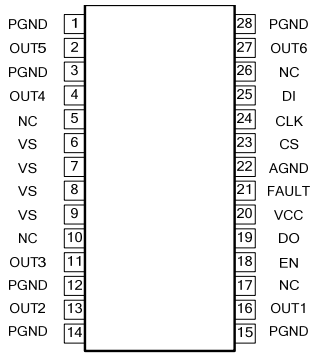
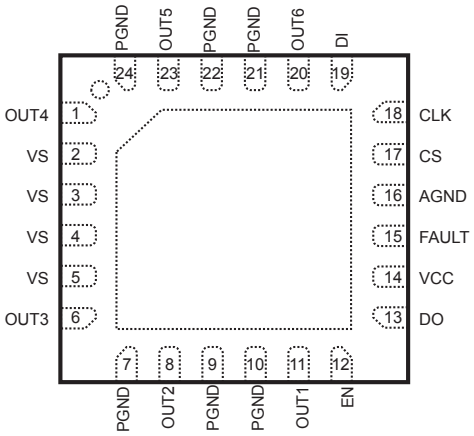
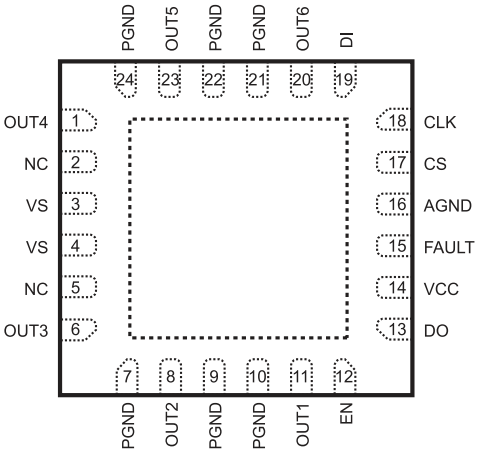
TOP MARKING (MP6526GU)

MPSYYWW
MP6526
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6526: Product code of MP6526GU
LLLLLLL: Lot number

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE REFERENCE

TOP VIEW	TOP VIEW	TOP VIEW
		
SOIC-28	**QFN-24 (4mmx4mm)**	**QFN-24 (5mmx5mm)**

PIN FUNCTIONS

SOIC-28 Pin #	QFN (4x4) Pin #	QFN (5x5) Pin #	Name	Description
1, 3, 12, 14, 15, 28	7, 9, 10, 21, 22, 24	7, 9, 10, 21, 22, 24	PGND	**Power ground.**
2	23	23	OUT5	**Half-bridge output 5.**
4	1	1	OUT4	**Half-bridge output 4.**
5, 10, 17, 26	-	2, 5	NC	**No connection.**
6 - 9	2 - 5	3, 4	VS	**Power supply.**
11	6	6	OUT3	**Half-bridge output 3.**
13	8	8	OUT2	**Half-bridge output 2.**
16	11	11	OUT1	**Half-bridge output 1.**
18	12	12	EN	**Enable.** Drive EN low to put the device in standby mode. Drive EN high for normal operation.
19	13	13	DO	**Serial data output.**
20	14	14	VCC	**Logic supply voltage.**
21	15	15	FAULT	**Fault output.** A low output at FAULT indicates that the IC has detected an over-temperature or over-current condition. This output is open-drain.
22	16	16	AGND	**Analog ground.**
23	17	17	CS	**Chip select input.**
24	18	18	CLK	**Serial clock input.**
25	19	19	DI	**Serial data input.**
27	20	20	OUT6	**Half-bridge output 6.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{VS}) 40V
V_{OUTx} ..... -0.3 to V_{VS} + 0.3V
Logic supply voltage (V_{VCC}) ..... -0.3 to +6.5V
Logic input voltage ..... -0.3 to V_{VCC} + 0.3V
Logic output voltage ..... -0.3 to V_{VCC} + 0.3V
Voltage at all other pins ..... -0.3 to +6.5V
Continuous power dissipation (T_A = +25°C) (2)
SOIC-28 ..... 2.1W
QFN-24 (4mmx4mm) 3W
QFN-24 (5mmx5mm) 3.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -60°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_S) ..... 7V to 28V
Logic supply voltage (V_{VCC}) ..... 4.75V to 5.25V
Operating junction temp. (T_J) ..... -40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC}

SOIC-28 ..... 60 ..... 30 ... °C/W
QFN-24 (4mmx4mm) ..... 42 ..... 9 .... °C/W
QFN-24 (5mmx5mm) ..... 36 ..... 8 .... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD sensitive. Handling precaution is recommended.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

7V < V_{VS} < 28V, V_{VCC} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating supply current (VS)	I_{VS}	V_{VS} < 28V normal operation, all output stages off		2.6	6	mA
		V_{VS} < 28V normal operation, all output low stages on, no load		2.7	6	
		V_{VS} < 28V normal operation, all output high stages on, no load		2.75	6	
Operating supply current (VCC)	I_{VCC}	4.75V < V_{VCC} < 5.25V, normal operation		67	90	µA
Quiescent current (VS)	I_{VS}	V_{VS} = 28V, V_{VCC} = 0V or V_{VCC} = 5V, EN = low, or V_{VCC} = 5V, bit SE = low, output pins to VS and GND		1.8	6	µA
Quiescent current (VCC)	I_{VCC}	4.75V < V_{VCC} < 5.25V, EN or bit SE = low		23	35	µA
Discharge current (VS)	I_{VS}	V_{VS} = 40V, EN = low			3	mA
Internal oscillator frequency	f_{OSC}		85	120	166	kHz
Power-on reset threshold	V_{VCC}		2.3	2.6	3.0	V
Power-on reset delay		After switching on V_{VCC}	30	100	190	µs
Under-voltage lockout threshold rising			5.5		6.5	V
Under-voltage lockout threshold hysteresis				0.6		V
Under-voltage lockout delay time			7	14	23	ms
Output Specification						
HS + LS switch-on resistance	$R_{DS(ON)}$	T_J = -40°C to +125°C		1.1	1.7	Ω
		T_J = +150°C (6)			2	Ω
Inductive shutdown energy (7)					15	mJ
Over-current limit	I_{OCP}		1	1.3	1.8	A
Over-current shutdown delay time		Bit14 (SCT) = low, V_{VS} = 13V	0.1	0.21	0.3	ms
		Bit14 (SCT) = high, V_{VS} = 13V	0.28	0.53	0.72	
Open-load detection current		Bit13 (OLD) = low, output off	1.4	1.9	2.4	mA
Output switch-on/-off delay		V_{VS} = 13V, R_{LOAD} = 50Ω			60	µs
OUTx rising time		V_{VS} = 13V, 10% to 90% V_{OUT}, R_{LOAD} = 50Ω	2	20	50	µs
OUTx falling time		V_{VS} = 13V, 10% to 90% V_{OUT}, R_{LOAD} = 50Ω	2	20	45	µs
Dead time		V_{VS} =13V, R_{LOAD} = 50Ω	2			µs
EN Input						
EN low-level threshold					0.8	V
EN high-level threshold			3	1.7		V
Pull-down current of EN input		V_{EN} = V_{VCC}	10		80	µA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

7V < V_{VS} < 28V, V_{VCC} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal Shutdown and Pre-Warning (7)						
Thermal pre-warning threshold			120	145	170	°C
Thermal pre-warning hysteresis				15		°C
Thermal shutdown threshold			150	175	200	°C
Thermal shutdown hysteresis				15		°C
Ratio thermal shutdown/thermal pre-warning			1.05	1.2		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

SERIAL INTERFACE TIMING ELECTRICAL CHARACTERISTICS (7)

7V < V_{VS} < 28V, V_{VCC} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Logic Inputs (DI, CLK, CS)						
Input low-level threshold					0.3 x V_{VCC}	V
Input high-level threshold			0.7 x V_{VCC}			V
Pull-down current of DI, CLK		V_{DI}, V_{CLK} = V_{VCC}	2		50	µA
Pull-up current of CS		V_{CS} = 0V	2		50	µA
Logic Output (DO)						
Output low level					0.5	V
Output high level			V_{VCC} - 0.7V			V
Leakage current (tri-state)		0V < V_{DO} < V_{VCC}, V_{CS} = V_{VCC}	-10		10	µA
Timing Characteristics						
DO enable after CS falling edge	T_1	C_{DO} = 100pF			200	ns
DO disable after CS rising edge	T_2	C_{DO} = 100pF			200	ns
DO falling/rising time		C_{DO} = 100pF			100	ns
DO valid time	T_{10}	C_{DO} = 100pF			200	ns
CS set-up time (high to low)	T_4		150			ns
CS set-up time (low to high)	T_8		150			ns
CS high time	T_9	Bit14 (SCT) = high	0.75			ms
		Bit14 (SCT) = low	0.3			ms
CLK high time	T_5		150			ns
CLK low time	T_6		150			ns
CLK period time			333			ns
CLK set-up time (high to low)	T_7		150			ns
CLK set-up time (low to high)	T_3		150			ns
DI set-up time	T_{11}		26			ns
DI hold time	T_{12}		26			ns

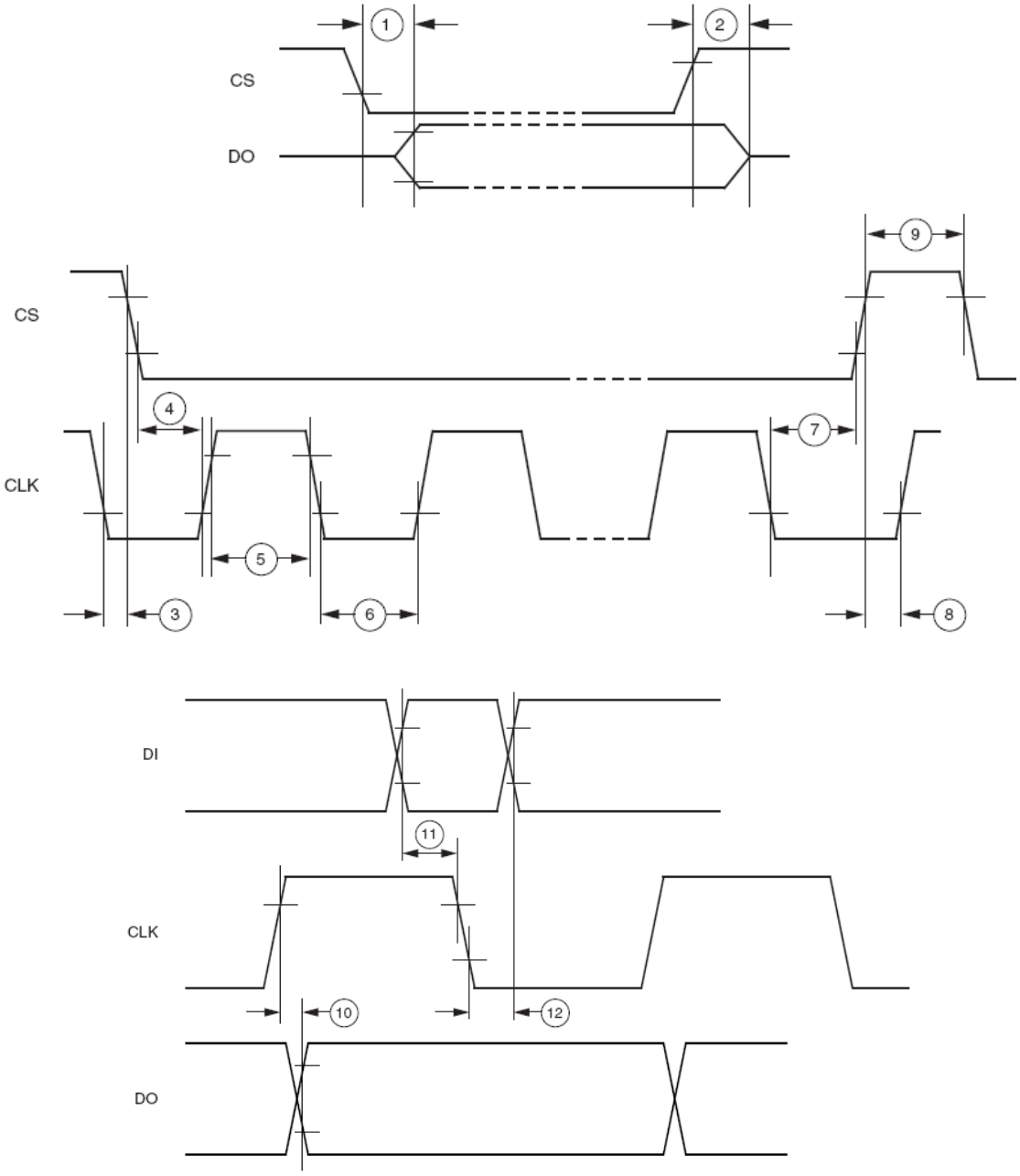
NOTES:

6) Guaranteed by characterization, not tested in production.

7) Not subject to production test, specified by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

SERIAL INTERFACE TIMING DIAGRAMS



Inputs DI, CLK, CS: High level = $0.7 \times V_{CC}$, low level = $0.2 \times V_{CC}$
Output DO: High level = $0.8 \times V_{CC}$, low level = $0.2 \times V_{CC}$

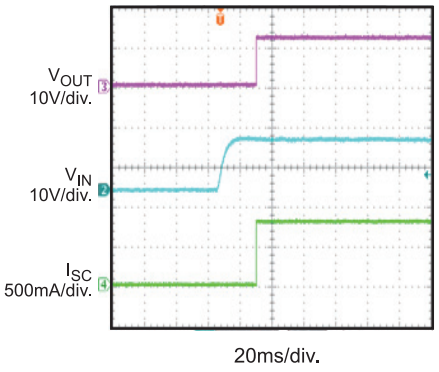
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VS} = 13V, V_{VCC} = 5V, T_A = 25°C, unless otherwise noted.

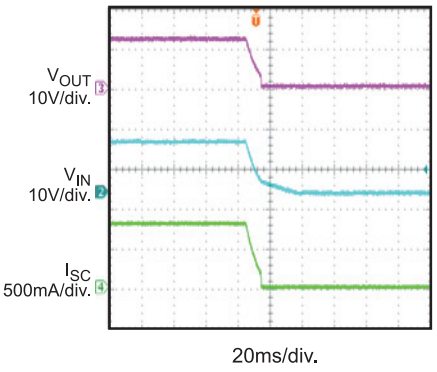
VS Power Start-Up

HS On, I_{OUT}=800mA



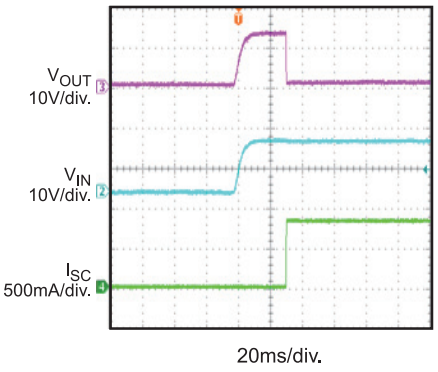
VS Power Shutdown

HS On, I_{OUT}=800mA



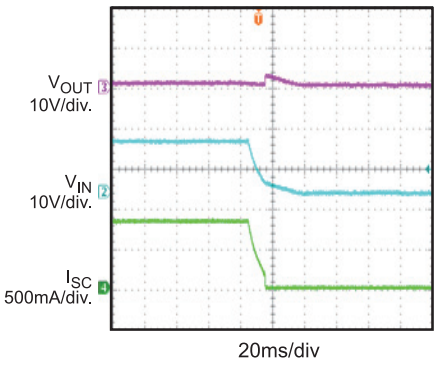
VS Power Start-Up

LS On, I_{OUT}=800mA



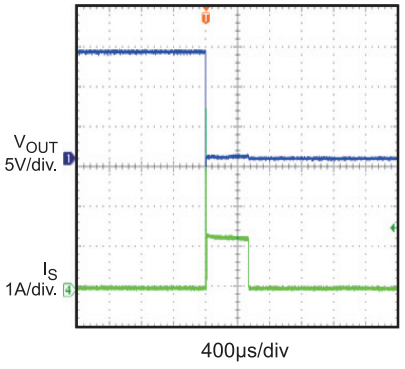
VS Power Shutdown

LS On, I_{OUT}=800mA



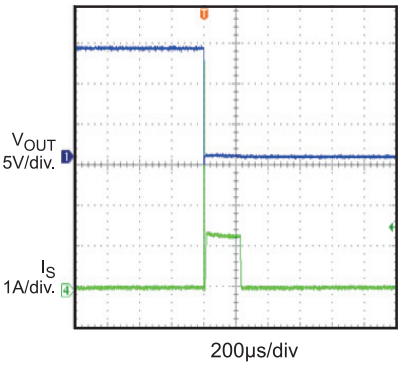
SCP

HS On, SCT=1, OUT Short to GND



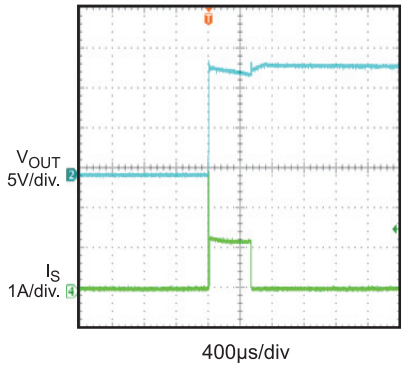
SCP

HS On, SCT=0, OUT Short to GND



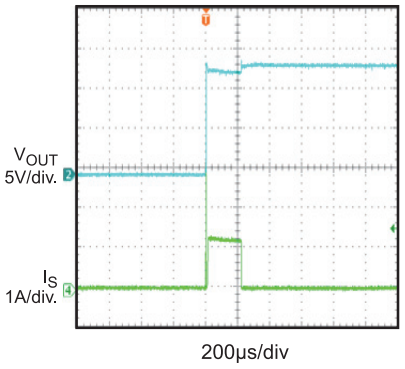
SCP

LS On, SCT=1, OUT Short to V_S



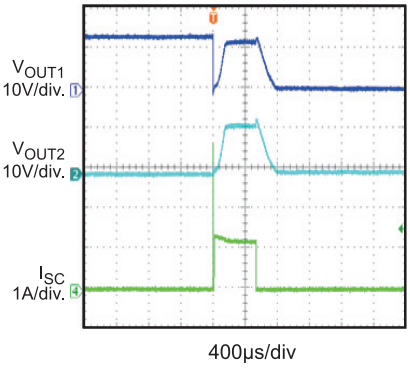
SCP

LS On, SCT=0, OUT Short to V_S



SCP

SCT=1, OUT1 short to OUT2



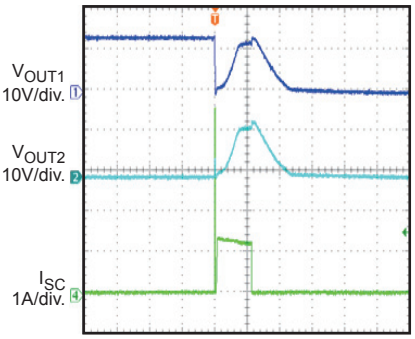
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{VS} = 13V, V_{VCC} = 5V, T_A = 25°C, unless otherwise noted.

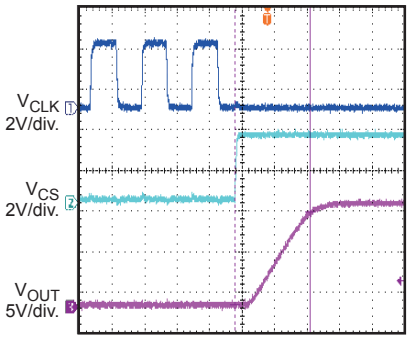
SCP

SCT=0, OUT1 short to OUT2



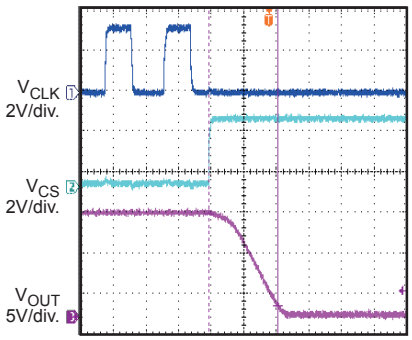
Output Delay Time

HS ON



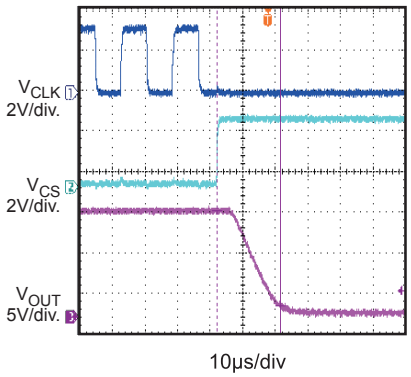
Output Delay Time

HS OFF



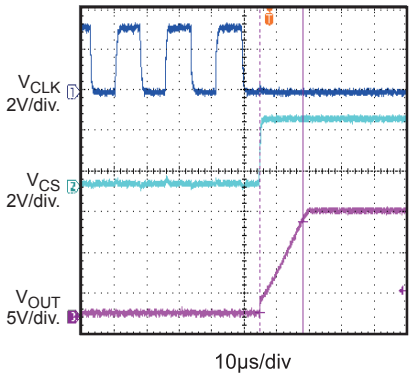
Output Delay Time

LS ON



Output Delay Time

LS OFF



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

BLOCK DIAGRAM

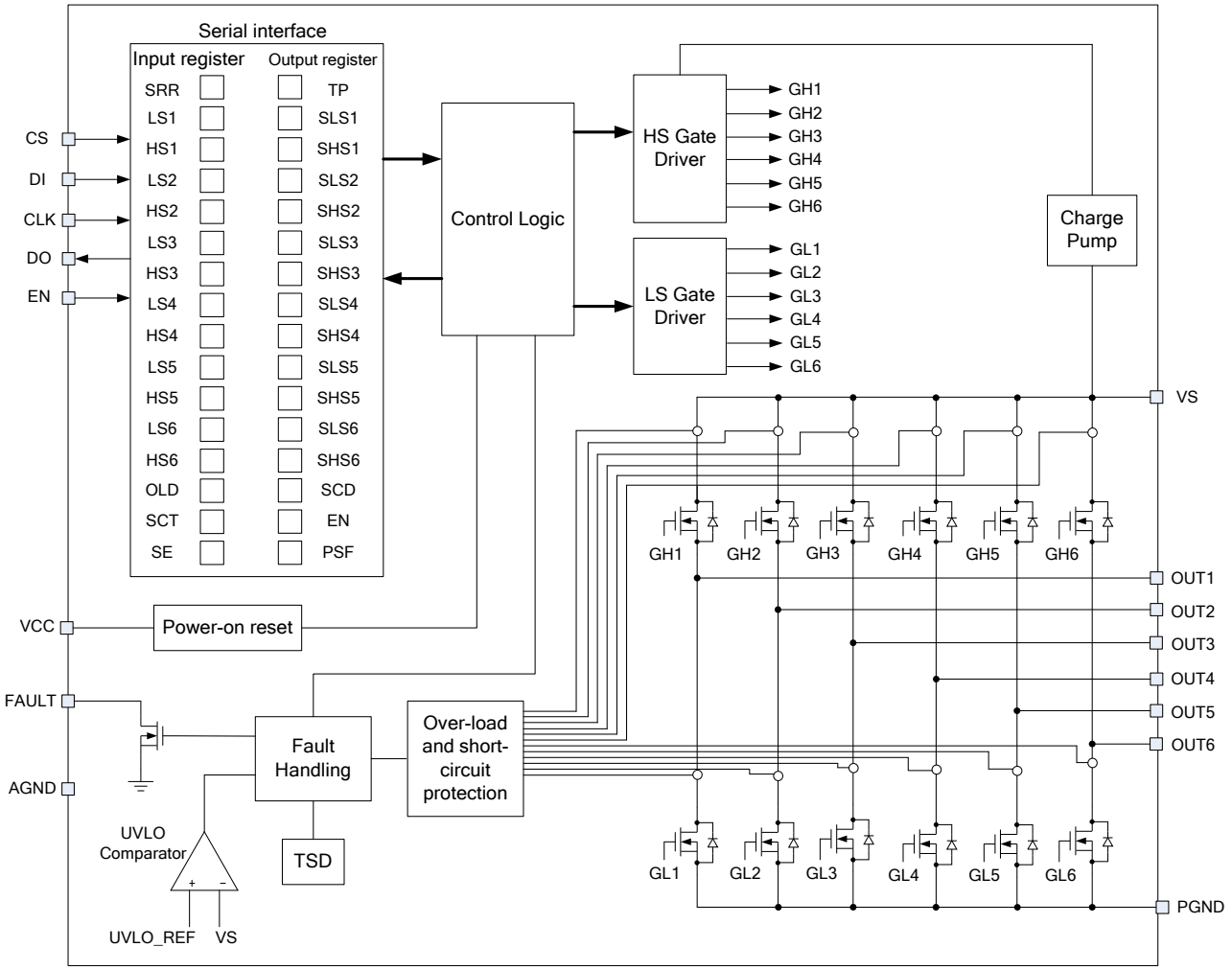


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

OPERATION

The MP6526 is a six-half-bridge motor driver that can drive up to six different loads with separate controls for high-side or low-side MOSFETs from a standard serial data interface.

Serial Interface

Data transfer starts with the falling edge of the CS signal (see Figure 2). Execution of new input data is enabled on the rising edge of the CS signal. Data must appear at DI synchronized to CLK and is accepted on the falling edge of the CLK signal. The LSB (bit0, SRR) must be transferred first.

The output data at DO is enabled on the falling edge of CS. The output data changes state with the rising edge of CLK and remains stable until the next rising edge of CLK appears. When CS is high, DO is in a tri-state condition. The LSB (bit0, TP) is transferred first.

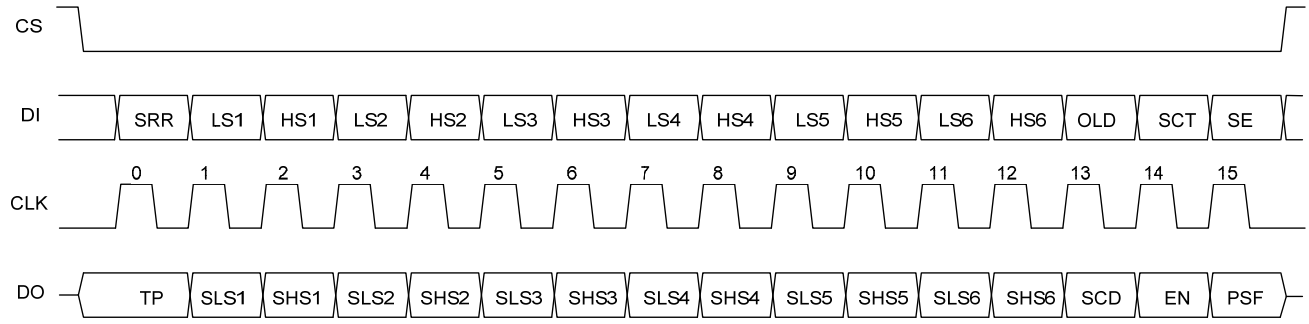


Figure 2: Data Transfer

Table 1: Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset. The bits PSF, SCD, and over-temperature shutdown in the output data register are set to low).
1	LS1	Controls output LS1 (high = switch output LS1 on).
2	HS1	Controls output HS1 (high = switch output HS1 on).
3	LS2	Controls output LS2 (high = switch output LS2 on).
4	HS2	Controls output HS2 (high = switch output HS2 on).
5	LS3	Controls output LS3 (high = switch output LS3 on).
6	HS3	Controls output HS3 (high = switch output HS3 on).
7	LS4	Controls output LS4 (high = switch output LS4 on).
8	HS4	Controls output HS4 (high = switch output HS4 on).
9	LS5	Controls output LS5 (high = switch output LS5 on).
10	HS5	Controls output HS5 (high = switch output HS5 on).
11	LS6	Controls output LS6 (high = switch output LS6 on).
12	HS6	Controls output HS6 (high = switch output HS6 on).
13	OLD	Open-load detection (low = on).
14	SCT	Programmable time delay for short circuit (shutdown delay high/low = 12ms/1.5ms).
15	SE	Software enable. Low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Table 2: Output Data Protocol

Bit	Input Register	Function
0	TP	Temperature pre-warning: high = warning (over-temperature shutdown see remark below).
1	Status LS1	Normal operation: high = output is on, low = output is off. Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off).
2	Status HS1	Normal operation: high = output is on, low = output is off. Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off).
3	Status LS2	See LS1.
4	Status HS2	See HS1.
5	Status LS3	See LS1.
6	Status HS3	See HS1.
7	Status LS4	See LS1.
8	Status HS4	See HS1.
9	Status LS5	See LS1.
10	Status HS5	See HS1.
11	Status LS6	See LS1.
12	Status HS6	See HS1.
13	SCD	Short circuit detected. Set SCD high when at least one output is switched off by a short-circuit condition.
14	EN	Enable. EN is controlled by software (bit SE in the input register) and hardware Enable (EN). Low = standby, high = normal operation.
15	PSF	Power supply fail. Under-voltage at VS detected.

NOTE: Bit0 to 15 = high: over-temperature shutdown.

Table 3: Status of the Input Register after Power-On Reset

Bit15 (SE)	Bit14 (SCT)	Bit13 (OLD)	Bit12 (HS6)	Bit11 (LS6)	Bit10 (HS5)	Bit9 (LS5)	Bit8 (HS4)	Bit7 (LS4)	Bit6 (HS3)	Bit5 (LS3)	Bit4 (HS2)	Bit3 (LS2)	Bit2 (HS1)	Bit1 (LS1)	Bit0 (SRR)
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Enable Control (EN)

There are two ways to enable or disable the MP6526:

1. Controlled by software: set bit SE in the input register. Low = standby, high = normal operation.
2. Hardware enable (EN): low = standby, high = normal operation.

In both cases, if the device is disabled, then all output stages are turned off, but the serial interface remains active. The output stages can be activated again by setting the bit SE high (when EN = high) or by switching EN back to high (when SE = high).

Open-Load Detection

When the open-load detection bit (OLD) is set to low, open-load detection is enabled. In this mode, a pull-down current for each low-side switch is turned on. When an open-load has been detected, the corresponding output bit (LSx or HSx) in the output data register is set to high. Once the open load is removed, the corresponding DO bit is cleared, indicating the end of the open-load event.

Testing the open load of the H-bridge configuration is a two-step process. First, switch off all high-side (HSx/HSy) and low-side (LSx/LSy) drivers. The voltage at both clamps in this condition is pulled down. Next, with both low-side drivers off, switch on one high-side driver (HSx or HSy). Since the DC motor has a relatively low internal resistance, the voltage of the inactive high-side output should be at the same level as the activated high-side output. In the case of an open load, the inactive high-side output register reports a 0 if the active high-side output is 1. Conversely, if the load is connected, the inactive high-side output reports a 1.

Discharge Circuit

Many typical applications use an inverse-polarity protection diode (see D1 in Figure 3). However, this method involves a certain risk. During inhibit mode, the IC consumes only an extremely low current (I_{VS}), (i.e.: 20µA max). Any peaks on the supply voltage charge the blocking capacitor gradually. D1 prevents the capacitor from discharging via the power supply. Due to the extremely small quiescent current, discharging via the IC can also be neglected. This means that during long periods in inhibit mode, the IC's supply voltage could increase continuously until the maximum supply voltage limit of 40V is exceeded, damaging the IC. The device features a discharger circuit that prevents such unwanted effects. If VS exceeds a threshold value of approximately 37V, the blocking capacitor is discharged via an integrated resistor until VS falls below the threshold again.

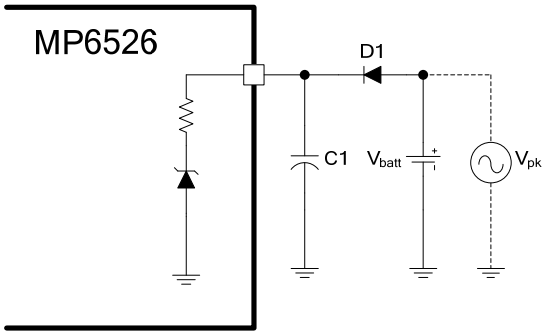


Figure 3: Functional Principle of the Discharger Circuit

Over-Current Protection (OCP)

The MP6526 has internal overload and short-circuit protection. The currents in both the high-side and low-side MOSFETs are measured. If the current exceeds the current limit, an internal timer is started. When a permanent over-current shutdown delay time programmed by the short-circuit timer bit (SCT) is reached, the short-circuit detection bit (SCD) is set, and the shorted output is disabled. By writing a high to the SRR bit in the input register, the SCD bit is reset, and the disabled outputs are enabled.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Thermal Shutdown and Pre-Warning

Thermal monitoring is also integrated into the MP6526. If the junction temperature rises above the thermal pre-warning threshold, the temperature pre-warning bit (TP) in the output register is set. When the temperature falls below the thermal pre-warning threshold, the bit TP is reset. The bit TP can be read without transferring a complete 16-bit data word. When CS = high to low, the state of TP appears at DO. After the microcontroller has read this information, CS is set high, and the data transfer is interrupted without affecting the state of the input and output registers.

If the junction temperature rises above the thermal shutdown threshold, all switches turn off, and all bits in the output register are set high. Operation resumes immediately when the junction temperature has fallen below the thermal shutdown threshold and when a high has been written to the SRR bit in the input register.

The thermal pre-warning and shutdown threshold have hysteresis.

Note that bit0 to 15 = high indicates an over-temperature shutdown.

Power-Supply Fail

If at any time the voltage on VS falls below the under-voltage lockout (UVLO) threshold voltage, an internal timer is started. The power supply fail bit (PSF) in the output register is set, and all outputs are disabled when a permanent UVLO delay time is reached.

Operation resumes immediately when VS rises above the UVLO threshold. The PSF bit remains high until it is reset by the SRR bit in the input register.

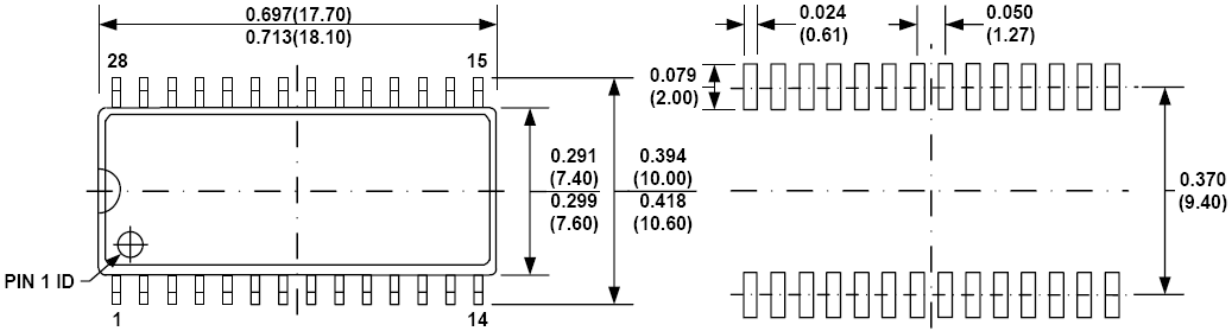
Fault Output

The MP6526 includes an open-drain, active-low, fault indicator output (FAULT). A fault is indicated if the current limit is tripped or thermal shutdown is tripped. A fault on any channel causes FAULT to be pulled low. The FAULT value is maintained until the fault condition is removed and normal operation resumes. Do not apply more than 6V to FAULT.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

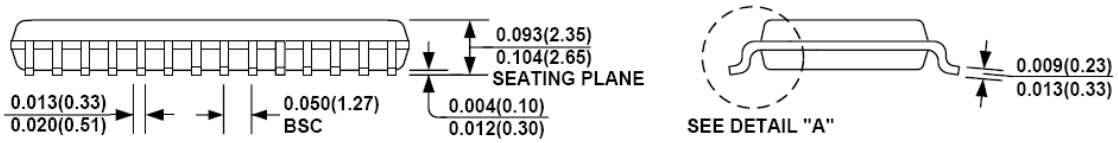
PACKAGE INFORMATION

SOIC-28



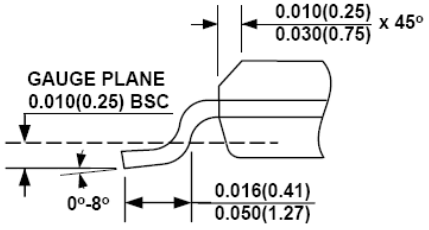
TOP VIEW

RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



DETAIL "A"

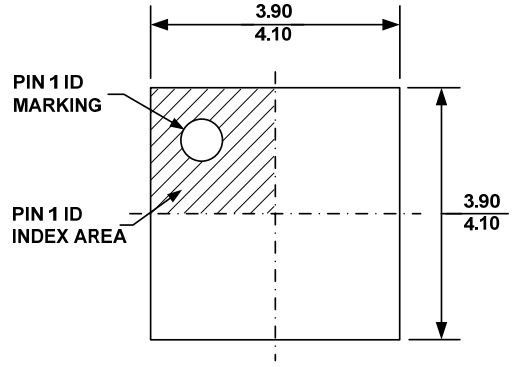
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

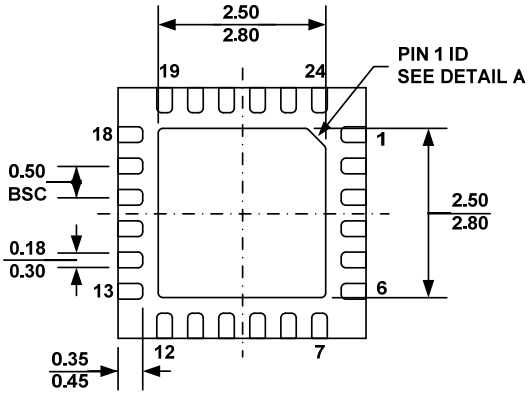
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION *(continued)*

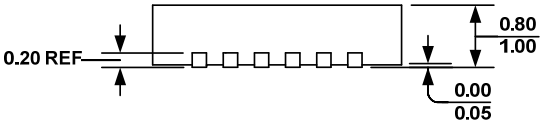
QFN-24 (4mmx4mm)



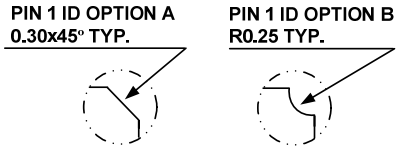
TOP VIEW



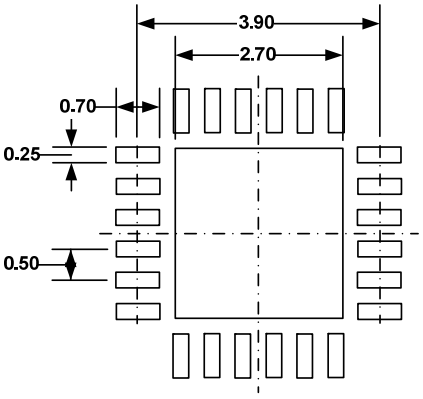
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

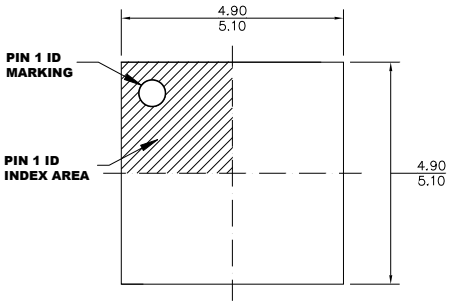
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGGD.
5) DRAWING IS NOT TO SCALE.

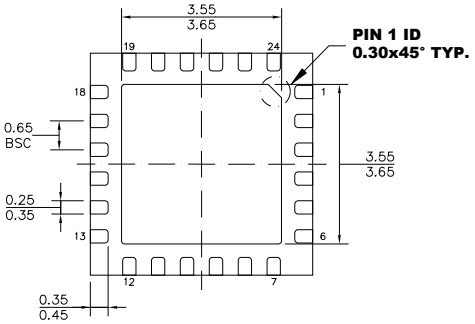
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION *(continued)*

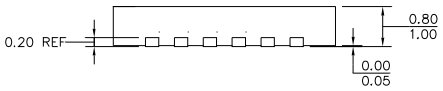
QFN-24 (5mmx5mm)



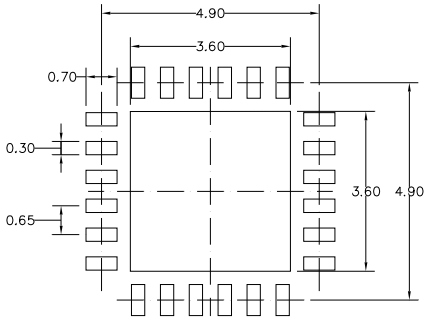
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.