Not Recommended For New Designs

12-BIT 30 MSPS DUAL CHANNEL CCD SIGNAL FRONT END FOR DIGITAL COPIER

FEATURES

- **Dual Channel CCD Signal Processing:**
  - **Correlated Double Sampler (CDS)**
  - **Sample Hold Mode**
  - **Digital Programmable Amplifier**
  - **CCD Offset Correction (OB loop)**
- **High Performance A/D:**
  - **12-Bit Resolution**
  - **INL: ±2 LSB**
  - **DNL: ±0.5 LSB**
  - **No Missing Codes**
- **High-Speed Operation**
  - **Sample Rate: 30 MHz (Minimum)**
- **78-dB Signal-To-Noise Ratio (at 0-dB Gain)**
- **Low Power Consumption:**
  - **Low Voltage: 3 V to 3.6 V**
  - **Low Power: 290 mW (Typ) at 3.3 V**
  - **Standby Mode: 20 mW (Typ)**

APPLICATIONS

- **Copiers**
- **Scanners**
- **Facsimiles**

DESCRIPTION

The VSP5000 device is a complete application specific standard product (ASSP) for charge-coupled device (CCD) line sensor applications such as copiers, scanners, and facsimiles. The VSP5000 device provides two independent channels of processing lines and performs analog front-end processing and analog-to-digital (A/D) conversion. Each channel has a correlated double sampler (CDS)/sample hold (SH) circuit, a 14-bit analog-to-digital converter (ADC), a digital programmable gain amplifier (DPGA), and an optical black (OB) correction loop. Data output is 12 bits in length and the 2-channel A/D data is multiplexed and output.

The VSP5000 is available in a 64-lead LQFP package and operates from a single 3.3-V supply.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP5000PM	NRND	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	SNBI	Level-1-260C-UNLIM	-25 to 85	VSP5000	
VSP5000PMG6	NRND	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	SNBI	Level-1-260C-UNLIM	-25 to 85	VSP5000	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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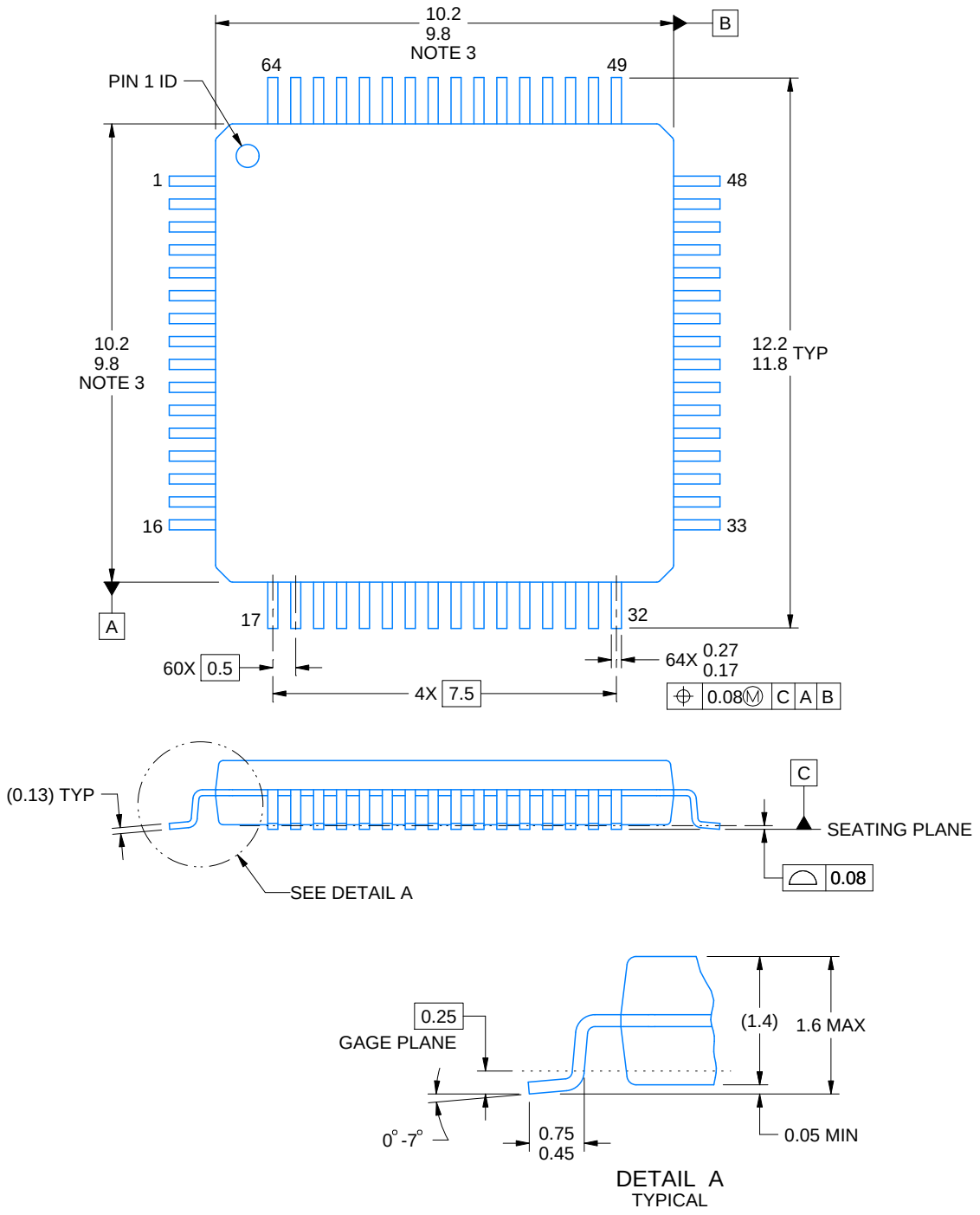
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PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

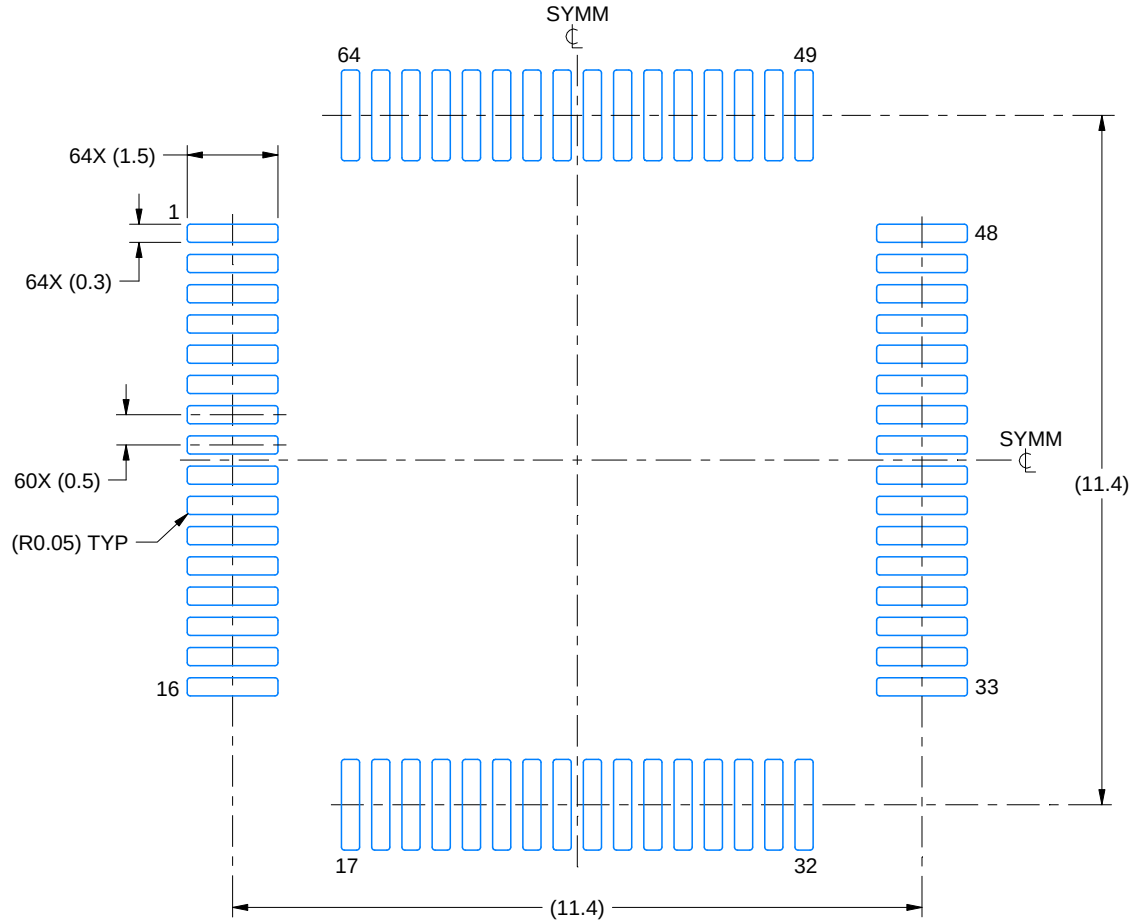
PLASTIC QUAD FLATPACK



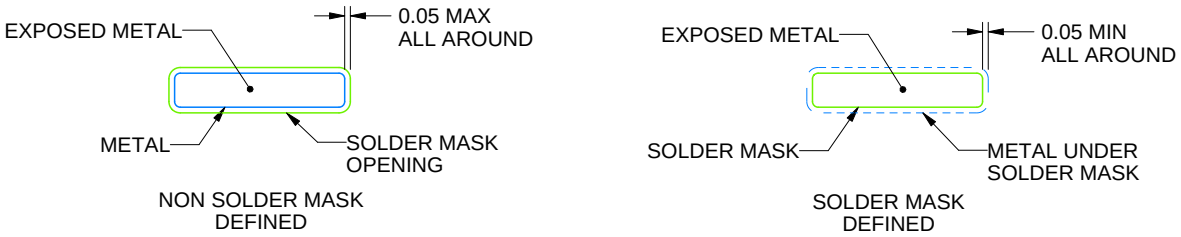
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

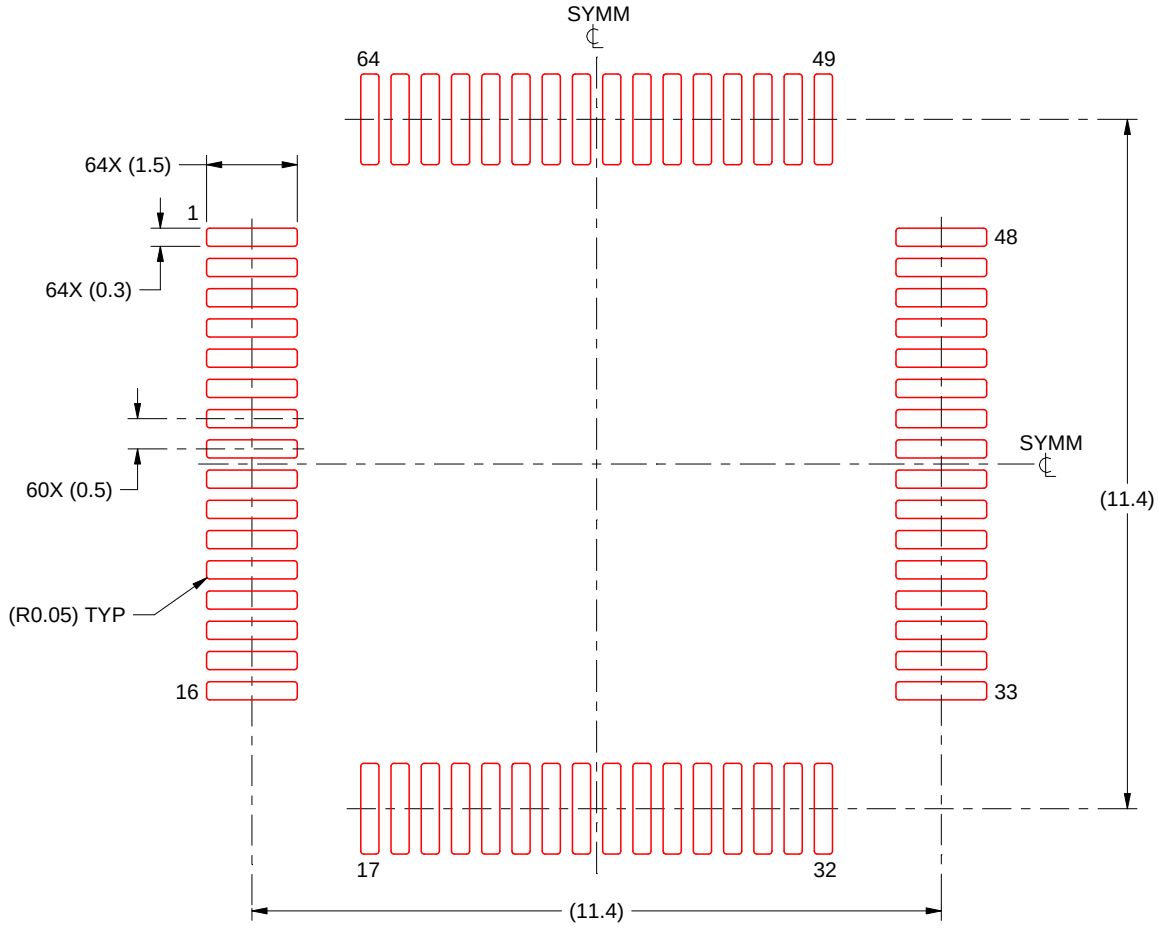


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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