Ordering number : ENA1939A

SCH1335

P-Channel Power MOSFET
−12V, −2.5A, 112mΩ, Single SCH6

ON Semiconductor®
http://onsemi.com

Features

- 1.8V drive
- Halogen free compliance

Specifications

Absolute Maximum Ratings at Ta=25°C

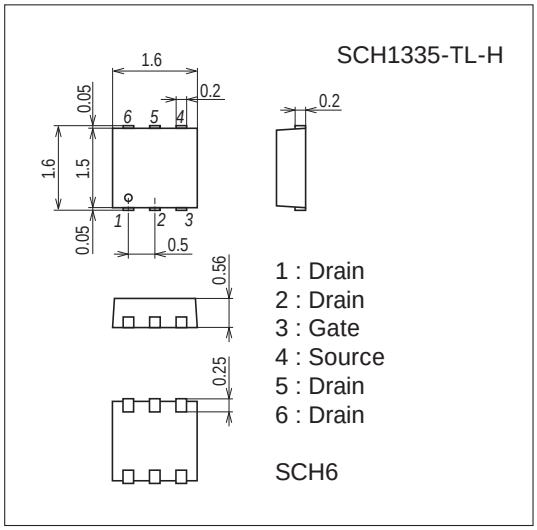
Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		−12	V
Gate-to-Source Voltage	V_{GSS}		±10	V
Drain Current (DC)	I_D		−2.5	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	−10	A
Allowable Power Dissipation	P_D	When mounted on ceramic substrate (900mm²×0.8mm)	0.8	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

This product is designed to "ESD immunity < 200V*", so please take care when handling.
* Machine Model

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

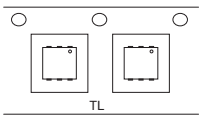
unit : mm (typ)
7028-002



Product & Package Information

- Package : SCH6
- JEITA, JEDEC : SOT-563
- Minimum Packing Quantity : 5,000 pcs./reel

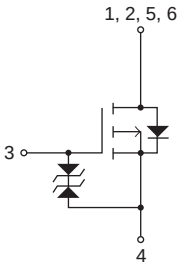
Packing Type : TL



Marking



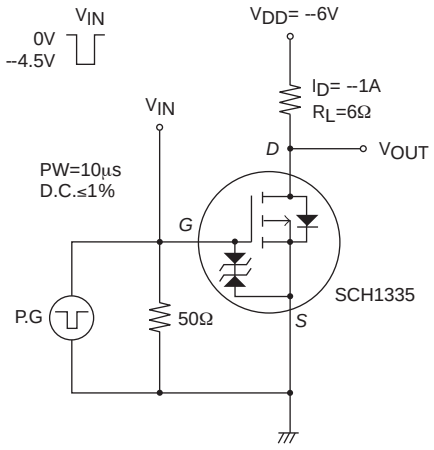
Electrical Connection



Electrical Characteristics at Ta=25°C

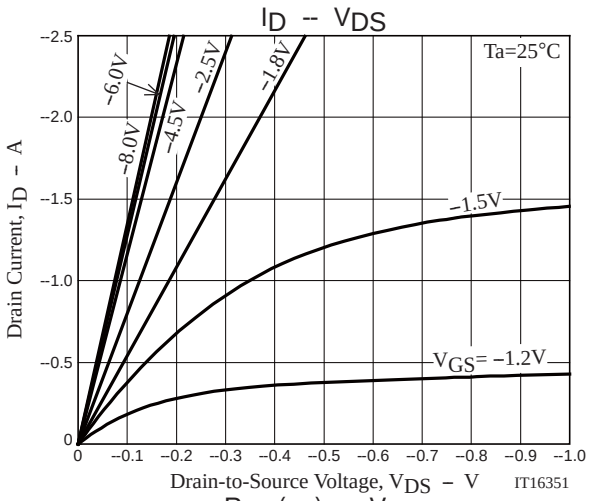
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−12			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−12V, V_{GS}=0V			−10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±8V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−6V, I_D=−1mA	−0.4		−1.3	V
Forward Transfer Admittance	| yfs |	V_{DS}=−6V, I_D=−1A		3.3		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−1A, V_{GS}=−4.5V		86	112	mΩ
	R_{DS}(on)2	I_D=−0.5A, V_{GS}=−2.5V		125	175	mΩ
	R_{DS}(on)3	I_D=−0.2A, V_{GS}=−1.8V		185	285	mΩ
Input Capacitance	Ciss	V_{DS}=−6V, f=1MHz		270		pF
Output Capacitance	Coss			90		pF
Reverse Transfer Capacitance	Crss			72		pF
Turn-ON Delay Time	t_{d}(on)	See specified Test Circuit.		6.5		ns
Rise Time	t_r			21		ns
Turn-OFF Delay Time	t_{d}(off)			33		ns
Fall Time	t_f			33		ns
Total Gate Charge	Qg	V_{DS}=−6V, V_{GS}=−4.5V, I_D=−2.5A		3.1		nC
Gate-to-Source Charge	Qgs			0.7		nC
Gate-to-Drain “Miller” Charge	Qgd			0.9		nC
Diode Forward Voltage	V_{SD}	I_S=−2.5A, V_{GS}=0V		−0.84	−1.2	V

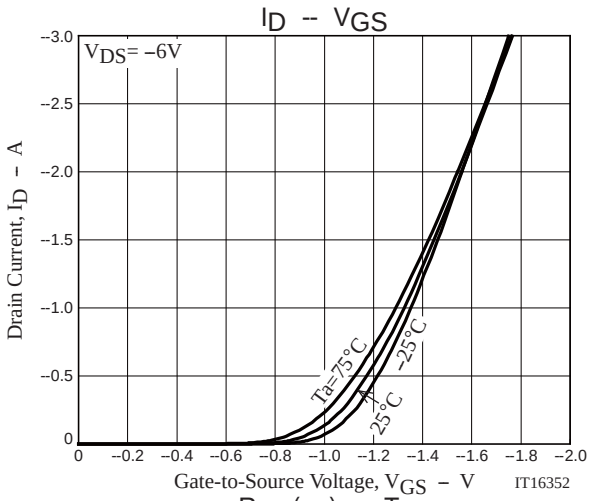
Switching Time Test Circuit

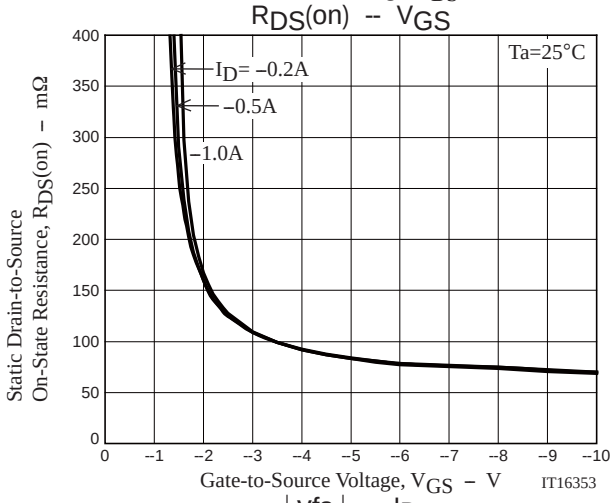


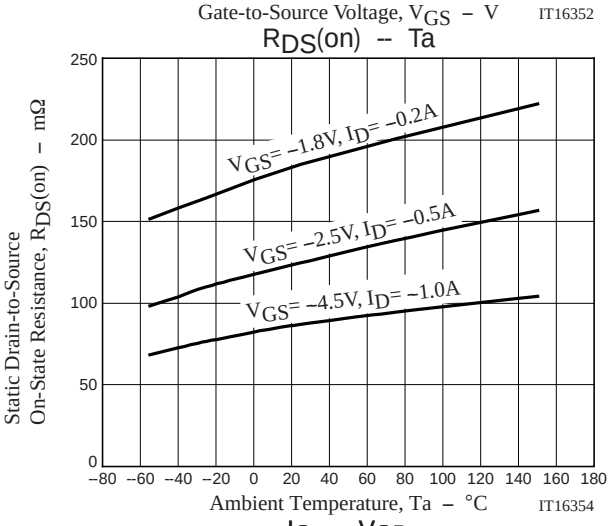
Ordering Information

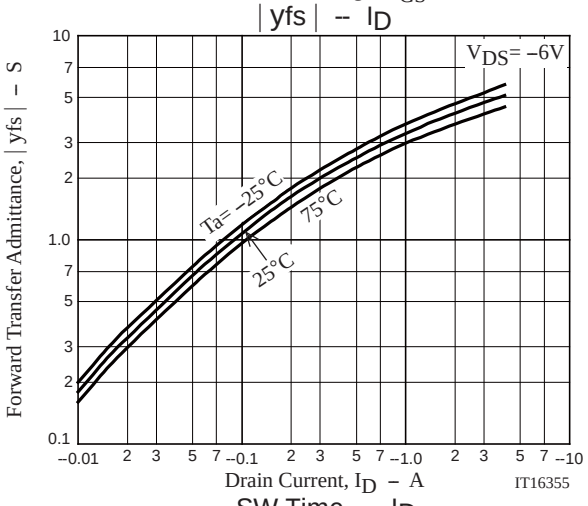
Device	Package	Shipping	memo
SCH1335-TL-H	SCH6	5,000pcs./reel	Pb Free and Halogen Free

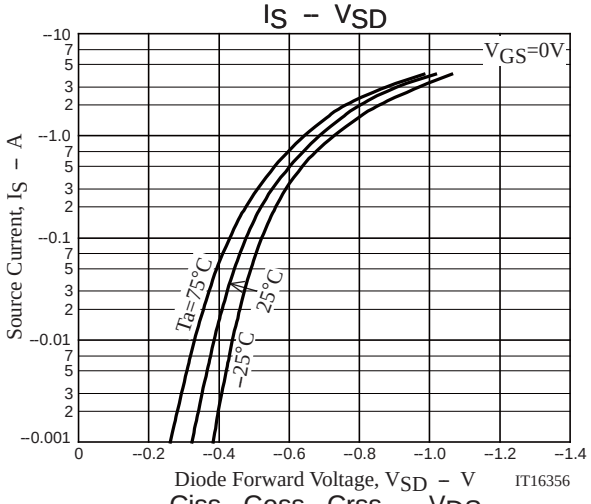

ID -- VDS
Ta=25°C
–6.0V
–8.0V
–4.5V
–2.5V
–1.8V
–1.5V
VGS= –1.2V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT16351

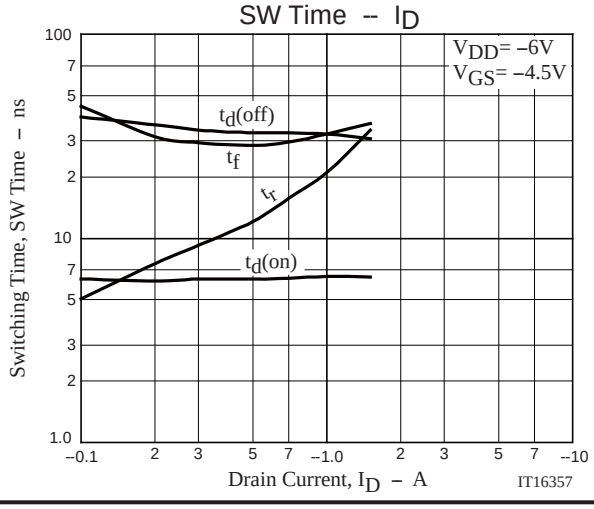

ID -- VGS
VDS= –6V
Ta=75°C
25°C
–25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT16352

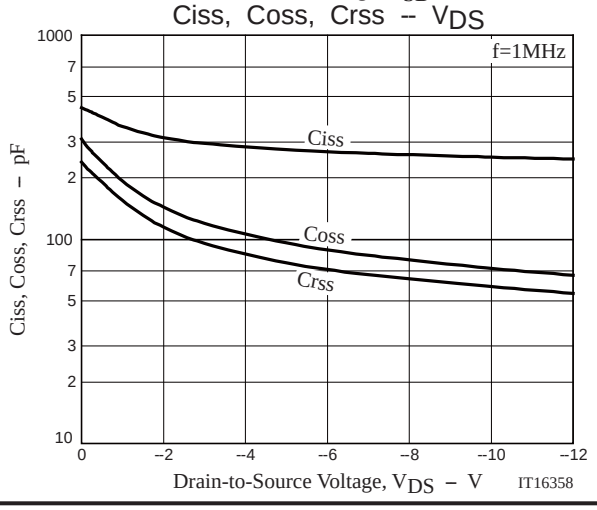

RDS(on) -- VGS
Ta=25°C
ID= –0.2A
–0.5A
–1.0A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT16353

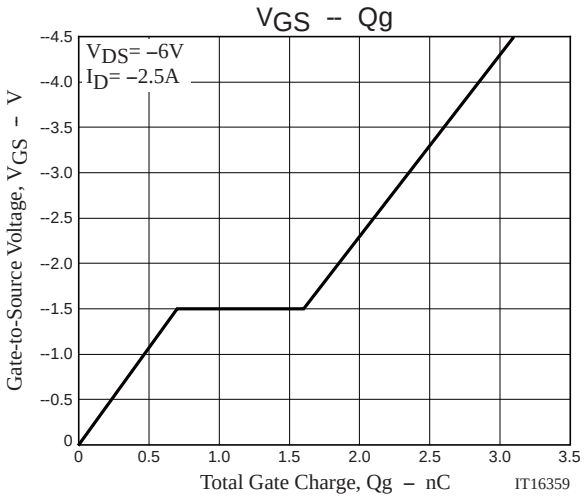

RDS(on) -- Ta
VGS= –1.8V, ID= –0.2A
VGS= –2.5V, ID= –0.5A
VGS= –4.5V, ID= –1.0A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT16354

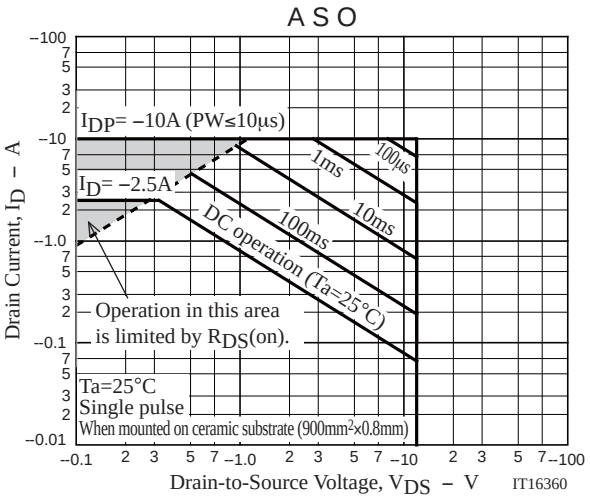

| yfs | -- ID
VDS= –6V
Ta= –25°C
25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT16355

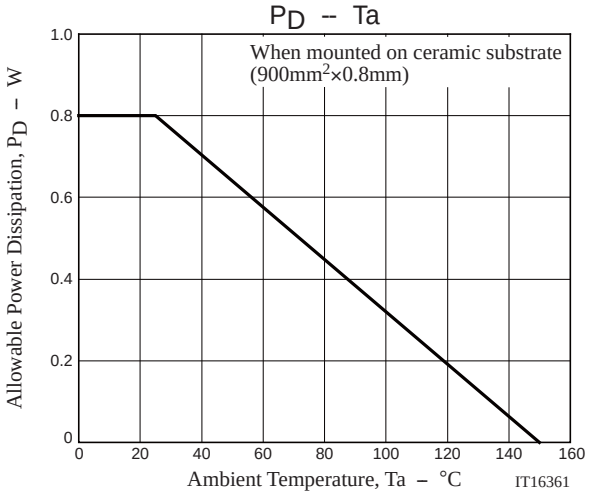

IS – VSD
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT16356


SW Time -- ID
VDD= –6V
VGS= –4.5V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT16357


Ciss, Coss, Crss -- VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT16358


VGS – Qg
VDS= –6V
ID= –2.5A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT16359


A S O
IDP= –10A (PW≤10μs)
ID= –2.5A
100μs
1ms
10ms
100ms
DC operation (Ta=25°C)
Operation in this area
is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate (900mm2×0.8mm)
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT16360


PD – Ta
When mounted on ceramic substrate
(900mm2×0.8mm)
Allowable Power Dissipation, PD – W
Ambient Temperature, Ta – °C
IT16361

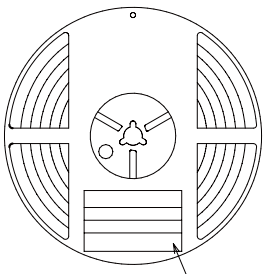
Taping Specification

SCH1335-TL-H

1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
SCH6	SCH6	5,000	25,000	150,000	5 reels contained Dimensions:mm(external) 183×72×185	6 inner boxes contained Dimensions:mm(external) 440×195×210

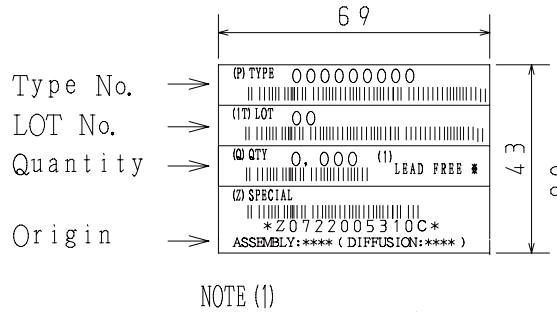
Packing method



Reel label

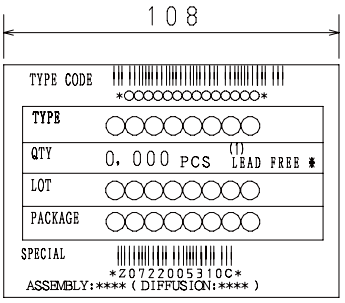
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.

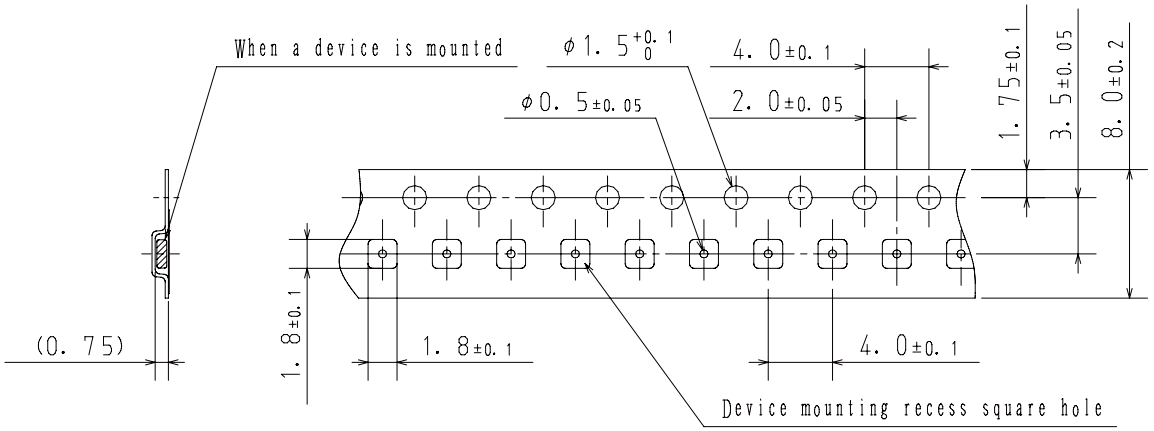


NOTE (1)
The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

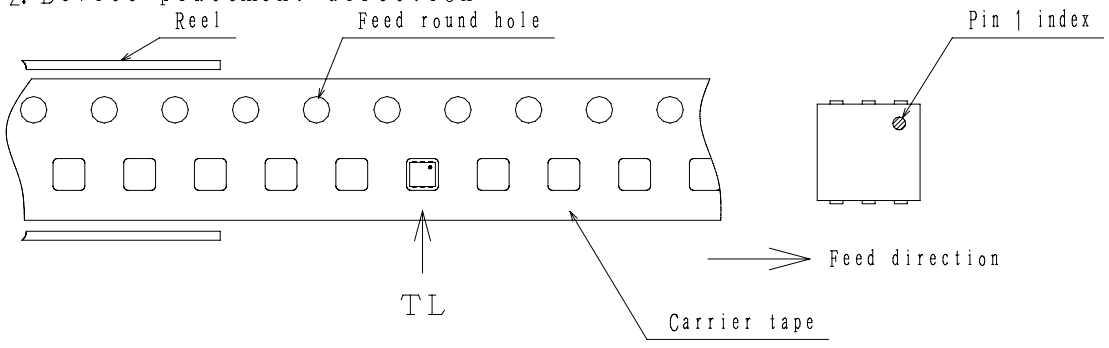
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



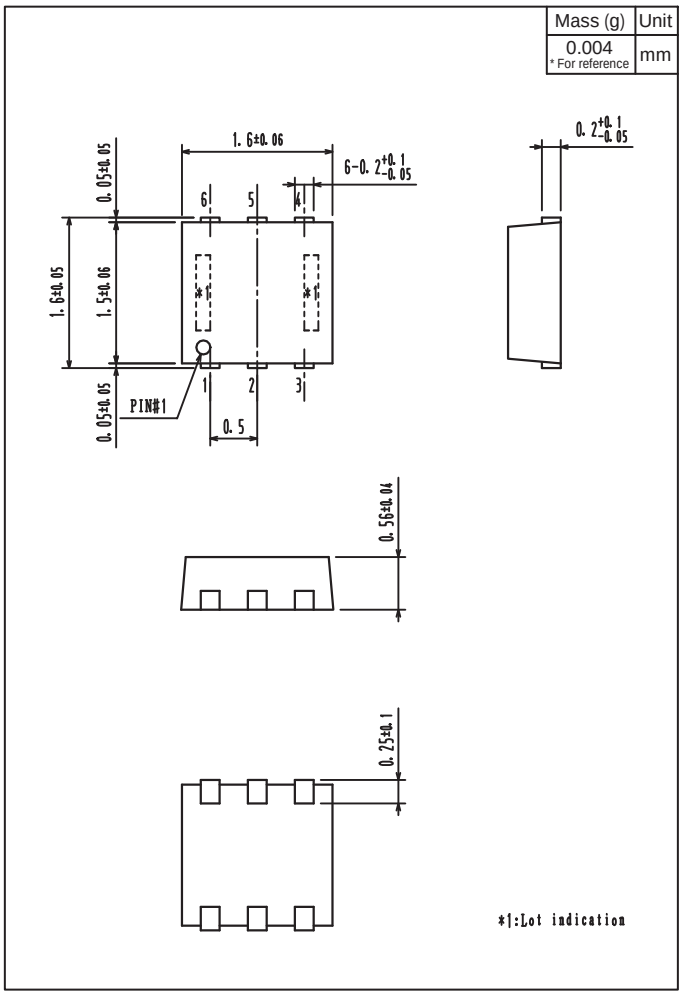
2-2. Device placement direction



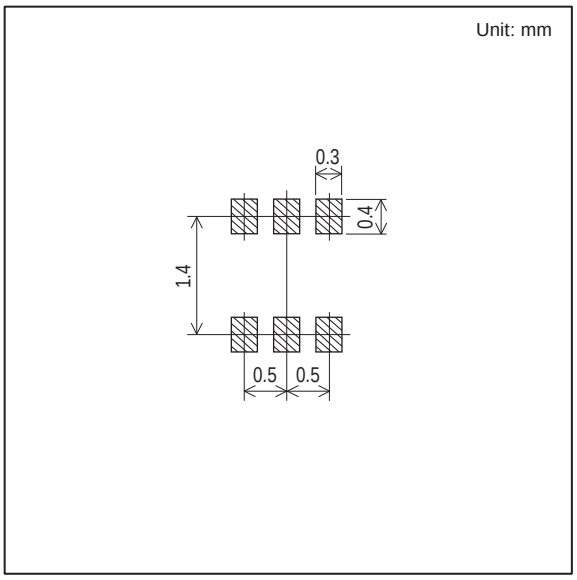
Those with pin 1 index on the feed hole side·····TL

Outline Drawing

SCH1335-TL-H



Land Pattern Example



Note on usage : Since the SCH1335 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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