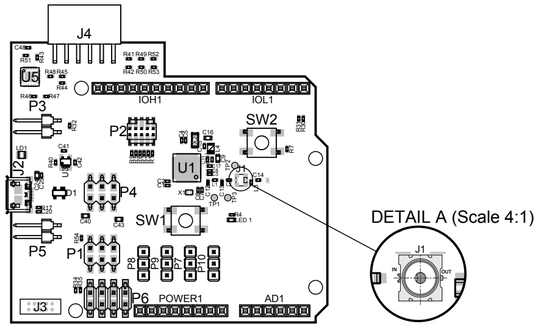
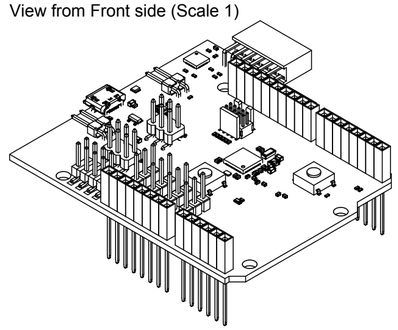
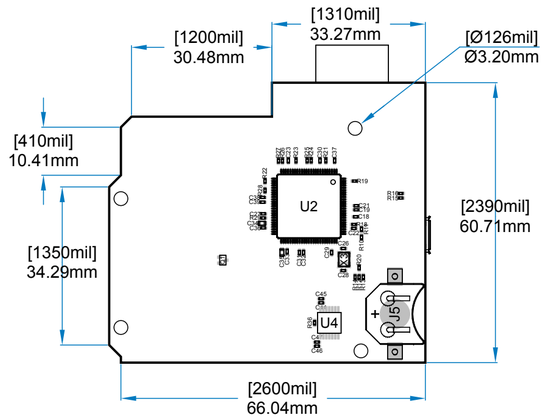
View from Top side (Scale 1:1)



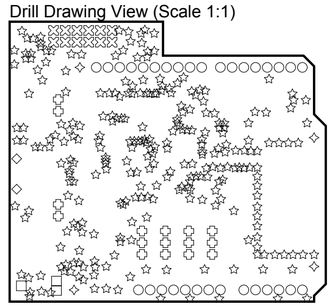
View from Front side (Scale 1)



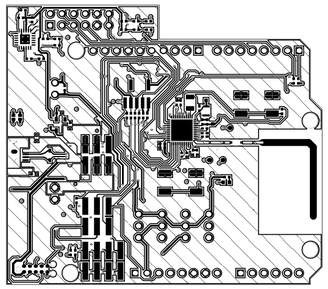
View from Bottom side (Scale 1:1)



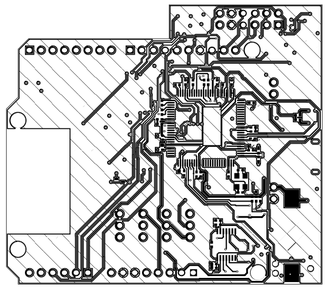
Drill Drawing View (Scale 1:1)



Top Layer (Scale 1:1)



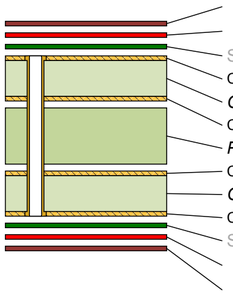
Bottom Layer (Scale 1:1)



Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair
☆	271	8.00mil	Plated	Round	Top Layer - Bottom Layer
◇	2	19.69mil	Plated	Slot	Top Layer - Bottom Layer
□	3	39.00mil	Non-Plated	Round	Top Layer - Bottom Layer
○	32	40.00mil	Plated	Round	Top Layer - Bottom Layer
⊠	12	40.16mil	Plated	Round	Top Layer - Bottom Layer
⌬	16	43.31mil	Plated	Round	Top Layer - Bottom Layer
✧	4	125.98mil	Non-Plated	Round	Top Layer - Bottom Layer
	340 Total				

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Paste			Paste Mask	GTP
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.50mil	Solder Resist	Solder Mask	GTS
Copper	Top Layer	2.00mil		Signal	GTL
Core		*15.30mil*	*FR-4-370HR*	*Dielectric*	
Copper	Signal Layer 1	0.60mil		Signal	G1
Prepreg		*24.00mil*	*FR4-370HR*	*Dielectric*	
Copper	Signal Layer 2	0.60mil		Signal	G2
Core		*15.30mil*	*FR-4-370HR*	*Dielectric*	
Copper	Bottom Layer	2.00mil		Signal	GBL
Surface Material	Bottom Solder	0.50mil	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
	Bottom Paste			Paste Mask	GBP

Total thickness: 60.80mil

Notes:

1. Fabricate to IPC6012 Class2.
2. Board material, Isola 370HR RoHS Compliant with nominal thickness of 0.062 INCH, 1/2 OZ copper on top and bottom layers, 1/2 OZ copper on inner layers.
3. Order of layers is Top_Layer, Signal_Layer1, Signal_Layer2, Bottom_Layer.
4. All dimensions +/- 5 MIL, unless otherwise specified.
5. LDI mask both sides, mask must be between lands. Minimum of 1.5 MIL per side around lands.
6. Silkscreen to be white ink, soldermask green. No ink to be on surface mount land pads. Vendor marking on bottom side.
7. Board to use ENIG (Electroless Nickel Immersion Gold) finish.
8. Board to be 100% tested to Gerber net list file.
9. Include a minimum of two fiducias per panel.
10. Controlled impedance board: Top_Layer -microstrip,Signal_Layer1-gnd.RF1 microstrip (25mil) traces on top layer shall be 50 ohms +/-10%.
11. USB Diff pair controlled impedance to be 90 ohm +/-10%, DHSD_N and DHSD_P traces.
12. Minimum copper hole wall plating 1 MIL.
13. Maximum warp/twist 0.005 INCH per INCH.
14. Finish all conductors +0.000/-0.002 from supplied artwork.

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL±
ANGULAR: MACH± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
INTERPRET GEOMETRIC TOLERANCING PER:
MATERIAL
FINISH
DO NOT SCALE DRAWING

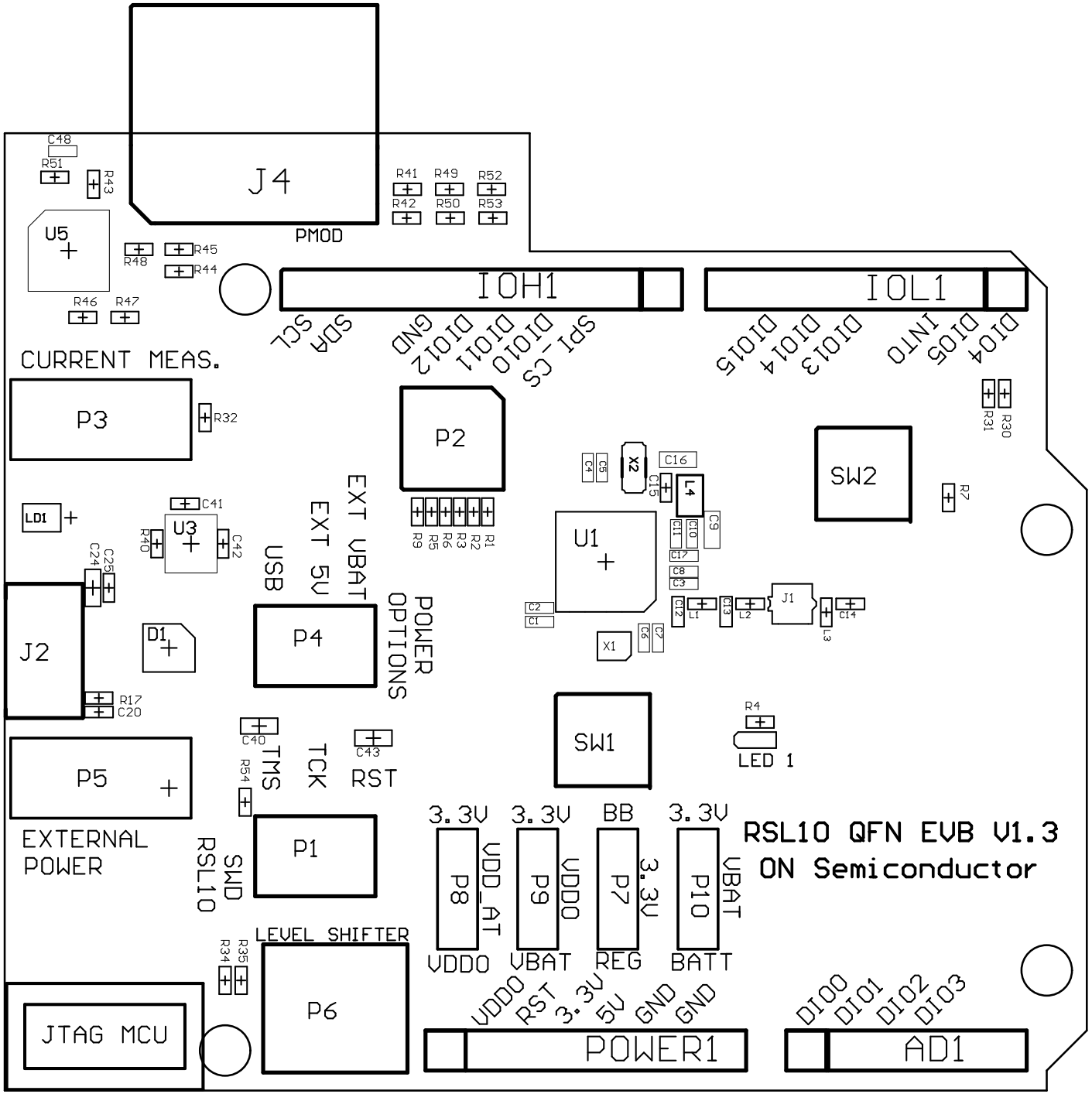
	NAME	DATE
DRAWN	M.C.	6/22/2017
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		

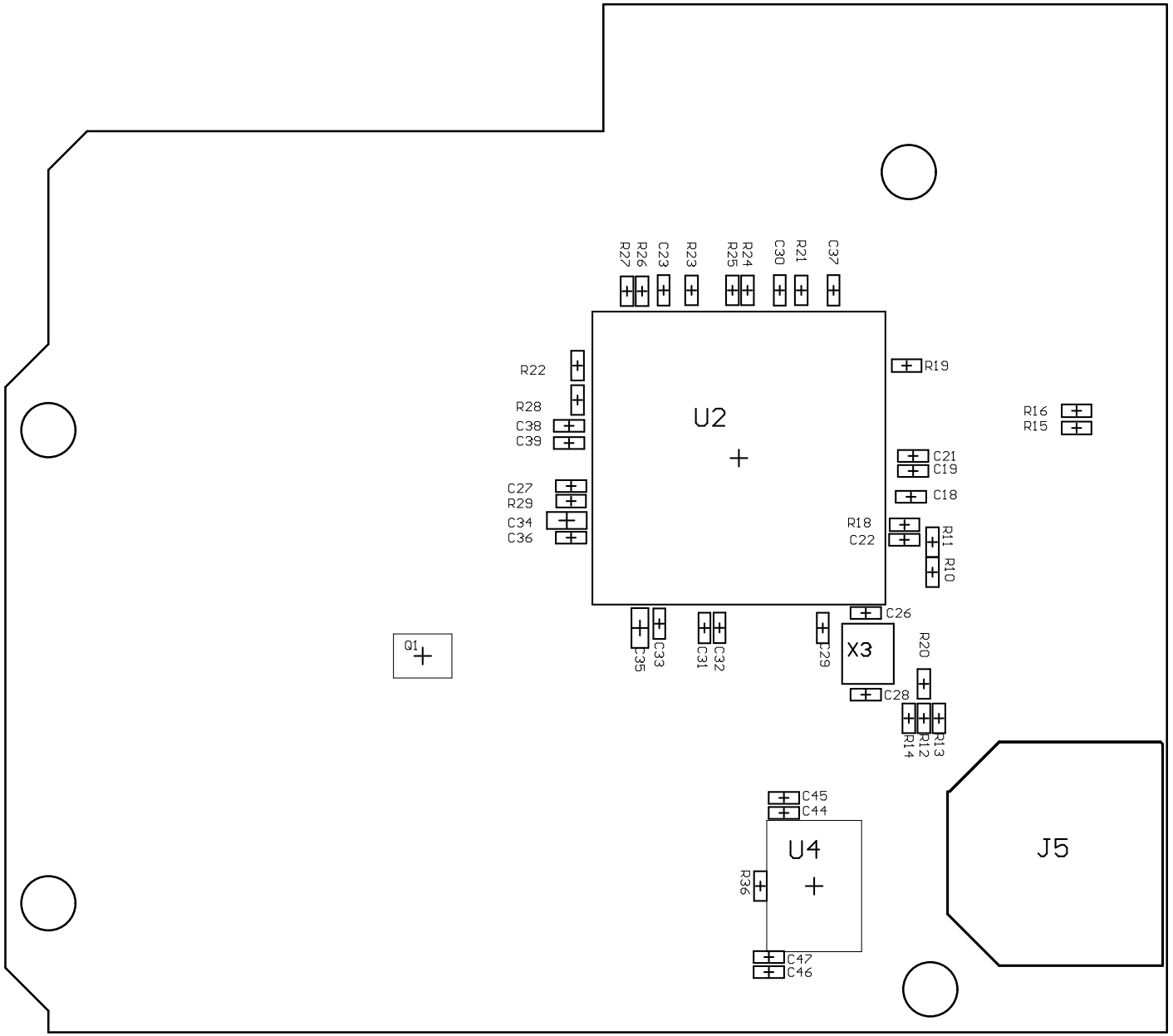
COMMENTS:

ON SEMICONDUCTOR

TITLE: RSL10 QFN EVB V1.3

SIZE | DWG. NO. | SCALE: 1:1 | WEIGHT: | SHEET 1 OF 1


J4
PMOD
IOH1
IOL1
SCL
SDA
GND
DIO2
DIO1
DIO0
SPI_CS
DIO5
DIO4
DIO3
INT0
CURRENT MEAS.
P3
P2
SW2
U1
U3
U5
LD1
D1
J2
P4
P5
P1
P6
SW1
J1
X1
X2
L4
POWER OPTIONS
EXT VBAT
EXT 5V
USB
TMS
TCK
RST
SWD RSL10
EXTERNAL POWER
LEVEL SHIFTER
LED 1
P8
P9
P7
P10
VDD_AT
VDDO
3.3V
VBAT
3.3V
3.3V
BB
3.3V
VDDO
VBAT
REG
BATT
RSL10 QFN EVB V1.3
ON Semiconductor
JTAG MCU
POWER1
AD1
VDDO
RST
3.3V
5V
GND
GND
DIO0
DIO1
DIO2
DIO3


R27
R26
C23
R23
R25
R24
C30
R21
C37
R22
R19
U2
R16
R15
R28
C38
C39
C21
C19
C27
R29
C34
C36
C18
R18
C22
R11
R10
C26
C33
C35
C31
C32
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Q1
C28
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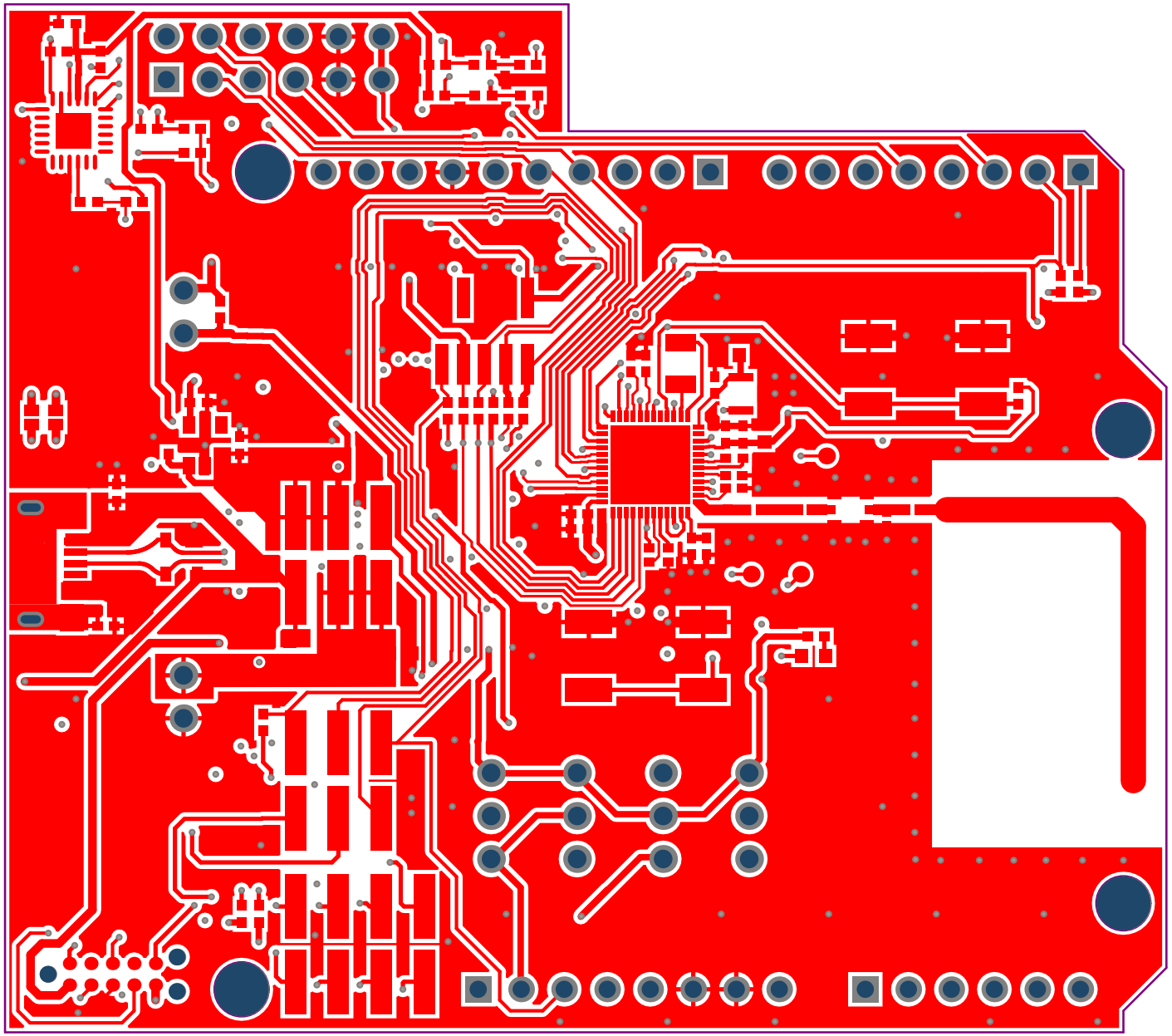
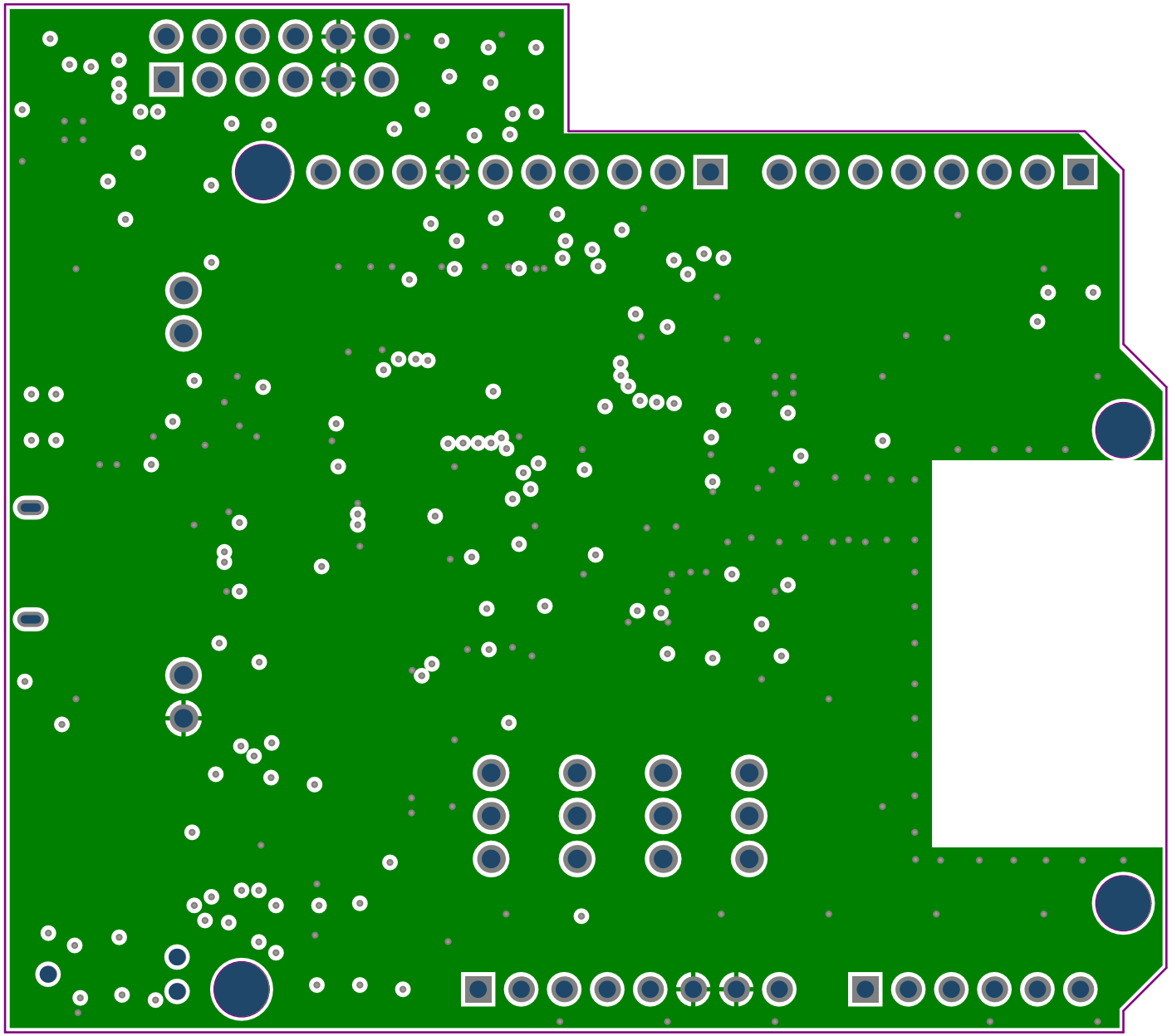
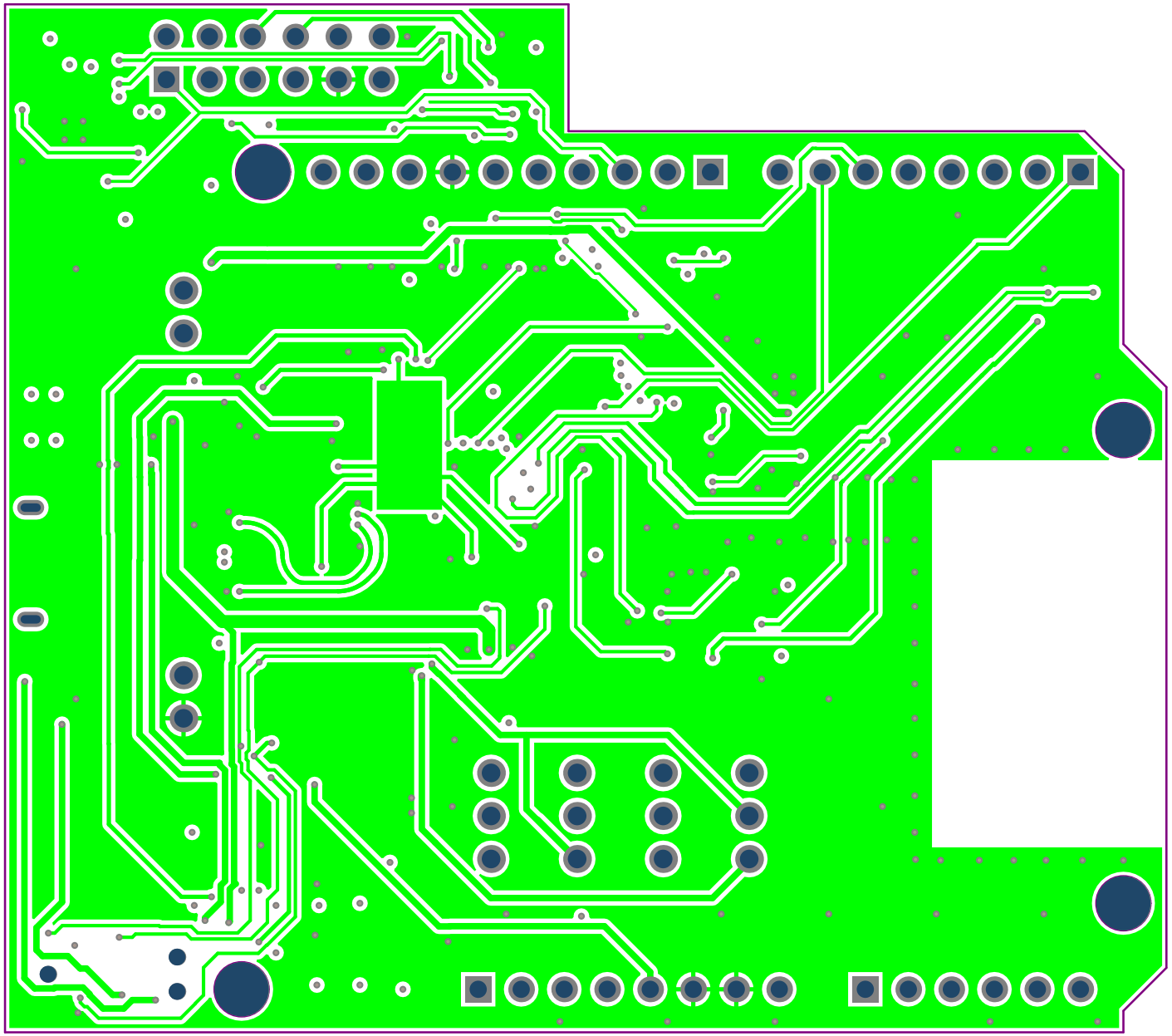
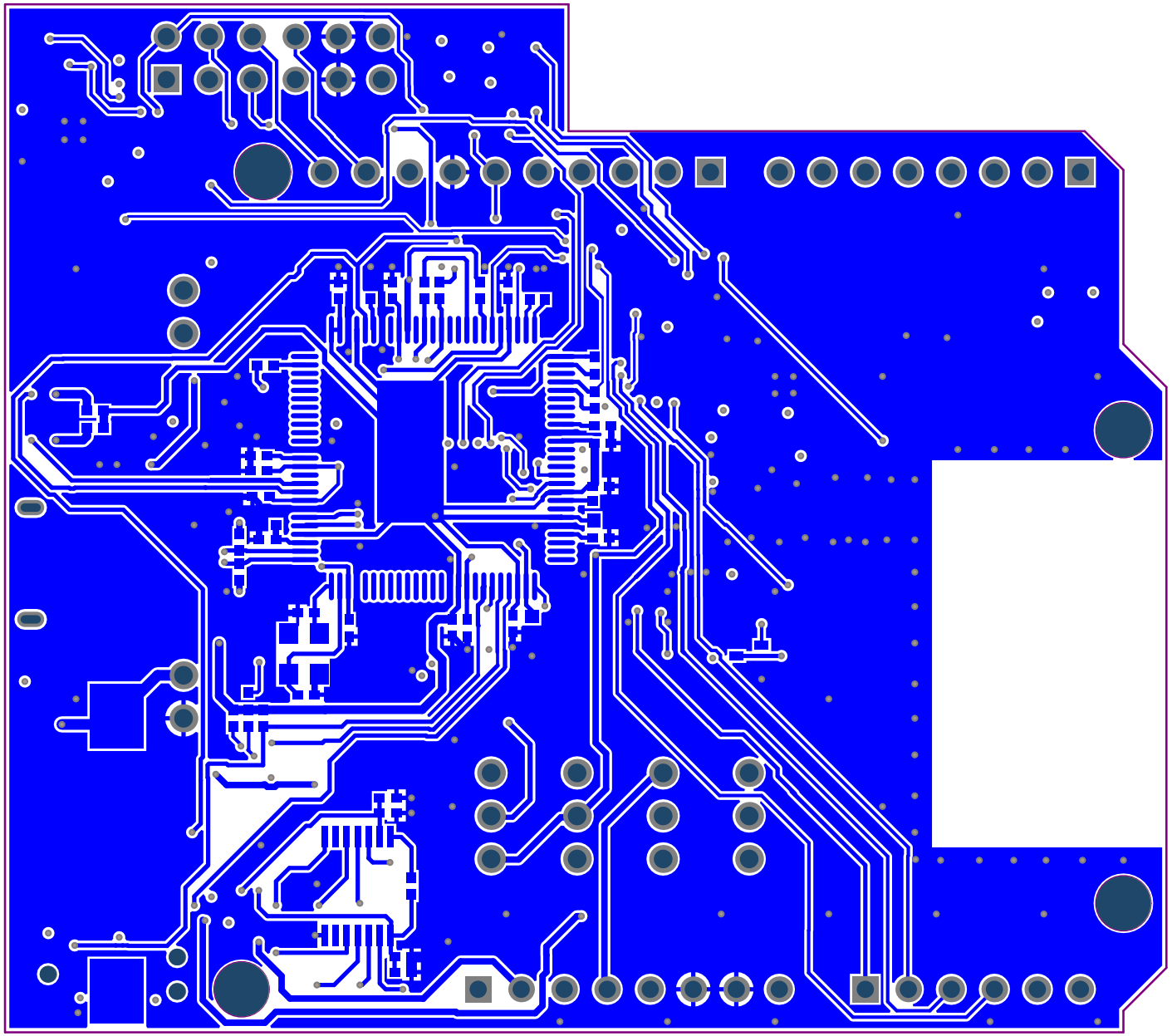
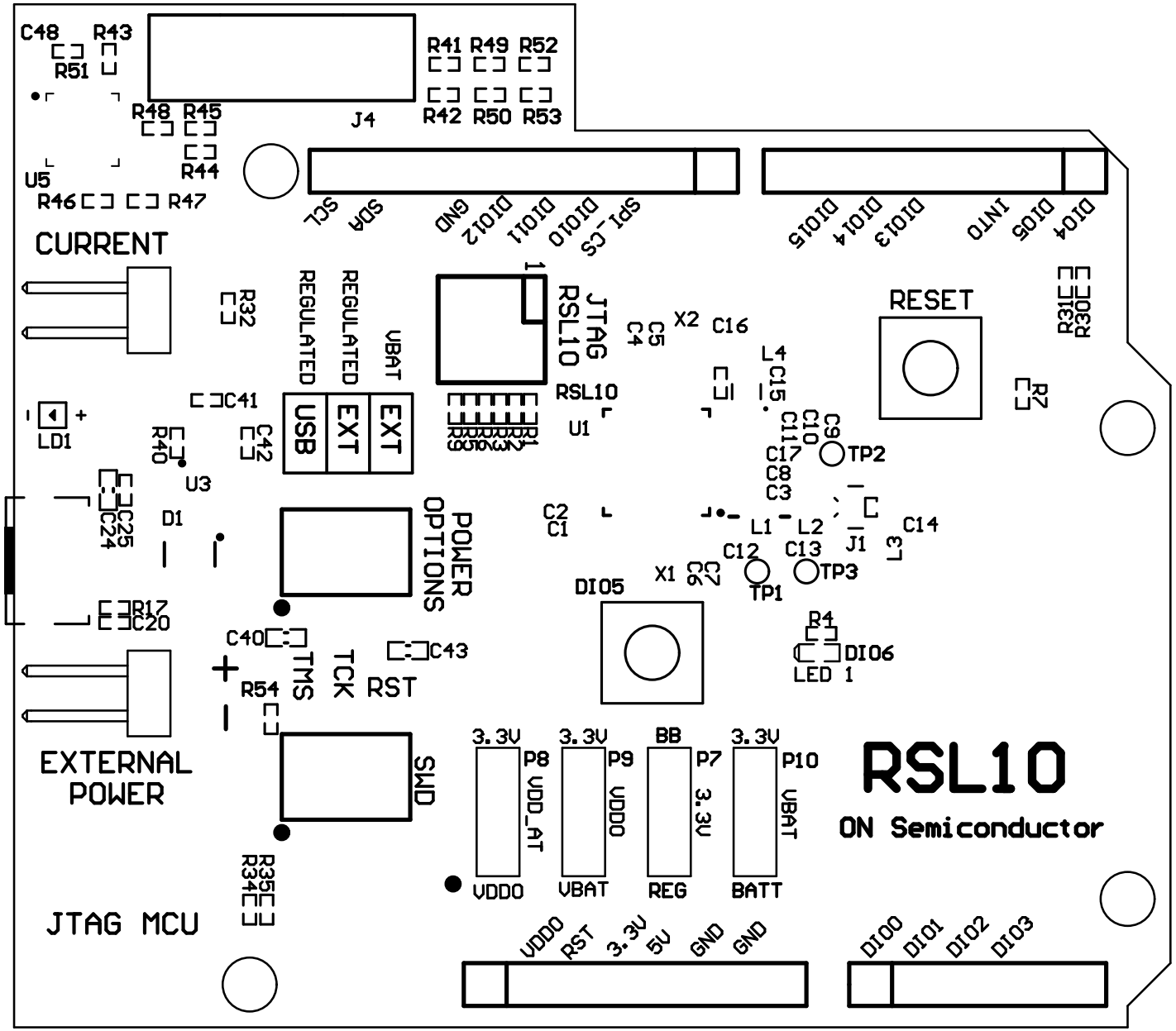
R13
C45
C44
U4
J5
R36
C47
C46










RSL10
ON Semiconductor
CURRENT
EXTERNAL POWER
JTAG MCU
RESET
POWER OPTIONS
JTAG
SWD
J4
U5
U1
U3
LD1
D1
X1
X2
TP1
TP2
TP3
J1
LED 1
USB
EXT
EXT
REGULATED
REGULATED
VBAT
RSL10
TMS
TCK
RST
DIO5
DIO6
SCL
SDA
GND
DIO12
DIO11
DIO10
SPI_CS
DIO15
DIO14
DIO13
INT0
DIO5
DIO4
P8
P9
P7
P10
VDD_AT
VDDO
3.3V
BB
VBAT
VDDO
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REG
BATT
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GND
GND
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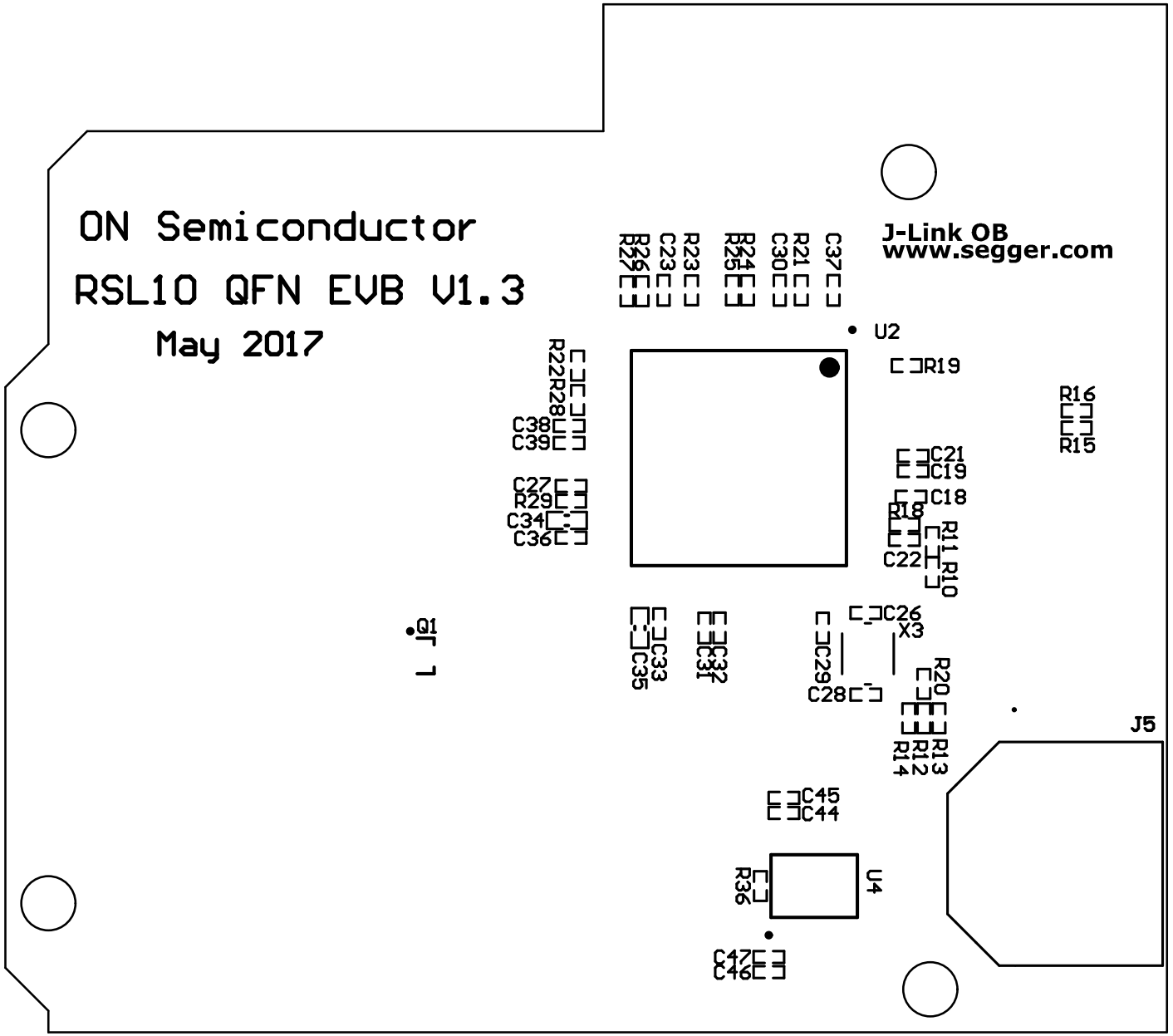
DIO1
DIO2
DIO3


ON Semiconductor
RSL10 QFN EVB V1.3
May 2017
J-Link OB
www.segger.com
U2
R19
R16
R15
C21
C19
C18
R18
R11
R10
C22
C26
X3
C29
C28
R20
R13
R12
R14
J5
C45
C44
U4
R36
C47
C46
Q1
C33
C35
C32
C31
C27
R29
C34
C36
C38
C39
R22
R28
R23
C23
R24
R25
C30
R21
C37
R26
R27