



CSD75207W15 Dual P-Channel NexFET™ Power MOSFET

1 Features

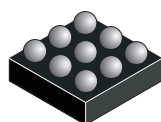
- Dual P-Channel MOSFETs
- Common Source Configuration
- Small Footprint 1.5-mm × 1.5-mm
- Gate-Source Voltage Clamp
- Gate ESD Protection >4 kV
 - HBM JEDEC standard JESD22-A114
- Pb and Halogen Free
- RoHS Compliant

2 Applications

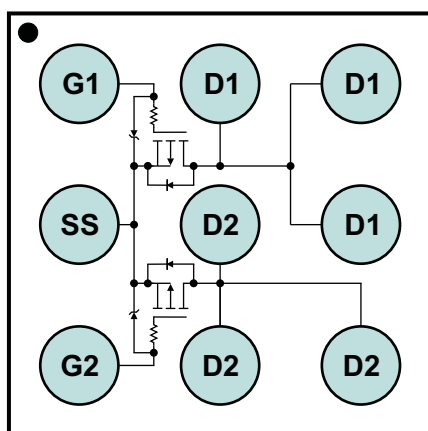
- Battery Management
- Battery Protection
- Load and Input Switching

3 Description

The CSD75207W15 device is designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on-resistance coupled with the small footprint and low profile make the device ideal for battery-operated space-constrained applications. The device has also been awarded with U.S. patents 7952145, 7420247, 7235845, and 6600182.



Top View



P0109-01

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{D1D2}	Drain-to-Drain Voltage	-20		V
Q_g	Gate Charge Total (-4.5 V)	2.9		nC
Q_{gd}	Gate Charge Gate to Drain	0.4		nC
$R_{D1D2(on)}$	Drain-to-Drain On Resistance	$V_{GS} = -1.8\text{ V}$	119	m Ω
		$V_{GS} = -2.5\text{ V}$	64	m Ω
		$V_{GS} = -4.5\text{ V}$	45	m Ω
$V_{GS(th)}$	Threshold Voltage	-0.8		V

Ordering Information⁽¹⁾

Device	Package	Media	Qty	Ship
CSD75207W15	1.5-mm × 1.5-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

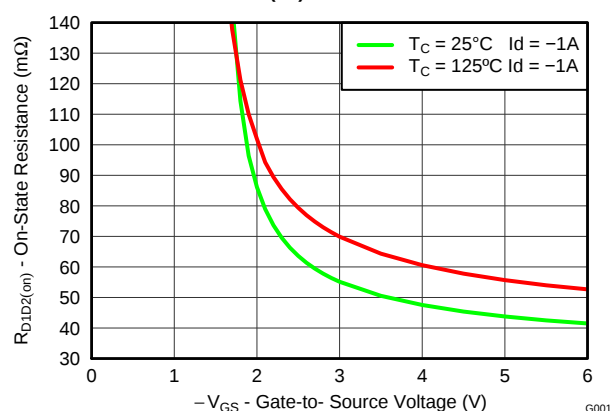
$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{D1D2}	Drain-to-Drain Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	-6.0	V
I_{D1D2}	Continuous Drain to Drain Current ^{(1) (2)}	-3.9	A
	Pulsed Drain to Drain Current, $T_C = 25^\circ\text{C}$ ⁽³⁾	-24	A
I_S	Continuous Source Pin Current	-1.2	A
	Pulsed Source Pin Current ⁽³⁾	-15	A
I_G	Continuous Gate Clamp Current	-0.5	A
	Pulsed Gate Clamp Current ⁽³⁾	-7	A
P_D	Power Dissipation ⁽¹⁾	0.7	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

(1) Per device, both sides in conduction

(2) Device operating at a temperature of 105 $^\circ\text{C}$

(3) Pulse duration 10 μs , duty cycle $\leq 2\%$

$R_{D1D2(on)}$ vs V_{GS}



G001



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4 Revision History

Changes from Original (June 2013) to Revision A	Page
• Increased continuous drain to drain current to 3.9 A	1
• Updated the continuous drain to drain current conditions to specify a temperature of 105°C	1

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated). Specifications and graphs are Per MOSFET unless otherwise stated. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

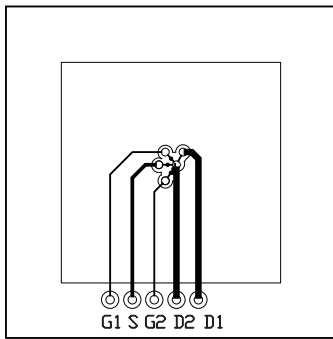
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{D1D2}	Drain-to-Drain Voltage	V _{GS} = 0 V, I _{D1D2} = −250 μA	−20			V
BV _{GSS}	Gate-to-Source Voltage	V _{D1D2} = 0 V, I _G = -250 μA	−6			V
I _{DDS}	Drain-to-Drain Leakage Current	V _{GS} = 0 V, V _{D1D2} = −16 V			−1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{D1D2} = 0 V, V _{GS} = −6 V			−100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{D1D2} = V _{GS} , I _{DS} = −250 μA	−0.6	−0.8	−1.1	V
R _{D1D2(on)}	Drain-to-Drain On-Resistance	V _{GS} = −1.8 V, I _{D1D2} = −1 A		119	162	mΩ
		V _{GS} = −2.5 V, I _{D1D2} = −1 A		64	77	mΩ
		V _{GS} = −4.5 V, I _{D1D2} = −1 A		45	54	mΩ
g _{fs}	Transconductance	V _{D1D2} = −10 V, I _{D1D2} = −1 A		6.2		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{D1D2} = −10 V, f = 1 MHz		458	595	pF
C _{OSS}	Output Capacitance			225	293	pF
C _{RSS}	Reverse Transfer Capacitance			10.4	13.5	pF
R _g	Series Gate Resistance			27		Ω
Q _g	Gate Charge Total (−4.5 V)	V _{D1D2} = −10 V, I _{D1D2} = −1 A		2.9	3.7	nC
Q _{gd}	Gate Charge – Gate to Drain			0.4		nC
Q _{gs}	Gate Charge – Gate to Source			0.7		nC
Q _{g(th)}	Gate Charge at V _{th}			0.4		nC
Q _{OSS}	Output Charge	V _{D1D2} = −9.5 V, V _{GS} = 0 V		3.1		nC
t _{d(on)}	Turn On Delay Time	V _{D1D2} = −10 V, V _{GS} = −4.5 V, I _{D1D2} = −1 A, R _G = 30 Ω		12.8		ns
t _r	Rise Time			8.6		ns
t _{d(off)}	Turn Off Delay Time			32.1		ns
t _f	Fall Time			16.0		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{D1D2} = −1 A, V _{GS} = 0 V	−0.8		−1	V
Q _{rr}	Reverse Recovery Charge	V _{dd} = −10 V, I _F = −1 A, di/dt = 200 A/μs		10.5		nC
t _{rr}	Reverse Recovery Time	V _{dd} = −10 V, I _F = −1 A, di/dt = 200 A/μs		23		ns

5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

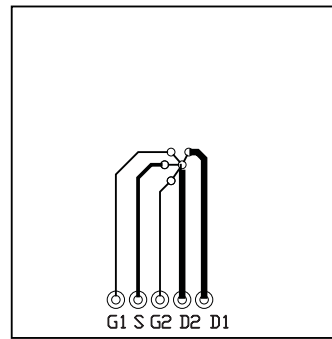
THERMAL METRIC		TYPICAL VALUE	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾ ⁽²⁾	70	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance ⁽³⁾ ⁽²⁾	165	

- (1) Device mounted on FR4 material with Minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1-inch² of Cu (2 oz).



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Typ $R_{\theta JA} = 70^{\circ}\text{C/W}$
when mounted on
1-inch² of 2 oz. Cu.

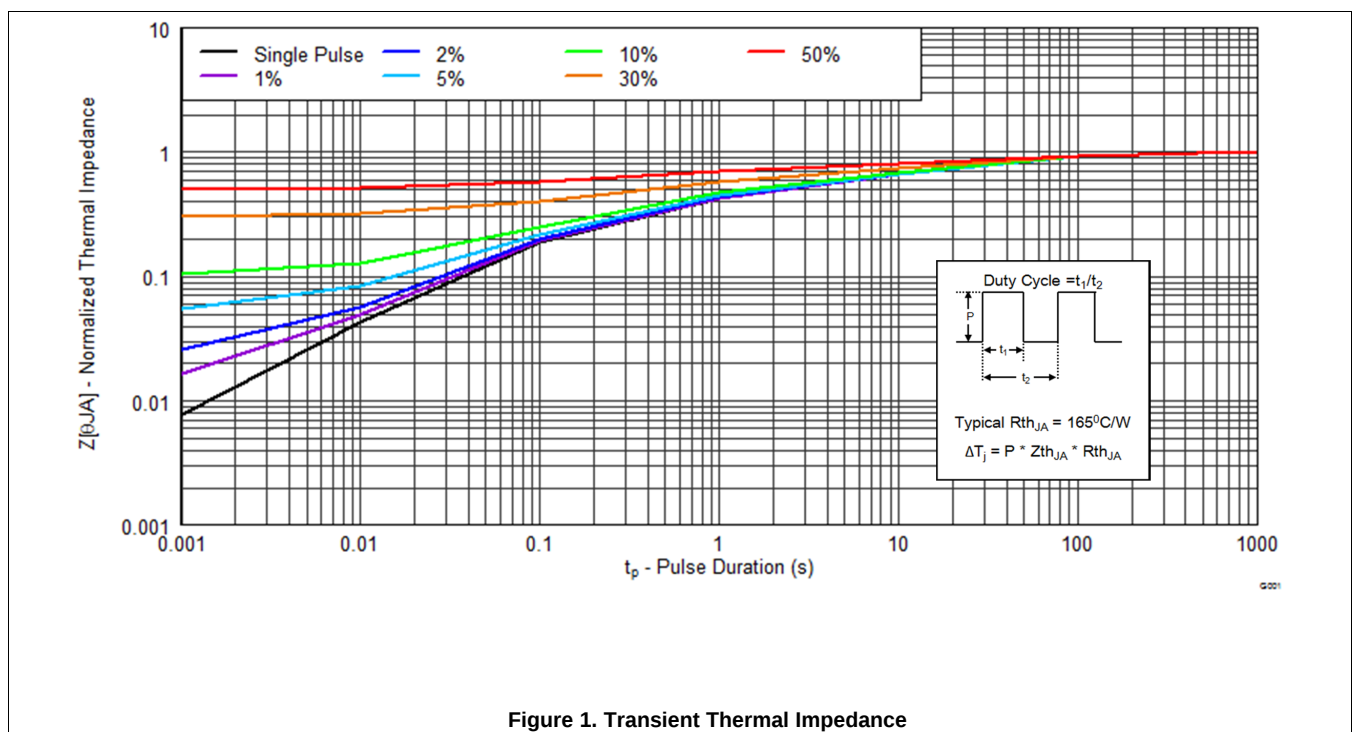


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Typ $R_{\theta JA} = 165^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

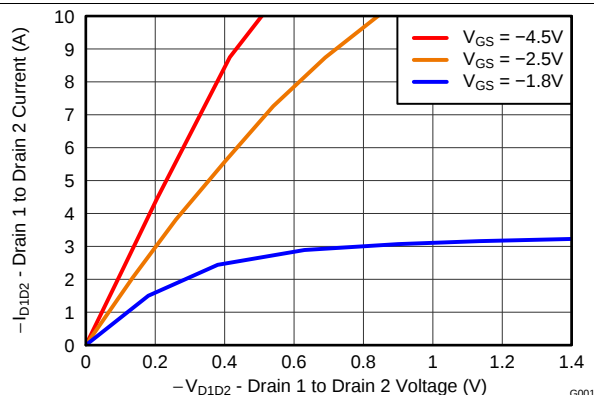


Figure 2. Saturation Characteristics

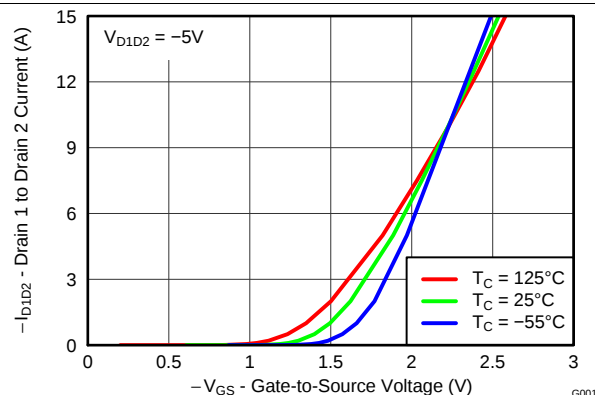


Figure 3. Transfer Characteristics

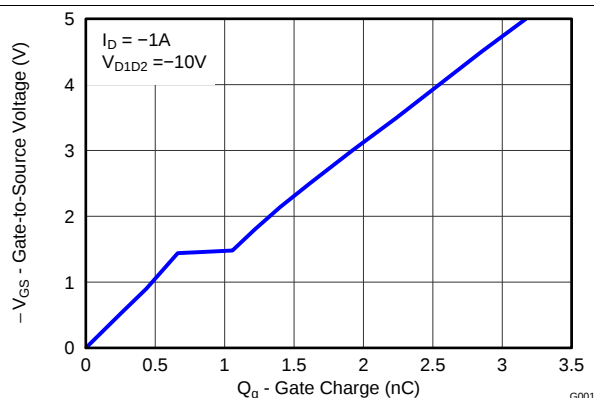


Figure 4. Gate Charge

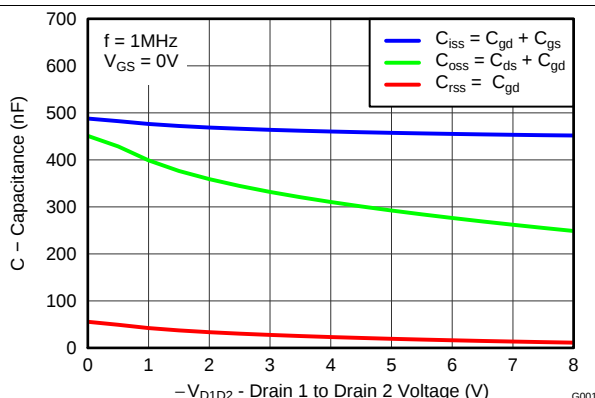


Figure 5. Capacitance

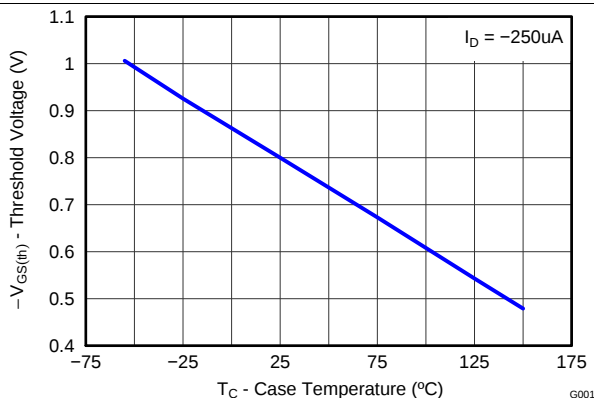


Figure 6. Threshold Voltage vs Temperature

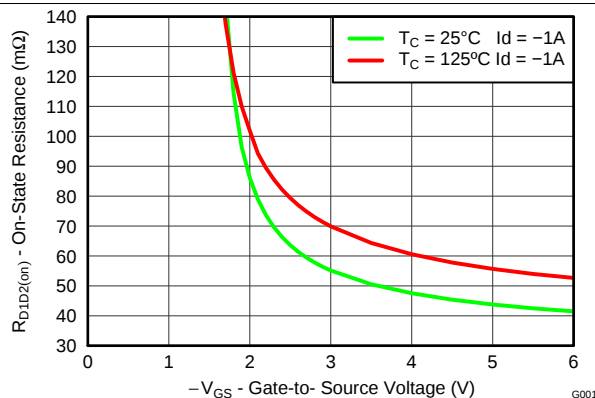


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

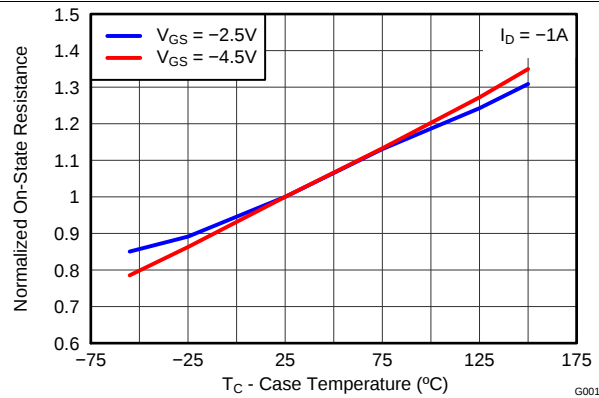


Figure 8. Normalized On-State Resistance vs Temperature

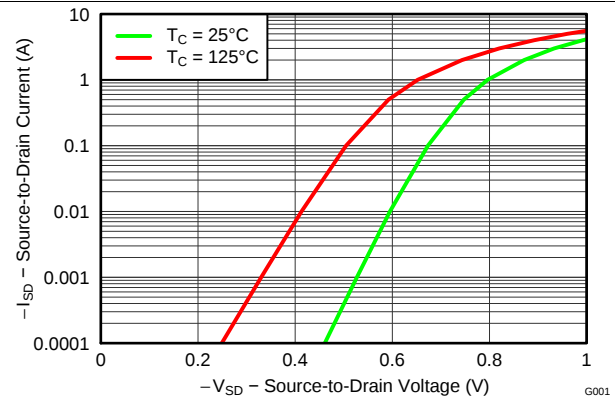


Figure 9. Typical Diode Forward Voltage

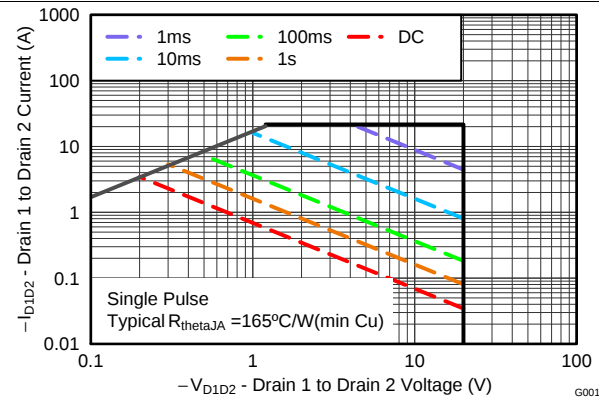


Figure 10. Maximum Safe Operating Area

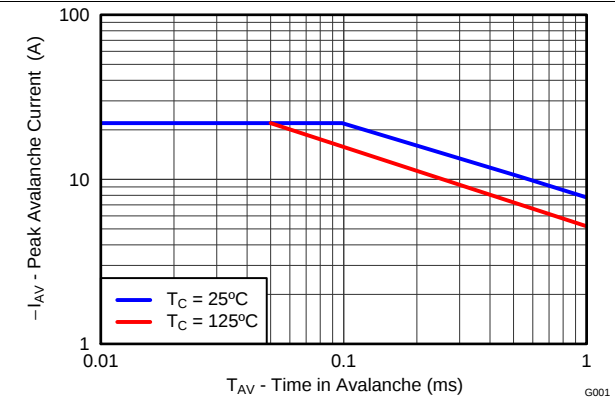


Figure 11. Single Pulse Unclamped Inductive Switching

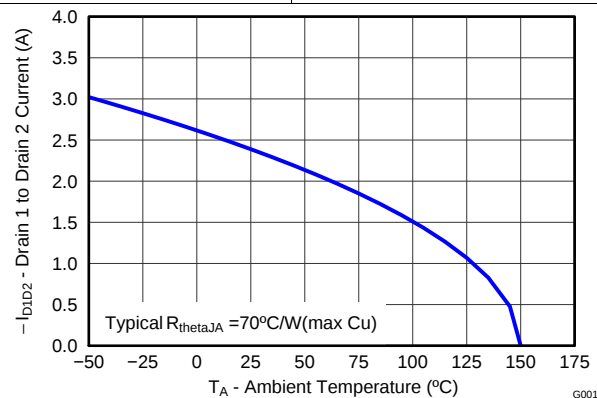


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

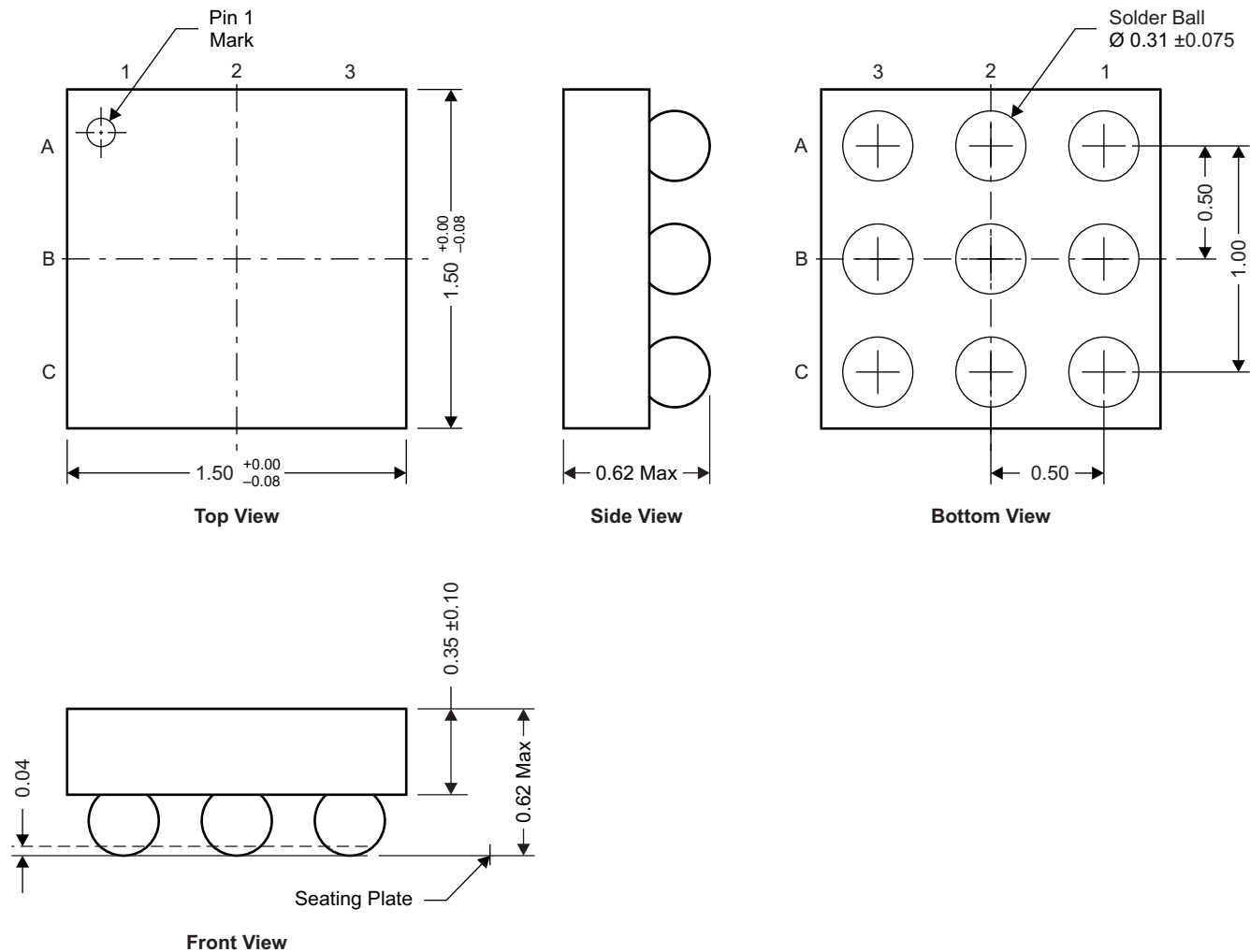
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD75207W15 Package Dimensions



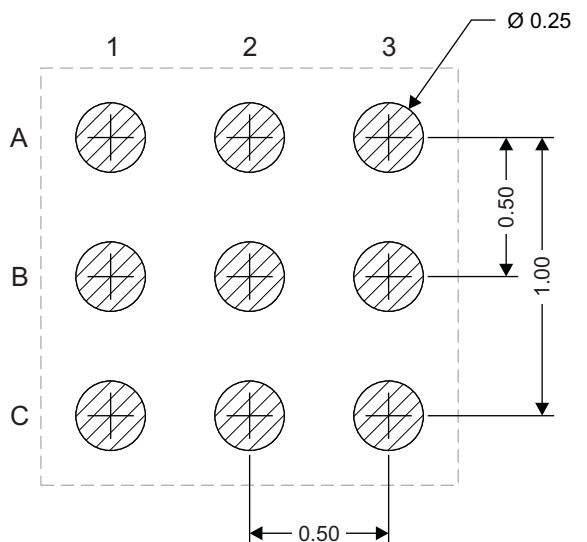
NOTE: All dimensions are in mm (unless otherwise specified)

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Pinout

POSITION	DESIGNATION
A1	Gate1
A2, A3, B3	Drain1
C1	Gate2
C2, C3, B2	Drain2
B1	Source Sense

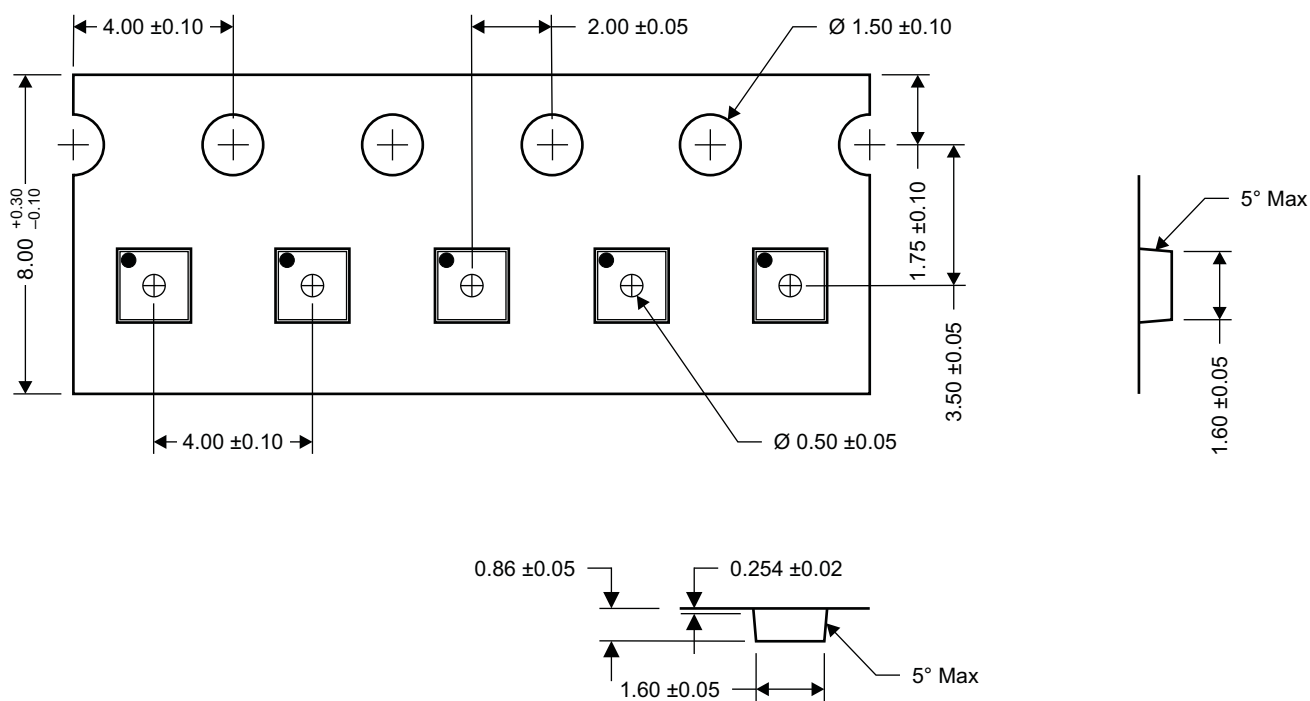
7.2 Recommended PCB Land Pattern



M0172-01

NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information



M0173-01

NOTE: All dimensions are in mm (unless otherwise specified).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD75207W15	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75207	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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