LMP7312 Evaluation Board User Guide (551600360-001 REV A)

This evaluation board contains the LMP7312, along with a SPI command generator to program the registers in the LMP7312

.Connectors, Jumpers, Test Point

POWER SUPPLY

+Vs banana plug for the positive power supply of the LMP7312 and the on-board SPI command generator.

VIO banana plug to power the SPI of the LMP7312 when an external micro is used to program the SPI.

GND banana plug for ground connection.

SIGNAL CONNECTORS

Input signals

+IN_CL banana plug for non-inverting input of the amplification pair.

-IN_CL banana plug for inverting input of the amplification pair.

+IN_LS BNC for non-inverting input of the attenuation pair.

-IN_LS BNC for inverting input of the attenuation pair.

J7 14-pin header available for microcontroller connection. The pin out is shown in Table 3.

Reference Signals

V_{ocm} banana plug for the common mode output signals and the output configuration (single ended, differential). See the Output Configuration section.

VR banana plug for the output reference when the output of the LMP7312 is used in single ended mode.

Output signals

OUT- BNC for the inverting Output in the differential output configuration

OUT+ BNC for the non-inverting output.

DP Differential Probe Header connector.

P1 5-pin header for ADC141S626 or ADC161S626 Eval Board connection.

JUMPERS

The eval board has 6 jumpers:

J1 connects the CSB pin of the LMP7312 to either the onboard SPI commands generator or to pin 1 of J7.

J2 connects the SCK pin of the LMP7312 to either the onboard SPI commands generator or to pin 3 of J7.

J3 connects the SDI pin of the LMP7312 to either the onboard SPI commands generator or to pin 5 of J7.

J4 connects the -VOUT/VR pin of the LMP7312 either to the VR reference or to the LOAD. (see the Output Configuration section).

J5 connects the VOCM pin of the LMP7312 to either the ground or to the VOCM reference. (see the Output Configuration section).

J6 connects the VIO pin of the LMP7312 to either the +Vs plug or to the VIO plug.

TEST POINTS

The test points are connected as follows:

TP1 GND
TP2 -IN pin
TP3 -VIN pin
TP4 -VOUT/VR pin
TP5 +IN pin
TP6 +VIN pin
TP7 +VOUT pin
TP8 VR
TP9 VOCM
TP10 +Vs
TP11 VIO

Hardware Setup

REGISTER PROGRAMMING SETUP

In order to use the on board SPI commands generator to program the LMP7312 the following jumpers need to be configured as follows:

J1 open
J2 open
J3 open
J6 short pin1 to pin 2

In order to use a microcontroller to program the LMP7312 the following jumpers need to be configured as follows:

J1 short
J2 short
J3 short
J6 short pin2 to pin 3

Connect the external microcontroller to J7.
Refer to Table 3 for J7 pin out.

POWER SUPPLY SETUP

When the LMP7312 is programmed through the onboard SPI command generator, a 5V supply is needed to power the eval board:

- Connect a +5V supply to the +Vs and GND banana plugs

When the LMP7312 is programmed through a microcontroller:

- Connect a +5V supply between +Vs and GND banana plugs
- Connect a supply (2.7V – 5.5V) that matches microcontroller voltage range between +VIO and GND banana plugs

SOURCE SETUP

Attenuation input pair

If signal source impedance matching is desired, solder the resistors R8 and R9 of appropriate value.

Amplification input pair

The 50Ω shunt resistor (R1) between the inputs needs to be removed if the amplification input pair is not used as a current loop receiver.

OUTPUT CONFIGURATION

The LMP7312 is able to work in both single ended and differential output mode. The selection of the output is made through the Vocm (output common mode voltage) pin.

Differential mode

- Open jumper J4
- Short pin1 and pin2 of J5
- Connect a supply in the range between 1V and 5V to the +Vocm and GND banana plugs

Single ended mode

- Short jumper J4
- Short pin2 and pin3 of J5
- Connect a supply in the range between 0V and 5V between VR and GND banana plugs

COMPONENTS

If the device is configured in the differential output mode, the series resistances R2 and R3, RLd and the capacitance CLd can be changed in order to build a first order low pass filter with desired bandwidth. In this configuration the capacitance CLs and the resistance RLs should be removed.
If the device is configured in the single-ended output mode, the series resistance R3, RLs and capacitance CLs can be changed in order to build a first order low pass filter with desired bandwidth. In this configuration the capacitance CLd and the resistance RLd should be removed.
If the value of the shunt resistance R1 does not fit the application needs, replace it as needed

Using the Board

INPUT AND OUTPUT SIGNALS

Attenuation mode

Connect a signal at +IN_LS and –IN_LS BNC; refer to the Datasheet for the allowed amplitude according to the set gain.

Amplification mode

Connect a signal at +IN_CL and –IN_CL banana; refer to the Datasheet for the allowed amplitude according to the set gain.

PROGRAMMING THE LMP7312

The register in the LMP7312 can be programmed using switches S1 and S2. S2 consists of five switches labeled B0, B1, B2, B3, B4, corresponding to the five bits of the LMP7312 register. If the switch is up a “0” is programmed to the corresponding bit. S1 is used to load the data into the register of the LMP7312.
For example, to load the gain of 0.384V/V set S2 as follows:

Gain_1 – Down 1
Gain_0 – Up 0
EN_CL – Up 0
Null_SW – Up 0
HiZ – Up 0

Then Push the switch S1 to load the data into the register of the LMP7312.
Table 1 shows the allowed register values.

Table 1 Register Values

LSB				MSB		
HI_Z	**NULL_SW**	**EN_CL**	**Gain_0**	**Gain_1**	**Gain Value (V/V)**	**Mode of Operation**
0	0	0	0	0	0.096	Attenuation
0	0	0	1	0	0.192	Attenuation
0	0	0	0	1	0.384	Attenuation
0	0	0	1	1	0.768	Attenuation
0	0	1	0	1	1	Amplification
0	0	1	1	1	2	Amplification
1	x	x	x	x	-	High Impedance output
0	1	x	x	x	1	Null Switch mode

Table 2 S2 Dip switch description

PINS	NAME
1-2	Hiz
3-4	Null_SW
5-6	EN_CL
7-8	Gain_0
9-10	Gain_1

WRITING TO THE REGISTER USING A MICROCONTROLLER

A microcontroller can be used to program the LMP7312. If the microcontroller is provided with a TTL logic signal connect pin1 and pin2 of J6 together, otherwise, apply a voltage compliant with the microcontroller logic value to the VIO banana plug, and short pin2 and pin3 of J6. The microcontroller signals are connected to the LMP7312 through J7. More information on the SPI configuration is provided in the SPI section of the LMP7312 datasheet.

Table 3 J7 connector description

PIN	NAME	PIN	NAME
1	CSB	8	NC
2	GND	9	NC
3	SCK	10	NC
4	NC	11	NC
5	SDI	12	NC
6	NC	13	NC
7	SDO	14	NC

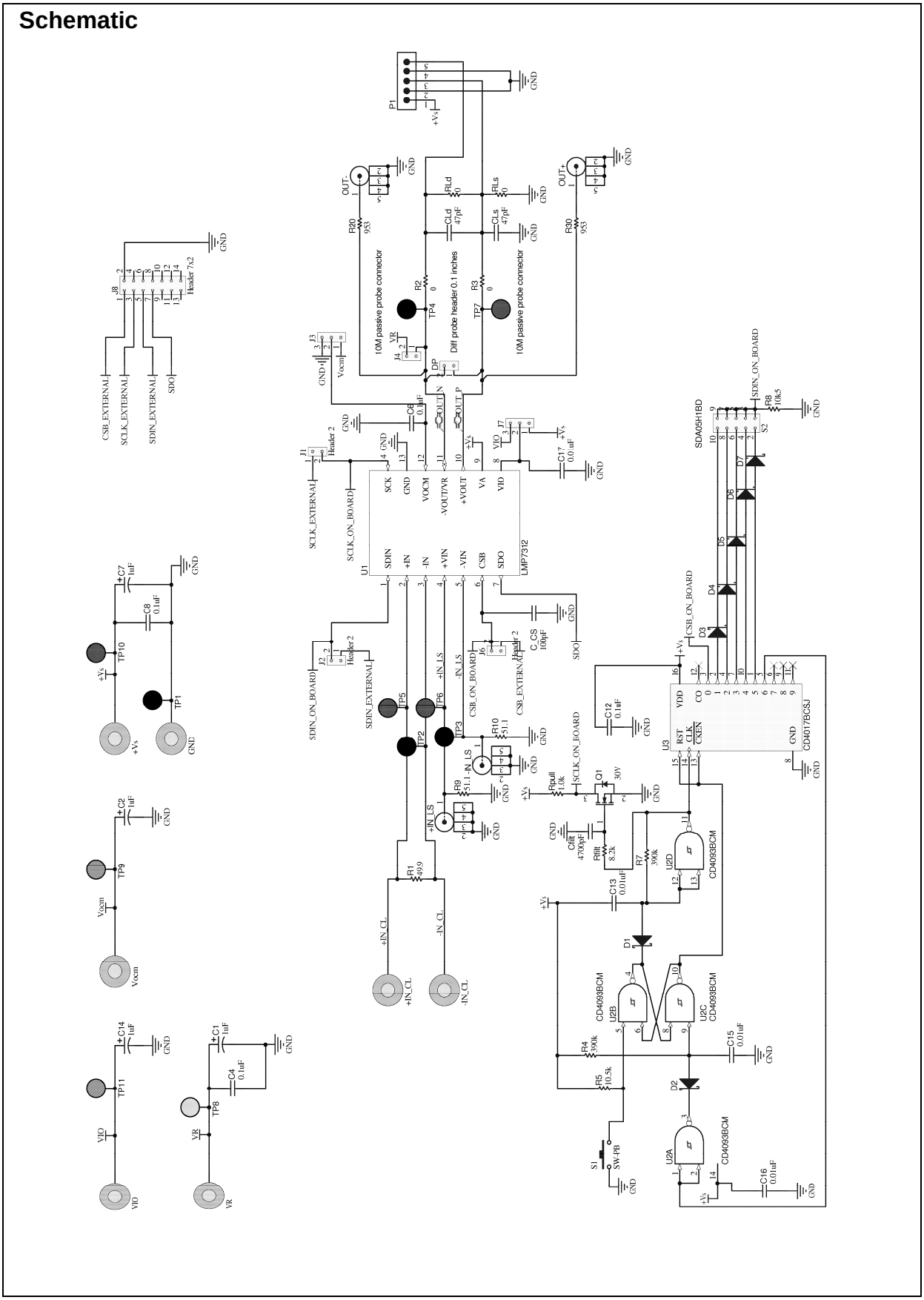
Interfacing ADC Eval Board

The LMP7312 Eval Board can be interfaced with the ADC141S626 and ADC161S626 Eval Boards through the P1 connector only when the LMP7312 is configured in the differential output mode (see Output Configuration section).

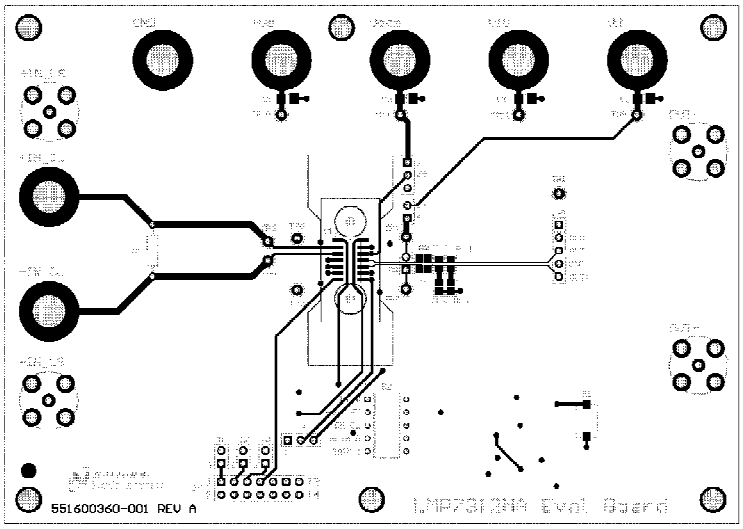
Table 4 P1 connector description

PIN	1	2	3	4	5
NAME	Vs	GND	OUT-	GND	OUT+

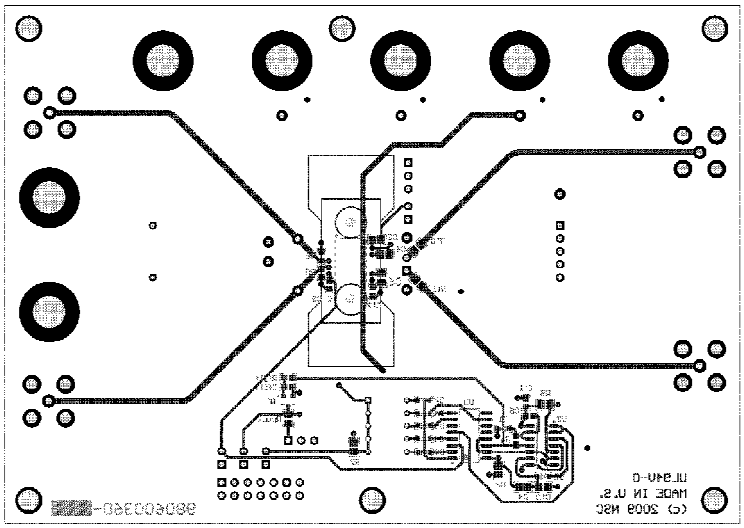
Schematic


LMP7312
U1
SDIN
+IN
-IN
+VIN
-VIN
CSB
SDO
SCK
GND
VOCM
-VOUT/VR
+VOUT
VA
VIO
SCLK_ON_BOARD
SCLK_EXTERNAL
SDIN_ON_BOARD
SDIN_EXTERNAL
CSB_ON_BOARD
CSB_EXTERNAL
SDO
+IN_LS
-IN_LS
+IN_CL
-IN_CL
OUT_N
OUT_P
OUT-
OUT+
10M passive probe connector
Diff probe header 0.1 inches
R20 953
R30 953
RLd 20
RLs 20
CLd 47pF
CLs 47pF
R2 0
R3 0
TP4
TP7
C6 0.1uF
C17 0.0 uF
C12 0.1uF
C13 0.01uF
C15 0.01uF
C16 0.01uF
C_CS 100pF
R10 51.1
R9 51.1
R1 999
Rpull 1.0k
Cflt 4700pF
Rflt 8.2k
R7 390k
R4 390k
R5 10.5k
R8 10K5
Q1 30V
S1 SW-PB
U2A CD4093BCM
U2B CD4093BCM
U2C CD4093BCM
U2D CD4093BCM
U3 CD4017BCSJ
D1
D2
D3
D4
D5
D6
D7
S2
P1
J1 Header 2
J2 Header 2
J3
J4
J6 Header 2
J7
J8 Header 7x2
C7 1uF
C8 0.1uF
C2 1uF
C14 1uF
C1 1uF
C4 0.1uF
TP1
TP2
TP3
TP5
TP6
TP8
TP9
TP10
TP11
Vcm
VIO
VR
+Vs
GND

Board Layout



Top layer



Bottom layer

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