IS31FL3194

3-CHANNEL LED DRIVER WITH PROGRAMMABLE PATTERN SEQUENCING

August 2017

GENERAL DESCRIPTION

IS31FL3194 is a 3-channel LED driver which features two-dimensional auto breathing mode. It has Pattern Mode and Current Level Mode for RGB lighting effects. The maximum output current can be adjusted in 4 levels (40mA Max.).

In Current Level Mode, the current level of each output can be independently programmed and controlled in 256 steps to simplify color mixing. In Pattern Mode, the timing characteristics for output current - current rising (T1), holding (T2), falling (T3) and off time (TS, TP, T4), can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single color breathing without requiring any additional interface activity, thus saving valuable system resources.

IS31FL3194 is available in WCSP-8 (1.0mm×1.6mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- 2.7V to 5.5V supply voltage
- One group RGB/RG+W, or 3 single color LED breathing system-free pre-established pattern
- Each output has own independent TS~T4 and own start command (Update register)
- I2C interface, automatic address increment function
- 4 band programmable output current for each output, each band has 256 current levels
- Selectable gamma value for automatic breathing for each output
- Each pattern have 3 pre-established color
- Over-temperature protection
- Operating temperature: -40°C ~ +85°C

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

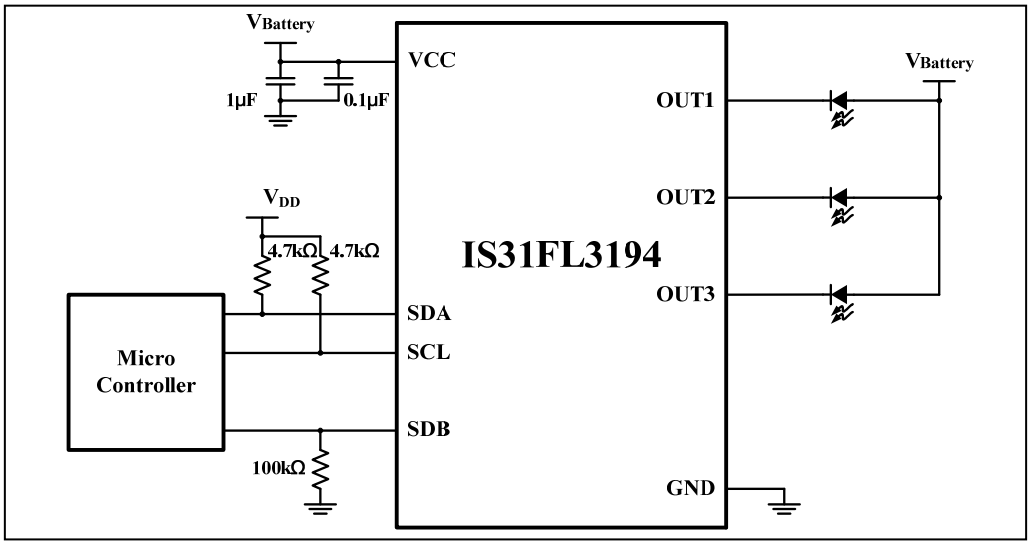
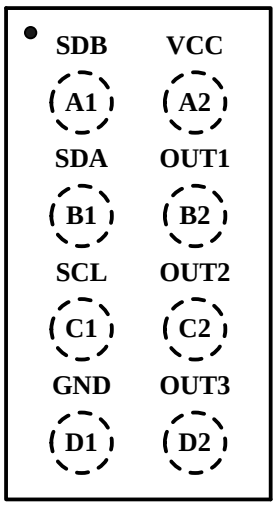


Figure 1 Typical Application Circuit

Note: The IC should be placed far away from the mobile antenna in order to prevent the EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WCSP-8	

PIN DESCRIPTION

No.	Pin	Description
A1	SDB	Shutdown the chip when pulled to low.
A2	VCC	Power supply.
B1	SDA	I2C serial data.
B2, C2, D2	OUT1~OUT3	Current source outputs.
C1	SCL	I2C serial clock.
D1	GND	Ground.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3194-CLS2-TR	WCSP-8, Lead-free	3000

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a.) the risk of injury or damage has been minimized;
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ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	150°C
Operating temperature range, T_A=T_J	-40°C ~ +85°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance (Mounted on JEDEC standard 4 layer (2s2p) PCB test board), θ_{JA}	79.34°C/W
ESD (HBM) ESD (CDM)	±2kV ±1kV

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = -40°C ~ +85°C, V_{CC} = 5V, unless otherwise noted. Typical value are T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB} = V_{CC}		0.8		mA
I_{SD}	Shutdown current	V_{SDB} = 0V		1	2.5	μA
		V_{SDB} = V_{CC}, software shutdown		1	3.5	
I_{OUT}	Output current	Current Level mode, V_{DS}= 0.4V CL Register= 0xFF Current band: 40mA		40		mA
V_{HR}	Current sink headroom voltage	I_{OUT} = 20mA		150		mV
Logic Electrical Characteristics (SDA, SCL, SDB)						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	(Note 1)		5		nA
I_{IH}	Logic "1" input current	(Note 1)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 2)		$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 2)		$20+0.1C_b$	300	ns

Note 1: Guaranteed by design.

Note 2: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3194 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3194 has a constant 7-bit slave address "101 0011" (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command.

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3194.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3194's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3194 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3194, the register address byte is sent, most significant bit first. IS31FL3194 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3194 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3194, load the address of the data register that the first data byte is intended for. During the IS31FL3194 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3194 will be placed in the new address, and so on (Figure 5).

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31FL3194 address with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31FL3194 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3194 to the master (Figure 6).

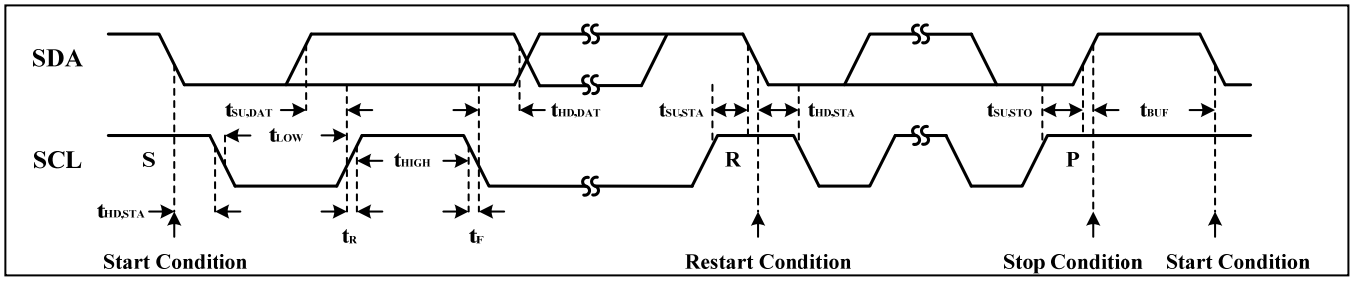


Figure 2 Interface Timing

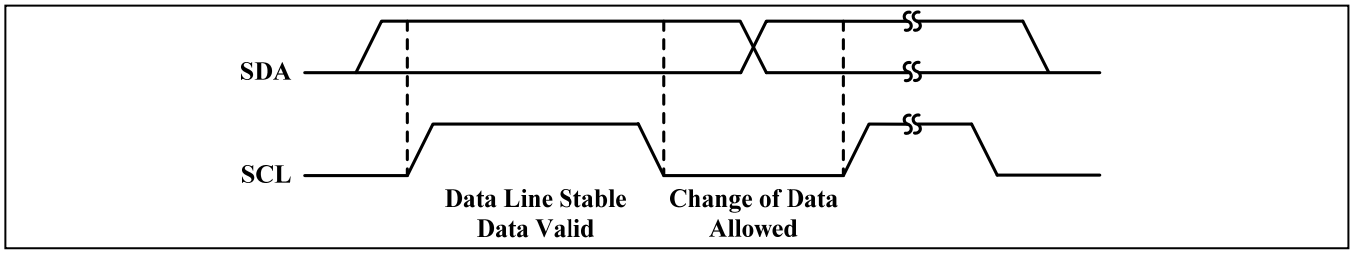


Figure 3 Bit Transfer

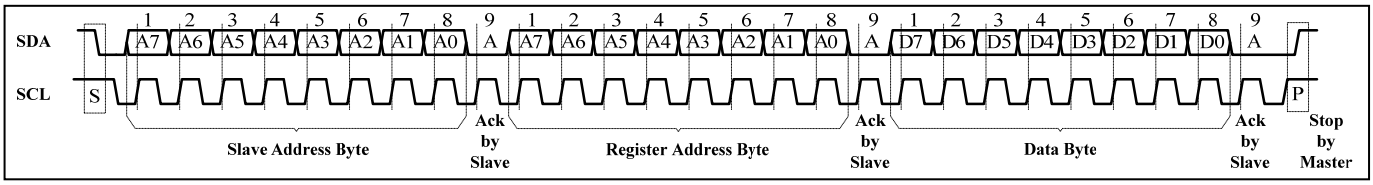


Figure 4 Writing to IS31FL3194 (Typical)

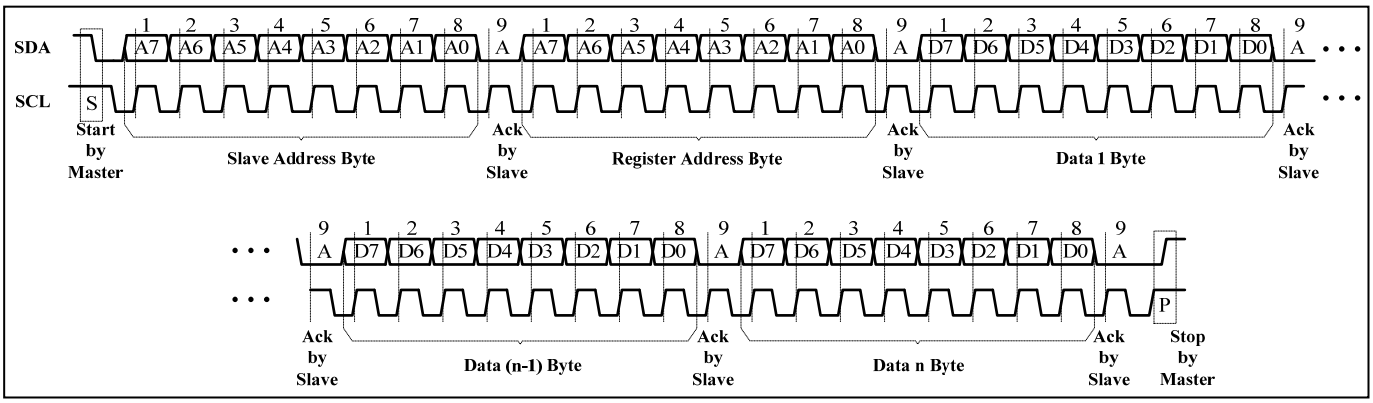


Figure 5 Writing to IS31FL3194 (Automatic Address Increment)

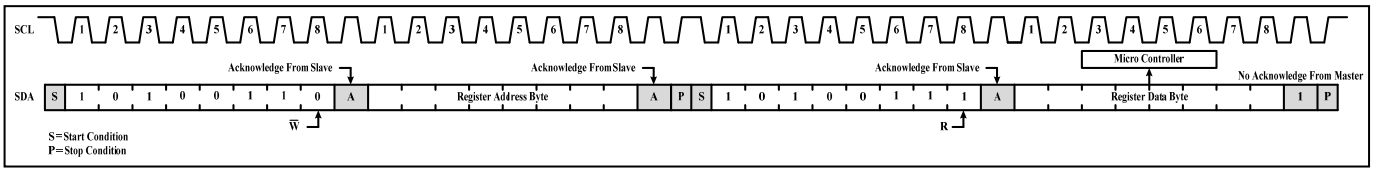


Figure 6 Reading from IS31FL3194

Table 1 REGISTERS DEFINITIONS

Address	Name	Function	R/W	Table	Default
00h	Product ID	For read only, read result is 0xCE	R	-	1100 1110
01h	Operating Configure Register	Set software shutdown mode and operation mode	W	2	0000 0000
02h	Output Enable Register	Output enable bit	W	3	0000 0111
03h	Current Band Register	Set current band of each Output	W	4	0001 0101
04h	Hold Function Register	Set the hold function of each Output	W	5	0000 0000
0Dh/0Eh/0Fh	P1/P2/P3 State Register	For reading the pattern running state	R	6	0000 0000
10h/21h/32h	OUT1/OUT2/OUT3 Current Level Register	Output current level data register	W	7	0000 0000
10h~12h/ 20h~22h/ 30h~32h	Color 1 Setting Register of P1/P2/P3	Output current level data register-Color 1	W	8	0000 0000
13h~15h/ 23h~25h/ 33h~35h	Color 2 Setting Register of P1/P2/P3	Output current level data register-Color 2	W	9	0000 0000
16h~18h/ 26h~28h/ 36h~38h	Color 3 Setting Register of P1/P2/P3	Output current level data register-Color 3	W	10	0000 0000
19h/29h/39h	P1/P2/P3 TS &T1 Setting Register	Set the TS~T1 time	W	11	0000 0000
1Ah/2Ah/3Ah	P1/P2/P3 T2 &T3 Setting Register	Set the T2~T3 time	W	12	0000 0000
1Bh/2Bh/3Bh	P1/P2/P3 TP &T4 Setting Register	Set the TP~T4 time	W	13	0000 0000
1Ch/2Ch/3Ch	P1/P2/P3 Color Enable Register	Set the color enable/disable	W	14	0000 0001
1Dh/2Dh/3Dh	P1/P2/P3 Color Cycle Times Register	Set color repeat time	W	15	0000 0000
1Eh/2Eh/3Eh	P1/P2/P3 NXT Register	Set next step and Gamma of each pattern	W	16~18	0000 0001
1Fh/2Fh/3Fh	P1/P2/P3 Loop Times Register	Set the loop time of P1~P3	W	19	0000 0000
40h	Color Update Register	Update color data	W	-	-
41h/42h/43h	P1/P2/P3 Update Register	Update the time data and start to run pattern	W		
4Fh	Reset Register	Reset the registers value to default	W		

Note: When T1 or T3= 0.03s, GAM will be set to 10 (Linearity).

Table 2 01h Operating Configure Register

Bit	D7	D6:D4	D3	D2:D1	D0
Name	-	OUT3:OUT1	-	RGB	SSD
Default	-	000	-	00	0

The Operating Configure Register sets software shutdown and operation modes of IS31FL3194.

SSD Software Shutdown Enable

0 Software shutdown mode

1 Normal operation

RGB LED Mode

00/11 Single mode

01 RG+W mode, OUT1 and OUT2 work together, OUT3 work independent

10 RGB mode, three outputs work together

OUTx Output Operating Mode

0 Current Level Mode

1 Pattern Mode

Table 3 02h Output Enable Register

Bit	D7:D3	D2:D0
Name	-	EN3:EN1
Default	00000	111

The Output Enable Register enables/disables the outputs independently.

ENx Output Enable Control

0 Output disable

1 Output enable

Table 4 03h Current Band Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	CB3	CB2	CB1
Default	00	01	01	01

The Current Setting Register stores the current band of each LED output.

CBx Current Band Setting

00 Band 1: 0mA~10mA, I_{MAX}=10mA

01 Band 2: 0mA~20mA, I_{MAX}=20mA

10 Band 3: 0mA~30mA, I_{MAX}=30mA

11 Band 4: 0mA~40mA, I_{MAX}=40mA

Table 5 04h Hold Function Register

Bit	D7:D6	D5	D4	D3	D2	D1	D0
Name	-	HF3	HT3	HF2	HT2	HF1	HT1
Default	00	0	0	0	0	0	0

The Hold Function Register configures hold time for each output in Pattern Mode.

HTx Hold Time Selection

0 Hold at end of T4 when pattern loop done (always off)

1 Hold at end of T2 when pattern loop done (always on)

HFx Hold Function Enable

0 Hold function disable

1 Hold function enable

Table 6 0Dh/0Eh/0Fh P1/P2/P3 State Register (Read Only)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	PSx	CS3x	CS2x	CS1x	-	TXx
Default	0	0	0	0	0	000

ODh is the state of Pattern 1, PS is the pattern enable or not, CSX is the color enable or not, TX will show the running position of Pattern 1.

OEh and OFh store the state of Pattern 2 and 3.

TXx Time state

000 Running at TS

001 Running at T1

010 Running at T2

011 Running at T3

100 Running at TP

101 Running at T4

CSXx Color State

0 Running at Color x

1 Running at Color x

PSx Pattern State

0 Running at Pattern x

1 Running at Pattern x

Table 7 10h/21h/32h OUT1/OUT2/OUT3 Current Level Register

Bit	D7:D0
Name	CL
Default	0000 0000

When IS31FL3194 operates in Current Level Mode, the value of Current Level Registers will decide the output current of OUTx in 256 levels.

The output current may be computed using the Formula (1):

$$I_{OUT} = \frac{I_{MAX}}{256} \cdot \sum_{n=0}^{7} D[n] * 2^n \qquad (1)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.
For example: if D7:D0 = 10110101,
$I_{OUT} = I_{MAX} (2^7+2^5+2^4+2^2+2^0)/256$
I_{MAX} is set by Current Band Register.

Table 8
10h~12h Color 1 Setting Register of P1

Bit	D7:D0
Name	P1COL1_Ox
Default	0000 0000

13h~15h Color 2 Setting Register of P1

Bit	D7:D0
Name	P1COL2_Ox
Default	0000 0000

16h~18h Color 3 Setting Register of P1

Bit	D7:D0
Name	P1COL3_Ox
Default	0000 0000

Table 9
20h~22h Color 1 Setting Register of P2

Bit	D7:D0
Name	P2COL1_Ox
Default	0000 0000

23h~25h Color 2 Setting Register of P2

Bit	D7:D0
Name	P2COL2_Ox
Default	0000 0000

26h~28h Color 3 Setting Register of P2

Bit	D7:D0
Name	P2COL3_Ox
Default	0000 0000

Table 10
30h~32h Color 1 Setting Register of P3

Bit	D7:D0
Name	P3COL1_Ox
Default	0000 0000

33h~35h Color 2 Setting Register of P3

Bit	D7:D0
Name	P3COL2_Ox
Default	0000 0000

36h~38h Color 3 Setting Register of P3

Bit	D7:D0
Name	P3COL3_Ox
Default	0000 0000

Color Setting Registers store the color setting for each output in Pattern Mode. Check Pattern Color Setting section for more information about the color setting registers.

Need to write Color Update Register (40h) to update the data.

Table 11 19h/29h/39h P1/P2/P3 TS &T1 Setting Register

Bit	D7:D3	D4:D0
Name	T1	TS
Default	0000	0000

The TS & T1 Setting Registers set the TS and T1 time in Pattern Mode.

TS	Pattern Start Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

T1	Rise Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

Table 12 1Ah/2Ah/3Ah P1/P2/P3 T2 &T3 Setting Register

Bit	D7:D3	D4:D0
Name	T3	T2
Default	0000	0000

The T2 & T3 Setting Registers set the T2 and T3 time in Pattern Mode.

T2	Hold Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

T3	Fall Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

Table 13 1Bh/2Bh/3Bh P1/P2/P3 TP &T4 Setting Register

Bit	D7:D3	D4:D0
Name	T4	TP
Default	0000	0000

The TP & T4 Setting Registers set the TP and T4 time in Pattern Mode.

TP	Time between Pulses
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
(1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

T4	Off Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

Table 14 1Ch/2Ch/3Ch P1/P2/P3 Color Enable Register

Bit	D7:D3	D2	D1	D0
Name	-	CE3	CE2	CE1
Default	00000	0	0	1

Color Enable Register enables the color function for each color in Pattern Mode.

CEx	Color Enable Selection
0	Color x disable
1	Color x enable

Table 15 1Dh/2Dh/3Dh P1/P2/P3 Color Cycle Times Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	CCT3	CCT2	CCT1
Default	00	00	00	00

Color Cycle Times Register sets Color loop times for each color.

CCTx	Color Cycle Times Selection
00	Endless
01	1 time
10	2 times
11	3 times

Table 16 1Eh P1 NXT Register

Bit	D7:D4	D3:D2	D1:D0
Name	MTPLT1	GAM1	NXT1
Default	0000	00	01

NXT1 defines next operation when Pattern 1 is done. GAM1 controls the gamma of Pattern 1. MTPLT1 controls the loop of Pattern 1.

NXT1	Pattern 1 Next
00/10/11	Just stop
01	Go to Pattern 2 (Only effective in RGB & RG+W Mode)

GAM1	Gamma Selection
00/11	Gamma=2.4
01	Gamma=3.5
10	Linearity

MTPLT1	Multy-Pulse loop time
0000	endless
0001	1 time
…	
1111	15 times

Table 17 2Eh P2 NXT Register

Bit	D7:D4	D3:D2	D1:D0
Name	MTPLT2	GAM2	NXT2
Default	0000	00	01

NXT2 defines next operation when Pattern 2 is done. GAM2 controls the gamma of Pattern 2. MTPLT2 controls the loop of Pattern 2.

NXT2	Pattern 2 Next
00/11	Just stop
01	Go to Pattern 1 (Only effective in RGB & RG+W Mode)
10	Go to Pattern 3 (Only effective in RGB Mode)

GAM2	Gamma Selection
00/11	Gamma=2.4
01	Gamma=3.5
10	Linearity

MTPLT2 Multy-Pulse loop time

0000 endless
0001 1 time
…
1111 15 times

Table 18 3Eh P3 NXT Register

Bit	D7:D4	D3:D2	D1:D0
Name	MTPLT3	GAM3	NXT3
Default	0000	00	01

NXT3 defines next operation when Pattern 3 is done. GAM3 controls the gamma of Pattern 3. MTPLT3 controls the loop of Pattern 3.

NXT3 Pattern 3 Next

00/10/11 Just stop
01 Go to Pattern 1 (Only effective in RGB Mode)
10 Go to Pattern 2 (Only effective in RGB Mode)

GAM3 Gamma Selection

00/11 Gamma=2.4
01 Gamma=3.5
10 Linearity

MTPLT3 Multy-Pulse loop time

0000 endless
0001 1 time
…
1111 15 times

Table 19 1Fh/2Fh/3Fh P1/P2/P3 Loop Times Register

Bit	D7	D6:D0
Name	PLTx_H	PLTx_L
Default	0	000 0000

If PLTx_H(D7)=0, PLTx_L!=0
Pattern loop times

$$LoopTime = \sum_{n=0}^{6} D[n] * 2^n \ (2) \qquad (3)$$

If PLTx_H(D7)=0, PLTx_L=0, endless
If PLTx_H(D7)=1, PLTx_L!=0
Pattern loop times

$$LoopTime = 16 \times \sum_{n=0}^{6} D[n] * 2^n \qquad (3)$$

If PLTx_H(D7)=1, PLTx_L=0, endless
Where D[n] stands for the individual bit value.

40h Color Update Register

Write 0xC5 to 40h will update the data of 10h~18h/20h~28h/30h~38h

41h/42h/43h P1/P2/P3 Update Register

Write 0xC5 to these registers will update the time parameters of Pattern x, and start to run Pattern x.
Note, for RG+W Mode, when write 0xC5 to P3 Update Register (43h), all the P1, P2 and P3 time parameters will be updated.

4Fh Reset Register

Once user writes “0xC5” to the Reset Register, IS31FL3194 will reset all registers to their default value. On initial power-up, the IS31FL3194 registers are reset to their default values for a blank display.

TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

IS31FL3194 is a 3-channel LED driver which features two-dimensional auto breathing mode. It has Pattern Mode and Current Lever Mode for RGB lighting effects.

POWER ON SEQUENCE

IS31FL3194 provides a power-on reset feature that is controlled by VBAT supply voltage. When the VBAT supply voltage exceeds 2.4V (TBD), the internal circuit starts to work. The reset signal will be generated to perform a power-on reset (POR) operation, which will reset all control circuits and configuration registers until the internal power voltage become stable.

Before SDB pull high, the I2C operation is allowed. The SDB rising edge will reset the I2C bus.

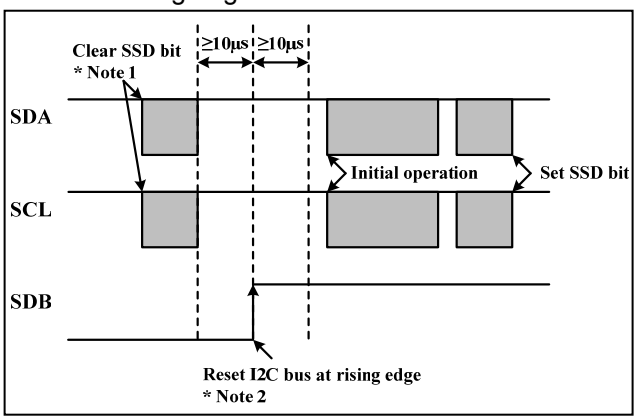


Figure 7 SDB Pin Sequence

Note 1: I2C operation is allowed when SDB is low.
Note 2: There should be no I2C operation 10μs before and after SDB rinsing edge.

In some case, like a mouse, when plug-out and quickly plug-in back the USB power, the LED will flicker for a very short time. The reason is the power is not lower than the POR voltage point (usually lower than 2.2V), and the device still stores the previous setting data, if user pull-up the SDB high when power up, following with the initial operation, the LED will be ON between SDB rising edge and Current Level initial effective, to avoid this, as above figure, a writing to 01h is recommended to shutdown the chip before pull-high the SDB pin.

CURRENT LEVEL MODE

There are four programmed current bands can be set by the Current Band Register (03h). It is used to set the global maximum of each output current, I_{MAX}.

By setting the OUTx bits of the Operating Configure Register (01h) to “0”, the corresponding OUTx will operate in Current Lever Mode. The Current Lever Registers (10h, 21h, 32h) are active and can modulate LED brightness of each output with 256 steps independently. For example, if the data in Current Lever Register is “0000 0100”, then the current lever is the fourth step, with a current level of 4/256.

In Current Lever Mode, user doesn’t need to turn on the CEx of 1Ch/2Ch/3Ch, a new value must be written to the Current Lever registers to change the output current. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing, blinking, or any other effects that the user defines.

PATTERN MODE

By setting the OUTx bits of the Operating Configure Register (01h) to “1”, the corresponding OUTx will operate in Pattern Mode. In Pattern Mode, the timing characteristics for output current – current rising (T1), holding (T2), falling (T3) and off time (TS, TP, T4), can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single color breathing without requiring any additional interface activity, thus saving valuable system resources.

PATTERN COLOR SETTING

In Pattern Mode, the LED color is defined by PxCOLy_Oz (x,y,z= 1,2,3) bits in Color Setting Registers (10h~18h, 20h~28h, 30h~38h). There are 3 RGB current combinations to generate 3 pre-defined colors for display. More than one of the 3 pre-defined colors can be chosen by setting Cex bits in Color Enable Register (1Ch/2Ch/3Ch). When Cex is set, the color x is allow to be displayed in current pattern.

Table 20~22 show the registers for each mode, for example, in the Current Level Mode, the current lever register is 10H for OUT1, 21H for OUT2, 32H for OUT3, in Single mode and pattern mode, Pattern 1 has 3 current level registers and enabled/disabled by Cex.

Table 20 Color Register Of Single Mode

Mode		Color Enable	P1 OUT1	P2 OUT2	P3 OUT3
Single Mode	Pattern Mode	CE1	10H	21H	32H
		CE2	13H	24H	35H
		CE3	16H	27H	38H
	Current Level Mode	-	10H	21H	32H

Table 21 Color Register Of RG+W Mode

RG+W Mode	Color Enable	OUT1	OUT2
Pattern 1	CE1(1Ch)	10H	11H
	CE2(1Ch)	13H	14H
	CE3(1Ch)	16H	17H
Pattern 2	CE1(2Ch)	20H	21H
	CE2(2Ch)	23H	24H
	CE3(2Ch)	26H	27H

RG+W Mode	Color Enable	P3 OUT3
Pattern Mode	CE1(3Ch)	32H
	CE2(3Ch)	35H
	CE3(3Ch)	38H
Current Level Mode	-	32H

Table 22 Color Register of RGB Mode

RGB Mode	Color Enable	OUT1	OUT2	OUT3
Pattern 1	CE1(1Ch)	10H	11H	12H
	CE2(1Ch)	13H	14H	15H
	CE3(1Ch)	16H	17H	18H
Pattern 2	CE1(2Ch)	20H	21H	22H
	CE2(2Ch)	23H	24H	25H
	CE3(2Ch)	26H	27H	28H
Pattern 3	CE1(3Ch)	30H	31H	32H
	CE2(3Ch)	33H	34H	35H
	CE3(3Ch)	36H	37H	38H

PATTERN TIME SETTING

User should configure the related pattern time setting registers according to actual timing requirements via I2C interface before starting pattern. There are three groups of pattern time can be set for P1~P3, which including TS, T1~T4 and TP. And each pattern has three continue lighting cycle as Color 1~Color 3. Please check the LED OPERATING MODE section for more about the time setting.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, the device integrates gamma correction to the Pattern Mode. The gamma correction causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3194 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

The IS31FL3194 provides three gamma corrections which can be set by GAM bits of NXT Registers (1Eh/2Eh/3Eh) for each pattern. The gamma correction is shown as below.

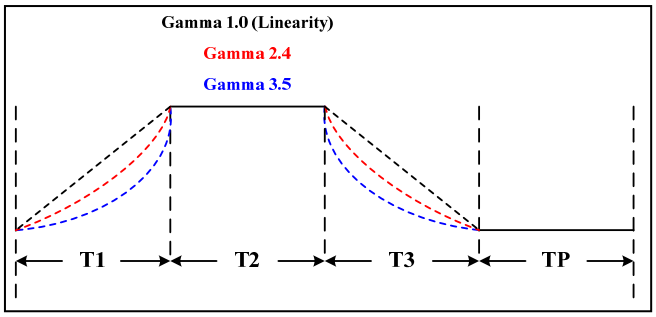


Figure 8 Gamma Correction

LED OPERATING MODE

The IS31FL3194 has three operating modes which can be chosen by the RGB bits of Operating Configure Register (01h).

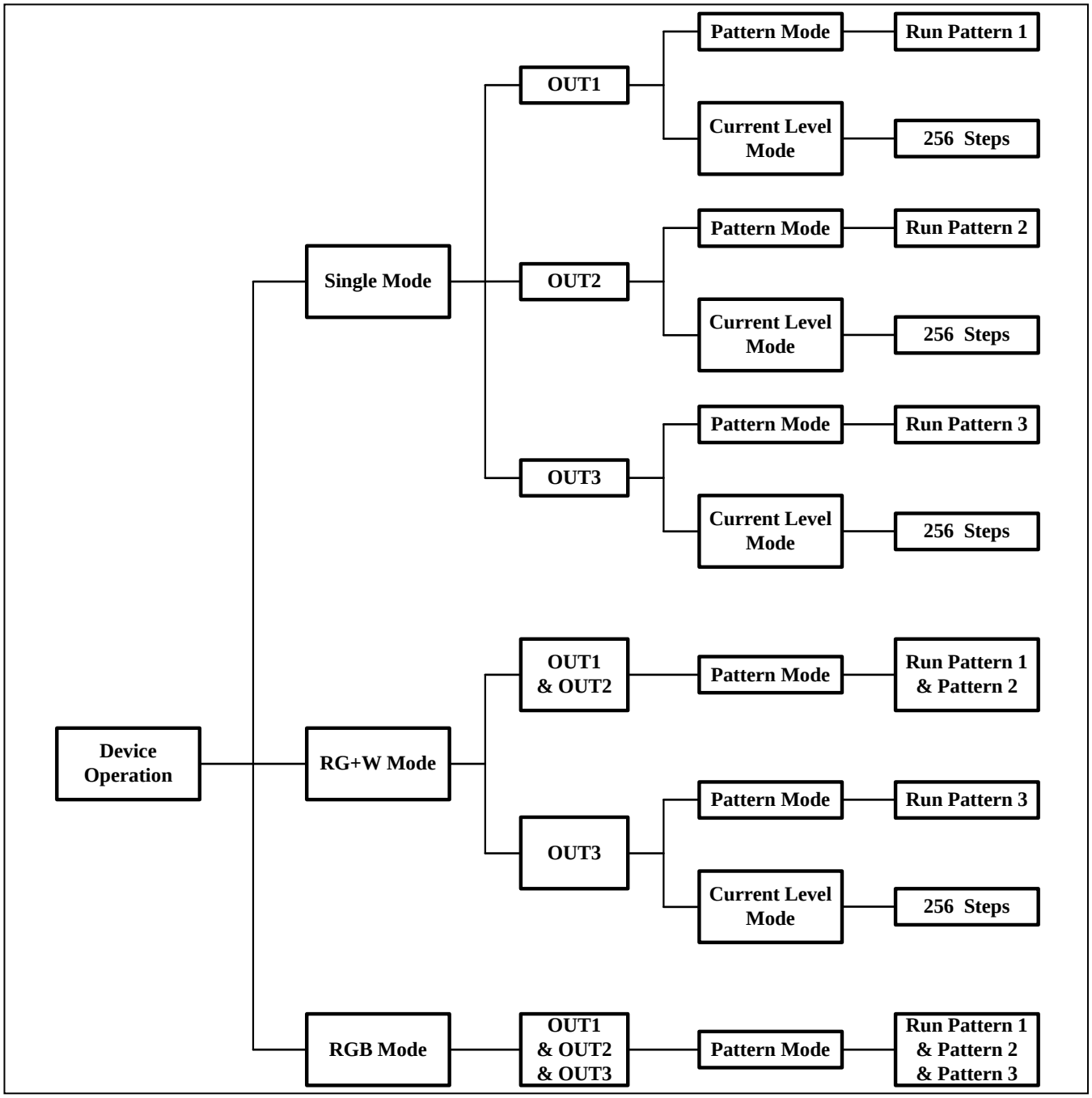


Figure 9 Three Operating Mode Map

Single Mode:

If RGB=00/11 (Single Mode), OUTx runs Px independently in Pattern Mode or operates in Current Level Mode.

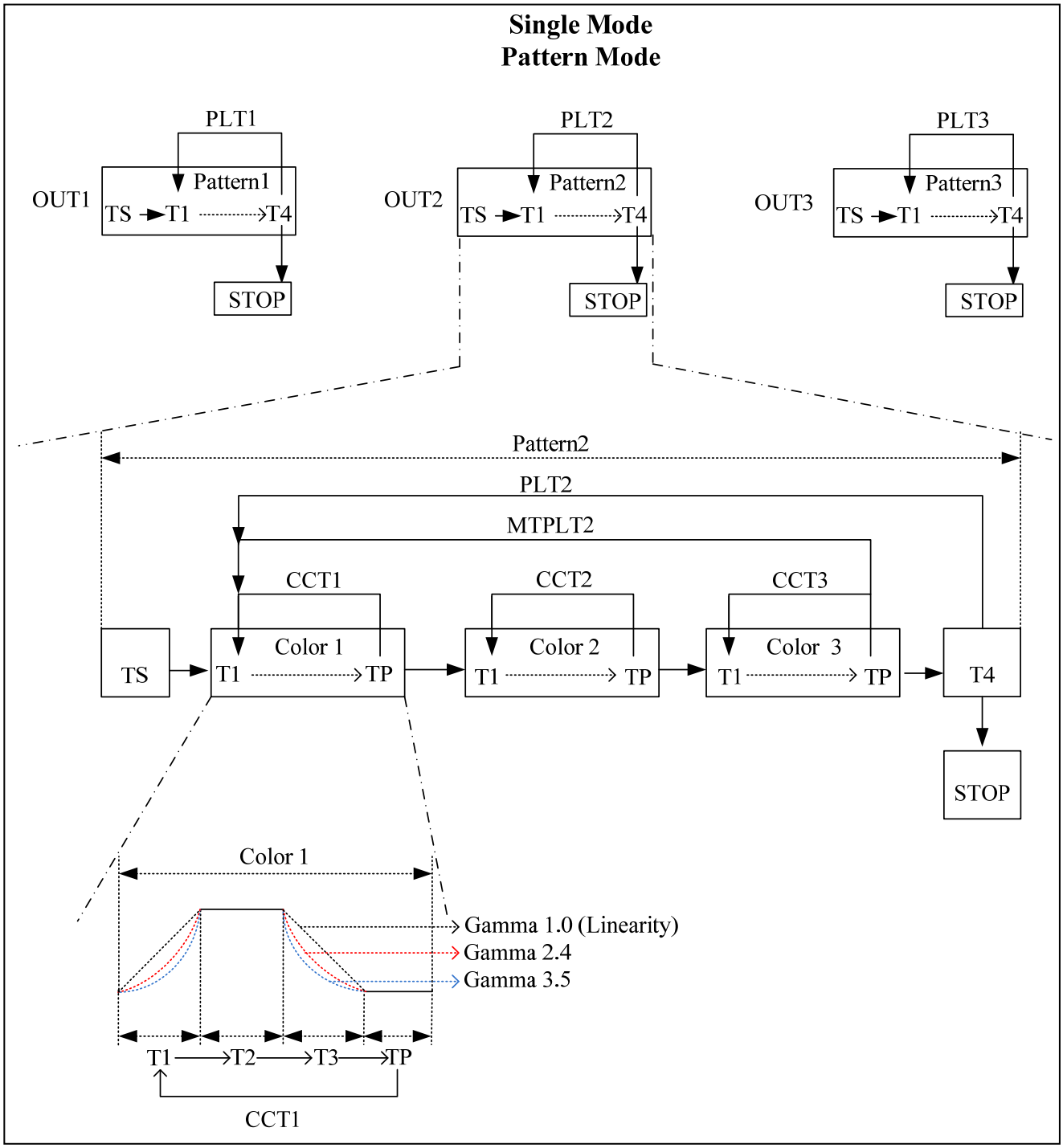


Figure 10 Single Mode

RG+W Mode:

If RGB=01 (RG+W Mode), OUT1 and OUT2 can operate in Pattern Mode only and run in the same pattern (P1~P2). OUT3 can be both mode and run in Pattern 3 independently. OUT1 and OUT2 bits can't be set.

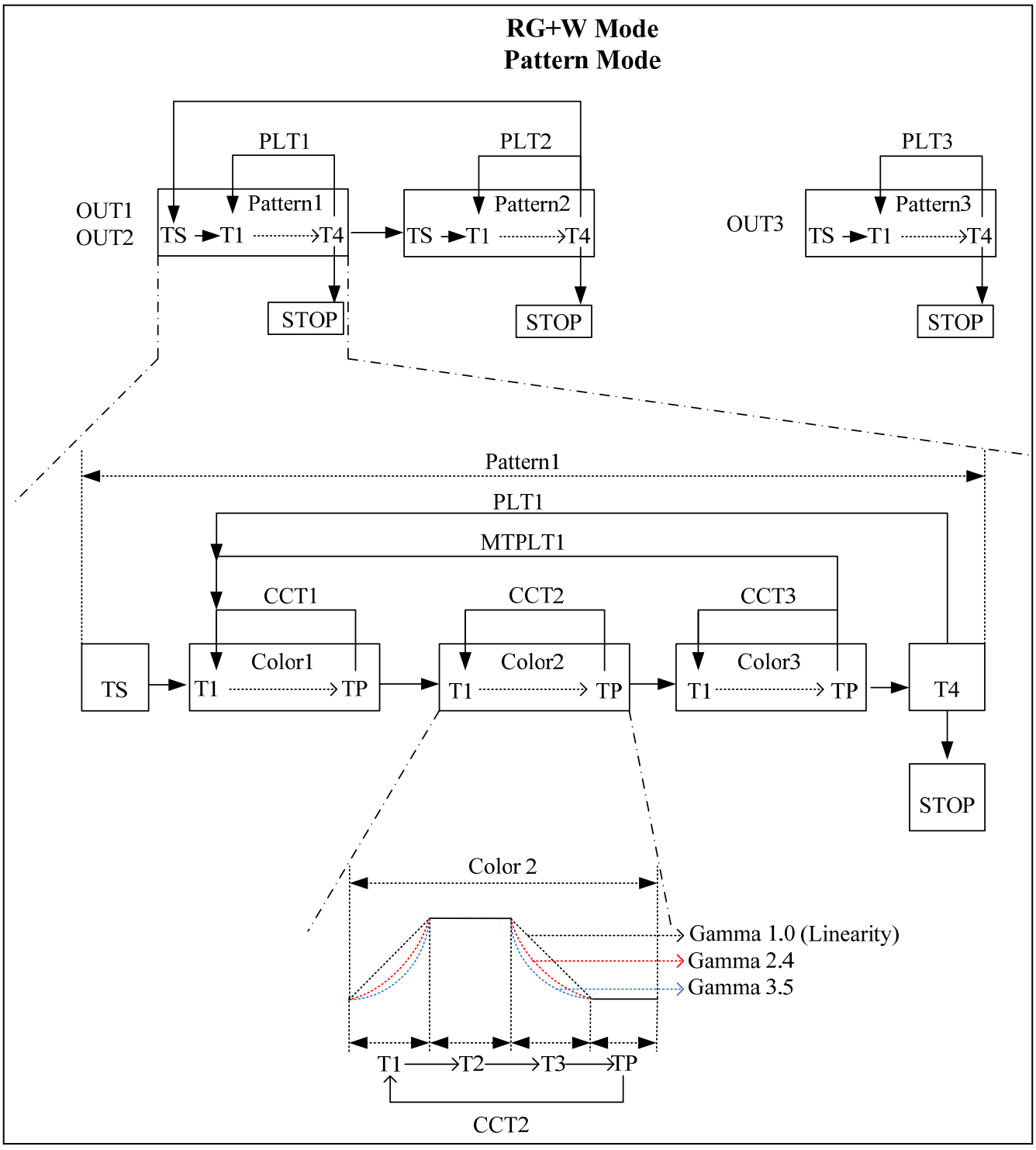


Figure 11 RG+W Mode

RGB Mode:

If RGB=10 (RGB Mode), OUT1~OUT3 can operate in Pattern Mode only and run in the same pattern (P1~P3). OUTx bit can't be set.

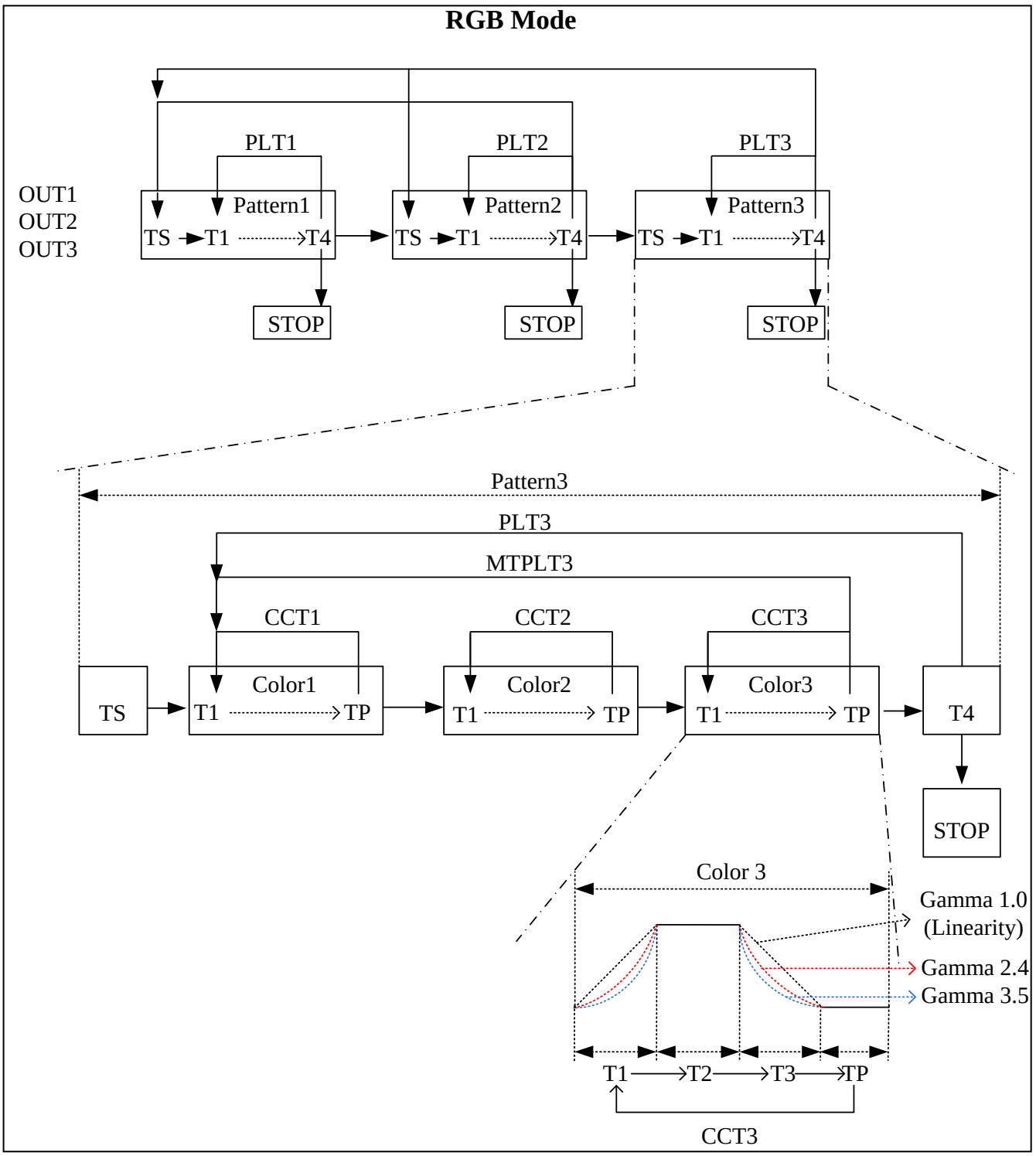


Figure 12 RGB Mode

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

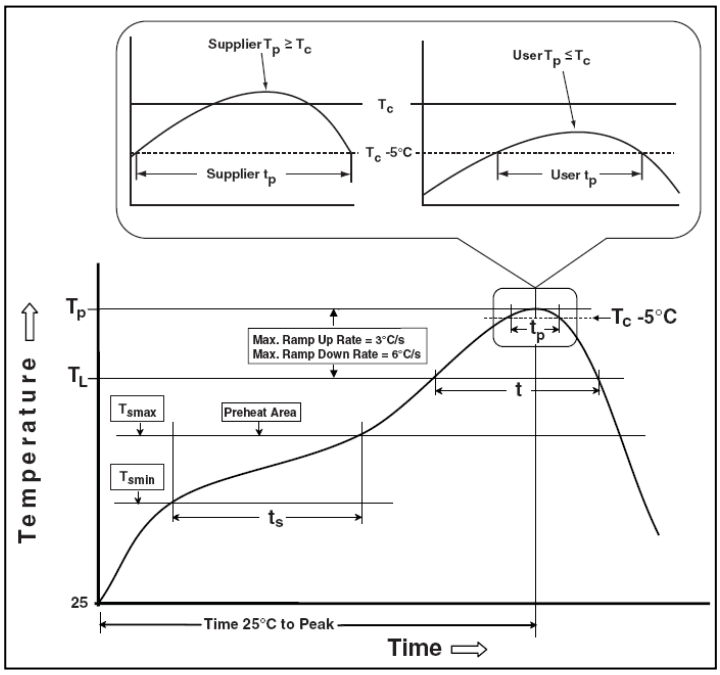
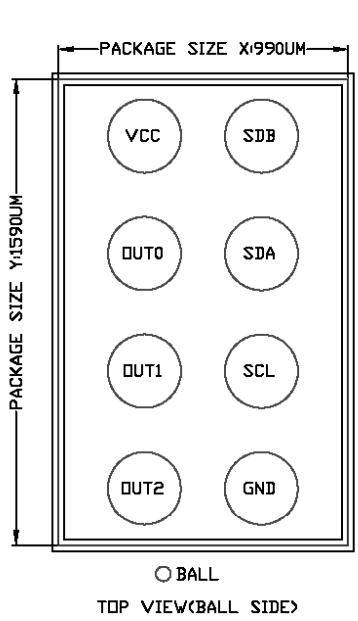
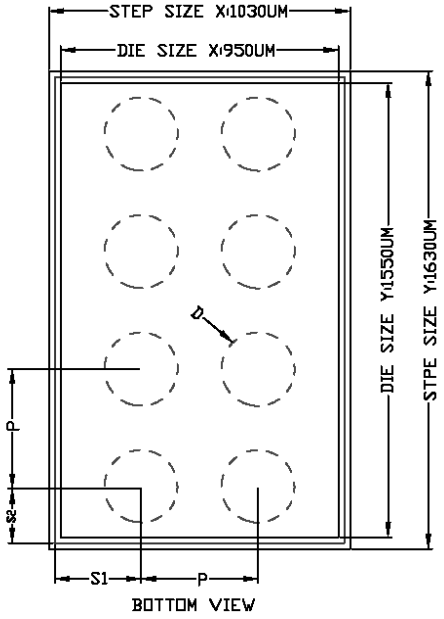


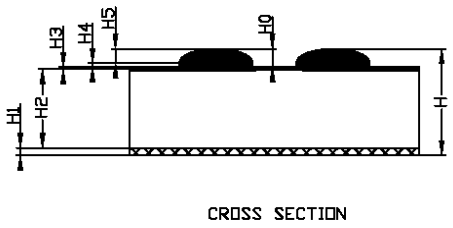
Figure 13 Classification Profile

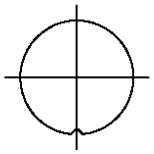
PACKAGE INFORMATION

WCSP-8



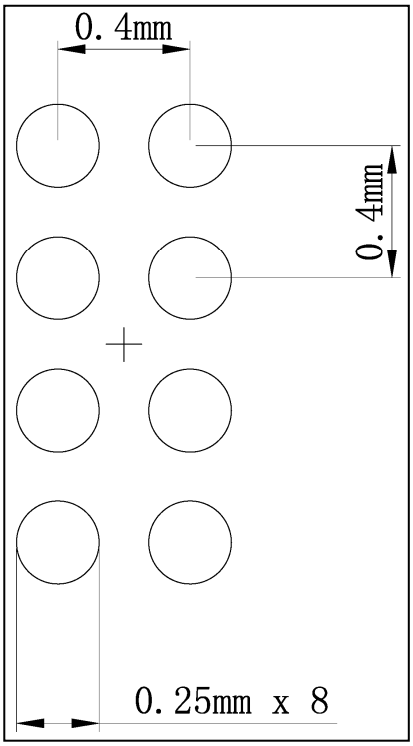






SYMBOL	ITEM	DATA(UM)
A*B	PACKAGE SIZE	990*1590±25
H	PACKAGE HEIGHT	390±31.5
D	BALL DIAMETER	250±25
H0	BALL HEIGHT	60±10
H4	UBM THICKNESS	8
H5	SNAG THICKNESS	52
H3	PI THICKNESS	5±1.5
H2	SI THICKNESS(AFTER GRINDING)	300±10
H1	BACK COATING THICKNESS	25±10
S1	BALL CENTER TO PACKAGEEDGE X AXIS	295
S2	BALL CENTER TO PACKAGE EDGE Y AXIS	195
P	BALL PITCH	400

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2017.03.02
A	Update to final version	2017.07.04
B	1. Update title 2. Add package size 3. Add description for 43h register	2017.08.04