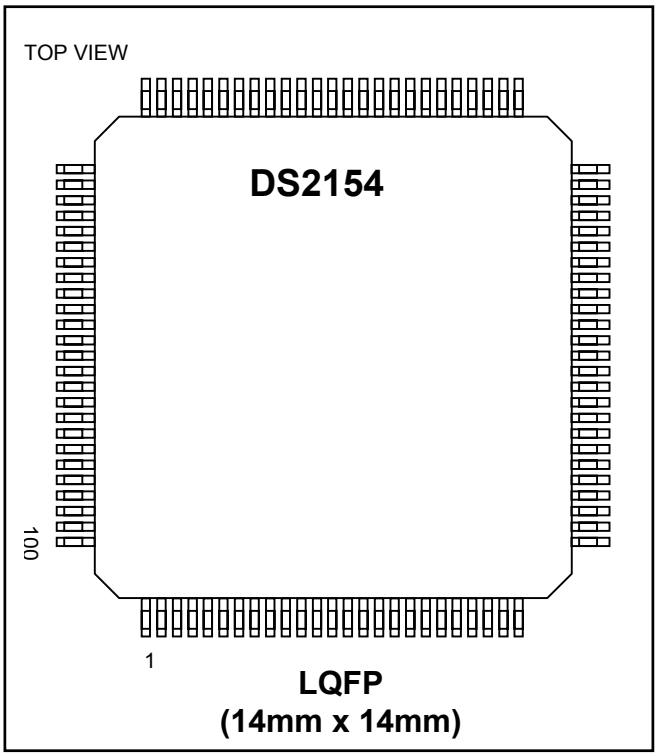
DS2154
Enhanced E1 Single-Chip Transceiver

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FEATURES

- Complete E1 (CEPT) PCM-30/ISDN-PRI Transceiver Functionality
- On-Board Long- and Short-Haul Line Interface for Clock/Data Recovery and Waveshaping
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator
- Generates Line Build-Outs for Both 120Ω and 75Ω Lines
- Frames to FAS, CAS, and CRC4 Formats
- Dual On-Board Two-Frame Elastic Store Slip Buffers That can Connect to Asynchronous Backplanes Up to 8.192MHz
- 8-Bit Parallel Control Port That can be Used Directly on Either Multiplexed or Nonmultiplexed Buses (Intel or Motorola)
- Extracts and Inserts CAS Signaling
- Detects and Generates Remote and AIS Alarms
- Programmable Output Clocks for Fractional E1, H0, and H12 Applications
- Fully Independent Transmit and Receive Functionality
- Full Access to Both Si and Sa Bits Aligned with CRC Multiframe
- Four Separate Loopbacks for Testing Functions
- Large Counters for Bipolar and Code Violations, CRC4 Codeword Errors, FAS Errors, and E Bits
- Pin Compatible with DS2152 T1 Enhanced Single-Chip Transceiver
- 5V Supply; Low-Power CMOS
- 100-Pin, 14mm^2 LQFP Package

PIN CONFIGURATION



ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2154L	0°C to +70°C	100 LQFP
DS2154L+	0°C to +70°C	100 LQFP
DS2154LN	-40°C to +85°C	100 LQFP
DS2154LN+	-40°C to +85°C	100 LQFP

+*Denotes lead-free/RoHS-compliant package.*

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1 DETAILED DESCRIPTION

The DS2154 enhanced single-chip transceiver (SCT) contains all the necessary functions for connection to E1 lines. The device is an upward compatible version of the DS2153 single-chip transceiver. The on-board clock/data recovery circuitry coverts the AMI/HDB3 E1 waveforms to an NRZ serial stream. The DS2154 automatically adjusts to E1 22 AWG (0.6mm) twisted-pair cables from 0 to over 2km in length. The device can generate the necessary G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The on-board jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, Si, and Sa bit information. The device contains a set of internal registers that the user can access to control the operation of the unit. Quick access via the parallel control port allows a single controller to handle many E1 lines. The device fully meets all the latest E1 specifications including ITU G.703, G.704, G.706, G.823, G.932, and I.431 as well as ETS 300 011, 300 233, 300 166, TBR 12 and TBR 13.

1.1 Introduction

The DS2154 is a superset version of the popular DS2153Q E1 single-chip transceiver offering the new features listed below. All the original features of the DS2153Q have been retained and software created for the original devices is transferable into the DS2154.

1.1.1 New Features

- Option for nonmultiplexed bus operation
- Crystal-less jitter attenuation
- Additional hardware signaling capability including:
  - Receive signaling reinsertion to a backplane multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
  - Interrupt generated on change of signaling data
- Improved receive sensitivity: 0dB to -43dB
- Per-channel code insertion in both transmit and receive paths
- Expanded access to Sa and Si bits
- RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state
- 8.192MHz clock synthesizer
- Per-channel loopback
- Addition of hardware pins to indicate carrier loss and signaling freeze
- Line interface function can be completely decoupled from the framer/formatter to allow:
  - Interface to optical, HDSL, and other NRZ interfaces
  - Ability to “tap” the transmit and receive bipolar data streams for monitoring purposes
  - Ability to corrupt data and insert framing errors, CRC errors, etc.
- Transmit and receive elastic stores now have independent backplane clocks
- Ability to monitor one DS0 channel in both the transmit and receive paths
- Access to the data streams in between the framer/formatter and the elastic stores
- AIS generation in the line interface that is independent of loopbacks
- Transmit current limiter to meet the 50mA short circuit requirement
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Automatic RAI generation to ETS 300 011 specifications

1.2 Functional Description

The analog AMI/HDB3 waveform off the E1 line is transformer-coupled into the RRING and RTIP pins of the DS2154. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing/multiframe pattern. The DS2154 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0dB to -43dB, which allows the device to operate on cables over 2km in length. The receive side framer locates the FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms, including carrier loss, loss of synchronization, AIS, and remote alarm. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock that is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048MHz clock or a 1.544MHz clock. The RSYSCLK can be a bursty clock with speeds up to 8.192MHz.

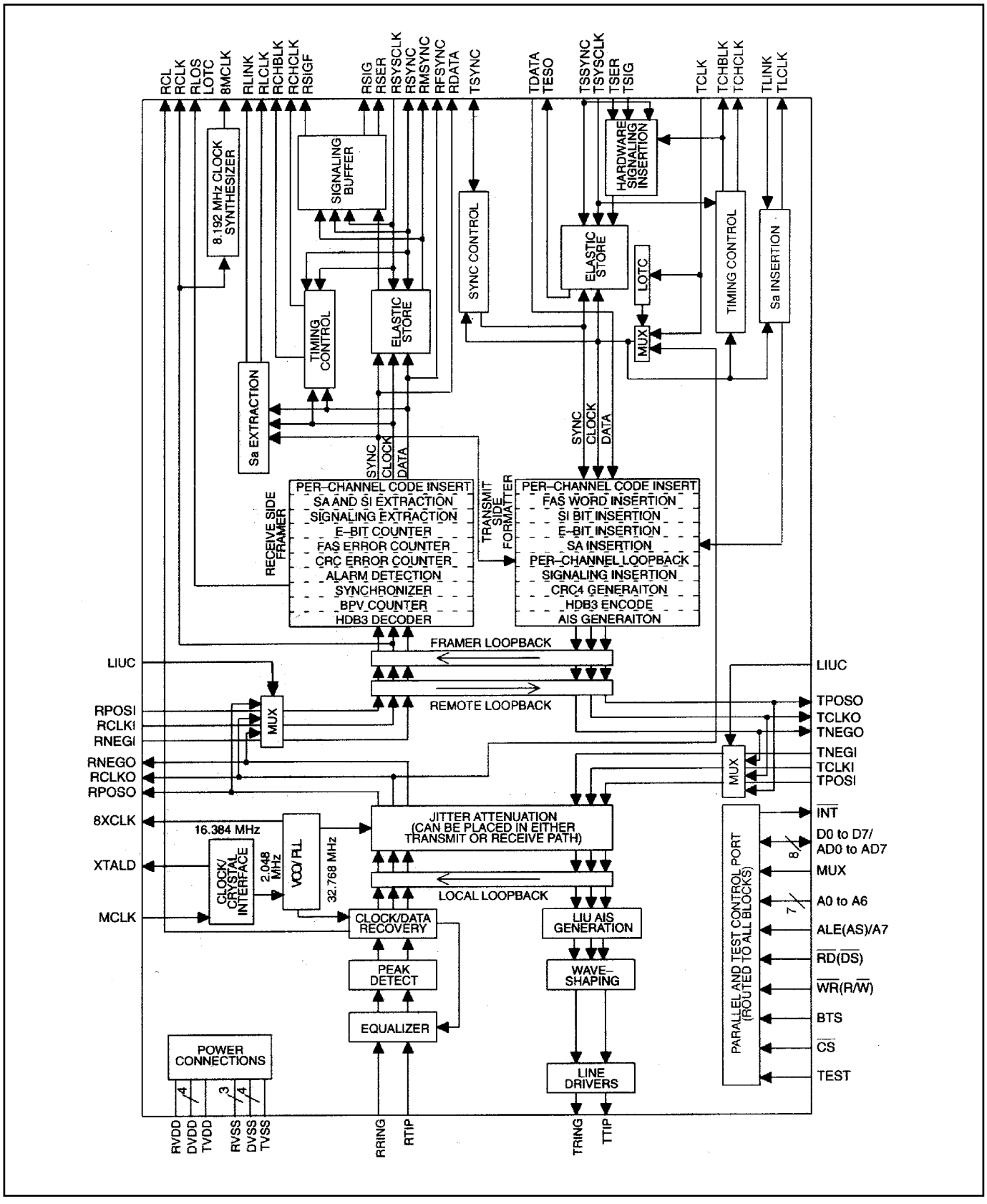
The transmit side of the DS2154 is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for E1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2154 will drive the E1 line from the TTIP and TRING pins via a coupling transformer. The line driver contains a current limiter that restricts the maximum current into a 1Ω load to less than 50mA (RMS).

1.3 Reader's Note

This data sheet assumes a particular nomenclature of the E1 operating environment. There are 32 8-bit time slots in an E1 system numbered 0 to 31. Time slot 0 is transmitted first and received first. These 32 time slots are also referred to as channels with a numbering scheme of 1 to 32. Time slot 0 is identical to channel 1, time slot 1 is identical to Channel 2, and so on. Each time slot (or channel) is made up of 8 bits numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations are used:

FAS	Frame Alignment Signal
CRC4	Cyclical Redundancy Check
CCS	Common Channel Signaling
CAS	Channel Associated Signaling
MF	Multiframe
Sa	Additional Bits
Si	International Bits
E-Bit	CRC4 Error Bits

Figure 1-1. DS2154 Enhanced E1 Single-Chip Transceiver



2 PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	RCHBLK	O	Receive Channel Block
2, 4, 5, 7–10, 15, 23, 26, 27, 28, 36, 54, 76	N.C.	—	No Connection. These pins should be left open circuited.
3	8MCLK	O	8.192MHz Clock
6	RCL	O	Receive Carrier Loss
11	BTS	I	Bus Type Select
12	LIUC	I	Line Interface Connect
13	8XCLK	O	Eight Times Clock
14	TEST	I	Test
16	RTIP	I	Receive Analog Tip Input
17	RRING	I	Receive Analog Ring Input
18	RVDD	—	Receive Analog Positive Supply
19, 20, 24	RVSS	—	Receive Analog Signal Ground
21	MCLK	I	Master Clock Input
22	XTALD	O	Quartz Crystal Driver
25	$\overline{\text{INT}}$	O	Active-Low Interrupt
29	TTIP	O	Transmit Analog Tip Output
30	TVSS	—	Transmit Analog Signal Ground
31	TVDD	—	Transmit Analog Positive Supply
32	TRING	O	Transmit Analog Ring Output
33	TCHBLK	O	Transmit Channel Block
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
37	TSYNC	I/O	Transmit Sync
38	TPOSI	I	Transmit Positive Data Input
39	TNEGI	I	Transmit Negative Data Input
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
42	TNEGO	O	Transmit Negative Data Output
43	TPOSO	O	Transmit Positive Data Output
44, 61, 81, 83	DVDD	—	Digital Positive Supply
45, 60, 80, 84	DVSS	—	Digital Signal Ground
46	TCLK	I	Transmit Clock
47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input
49	TESO	O	Transmit Elastic Store Output
50	TDATA	I	Transmit Data
51	TSYSCLK	I	Transmit System Clock
52	TSSYNC	I	Transmit System Sync
53	TCHCLK	O	Transmit Channel Clock
55	MUX	I	Bus Operation
56	D0/AD0	I/O	Data Bus Bit 0/Address/Data Bus Bit 0

PIN	NAME	TYPE	FUNCTION
57	D1/AD1	I/O	Data Bus Bit 1/Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus Bit 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
62	D4/AD4	I/O	Data Bus Bit 4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
66–72	A0–A6	I	Address Bus Bit 0
73	A7/ALE	I	Address Bus Bit 7/Address Latch Enable
74	$\overline{RD}(\overline{DS})$	I	Active-Low Read Input (Data Strobe)
75	$\overline{CS}$	I	Active-Low Chip Select
77	$\overline{WR}(R/\overline{W})$	I	Active-Low Write Input (Read/Write)
78	RLINK	O	Receive Link Data
79	RLKCLK	O	Receive Link Clock
82	RCLK	O	Receive Clock
85	RDATA	O	Receive Data
86	RPOSI	I	Receive Positive Data Input
87	RNEGI	I	Receive Negative Data Input
88	RCLKI	I	Receive Clock Input
89	RCLKO	O	Receive Clock Output
90	RNEGO	O	Receive Negative Data Output
91	RPOSO	O	Receive Positive Data Output
92	RCHCLK	O	Receive Channel Clock
93	RSIGF	O	Receive Signaling Freeze Output
94	RSIG	O	Receive Signaling Output
95	RSER	O	Receive Serial Data
96	RMSYNC	O	Receive Multiframe Sync
97	RFSYNC	O	Receive Frame Sync
98	RSYNC	I/O	Receive Sync
99	RLOS/LOTC	O	Receive Loss of Sync/Loss of Transmit Clock
100	RSYSCLK	I	Receive System Clock

2.1 Transmit Side Digital Pins

PIN	NAME	FUNCTION
46	TCLK	**Transmit Clock.** A 2.048MHz primary clock. Used to clock data through the transmit side formatter. Must be present for the parallel control port to operate properly. If not present, the Loss of Transmit Clock (LOTC) function can provide a clock.
47	TSER	**Transmit Serial Data.** Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
53	TCHCLK	**Transmit Channel Clock.** A 256kHz clock that pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data.
33	TCHBLK	**Transmit Channel Block.** A user-programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384kbps (H0), 768kbps, 1920kbps (H12), or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 10 for details.
51	TSYSCLK	**Transmit System Clock.** 1.544MHz or 2.048MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store. Can be burst at rates up to 8.192MHz.
34	TLCLK	**Transmit Link Clock.** 4 kHz or 20kHz demand clock (Sa bits) for the TLINK input. See Section 12 for details.
35	TLINK	**Transmit Link Data.** If enabled, this pin will be sampled on the falling edge of TCLK for data insertion into any combination of the Sa bit positions (Sa4 to Sa8). See Section 12 for details.
37	TSYNC	**Transmit Sync.** A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. This pin can also be programmed to output either a frame or multiframe pulse. It is always synchronous with TCLK. See Section 14 for details.
52	TSSYNC	**Transmit System Sync.** Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit side elastic store. Always synchronous with TSYSCLK.
48	TSIG	**Transmit Signaling Input.** When enabled, this input will sample signaling bits for insertion into outgoing PCM E1 data stream. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled. See Section 14 for details.
49	TESO	**Transmit Elastic Store Data Output.** Updated on the rising edge of TCLK with data out of the transmit side elastic store whether the elastic store is enabled or not. This pin is normally tied to TDATA.
50	TDATA	**Transmit Data.** Sampled on the falling edge of TCLK with data to be clocked through the transmit side formatter. This pin is normally tied to TESO.
43	TPOSO	**Transmit Positive Data Output.** Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the Output Data Format (TCR1.7) control bit. This pin is normally tied to TPOSI.
42	TNEGO	**Transmit Negative Data Output.** Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. This pin is normally tied to TNEGI.
41	TCLKO	**Transmit Clock Output.** Buffered clock that is used to clock data through the transmit side formatter (i.e., either TCLK or RCLKO if Loss of Transmit Clock is enabled and in effect, or RCLKI if remote loopback is enabled). This pin is normally tied to TCLKI.

PIN	NAME	FUNCTION
38	TPOSI	**Transmit Positive Data Input.** Sampled on the falling edge of TCLKI for data to be transmitted out onto the E1 line. Can be internally connected to TPOSO by tying the LIUC pin high.
39	TNEGI	**Transmit Negative Data Input.** Sampled on the falling edge of TCLKI for data to be transmitted out onto the E1 line. Can be internally connected to TNEGO by tying the LIUC pin high.
40	TCLKI	**Transmit Clock Input.** Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC pin high.

2.2 Receive Side Digital Pins

PIN	NAME	FUNCTION
78	RLINK	**Receive Link Data.** Updated with the full recovered E1 datastream on the rising edge of RCLK.
79	RLCLK	**Receive Link Clock.** A 4kHz to 20kHz clock (Sa bits) for the RLINK output. See Section 12 for details.
82	RCLK	**Receive Clock.** 2.048MHz clock that is used to clock data through the receive side framer.
92	RCHCLK	**Receive Channel Clock.** A 256kHz clock that pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data.
1	RCHBLK	**Receive Channel Block.** A user-programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used, such as Fractional E1, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 10 for details.
95	RSER	**Receive Serial Data.** Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.
98	RSYNC	**Receive Sync.** An extracted pulse, one RCLK wide, is output at this pin, which identifies either frame or CAS/CRC4 multiframe boundaries. If the receive side elastic store is enabled, then this pin can be enabled to be an input at which a frame or multiframe boundary pulse synchronous with RSYSCLK is applied.
97	RFSYNC	**Receive Frame Sync.** An extracted 8kHz pulse, one RCLK wide, is output at this pin that identifies frame boundaries.
96	RMSYNC	**Receive Multiframe Sync.** An extracted pulse, one RSYSCLK wide, is output at this pin, which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK.
85	RDATA	**Receive Data.** Updated on the rising edge of RCLK with the data out of the receive side framer.
100	RSYSCLK	**Receive System Clock.** 1.544MHz or 2.048MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Can be burst at rates up to 8.192MHz.
94	RSIG	**Receive Signaling Output.** Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled. See Section 14.
99	RLOS/LOTC	**Receive Loss of Sync/Loss of Transmit Clock.** A dual function output that is

PIN	NAME	FUNCTION
		controlled by the TCR2.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs.
6	RCL	**Receive Carrier Loss.** Set high when the line interface detects a loss of carrier. Note: A test mode exists to allow the DS2154 to detect carrier loss at RPOSI and RNEGI in place of detection at RTIP and RRING.
93	RSIGF	**Receive Signaling Freeze.** Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.
3	8MCLK	**8MHz Clock.** A 8.192MHz output clock that is referenced to the clock that is output at the RCLK pin.
91	RPOSO	**Receive Positive Data Output.** Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RPOSI.
90	RNEGO	**Receive Negative Data Output.** Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RNEGI.
89	RCLKO	**Receive Clock Output.** Buffered recovered clock from the E1 line. This pin is normally tied to RCLKI.
86	RPOSI	**Receive Positive Data Input.** Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC pin high.
87	RNEGI	**Receive Negative Data Input.** Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC pin high.
88	RCLKI	**Receive Clock Input.** Clock used to clock data through the receive side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC pin high. RCLKI must be present for the parallel control port to operate properly.

2.3 Parallel Control Port Pins

PIN	NAME	FUNCTION
25	$\overline{\text{INT}}$	**Interrupt.** Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2. Active-low, open-drain output.
14	TEST	**Tri-State Control.** Set high to tri-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.
55	MUX	**Bus Operation.** Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation.
56–65	D0–D7/ AD0–AD7	**Data Bus or Address/Data Bus.** In nonmultiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as an 8-bit multiplexed address/data bus.
66–72	A0–A6	**Address Bus.** In nonmultiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.
11	BTS	**Bus Type Select.** Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{\text{RD}}$ ($\overline{\text{DS}}$), ALE(AS), and $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) pins. If BTS = 1, then these pins assume the function listed in parentheses.
74	$\overline{\text{RD}}$($\overline{\text{DS}}$)	**Read Input (Data Strobe).** $\overline{\text{RD}}$ and $\overline{\text{DS}}$ are active-low signals when MUX = 1. DS is active high when MUX = 0. See the bus timing diagrams.
75	$\overline{\text{CS}}$	**Chip Select.** Must be low to read or write to the device. $\overline{\text{CS}}$ is an active-low signal.
73	ALE(AS)	**A7 or Address Latch Enable (Address Strobe).** In nonmultiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive-going edge.
77	$\overline{\text{WR}}$(R/$\overline{\text{W}}$)	**Write Input (Read/Write).** $\overline{\text{WR}}$ is an active-low signal.

2.4 Line Interface Pins

PIN	NAME	FUNCTION
21	MCLK	**Master Clock Input.** A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A quartz crystal of 2.048MHz may be applied across MCLK and XTALD instead of the TTL level clock source.
22	XTALD	**Quartz Crystal Driver.** A quartz crystal of 2.048MHz may be applied across MCLK and XTALD instead of a TTL level clock source at MCLK. Leave open circuited if a TTL clock source is applied at MCLK.
13	8XCLK	**Eight Times Clock**. A 16.384MHz clock that is frequency locked to the 2.048MHz clock provided from the clock/data recovery block (if the jitter attenuator is enabled on the receive side) or from the TCLKI pin (if the jitter attenuator is enabled on the transmit side). Can be internally disabled via the TEST2 register if not needed.
12	LIUC	**Line Interface Connect.** Tie low to separate the line interface circuitry from the framer/formatter circuitry and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/ RCLKI pins. Tie high to connect the line interface circuitry to the framer/formatter circuitry and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. When LIUC is tied high, the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins should be tied low.
16, 17	RTIP, RRING	**Receive Tip and Ring.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the E1 line. See Section 13 for details.
29, 32	TTIP, TRING	**Transmit Tip and Ring.** Analog line driver outputs. These pins connect via a 1:1.15 or 1:1.36 step-up transformer to the E1 line. See Section 13 for details.

2.5 Supply Pins

PIN	NAME	FUNCTION
44, 61, 81, 83	DVDD	**Digital Positive Supply.** 5.0V ±5%. Should be tied to the RVDD and TVDD pins.
18	RVDD	**Receive Analog Positive Supply.** 5.0V ±5%. Should be tied to the DVDD and TVDD pins.
31	TVDD	**Transmit Analog Positive Supply.** 5.0V ±5%. Should be tied to the RVDD and DVDD pins.
45, 60, 80, 84	DVSS	**Digital Signal Ground.** Should be tied to the RVSS and TVSS pins.
19, 20, 24	RVSS	**Receive Analog Signal Ground.** 0V. Should be tied to the DVSS and TVSS pins.
30	TVSS	**Transmit Analog Ground.** 0V. Should be tied to the RVSS and DVSS pins.

Table 2-1. Register Map

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
00	R	BPV or Code Violation Count 1	VCR1
01	R	BPV or Code Violation Count 2	VCR2
02	R	CRC4 Error Count 1/FAS Error Count 1	CRCCR1
03	R	CRC4 Error Count 2	CRCCR2
04	R	E-Bit Count 1/FAS Error Count 2	EBCR1
05	R	E-Bit Count 2	EBCR2
06	R/W	Status 1	SR1
07	R/W	Status 2	SR2
08	R/W	Receive Information	RIR
09, 0A–0E, 1D	—	Not Present	—
0F	R	Device ID Register	IDR
10	R/W	Receive Control 1	RCR1
11	R/W	Receive Control 2	RCR2
12	R/W	Transmit Control 1	TCR1
13	R/W	Transmit Control 2	TCR2
14	R/W	Common Control 1	CCR1
15	R/W	Test 1	TEST1 (set to 00h)
16	R/W	Interrupt Mask 1	IMR1
17	R/W	Interrupt Mask 2	IMR2
18	R/W	Line Interface Control	LICR
19	R/W	Test 2	TEST2 (set to 00h)
1A	R/W	Common Control 2	CCR2
1B	R/W	Common Control	CCR3
1C	R/W	Transmit Sa Bit Control	TSaCR
1E	R	Synchronizer Status	SSR
1F	R	Receive Non-Align Frame	RNAF
20	R/W	Transmit Align Frame	TAF
21	R/W	Transmit Non-Align Frame	TNAF
22	R/W	Transmit Channel Blocking 1	TCBR1
23	R/W	Transmit Channel Blocking 2	TCBR2
24	R/W	Transmit Channel Blocking 3	TCBR3
25	R/W	Transmit Channel Blocking 4	TCBR4
26	R/W	Transmit Idle 1	TIR1
27	R/W	Transmit Idle 2	TIR2
28	R/W	Transmit Idle 3	TIR3
29	R/W	Transmit Idle 4	TIR4

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
2A	R/W	Transmit Idle Definition	TIDR
2B	R/W	Receive Channel Blocking 1	RCBR1
2C	R/W	Receive Channel Blocking 2	RCBR2
2D	R/W	Receive Channel Blocking 3	RCBR3
2E	R/W	Receive Channel Blocking 4	RCBR4
2F	R	Receive Align Frame	RAF
30	R	Receive Signaling 1	RS1
31	R	Receive Signaling 2	RS2
32	R	Receive Signaling 3	RS3
33	R	Receive Signaling 4	RS4
34	R	Receive Signaling 5	RS5
35	R	Receive Signaling 6	RS6
36	R	Receive Signaling 7	RS7
37	R	Receive Signaling 8	RS8
38	R	Receive Signaling 9	RS9
39	R	Receive Signaling 10	RS10
3A	R	Receive Signaling 11	RS11
3B	R	Receive Signaling 12	RS12
3C	R	Receive Signaling 13	RS13
3D	R	Receive Signaling 14	RS14
3E	R	Receive Signaling 15	RS15
3F	R	Receive Signaling 16	RS16
40	R/W	Transmit Signaling 1	TS1
41	R/W	Transmit Signaling 2	TS2
42	R/W	Transmit Signaling 3	TS3
43	R/W	Transmit Signaling 4	TS4
44	R/W	Transmit Signaling 5	TS5
45	R/W	Transmit Signaling 6	TS6
46	R/W	Transmit Signaling 7	TS7
47	R/W	Transmit Signaling 8	TS8
48	R/W	Transmit Signaling 9	TS9
49	R/W	Transmit Signaling 10	TS10
4A	R/W	Transmit Signaling 11	TS11
4B	R/W	Transmit Signaling 12	TS12
4C	R/W	Transmit Signaling 13	TS13
4D	R/W	Transmit Signaling 14	TS14
4E	R/W	Transmit Signaling 15	TS15
4F	R/W	Transmit Signaling 16	TS16

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
50	R/W	Transmit Si Bits Align Frame	TSiAF
51	R/W	Transmit Si Bits Non-Align Frame	TSiNAF
52	R/W	Transmit Remote Alarm Bits	TRA
53	R/W	Transmit Sa4 Bits	TSa4
54	R/W	Transmit Sa5 Bits	TSa5
55	R/W	Transmit Sa6 Bits	TSa6
56	R/W	Transmit Sa7 Bits	TSa7
57	R/W	Transmit Sa8 Bits	TSa8
58	R	Receive Si Bits Align Frame	RSiAF
59	R	Receive Si Bits Non-Align Frame	RSiNAF
5A	R	Receive Remote Alarm Bits	RRA
5B	R	Receive Sa4 Bits	RSa4
5C	R	Receive Sa5 Bits	RSa5
5D	R	Receive Sa6 Bits	RSa6
5E	R	Receive Sa7 Bits	RSa7
5F	R	Receive Sa8 Bits	RSa8
60	R/W	Transmit Channel 1	TC1
61	R/W	Transmit Channel 2	TC2
62	R/W	Transmit Channel 3	TC3
63	R/W	Transmit Channel 4	TC4
64	R/W	Transmit Channel 5	TC5
65	R/W	Transmit Channel 6	TC6
66	R/W	Transmit Channel 7	TC7
67	R/W	Transmit Channel 8	TC8
68	R/W	Transmit Channel 9	TC9
69	R/W	Transmit Channel 10	TC10
6A	R/W	Transmit Channel 11	TC11
6B	R/W	Transmit Channel 12	TC12
6C	R/W	Transmit Channel 13	TC13
6D	R/W	Transmit Channel 14	TC14
6E	R/W	Transmit Channel 15	TC15
6F	R/W	Transmit Channel 16	TC16
70	R/W	Transmit Channel 17	TC17
71	R/W	Transmit Channel 18.	TC18
72	R/W	Transmit Channel 19	TC19
73	R/W	Transmit Channel 20	TC20
74	R/W	Transmit Channel 21	TC21
75	R/W	Transmit Channel 22	TC22

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
76	R/W	Transmit Channel 23	TC23
77	R/W	Transmit Channel 24	TC24
78	R/W	Transmit Channel 25	TC25
79	R/W	Transmit Channel 26	TC26
7A	R/W	Transmit Channel 27	TC27
7B	R/W	Transmit Channel 28	TC28
7C	R/W	Transmit Channel 29	TC29
7D	R/W	Transmit Channel 30	TC30
7E	R/W	Transmit Channel 31	TC31
7F	R/W	Transmit Channel 32	TC32
80	R/W	Receive Channel 1	RC1
81	R/W	Receive Channel 2	RC2
82	R/W	Receive Channel 3	RC3
83	R/W	Receive Channel 4	RC4
84	R/W	Receive Channel 5	RC5
85	R/W	Receive Channel 6	RC6
86	R/W	Receive Channel 7	RC7
87	R/W	Receive Channel 8	RC8
88	R/W	Receive Channel 9	RC9
89	R/W	Receive Channel 10	RC10
8A	R/W	Receive Channel 11	RC11
8B	R/W	Receive Channel 12	RC12
8C	R/W	Receive Channel 13	RC13
8D	R/W	Receive Channel 14	RC14
8E	R/W	Receive Channel 15	RC15
8F	R/W	Receive Channel 16	RC16
90	R/W	Receive Channel 17	RC17
91	R/W	Receive Channel 18	RC18
92	R/W	Receive Channel 19	RC19
93	R/W	Receive Channel 20	RC20
94	R/W	Receive Channel 21	RC21
95	R/W	Receive Channel 22	RC22
96	R/W	Receive Channel 23	RC23
97	R/W	Receive Channel 24	RC24
98	R/W	Receive Channel 25	RC25
99	R/W	Receive Channel 26	RC26
9A	R/W	Receive Channel 27	RC27
9B	R/W	Receive Channel 28	RC28

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
9C	R/W	Receive Channel 29	RC29
9D	R/W	Receive Channel 30	RC30
9E	R/W	Receive Channel 31	RC31
9F	R/W	Receive Channel 32	RC32
A0	R/W	Transmit Channel Control 1	TCC1
A1	R/W	Transmit Channel Control 2	TCC2
A2	R/W	Transmit Channel Control 3	TCC3
A3	R/W	Transmit Channel Control 4	TCC4
A4	R/W	Receive Channel Control 1	RCC1
A5	R/W	Receive Channel Control 2	RCC2
A6	R/W	Receive Channel Control 3	RCC3
A7	R/W	Receive Channel Control 4	RCC4
A8	R/W	Common Control 4	CCR4
A9	R	Transmit DS0 Monitor	TDS0M
AA	R/W	Common Control 5	CCR5
AB	R	Receive DS0 Monitor	RDS0M
AC	R/W	Test 3	TEST3 (set to 00h)
AD	R/W	Not Used	(set to 00h)
AE	R/W	Not Used	(set to 00h)
AF	R/W	Not Used	(set to 00h)

Note 1: *Test Registers 1, 2, and 3 are used only by the factory; these registers must be cleared (set to all 0s) on power-up initialization to ensure proper operation.*
Note 2: *Register banks Bxh, Cxh, Dxh, Exh, and Fxh are not accessible.*

3 PARALLEL PORT

The DS2154 is controlled via either a nonmultiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The DS2154 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses. See the timing diagrams in the AC Electrical Characteristics in Section 16 for more details.

4 CONTROL, ID, AND TEST REGISTERS

The operation of the DS2154 is configured via a set of nine control registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2154 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and five Common Control Registers (CCR1 to CCR5). Each of the nine registers is described in this section.

There is a device Identification Register (IDR) at address 0Fh. The MSB of this read-only register is fixed to a 1 indicating that the DS2154 is present. The pin-for-pin compatible T1 version of the DS2154 is the DS2152, which also has an ID register at address 0Fh. The user can read the MSB to determine which chip is present because the MSB is set to 1 in the DS2154, and is set to 0 in the DS2152. The lower 4 bits of the IDR are used to display the die revision of the chip.

The Test Registers at addresses 15, 19, and AC hex are used by the factory in testing the DS2154. On power-up, the Test Registers should be set to 00 hex for the DS2154 to operate properly.

IDR: DEVICE IDENTIFICATION REGISTER (Address = 0F Hex)

(MSB)							(LSB)
T1E1	0	0	0	ID3	ID2	ID1	ID0

SYMBOL	POSITION	NAME AND DESCRIPTION
T1E1	IDR.7	**T1 or E1 Chip Determination Bit.** 0 = T1 chip 1 = E1 chip
ID3	IDR.3	**Chip Revision Bit 3.** MSB of a decimal code that represents the chip revision.
ID2	IDR.1	**Chip Revision Bit 2.**
ID1	IDR.2	**Chip Revision Bit 1.**
ID0	IDR.0	**Chip Revision Bit 0.** LSB of a decimal code that represents the chip revision.

RCR1: RECEIVE CONTROL REGISTER 1 (Address = 10 Hex)

(MSB)							(LSB)
RSMF	RSM	RSIO	—	—	FRC	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
RSMF	RCR1.7	**RSYNC Multiframe Function.** Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6 = 1). 0 = RSYNC outputs CAS multiframe boundaries 1 = RSYNC outputs CRC4 multiframe boundaries
RSM	RCR1.6	**RSYNC Mode Select.** 0 = frame mode (see the timing in Section 14) 1 = multiframe mode (see the timing in Section 14)
RSIO	RCR1.5	**RSYNC I/O Select.** (Note: This bit must be set to 0 when RCR2.1 = 0.) 0 = RSYNC is an output (depends on RCR1.6) 1 = RSYNC is an input (only valid if elastic store enabled)
—	RCR1.4, RCR1.3	**Not Assigned.** Should be set to 0 when written.
FRC	RCR1.2	**Frame Resync Criteria.** 0 = resync if FAS received in error three consecutive times 1 =resync if FAS or bit 2 of non-FAS is received in error three consecutive times
SYNCE	RCR1.1	**Sync Enable.** 0 = auto resync enabled 1 = auto resync disabled
RESYNC	RCR1.0	**Resync.** When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

Table 4-1. Sync/Resync Criteria

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N + 2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate (RCR1.2 = 1) the above criteria is met or three consecutive incorrect bit 2 of non-FAS received	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found and previous time slot 16 contains code other than all 0s	Two consecutive MF alignment words received in error	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address = 11 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	RBCS	RESE	—

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	RCR2.7	**Sa8 Bit Select.** Set to 1 to have RLCLK pulse at the Sa8 bit position; set to 0 to force RLCLK low during Sa8 bit position. See Section 14 for timing details.
Sa7S	RCR2.6	**Sa7 Bit Select.** Set to 1 to have RLCLK pulse at the Sa7 bit position; set to 0 to force RLCLK low during Sa7 bit position. See Section 14 for timing details.
Sa6S	RCR2.5	**Sa6 Bit Select.** Set to 1 to have RLCLK pulse at the Sa6 bit position; set to 0 to force RLCLK low during Sa6 bit position. See Section 14 for timing details.
Sa5S	RCR2.4	**Sa5 Bit Select.** Set to 1 to have RLCLK pulse at the Sa5 bit position; set to 0 to force RLCLK low during Sa5 bit position. See Section 14 for timing details.
Sa4S	RCR2.3	**Sa4 Bit Select.** Set to 1 to have RLCLK pulse at the Sa4 bit position; set to 0 to force RLCLK low during Sa4 bit position. See Section 14 for timing details.
RBCS	RCR2.2	**Receive Side Backplane Clock Select.** 0 = if RSYSCLK is 1.544MHz 1 = if RSYSCLK is 2.048MHz
RESE	RCR2.1	**Receive Side Elastic Store Enable.** 0 = elastic store is bypassed 1 = elastic store is enabled
—	RCR2.0	**Not Assigned.** Should be set to 0 when written.

TCR1: TRANSMIT CONTROL REGISTER 1 (Address = 12 Hex)

(MSB)							(LSB)
ODF	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOL	POSITION	NAME AND DESCRIPTION
ODF	TCR1.7	**Output Data Format.** 0 = bipolar data at TPOSO and TNEGO 1 = NRZ data at TPOSO; TNEGO = 0
TFPT	TCR1.6	**Transmit Time Slot 0 Pass Through.** 0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1 = FAS bits/Sa bits/Remote Alarm sourced from TSER
T16S	TCR1.5	**Transmit Time Slot 16 Data Select.** 0 = sample time slot 16 at TSER pin 1 = source time slot 16 from TS0 to TS15 registers
TUA1	TCR1.4	**Transmit Unframed All 1s.** 0 = transmit data normally 1 = transmit an unframed all 1's code at TPOSO and TNEGO
TSiS	TCR1.3	**Transmit International Bit Select.** 0 = sample Si bits at TSER pin 1 = source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)
TSA1	TCR1.2	**Transmit Signaling All 1s.** 0 = normal operation 1 = force time slot 16 in every frame to all 1s
TSM	TCR1.1	**TSYNC Mode Select**. 0 = frame mode (see the timing in Section 14) 1 = CAS and CRC4 multiframe mode (see the timing in Section 14)
TSIO	TCR1.0	**TSYNC I/O Select.** 0 = TSYNC is an input 1 = TSYNC is an output

Note: See Figure 14-11 for more details about how the Transmit Control Registers affect the operation of the DS2154.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address = 13 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	ODM	AEBE	PF

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	**Sa8 Bit Select.** Set to 1 to source the Sa8 bit from the TLINK pin; set to 0 to not source the Sa8 bit. See Section 14 for timing details.
Sa7S	TCR2.6	**Sa7 Bit Select.** Set to 1 to source the Sa7 bit from the TLINK pin; set to 0 to not source the Sa7 bit. See Section 14 for timing details.
Sa6S	TCR2.5	**Sa6 Bit Select.** Set to 1 to source the Sa6 bit from the TLINK pin; set to 0 to not source the Sa6 bit. See Section 14 for timing details.
Sa5S	TCR2.4	**Sa5 Bit Select**. Set to 1 to source the Sa5 bit from the TLINK pin; set to 0 to not source the Sa5 bit. See Section 14 for timing details.
Sa4S	TCR2.3	**Sa4 Bit Select.** Set to 1 to source the Sa4 bit from the TLINK pin; set to 0 to not source the Sa4 bit. See Section 14 for timing details.
ODM	TCR2.2	**Output Data Mode.** 0 = pulses at TPOSO and TNEGO are one full TCLKO period wide 1 = pulses at TPOSO and TNEGO are 1/2 TCLKO period wide
AEBE	TCR2.1	**Automatic E-Bit Enable.** 0 = E-bits not automatically set in the transmit direction 1 = E-bits automatically set in the transmit direction
PF	TCR2.0	**Function of RLOS/LOTC Pin.** 0 = Receive Loss of Sync (RLOS) 1 = Loss of Transmit Clock (LOTC)

CCR1: COMMON CONTROL REGISTER 1 (Address = 14 Hex)

(MSB)							(LSB)
FLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOL	POSITION	NAME AND DESCRIPTION
FLB	CCR1.7	**Framer Loopback.** 0 = loopback disabled 1 =loopback enabled
THDB3	CCR1.6	**Transmit HDB3 Enable.** 0 = HDB3 disabled 1 = HDB3 enabled
TG802	CCR1.5	**Transmit G.802 Enable.** See Section 14 for details. 0 = do not force TCHBLK high during bit 1 of time slot 26 1 = force TCHBLK high during bit 1 of time slot 26
TCRC4	CCR1.4	**Transmit CRC4 Enable.** 0 = CRC4 disabled 1 = CRC4 enabled
RSM	CCR1.3	**Receive Signaling Mode Select.** 0 = CAS signaling mode 1 = CCS signaling mode
RHDB3	CCR1.2	**Receive HDB3 Enable.** 0 = HDB3 disabled 1 = HDB3 enabled
RG802	CCR1.1	**Receive G.802 Enable.** See Section 14 for details. 0 = do not force RCHBLK high during bit 1 of time slot 26 1 = force RCHBLK high during bit 1 of time slot 26
RCRC4	CCR1.0	**Receive CRC4 Enable.** 0 = CRC4 disabled 1 = CRC4 enabled

CCR2: COMMON CONTROL REGISTER 2 (Address = 1A Hex)

(MSB)							(LSB)
ECUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	RFF	RFE

SYMBOL	POSITION	NAME AND DESCRIPTION
ECUS	CCR2.7	**Error Counter Update Select.** See Section 6 for details. 0 = update error counters once a second 1 = update error counters every 62.5ms (500 frames)
VCRFS	CCR2.6	**VCR Function Select.** See Section 6 for details. 0 = count Bipolar Violations (BPVs) 1 = count Code Violations (CVs)
AAIS	CCR2.5	**Automatic AIS Generation.** 0 = disabled 1 = enabled
ARA	CCR2.4	**Automatic Remote Alarm Generation.** 0 = disabled 1 = enabled
RSERC	CCR2.3	**RSER Control.** 0 = allow RSER to output data as received under all conditions 1 = force RSER to 1 under loss of frame alignment conditions
LOTCMC	CCR2.2	**Loss of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to the ever-present RCLKO if the TCLK should fail to transition (see Figure 1-1). 0 = do not switch to RCLKO if TCLK stops 1 = switch to RCLKO if TCLK stops
RFF	CCR2.1	**Receive Force Freeze.** Freezes receive side signaling at RSIG (and RSER if CCR3.3 = 1); will override Receive Freeze Enable (RFE). See Section 8.2 for details. 0 = do not force a freeze event 1 = force a freeze event
RFE	CCR2.0	**Receive Freeze Enable.** See Section 8.2 for details. 0 = no freezing of receive signaling data will occur 1 = allow freezing of receive signaling data at RSIG (and RSER if CCR3.3 = 1).

CCR3: COMMON CONTROL REGISTER 3 (Address = 1B Hex)

(MSB)							(LSB)
TESE	TCBFS	TIRFS	ESR	RSRE	THSE	TBCS	RCLA

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR3.7	**Transmit Side Elastic Store Enable.** 0 = elastic store is bypassed 1 = elastic store is enabled
TCBFS	CCR3.6	**Transmit Channel Blocking Registers (TCBR) Function Select.** 0 = TCBRs define the operation of the TCHBLK output pin 1 = TCBRs define which signaling bits are to be inserted
TIRFS	CCR3.5	**Transmit Idle Registers (TIR) Function Select.** See Section 9 for details. 0 = TIRs define in which channels to insert idle code 1 = TIRs define in which channels to insert data from RSER (i.e., Per-Channel Loopback function)
ESR	CCR3.4	**Elastic Stores Reset.** Setting this bit from a 1 to a 0 will force the elastic stores to a known depth. ESR is level triggered. Should be toggled after RSYSCLK and TSYSCLK have been applied and are stable. Must be set and cleared again for a subsequent reset. Do not leave this bit set high.
RSRE	CCR3.3	**Receive Side Signaling Re-Insertion Enable.** See Section 8.2 for details. 0 = do not reinsert signaling bits into the data stream presented at the RSER pin 1 = reinsert the signaling bits into data stream presented at the RSER pin
THSE	CCR3.2	**Transmit Side Hardware Signaling Insertion Enable.** See Section 8.2 for details. 0 = do not insert signaling from the TSIG pin into the data stream presented at the TSER pin 1 = insert signaling from the TSIG pin into the data stream presented at the TSER pin
TBCS	CCR3.1	**Transmit Side Backplane Clock Select.** 0 = if TSYSCLK is 1.544MHz 1 = if TSYSCLK is 2.048MHz
RCLA	CCR3.0	**Receive Carrier Loss (RCL) Alternate Criteria.** 0 = RCL declared upon 255 consecutive 0s (125µs) 1 = RCL declared upon 2048 consecutive 0s (1ms)

CCR4: COMMON CONTROL REGISTER 4 (Address = A8 Hex)

(MSB)							(LSB)
RLB	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RLB	CCR4.7	**Remote Loopback.** 0 = loopback disabled 1 = loopback enabled
LLB	CCR4.6	**Local Loopback.** 0 = loopback disabled 1 = loopback enabled
LIAIS	CCR4.5	**Line Interface AIS Generation Enable.** See Figure 1-1 for details. 0 = allow normal data from TPOSI/TNEGI to be transmitted at TTIP and TRING 1 = force unframed all 1s to be transmitted at TTIP and TRING
TCM4	CCR4.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register. See Section 7 for details.
TCM3	CCR4.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR4.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR4.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR4.0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode.

CCR5: COMMON CONTROL REGISTER 5 (Address = AA Hex)

(MSB)							(LSB)
LIRST	—	—	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
LIRST	CCR5.7	**Line Interface Reset.** Setting this bit from a 0 to a 1 will initiate an internal reset that affects the clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.
—	CCR5.6, CCR5.5	**Not Assigned.** Should be set to 0 when written.
RCM4	CCR5.4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 7 for details.
RCM3	CCR5.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR5.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR5.1	**Receive Channel Monitor Bit 1.**
RCM0	CCR5.0	**Receive Channel Monitor Bit 0.** LSB of the channel decode.

4.1 Framer Loopback

When CCR1.7 is set to 1, the DS2154 enters a Framer Loopback (FLB) mode. See Figure 1-1 for details. This loopback is useful in testing and debugging applications. In FLB, the DS2154 loops data from the transmit side back to the receive side. When FLB is enabled, the following occurs:

1) Data is transmitted as normal at TPOSO and TNEGO.
2) Data input via RPOSI and RNEGI is ignored.
3) The RCLK output is replaced with the TCLK input.

4.2 Local Loopback

When CCR4.6 is set to 1, the DS2154 is forced into Local Loopback (LLB). In this loopback, data continues to be transmitted as normal through the transmit side of the DS2154. Data being received at RTIP and RRING is replaced with the data being transmitted. Data in this loopback passes through the jitter attenuator. See Figure 1-1 for more details.

4.3 Remote Loopback

When CCR4.7 is set to 1, the DS2154 is forced into Remote Loopback (RLB). In this loopback, data input via the RPOSI and RNEGI pins is transmitted back to the TPOSO and TNEGO pins. Data continues to pass through the receive side framer of the DS2154 as it would normally, and the data from the transmit side formatter is ignored. See Figure 1-1 for more details.

4.4 Power-Up Sequence

On power-up, after the supplies are stable, the DS2154 should be configured for operation by writing to all of the internal registers (this includes the Test Registers) since the contents of the internal registers cannot be predicted on power-up. Next, the LIRST (CCR5.7) bit should be toggled from 0 to 1 to reset the line interface circuitry (it will take the DS2154 about 40ms to recover from the LIRST bit being toggled). Finally, after the RSYSCLK and TSYSCLK inputs are stable, the ESR bit should be toggled from a 0 to a 1 and then back to 0 (this step can be skipped if the elastic stores are not being used). Both TCLK and RCLKI must be present for the parallel control port to operate properly.

4.5 Automatic Alarm Generation

When either CCR2.4 or CCR2.5 is set to 1, the DS2154 monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all 1s) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the DS2154 will either force an AIS alarm (if CCR2.5 = 1) or a Remote Alarm (CCR2.4 = 1) to be transmitted via the TPOSO and TNEGO pins. It is an illegal state to have both CCR2.4 and CCR2.5 set to 1 at the same time. If CCR2.4 = 1, then RAI will be transmitted according to ETS 300 011 specifications and a constant Remote Alarm will be transmitted if the DS2154 cannot find CRC4 multiframe synchronization within 400ms as per G.706.

5 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real-time status of the DS2154: Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers is set to 1. All the bits in these registers operate in a latched fashion (except for the SSR). This means that if an event or an alarm occurs and a bit is set to a 1 in any of the registers, it remains set until the user reads that bit. The bit is cleared when it is read and it is not set again until the event has occurred again (or in the case of the RSA1, RSA0, RDMA, RUA1, RRA, RCL, and RLOS alarms, the bit remains set if the alarm is still present).

The user always precedes a read of the SR1, SR2, and RIR registers with a write. The byte written to the register informs the DS2154 which bits the user wishes to read and have cleared. The user writes a byte to one of these three registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register is updated with the latest information. When a 0 is written to a bit position, the read register is not updated and the previous value is held. A write to the status and information registers is immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written, and this value should be written back into the same register to ensure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2154 with higher-order software languages.

The SSR register operates differently than the other three. It is a read-only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this register with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT}}$ output pin. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2), respectively.

The interrupts caused by RUA1, RRA, RCL, and RLOS act differently than the interrupts caused by RSA1, RDMA, RSA0, RSLIP, RMF, RAF, TMF, SEC, TAF, LOTC, RCMF, and TSLIP. The four interrupts force the $\overline{\text{INT}}$ pin low whenever the alarm changes state (i.e., the alarm goes active or inactive according to the set/clear criteria in Table 5-1). The $\overline{\text{INT}}$ pin is allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur. If the alarm is still present, the register bit remains set.

The event-caused interrupts force the $\overline{\text{INT}}$ pin low when the event occurs. The $\overline{\text{INT}}$ pin is allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

RIR: RECEIVE INFORMATION REGISTER (Address = 08 Hex)

(MSB)							(LSB)
TESF	TESE	JALT	RESF	RESE	CRCRC	FASRC	CASRC

SYMBOL	POSITION	NAME AND DESCRIPTION
TESF	RIR.7	**Transmit Side Elastic Store Full.** Set when the transmit side elastic store buffer fills and a frame is deleted.
TESE	RIR.6	**Transmit Side Elastic Store Empty.** Set when the transmit side elastic store buffer empties and a frame is repeated.
JALT	RIR.5	**Jitter Attenuator Limit Trip.** Set when the jitter attenuator FIFO reaches to within 4 bits of its limit; useful for debugging jitter attenuation operation.
RESF	RIR.4	**Receive Side Elastic Store Full.** Set when the receive side elastic store buffer fills and a frame is deleted.
RESE	RIR.3	**Receive Side Elastic Store Empty.** Set when the receive side elastic store buffer empties and a frame is repeated.
CRCRC	RIR.2	**CRC Resync Criteria Met.** Set when 915/1000 code words are received in error.
FASRC	RIR.1	**FAS Resync Criteria Met.** Set when 3 consecutive FAS words are received in error.
CASRC	RIR.0	**CAS Resync Criteria Met.** Set when 2 consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address = 1E Hex)

(MSB)							(LSB)
CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA

SYMBOL	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	**CRC4 Sync Counter Bit 5.** MSB of the 6-bit counter.
CSC4	SSR.6	**CRC4 Sync Counter Bit 4.**
CSC3	SSR.5	**CRC4 Sync Counter Bit 3.**
CSC2	SSR.4	**CRC4 Sync Counter Bit 2.**
CSC0	SSR.3	**CRC4 Sync Counter Bit 0.** LSB of the 6-bit counter. The next to LSB is not accessible.
FASSA	SSR.2	**FAS Sync Active.** Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	**CAS MF Sync Active.** Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	**CRC4 MF Sync Active.** Set while the synchronizer is searching for the CRC4 MF alignment word.

5.1 CRC4 Sync Counter

The CRC4 sync counter increments each time the 8ms CRC4 multiframe search times out. The counter is cleared when the DS2154 has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0 = 0). This counter is useful for determining the amount of time the DS2154 has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400ms, then the search should be abandoned and proper action taken. The CRC4 sync counter will rollover.

SR1: STATUS REGISTER 1 (Address = 06 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	SR1.7	**Receive Signaling All 1s/Signaling Change.** Set when the contents of time slot 16 contains less than three 0s over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode. Both RSA1 and RSA0 will be set if a change in signaling is detected.
RDMA	SR1.6	**Receive Distant MF Alarm.** Set when bit 6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.
RSA0	SR1.5	**Receive Signaling All 0s/Signaling Change.** Set when over a full MF, time slot 16 contains all 0s. Both RSA1 and RSA0 will be set if a change in signaling is detected.
RSLIP	SR1.4	**Receive Side Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.
RUA1	SR1.3	**Receive Unframed All 1s.** Set when an unframed all 1s code is received at RPOSI and RNEGI.
RRA	SR1.2	**Receive Remote Alarm.** Set when a remote alarm is received at RPOSI and RNEGI.
RCL	SR1.1	**Receive Carrier Loss.** Set when 255 (or 2048 if CCR3.0 = 1) consecutive 0s have been detected at RTIP and RRING. (Note: a test mode exists to allow the DS2154 to detect carrier loss at RPOSI and RNEGI in place of detection at RTIP and RRING).
RLOS	SR1.0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive E1 stream.

Table 5-1. Alarm Criteria

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all 1s)	Over 16 consecutive frames (one full MF) time slot 16 contains less than three 0s	Over 16 consecutive frames (one full MF) time slot 16 contains three or more 0s	G.732 4.2
RSA0 (receive signaling all 0s)	Over 16 consecutive frames (one full MF) timeslot 16 contains all 0s	Over 16 consecutive frames (one full MF) time slot 16 contains at least a single 1	G.732 5.2
RDMA (receive distant multiframe alarm)	Bit 6 in time slot 16 of frame 0 set to 1 for two consecutive MF	Bit 6 in time slot 16 of frame 0 set to 0 for a two consecutive MF	O.162 2.1.5
RUA1 (receive unframed all 1s)	Less than three 0s in two frames (512 bits)	More than two 0s in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	Bit 3 of non-align frame set to 1 for three consecutive occasions	Bit 3 of non-align frame set to 0 for three consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 (or 2048) consecutive 0s received	In 255-bit times, at least 32 1s are received	G.775 / G.962

SR2: STATUS REGISTER 2 (Address = 07 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive CAS Multiframe**. Set every 2ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	**Receive Align Frame**. Set every 250µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	**Transmit Multiframe**. Set every 2ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	**1-Second Timer**. Set on increments of 1 second based on RCLK. If CCR2.7 = 1, then this bit will be set every 62.5 ms instead of once a second.
TAF	SR2.3	**Transmit Align Frame**. Set every 250µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.
LOTC	SR2.2	**Loss of Transmit Clock**. Set when the TCLK pin has not transitioned for one channel time (or 3.9µs). Will force the LOTC pin high if enabled via TCR2.0.
RCMF	SR2.1	**Receive CRC4 Multiframe**. Set on CRC4 multiframe boundaries; will continue to be set every 2ms on an arbitrary boundary if CRC4 is disabled.
TSLIP	SR2.0	**Transmit Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.

IMR1: INTERRUPT MASK REGISTER 1 (Address = 16 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	IMR1.7	**Receive Signaling All 1s/Signaling Change.** 0 = interrupt masked 1 = interrupt enabled
RDMA	IMR1.6	**Receive Distant MF Alarm**. 0 = interrupt masked 1 = interrupt enabled
RSA0	IMR1.5	**Receive Signaling All 0s/Signaling Change.** 0 = interrupt masked 1 = interrupt enabled
RSLIP	IMR1.4	**Receive Elastic Store Slip Occurrence**. 0 = interrupt masked 1 = interrupt enabled
RUA1	IMR1.3	**Receive Unframed All 1s**. 0 = interrupt masked 1 = interrupt enabled
RRA	IMR1.2	**Receive Remote Alarm**. 0 = interrupt masked 1 = interrupt enabled
RCL	IMR1.1	**Receive Carrier Loss**. 0 = interrupt masked 1 = interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync**. 0 = interrupt masked 1 = interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address = 17 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive CAS Multiframe.** 0 = interrupt masked 1 = interrupt enabled
RAF	IMR2.6	**Receive Align Frame.** 0 = interrupt masked 1 = interrupt enabled
TMF	IMR2.5	**Transmit Multiframe.** 0 = interrupt masked 1 = interrupt enabled
SEC	IMR2.4	**1-Second Timer.** 0 = interrupt masked 1 = interrupt enabled
TAF	IMR2.3	**Transmit Align Frame.** 0 = interrupt masked 1 = interrupt enabled
LOTC	IMR2.2	**Loss Of Transmit Clock.** 0 = interrupt masked 1 = interrupt enabled
RCMF	IMR2.1	**Receive CRC4 Multifram**e. 0 = interrupt masked 1 = interrupt enabled
TSLIP	IMR2.0	**Transmit Side Elastic Store Slip Occurrence.** 0 = interrupt masked 1 = interrupt enabled

6 ERROR COUNT REGISTERS

There are a set of four counters in the DS2154 that record bipolar or code violations, errors in the CRC4 SMF codewords, E bits as reported by the far end, and word errors in the FAS. Each of these four counters is automatically updated on either 1-second boundaries (CCR2.7 = 0) or every 62.5ms (CCR2.7 = 1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 62.5ms. The user can use the interrupt from the timer to determine when to read these registers. The user has a full second (or 62.5ms) to read the counters before the data is lost.

6.1 BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a 16-bit counter that records either Bipolar Violations (BPVs) or Code Violations (CVs). If CCR2.6 = 0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side via CCR1.2, then HDB3 codewords are not counted as BPVs. If CCR2.6 = 1, then the VCR counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the DS2154 should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on an E1 line would have to be greater than 10**$^{-2}$ before the VCR would saturate.

VCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address = 00 Hex)
VCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address = 01 Hex)

(MSB)							(LSB)	
V15	V14	V13	V12	V11	V10	V9	V8	VCR1
V7	V6	V5	V4	V3	V2	V1	V0	VCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
V15	VCR1.7	**MSB of the 16-bit bipolar or code violation count .**
V0	VCR2.0	**LSB of the 16-bit bipolar or code violation count.**

6.2 CRC4 Error Counter

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 10-bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a 1-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

CRCCR1: CRC4 COUNT REGISTER 1 (Address = 02 Hex)
CRCCR2: CRC4 COUNT REGISTER 2 (Address = 03 Hex)

(MSB)							(LSB)	
(Note 1)	(Note 1)	(Note 1)	(Note 1)	(Note 1)	(Note 1)	CRC9	CRC8	CRCCR1
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC9	CRCCR1.1	**MSB of the 10-bit CRC4 error count.**
CRC0	CRCCR2.0	**LSB of the 10-bit CRC4 error count.**

Note 1: *The upper 6 bits of CRCCR1 at address 02 are the most significant bits of the 12-bit FAS error counter.*

6.3 E-Bit Counter

E-bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 10-bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E-bit is set to 0. Since the maximum E-bit count in a 1-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

EBCR1: E-BIT COUNT REGISTER 1 (Address = 04 Hex)
EBCR2: E-BIT COUNT REGISTER 2 (Address = 05 Hex)

(MSB)							(LSB)	
(Note 1)	(Note 1)	(Note 1)	(Note 1)	(Note 1)	(Note 1)	EB9	EB8	EBCR1
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
EB9	EBCR1.1	**MSB of the 10-bit E-Bit count.**
EB0	EBCR2.0	**LSB of the 10-bit E-Bit count.**

Note 1: *The upper 6 bits of EBCR1 at address 04 are the least significant bits of the 12-bit FAS error counter.*

6.4 FAS Error Counter

FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 12-bit counter that records word errors in the Frame Alignment Signal in time slot 0. This counter is disabled during loss of synchronization conditions, (RLOS = 1). Since the maximum FAS word error count in a 1-second period is 4000, this counter cannot saturate.

FASCR1: FAS BIT COUNT REGISTER 1 (Address = 02 Hex)
FASCR2: FAS BIT COUNT REGISTER 2 (Address = 04 Hex)

(MSB)							(LSB)	
FAS11	FAS10	FAS9	FAS8	FAS7	FAS6	(Note 1)	(Note 1)	FASCR1
FAS5	FAS4	FAS3	FAS2	FAS1	FAS0	(Note 2)	(Note 2)	FASCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
FAS11	FASCR1.7	**MSB of the 12-bit FAS error count.**
FAS0	FASCR2.2	**LSB of the 12-bit FAS error count.**

Note 1: *The lower 2 bits of FASCR1 at address 02 are the most significant bits of the 10-bit CRC4 error counter.*
Note 2: *The lower 2 bits of FASCR2 at address 04 are the most significant bits of the 10-bit E-bit counter.*

7 DS0 MONITORING FUNCTION

The DS2154 can monitor one DS0 64kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction, the user determines which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the CCR4 register. In the receive direction, the RCM0 to RCM4 bits in the CCR5 register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register.

The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate E1 channel. For example, if DS0 channel 6 (time slot 5) in the transmit direction and DS0 channel 15 (time slot 14) in the receive direction needed to be monitored, then the following values would be programmed into CCR4 and CCR5:

TCM4 = 0	RCM4 = 0
TCM3 = 0	RCM3 = 1
TCM2 = 1	RCM2 = 1
TCM1 = 0	RCM1 = 1
TCM0 = 1	RCM0 = 0

CCR4: DS0 MONITORING FUNCTION (Address = A8 Hex)

(Repeated here from Section 4 for convenience.)

(MSB)							(LSB)
RLB	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RLB	CCR4.7	**Remote Loopback.** See Section 4 for details.
LLB	CCR4.6	**Local Loopback.** See Section 4 for details.
LIAIS	CCR4.5	**Line Interface AIS Generation Enable.** See Section 4 for details.
TCM4	CCR4.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register.
TCM3	CCR4.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR4.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR4.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR4.0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode that determines which transmit DS0 channel data will appear in the TDS0M register.

CCR5: COMMON CONTROL REGISTER 5 (Address = AA Hex)

(Repeated here from Section 4 for convenience.)

(MSB)							(LSB)
LIRST	—	—	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
LIRST	CCR5.7	**Line Interface Reset.** See Section 4 for details.
—	CCR5.6, CCR5.5	**Not Assigned.** Should be set to 0 when written.
RCM4	CCR5.4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register.
RCM3	CCR5.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR5.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR5.1	**Receive Channel Monitor Bit 1.**
RCM0	CCR5.0	**Receive Channel Monitor Bit 0.** LSB of the channel decode that determines which receive DS0 channel data will appear in the RDS0M register.

TDS0M: TRANSMIT DS0 MONITOR REGISTER (Address = A9 Hex)

(MSB)							(LSB)
B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	TDS0M.7	**Transmit DS0 Channel Bit 8.** MSB of the DS0 channel (first bit to be transmitted).
B2	TDS0M.6	**Transmit DS0 Channel Bit 7.**
B3	TDS0M.5	**Transmit DS0 Channel Bit 6.**
B4	TDS0M.4	**Transmit DS0 Channel Bit 5.**
B5	TDS0M.3	**Transmit DS0 Channel Bit 4.**
B6	TDS0M.2	**Transmit DS0 Channel Bit 3.**
B7	TDS0M.1	**Transmit DS0 Channel Bit 2.**
B8	TDS0M.0	**Transmit DS0 Channel Bit 1.** LSB of the DS0 channel (last bit to be transmitted).

RDS0M: RECEIVE DS0 MONITOR REGISTER (Address = 1F Hex)

(MSB)							(LSB)
B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	RDS0M.7	**Receive DS0 Channel Bit 1.** MSB of the DS0 channel (first bit to be received).
B2	RDS0M.6	**Receive DS0 Channel Bit 2.**
B3	RDS0M.5	**Receive DS0 Channel Bit 3.**
B4	RDS0M.4	**Receive DS0 Channel Bit 4.**
B5	RDS0M.3	**Receive DS0 Channel Bit 5.**
B6	RDS0M.2	**Receive DS0 Channel Bit 6.**
B7	RDS0M.1	**Receive DS0 Channel Bit 7.**
B8	RDS0M.0	**Receive DS0 Channel Bit 8.** LSB of the DS0 channel (last bit to be received).

8 SIGNALING OPERATION

The DS2154 contains provisions for both processor-based (i.e., software based) signaling bit access and for hardware-based access. Both the processor-based access and the hardware-based access can be used simultaneously if necessary. The processor-based signaling is covered in Section 8.1 and the hardware based signaling is covered in Section 8.2.

8.1 Processor-Based Signaling

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2154. Each of the 30 voice channels has four signaling bits (A to D) associated with it. The numbers in parentheses () are the voice channels associated with a particular signaling bit. The voice channel numbers have been assigned as described in the ITU documents. Note that this is different than the channel numbering scheme (1 to 32) that is used in the rest of the data sheet. For example, voice channel 1 is associated with time slot 1 (Channel 2) and voice Channel 30 is associated with time slot 31 (Channel 32). There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address = 30 to 3F Hex)

(MSB)							(LSB)	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	RS4 (33)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	RS7 (36)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	RS16 (3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	**Spare Bits.**
Y	RS1.2	**Remote Alarm Bit (integrated and reported in SR1.6).**
A(1)	RS2.7	**Signaling Bit A for Channel 1.**
D(30)	RS16.0	**Signaling Bit D for Channel 30.**

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling from two time slots. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can use the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2ms to retrieve the data before it is lost. The signaling data reported in RS1 to RS16 is also available at the RSIG and RSER pins.

A change in the signaling bits from one multiframe to the next causes the RSA1 (SR1.7) and RSA0 (SR1.5) status bits to be set at the same time. The user can enable the $\overline{\text{INT}}$ pin to toggle low upon detection of a change in signaling by setting either the IMR1.7 or IMR1.5 bit. Once a signaling change has been detected, the user has at least 1.75ms to read the data out of the RS1 to RS16 registers before the data will be lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address = 40 to 4F Hex)

(MSB)							(LSB)	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	**Spare Bits.**
Y	TS1.2	**Remote Alarm Bit.**
A(1)	TS2.7	**Signaling Bit A for Channel 1.**
D(30)	TS16.0	**Signaling Bit D for Channel 30.**

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the DS2154 will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can use the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2ms and the user has 2ms to update the TSRs before the old data will be retransmitted. ITU specifications recommend that the ABCD signaling not be set to all 0s because they will emulate a CAS multiframe alignment word.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper nibble must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.2 bit should be set to a 1. If no alarm is to be transmitted, then the TS1.2 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to 1. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be informed when the signaling registers need to be loaded with data. The user has 2ms to load the data before the old data will be retransmitted.

Via the CCR3.6 bit, the user has the option to use the Transmit Channel Blocking Registers (TCBRs) to determine, on a channel-by-channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs = 1) and which are to be sourced from the TSER or TSIG pin (the corresponding bit in the TCBRs = 0). See the *Transmit Data Flow* diagram (Figure 14-11) for more details.

8.2 Hardware-Based Signaling

8.2.1 Receive Side

In the receive side of the hardware based signaling, there are two operating modes for the signaling buffer: signaling extraction and signaling reinsertion. Signaling extraction involves pulling the signaling bits from the receive data stream and buffering them over a 2-multiframe buffer and outputting them in a serial PCM fashion on a channel-by-channel basis at the RSIG output pin. This mode is always enabled. In this mode, the receive elastic store may be enabled or disabled. If the receive elastic store is enabled, then the backplane clock (RSYSCLK) must be 2.048MHz. The ABCD signaling bits are output on RSIG in the lower nibble of each channel. See the timing diagrams in Section 14 for an example. The RSIG data is updated once a multiframe (2ms) unless a freeze is in effect.

The other hardware based signaling operating mode called signaling re-insertion can be invoked by setting the RSRE control bit high (CCR3.3 = 1). In this mode, the user will provide a multiframe sync at the RSYNC pin and the signaling data will be re-aligned in the PCM data stream provided at the RSER output pin according to this applied multiframe boundary. In this mode, the elastic store must be enabled and the backplane clock (RSYSCLK) must be 2.048MHz.

The signaling data in the two-multiframe buffer will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or frame slip. To allow this freeze action to occur, the RFE control bit (CCR2.0) should be set high. The user can force a freeze by setting the RFF control bit (CCR2.1) high. Setting the RFF bit high causes the same freezing action as if a loss of synchronization, carrier loss, or slip has occurred. The RSIGF output pin provides a hardware indication that a freeze is in effect. The RSIGF pin will go high immediately upon detection of any of the events that can cause a freeze to occur. The RSIGF pin will return low 3ms to 5ms after the event subsides. The RSIGF pin action cannot be disabled.

The two-multiframe buffer provides an approximate one-multiframe delay in the signaling bits provided at the RSIG pin (and at the RSER pin if RSRE = 1 via CCR3.3). When freezing is enabled (RFE = 1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data will be held in the old state for an additional 3ms to 5ms before being allowed to be updated with new signaling data.

8.2.2 Transmit Side

Via the THSE control bit (CCR3.2), the DS2154 can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The hardware signaling insertion capabilities of the DS2154 are available whether the transmit side elastic store is enabled or disabled. If the transmit side elastic store is enabled, the backplane clock (TSYSCLK) must be 2.048MHz.

When hardware signaling insertion is enabled on the DS2154 (TSRE = 1), then the user must enable the Transmit Channel Blocking Register Function Select (TCBFS) control bit (CCR3.6 = 1). This is needed so that the CAS multiframe alignment word, multiframe remote alarm, and spare bits can be added to timeslot 16 in frame 0 of the multiframe. The TS1 register should be programmed with the proper information. If CCR3.6 = 1, then a 0 in the TCBRs implies that signaling data is to be sourced from TSER (or TSIG if CCR3.2 = 1) and a 1 implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See the following definition.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6 = 1

(MSB)							(LSB)	
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1(22)
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2(23)
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3(24)
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4(25)

**CH1 and CH17 should be set to 1 to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.*

The user can also take advantage of this functionality to intermix signaling data from the TSIG pin and from the internal Transmit Signaling Registers (TS1 to TS16). As an example, assume that the user wishes to source all the signaling data except for voice channels 5 and 10 from the TSIG pin. In this application, the following bits and registers would be programmed as follows:

CONTROL BITS	REGISTER VALUES
TSRE = 1 (CCR3.2)	TS1 = 0Bh (MF alignment word, remote alarm etc.)
TCBFS = 1 (CCR3.6)	TCBR1 = 03h (source time slot 16, frame 1 data)
T16S = 1 (TCR1.5)	TCBR2 = 01h (source voice Channel 5 signaling data from TS6)
	TCBR3 = 04h (source voice Channel 10 signaling data from TS11)
	TCBR4 = 00h

9 PER-CHANNEL CODE (IDLE) GENERATION AND LOOPBACK

The DS2154 can replace data on a channel-by-channel basis in both the transmit and receive directions. The transmit direction is from the backplane to the E1 line and is covered in Section 9.1. The receive direction is from the E1 line to the backplane and is covered in Section 9.2.

9.1 Transmit Side Code Generation

In the transmit direction there are two methods by which channel data from the backplane can be overwritten with data generated by the DS2154. The first method, which is covered in Section 9.1.1, was a feature contained in the original DS2153 while the second method, which is covered in Section 9.1.2, is a new feature of the DS2154.

9.1.1 Simple Idle Code Insertion and Per-Channel Loopback

The first method involves using the Transmit Idle Registers (TIR1/2/3/4) to determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Idle Definition Register (TIDR). This method allows the same 8-bit code to be placed into any of the 32 E1 channels. If this method is used, then the CCR3.5 control bit must be set to 0.

The Transmit Idle Registers (TIRs) have an alternate function that allows them to define a Per-Channel Loopback (PCLB). If the CCR3.5 control bit is set to 1, then the TIRs will determine which channels (if any) from the backplane should be replaced with the data from the receive side or, in other words, off of the E1 line. See Figure 1-1. If this mode is enabled, then transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this would be to tie RCLK to TCLK and RFSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

TIR1/TIR2/TIR3/TIR4: TRANSMIT IDLE REGISTERS (Address = 26 to 29 Hex)

(Also used for Per-Channel Loopback.)

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TIR4.7	**Transmit Idle Registers.** 0 = do not insert the Idle Code in the TIDR into this channel
CH1	TIR1.0	1 = insert the Idle Code in the TIDR into this channel

Note: *If CCR3.5 = 1, then a 0 in the TIRs implies that channel data is to be sourced from TSER and a 1 implies that channel data is to be sourced from the output of the receive side framer (i.e., Per-Channel Loopback; see Figure 1-1).*

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address = 2A Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	**MSB of the Idle Code (this bit is transmitted first).**
TIDR0	TIDR.0	**LSB of the Idle Code (this bit is transmitted last).**

9.1.2 Per-Channel Code Insertion

The second method involves using the Transmit Channel Control Registers (TCC1/2/3/4) to determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Channel Registers (TC1 to TC32). This method is more flexible than the first in that it allows a different 8-bit code to be placed into each of the 32 E1 channels.

TC1 TO TC32: TRANSMIT CHANNEL REGISTERS (Address = 60 to 7F Hex)

(For brevity, only channel 1 is shown; see Table 2-1 for other register address.)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	TC1 (60)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	TC1.7	**MSB of the Code (this bit is transmitted first).**
C0	TC1.0	**LSB of the Code (this bit is transmitted last).**

TCC1/TCC2/TCC3/TCC4: TRANSMIT CHANNEL CONTROL REGISTER (Address = A0 to A3 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCC1 (A0)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCC2 (A1)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCC3 (A2)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCC4 (A3)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH1	TCC1.0	**Transmit Channel 1 Code Insertion Control Bit** 0 = do not insert data from the TC1 register into the transmit data stream 1 = insert data from the TC1 register into the transmit data stream
CH32	TCC4.7	**Transmit Channel 32 Code Insertion Control Bit** 0 = do not insert data from the TC32 register into the transmit data stream 1 = insert data from the TC32 register into the transmit data stream

9.2 Receive Side Code Generation

On the receive side, the Receive Channel Control Registers (RCC1/2/3/4) are used to determine which of the 32 E1 channels off the E1 line and going to the backplane should be overwritten with the code placed in the Receive Channel Registers (RC1 to RC32).

RC1 TO RC32: RECEIVE CHANNEL REGISTERS (Address = 80 to 9F)

(For brevity, only channel 1 is shown; see Table 2-1 for other register address.)

(MSB)							**(LSB)**	
C7	C6	C5	C4	C3	C2	C1	C0	RC1 (80)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RC1.7	**MSB of the Code (this bit is sent first to the backplane)**
C0	RC1.0	**LSB of the Code (this bit is sent last to the backplane)**

RCC1/RCC2/RCC3/RCC4: RECEIVE CHANNEL CONTROL REGISTER (Address = A4 to A7 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCC1 (A4)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCC2 (A5)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCC3 (A6)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCC4 (A7)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH1	RCC1.0	**Receive Channel 1 Code Insertion Control Bit** 0 = do not insert data from the RC1 register into the receive data stream 1 = insert data from the RC1 register into the receive data stream
CH32	RCC4.7	**Receive Channel 32 Code Insertion Control Bit** 0 = do not insert data from the RC32 register into the receive data stream 1 = insert data from the RC32 register into the receive data stream

10 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3/RCBR4) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins, respectively. The RCHBLK and TCHCLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing diagrams in Section 14 for an example. The TCBRs have alternate mode of use. Via the CCR3.6 bit, the user has the option to use the TCBRs to determine, on a channel-by-channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs = 1) and which are to be sourced from the TSER or TSIG pins (the corresponding bit in the TCBR = 0). See Section 8 for more details about this mode of operation.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS (Address = 2B to 2E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	RCBR4.7	**Receive Channel Blocking Registers.** 0 = force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1 = force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS (Address = 22 to 25 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR1 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR1 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TCBR4.7	**Transmit Channel Blocking Registers.** 0 = force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1 = force the TCHBLK pin high during this channel time

Note: If CCR3.6 = 1, then a 0 in the TCBRs implies that signaling data is to be sourced from TSER (or TSIG if CCR3.2 = 1) and a 1 implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See the following definition.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6 = 1

(MSB)							**(LSB)**	
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1 (22)
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2 (23)
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3 (24)
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4 (25)

**CH1 and CH17 should be set to 1 to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.*

11 ELASTIC STORES OPERATION

The DS2154 contains dual two-frame (512 bits) elastic stores: one for the receive direction and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the E1 data stream to 1.544Mbps (or a multiple of 1.544Mbps), which is the T1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e., not frequency locked) backplane clock (which can be 1.544MHz or 2.048MHz). The backplane clock can burst at rates up to 8.192MHz. Both elastic stores contain full controlled slip capability, which is necessary for this second purpose. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.4). Toggling the CCR3.4 bit forces the read and write pointers into opposite frames. Both elastic stores within the DS2154 are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544MHz or 2.048MHz backplane without regard to the backplane rate the other elastic store is interfacing.

11.1 Receive Side

If the receive side elastic store is enabled (RCR2.1 = 1), then the user must provide either a 1.544MHz (RCR2.2 = 0) or 2.048MHz (RCR2.2 = 1) clock at the RSYSCLK pin. The user has the option of either providing a frame/multiframe sync at the RSYNC pin (RCR1.5 = 1) or having the RSYNC pin provide a pulse on frame/multiframe boundaries (RCR1.5 = 0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to 0; if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to 1. The DS2154 will always indicate frame boundaries via the RFSYNC output whether the elastic store is enabled or not. If the elastic store is enabled, then either CAS (RCR1.7 = 0) or CRC4 (RCR1.7 = 1) multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 1.544MHz clock to the RSYSCLK pin, then every fourth channel of the received E1 data will be deleted and an F-bit position (which will be forced to 1) will be inserted. Hence Channels 1, 5, 9, 13, 17, 21, 25, and 29 (time slots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted from the received E1 data stream. Also, in 1.544MHz applications, the RCHBLK output will not be active in Channels 25 through 32 (or in other words, RCBR4 is not active). See Section 14 for timing details. If the 512-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a 1. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a 1.

11.2 Transmit Side

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR3.7. A 1.544MHz (CCR3.1 = 0) or 2.048MHz (CCR3.1 = 1) clock can be applied to the TSYSCLK input. The TSYSCLK can be a bursty clock with rates up to 8.192MHz. If the user selects to apply a 1.544MHz clock to the TSYSCLK pin, then the data sampled at TSER will be stuffed with eight empty channels. The user must supply an 8kHz frame sync pulse to the TSSYNC input. See Section 14 for timing details. Controlled slips in the transmit elastic store are reported in the SR2.0 bit and the direction of the slip is reported in the RIR.6 and RIR.7 bits.

12 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS2154 provides for access to both the Sa and the Si bits via three different methods. The first is via a hardware scheme using the RLINK/RLCLK and TLINK/ TLCLK pins. The first method is discussed in Section 12.1. The second involves using the internal RAF/RNAF and TAF/TNAF registers and is discussed in Section 12.2. The third method, which is covered in Section 12.3, involves an expanded version of the second method and is one of the features added to the DS2154 from the original DS2153 definition.

12.1 Hardware Scheme

On the receive side, all the received data is reported at the RLINK pin. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits. If RSYNC is programmed to output a frame boundary, it will identify the Si bits. See Section 14 for detailed timing.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (see Section 12.2 for details) or from the external TLINK pin. Via TCR2, the DS2154 can be programmed to source any combination of the additional bits from the TLINK pin. If the user wishes to pass the Sa bits through the DS2154 without them being altered, then the device should be set up to source all five Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Si bits can be inserted through the TSER pin via the clearing of the TCR1.3 bit. See the timing diagrams and the transmit data flow diagram in Section 14 for examples.

12.2 Internal Register Scheme Based on Double-Frame

On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250µs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250µs to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the DS2154 is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to 1 (see Section 12.1 for details). See the register descriptions for TCR1 and TCR2 and the *Transmit Data Flow* diagram (Figure 14-11) for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address = 2F Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RAF.7	**International Bit.**
0	RAF.6	**Frame Alignment Signal Bit.**
0	RAF.5	**Frame Alignment Signal Bit.**
1	RAF.4	**Frame Alignment Signal Bit.**
1	RAF.3	**Frame Alignment Signal Bit.**
0	RAF.2	**Frame Alignment Signal Bit.**
1	RAF.1	**Frame Alignment Signal Bit.**
1	RAF.0	**Frame Alignment Signal Bit.**

RNAF: RECEIVE NON-ALIGN FRAME REGISTER (Address = 1F Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RNAF.7	**International Bit.**
1	RNAF.6	**Frame Non-Alignment Signal Bit.**
A	RNAF.5	**Remote Alarm.**
Sa4	RNAF.4	**Additional Bit 4.**
Sa5	RNAF.3	**Additional Bit 5.**
Sa6	RNAF.2	**Additional Bit 6.**
Sa7	RNAF.1	**Additional Bit 7.**
Sa8	RNAF.0	**Additional Bit 8.**

TAF: TRANSMIT ALIGN FRAME REGISTER (Address = 20 Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

*(**Note:** Must be programmed with the 7-bit FAS word; the DS2154 does not automatically set these bits.)*

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TAF.7	**International Bit.**
0	TAF.6	**Frame Alignment Signal Bit.**
0	TAF.5	**Frame Alignment Signal Bit.**
1	TAF.4	**Frame Alignment Signal Bit.**
1	TAF.3	**Frame Alignment Signal Bit.**
0	TAF.2	**Frame Alignment Signal Bit.**
1	TAF.1	**Frame Alignment Signal Bit.**
1	TAF.0	**Frame Alignment Signal Bit.**

TNAF: TRANSMIT NON-ALIGN FRAME REGISTER (Address = 21 Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

*(**Note:** Bit 2 must be programmed to 1; the DS2154 does not automatically set this bit.)*

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TNAF.7	**International Bit.**
1	TNAF.6	**Frame Non-Alignment Signal Bit.**
A	TNAF.5	**Remote Alarm (used to transmit the alarm).**
Sa4	TNAF.4	**Additional Bit 4.**
Sa5	TNAF.3	**Additional Bit 5.**
Sa6	TNAF.2	**Additional Bit 6.**
Sa7	TNAF.1	**Additional Bit 7.**
Sa8	TNAF.0	**Additional Bit 8.**

12.3 Internal Register Scheme Based on CRC4 Multiframe

On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the Receive CRC4 Multiframe bit in Status Register 2 (SR2.1). The host can use the SR2.1 bit to know when to read these registers. The user has 2ms to retrieve the data before it is lost. The MSB of each register is the first received. See the register descriptions below and the *Transmit Data Flow* diagram (Figure 14-11) for more details.

On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that can be programmed to insert both Si and Sa data via the Transmit Sa Bit Control Register (TSaCR). Data is sampled from these registers with the setting of the Transmit Multiframe bit in Status Register 2 (SR2.5). The host can use the SR2.5 bit to know when to update these registers. It has 2ms to update the data or else the old data will be retransmitted. The MSB of each register is the first bit transmitted. See the register descriptions below and the *Transmit Data Flow* diagram (Figure 14-11) for more details.

REGISTER NAME	ADDRESS (HEX)	FUNCTION
RSiAF	58	The 8 Si bits in the align frame
RSiNAF	59	The 8 Si bits in the non-align frame
RRA	5A	The 8 reportings of the receive remote alarm (RA)
RSa4	5B	The 8 Sa4 reported in each CRC4 multiframe
RSa5	5C	The 8 Sa5 reported in each CRC4 multiframe
RSa6	5D	The 8 Sa6 reported in each CRC4 multiframe
RSa7	5E	The 8 Sa7 reported in each CRC4 multiframe
RSa8	5F	The eight Sa8 reported in each CRC4 multiframe
TSiAF	50	The 8 Si bits to be inserted into the align frame
TSiNAF	51	The 8 Si bits to be inserted into the non-align frame
TRA	52	The 8 settings of remote alarm (RA)
TSa4	53	The 8 Sa4 settings in each CRC4 multiframe
TSa5	54	The 8 Sa5 settings in each CRC4 multiframe
TSa6	55	The 8 Sa6 settings in each CRC4 multiframe
TSa7	56	The 8 Sa7 settings in each CRC4 multiframe
TSa8	57	The 8 Sa8 settings in each CRC4 multiframe

TSaCR: TRANSMIT Sa BIT CONTROL REGISTER (Address = 1C Hex)

(MSB)							(LSB)
SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
SiAF	TSaCR.7	**International Bit in Align Frame Insertion Control Bit.** 0 = do not insert data from the TSiAF register into the transmit data stream 1 = insert data from the TSiAF register into the transmit data stream
SiNAF	TSaCR.6	**International Bit in Non-Align Frame Insertion Control Bit.** 0 = do not insert data from the TSiNAF register into the transmit data stream 1 = insert data from the TSiNAF register into the transmit data stream
RA	TSaCR.5	**Remote Alarm Insertion Control Bit.** 0 = do not insert data from the TRA register into the transmit data stream 1 = insert data from the TRA register into the transmit data stream
Sa4	TSaCR.4	**Additional Bit 4 Insertion Control Bit.** 0 = do not insert data from the TSa4 register into the transmit data stream 1 = insert data from the TSa4 register into the transmit data stream
Sa5	TSaCR.3	**Additional Bit 5 Insertion Control Bit.** 0 = do not insert data from the TSa5 register into the transmit data stream 1 = insert data from the TSa5 register into the transmit data stream
Sa6	TSaCR.2	**Additional Bit 6 Insertion Control Bit.** 0 = do not insert data from the TSa6 register into the transmit data stream 1 = insert data from the TSa6 register into the transmit data stream
Sa7	TSaCR.1	**Additional Bit 7 Insertion Control Bit.** 0 = do not insert data from the TSa7 register into the transmit data stream 1 = insert data from the TSa7 register into the transmit data stream
Sa8	TSaCR.0	**Additional Bit 8 Insertion Control Bit.** 0 = do not insert data from the TSa8 register into the transmit data stream 1 = insert data from the TSa8 register into the transmit data stream

13 LINE INTERFACE FUNCTION

The line interface function in the DS2152 contains three sections: the receiver, which handles clock and data recovery; the transmitter, which waveshapes and drives the E1 line; and the jitter attenuator. Each of these three sections is controlled by the Line Interface Control Register (LICR), which is described below.

LICR: LINE INTERFACE CONTROL REGISTER (Address = 18 Hex)

(MSB)							(LSB)	
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD	LICR

SYMBOL	POSITION	NAME AND DESCRIPTION
L2	LICR.7	**Line Build-Out Select Bit 2.** Sets the transmitter build out; see the Table 13-2.
L1	LICR.6	**Line Build-Out Select Bit 1.** Sets the transmitter build out; see the Table 13-2.
L0	LICR.5	**Line Build-Out Select Bit 0.** Sets the transmitter build out; see the Table 13-2.
EGL	LICR.4	**Receive Equalizer Gain Limit.** 0 = -12dB 1 = -43dB
JAS	LICR.3	**Jitter Attenuator Select.** 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
JABDS	LICR.2	**Jitter Attenuator Buffer Depth Select** 0 = 128 bits 1 = 32 bits (use for delay sensitive applications)
DJA	LICR.1	**Disable Jitter Attenuator.** 0 = jitter attenuator enabled 1 = jitter attenuator disabled
TPD	LICR.0	**Transmit Power-Down.** 0 = normal transmitter operation 1 = powers down the transmitter and tri-states the TTIP and TRING pins

13.1 Receive Clock and Data Recovery

The DS2154 contains a digital clock recovery system. See Figure 1-1 and Figure 13-1 for more details. The DS2154 couples to the receive E1 shielded twisted pair or coax via a 1:1 transformer. See Table 13-2 for transformer details. The 2.048MHz clock attached at the MCLK pin is internally multiplied by 16 via an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times oversampler, which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance (see Figure 13-2).

Normally, the clock that is output at the RCLKO pin is the recovered clock from the E1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (LRCL) condition will occur and the RCLKO will be sourced from the clock applied at the MCLK pin. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLKO output can exhibit slightly shorter high cycles of the clock. This is due to the highly over-sampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. See the Receive AC Timing Characteristics in Section 16 for more details.

13.2 Transmit Waveshaping and Line Driving

The DS2154 uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the E1 line. The waveforms created by the DS2154 meet the ITU G.703 specifications. See Figure 13-3. The user will select which waveform is to be generated by properly programming the L2/L1/L0 bits in the Line Interface Control Register (LICR). The DS2154 can set up in a number of various configurations depending on the application. See Table 13-1 and Figure 13-1.

Table 13-1. Line Build-Out Select in LICR

LLL 210	APPLICATION	TRANSFORMER	RETURN LOSS (dB)	R_T (Ω) (SEE Figure 13-1)
000	75Ω normal (See Note 1)	1:1.15 step-up	N.M.	0
001	120Ω normal	1:1.15 step-up	N.M.	0
010	75Ω with protection resistors	1:1.15 step-up	N.M.	8.2
011	120Ω with protection resistors	1:1.15 step-up	N.M.	8.2
100	75Ω with high return loss	1:1.15 step-up	21	27
110	75Ω with high return loss	1:1.36 step-up	21	18
100	120Ω with high return loss	1:1.36 step-up	21	27

N.M. = not meaningful
Note: *This LBO is not recommended for use in the DS2154 A2 revision.*

Due to the nature of the design of the transmitter in the DS2154, very little jitter (less than $0.005UI_{P-P}$ broadband from 10Hz to 100kHz) is added to the jitter present on TCLKI. Also, the waveforms that they create are independent of the duty cycle of TCLK. The transmitter in the DS2154 couples to the E1 transmit shielded twisted pair or coax via a 1:1.15 or 1:1.36 step-up transformer as shown in Figure 13-1. For the devices to create the proper waveforms, this transformer used must meet the specifications listed

in Table 13-2. The line driver in the DS2154 contains a current limiter that prevents more than 50mA (RMS) from being sourced in a 1Ω load.

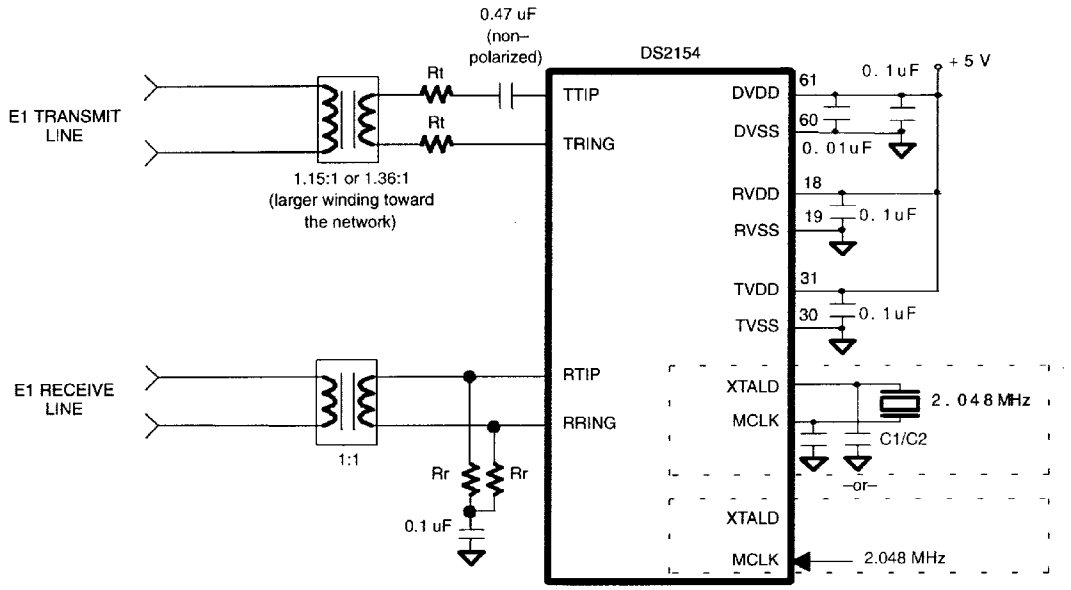
Table 13-2. Transformer Specifications

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:1.15 or 1:1.36 (transmit) ±5%
Primary Inductance	600µH minimum
Leakage Inductance	1.0µH maximum
Intertwining Capacitance	40pF maximum
DC Resistance	1.2Ω maximum

13.3 Jitter Attenuator

The DS2154 contains an on-board jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 13-4. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit in the LICR. In order for the jitter attenuator to operate properly, a 2.048MHz clock (±50ppm) must be applied at the MCLK pin or a crystal with similar characteristics must be applied across the MCLK and XTALD pins. If a crystal is applied across the MCLK and XTALD pins, then capacitors should be placed from each leg of the crystal to the local ground plane as shown in Figure 13-1. On-board circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLKI pin to create a smooth jitter-free clock that is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLKI pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either $120UI_{P-P}$ (buffer depth is 128 bits) or $28UI_{P-P}$ (buffer depth is 32 bits), then the DS2154 will divide the internal nominal 32.768MHz clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register (RIR.5).

Figure 13-1. External Analog Connections



NOTE 1: RESISTOR VALUES ARE ±1%.
NOTE 2: THE R_T RESISTORS ARE USED TO INCREASE THE TRANSMITTER RETURN LOSS OR TO PROTECT THE DEVICE FROM OVERVOLTAGE.
NOTE 3: THE R_R RESISTORS ARE USED TO TERMINATE THE RECEIVE E1 LINE.
NOTE 4: FOR 75Ω TERMINATION, R_R = 37.4Ω; FOR 120Ω TERMINATION R_R = 60Ω.
NOTE 5: SEE THE SEPARATE APPLICATION NOTE FOR DETAILS ON HOW TO CONSTRUCT A PROTECTED INTERFACE.
NOTE 6: EITHER A CRYSTAL CAN BE APPLIED ACROSS THE MCLK AND XTALD PINS OR A TTL LEVEL CLOCK CAN BE APPLIED TO JUST MCLK.
NOTE 7: C1 AND C2 SHOULD BE 5PF LOWER THAN TWO TIMES THE NOMINAL LOADING CAPACITANCE OF THE CRYSTAL TO ADJUST FOR THE INPUT CAPACITANCE OF THE DS2154.

Figure 13-2. Jitter Tolerance

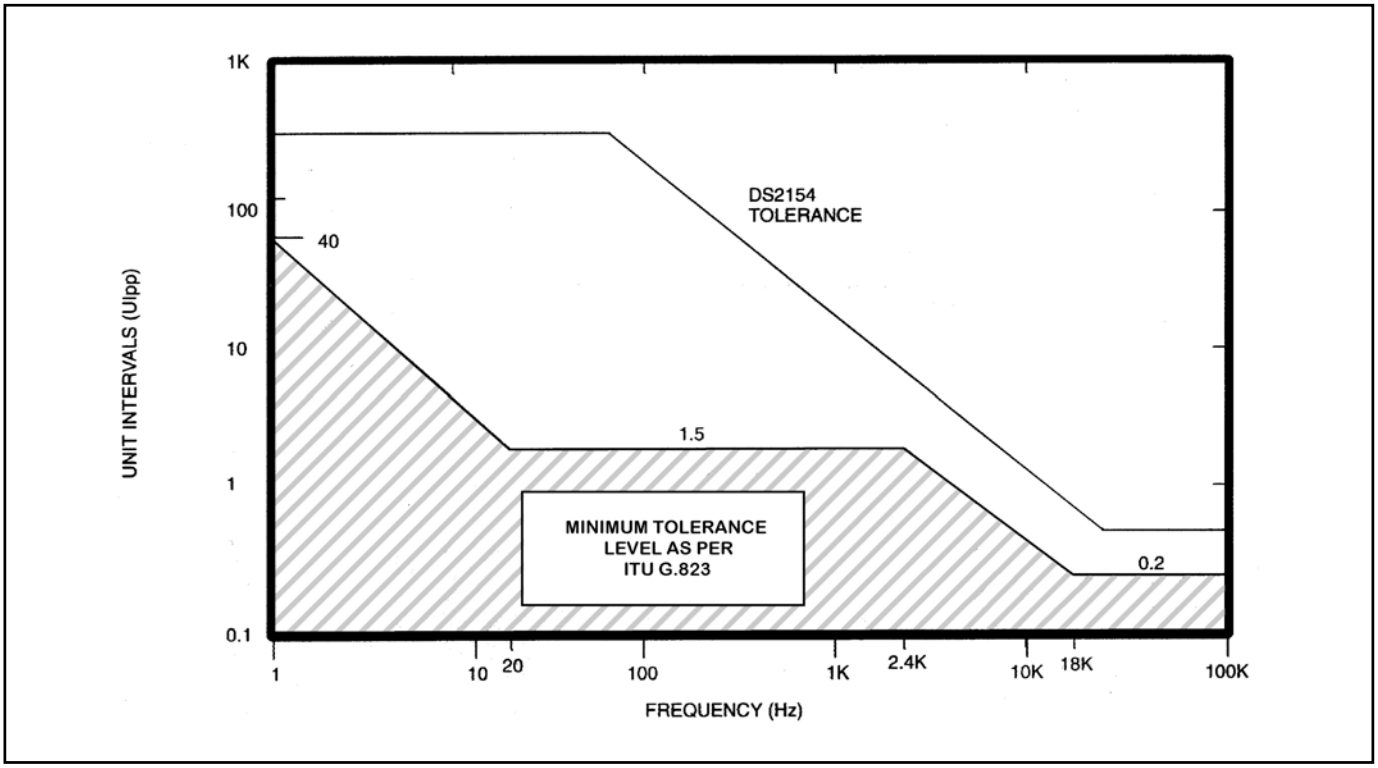


Figure 13-3. Transmit Waveform Template

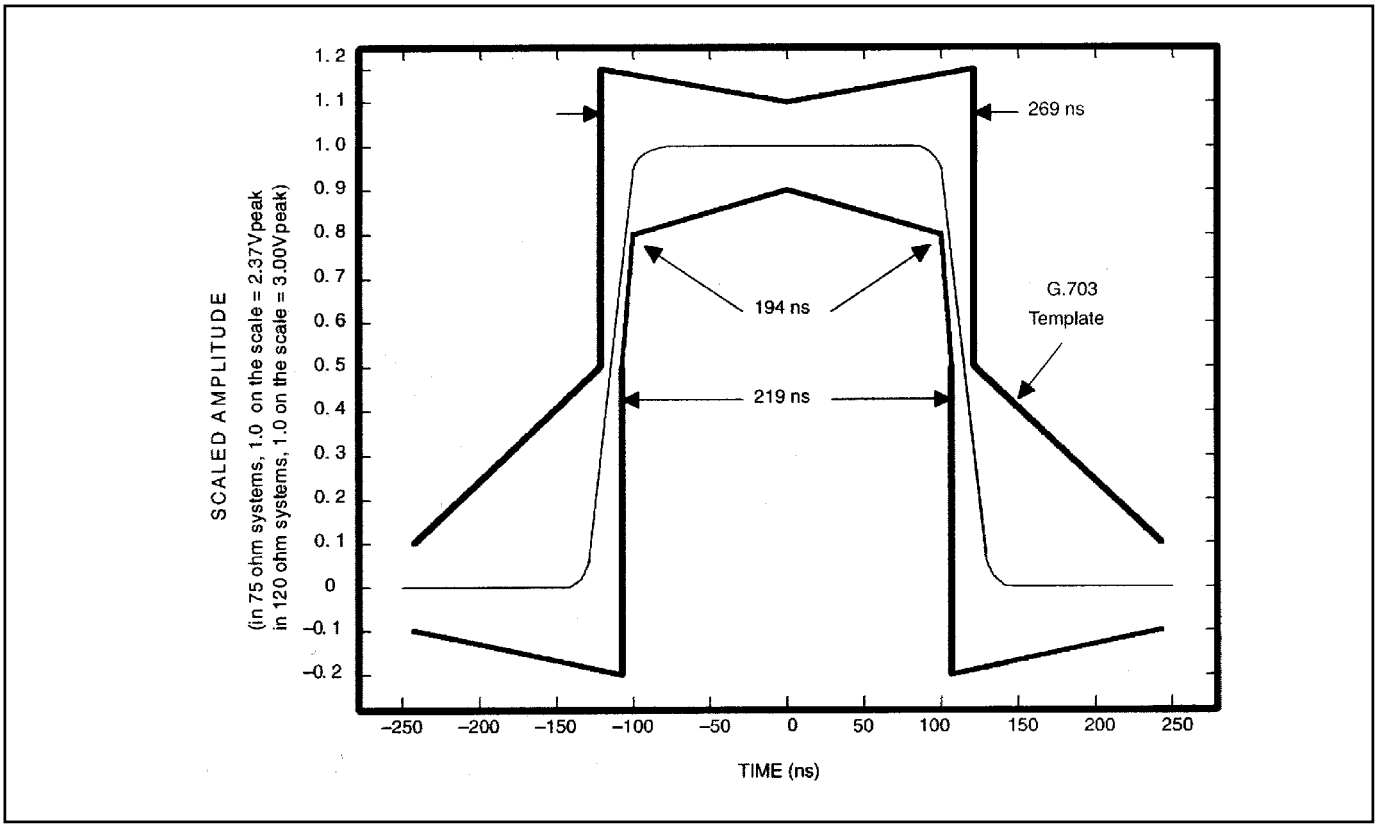
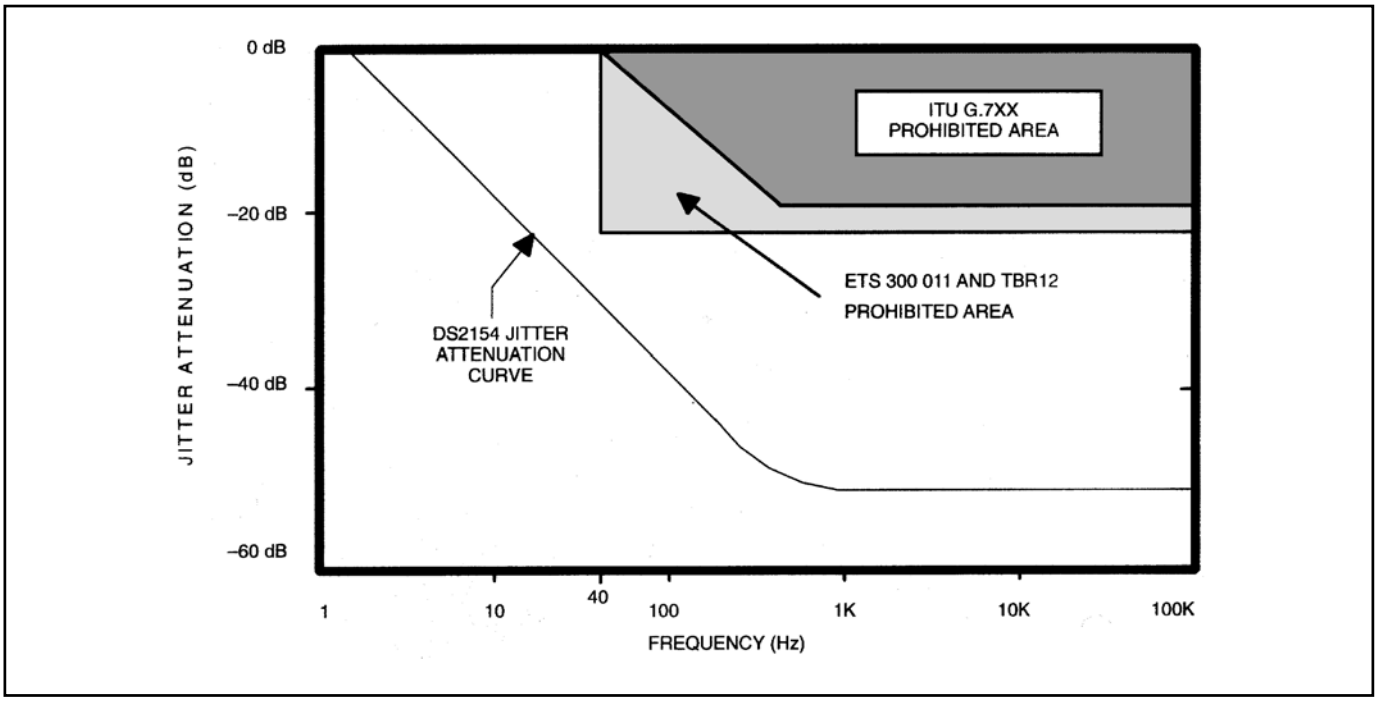
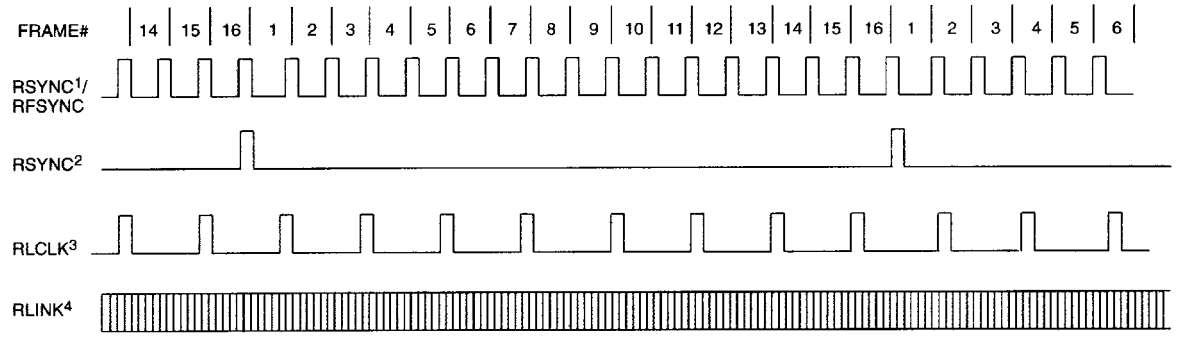


Figure 13-4. Jitter Attenuation



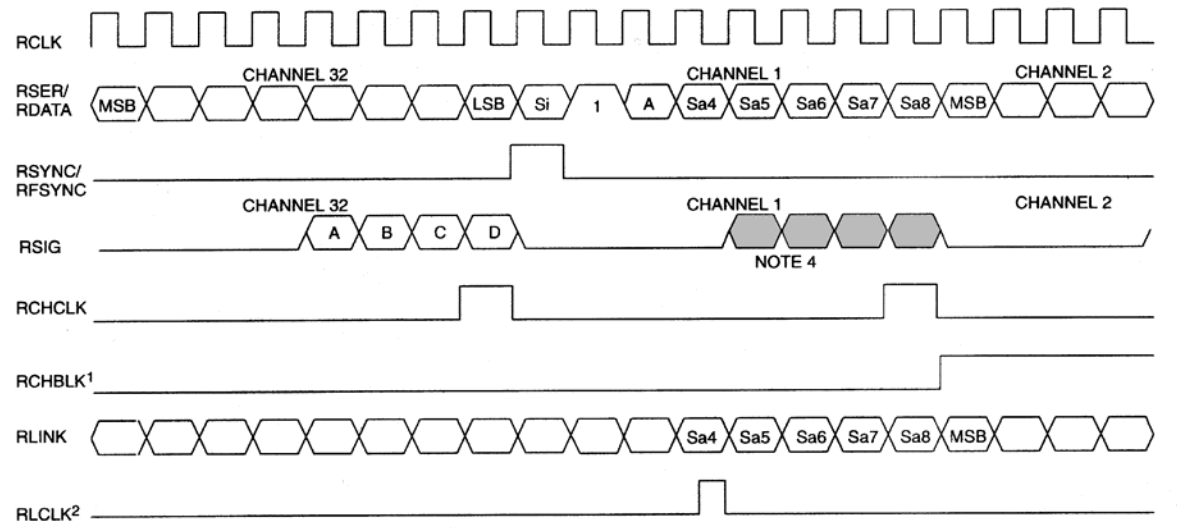
14 TIMING DIAGRAMS

Figure 14-1. Receive Side Timing



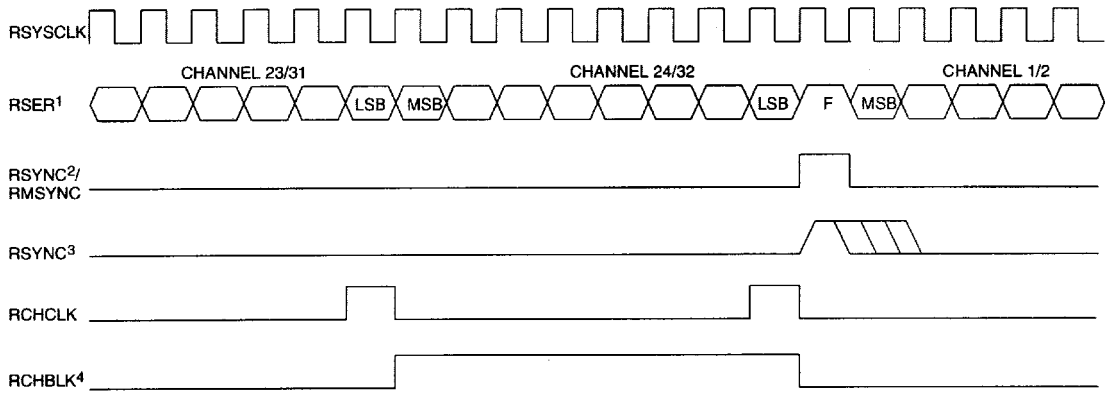
NOTE 1: RSYNC IN THE FRAME MODE (RCR1.6 = 0).
NOTE 2: RSYNC IN THE FRAME MODE (RCR1.6 = 0).
NOTE 3: RSYNC IS PROGRAMMED TO PULSE HIGH DURING THE Sa4 BIT POSITION.
NOTE 4: RLINK WILL ALWAYS OUTPUT ALL FIVE Sa BITS AS WELL AS THE REST OF THE RECEIVE DATASTREAM.
NOTE 5: THIS DIAGRAM ASSUMES THE CAS MF BEGINS WITH THE FAS WORD.

Figure 14-2. Receive Side Boundary Timing (with Elastic Store Disabled)



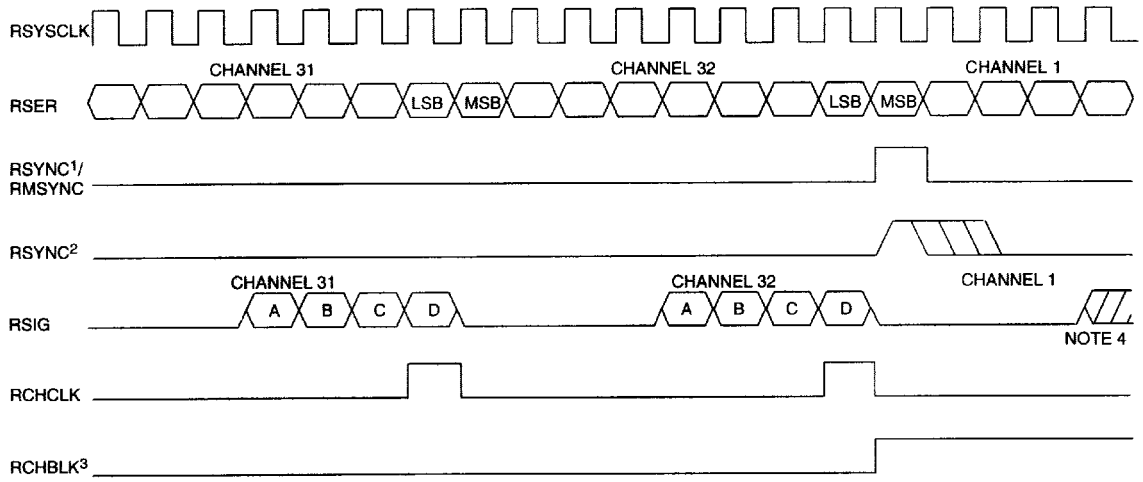
NOTE 1: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 2.
NOTE 2: RLCLK IS PROGRAMMED TO PULSE HIGH DURING THE Sa4 BITS POSITION.
NOTE 3: SHOWN IS A NON-ALIGN FRAME BOUNDARY.
NOTE 4: RSIG NORMALLY CONTAINS THE CAS MULTIFRAME ALIGNMENT NIBBLE (0000) IN CHANNEL 1.

Figure 14-3. Receive Side 1.544MHz Boundary Timing (with Elastic Store Enabled)



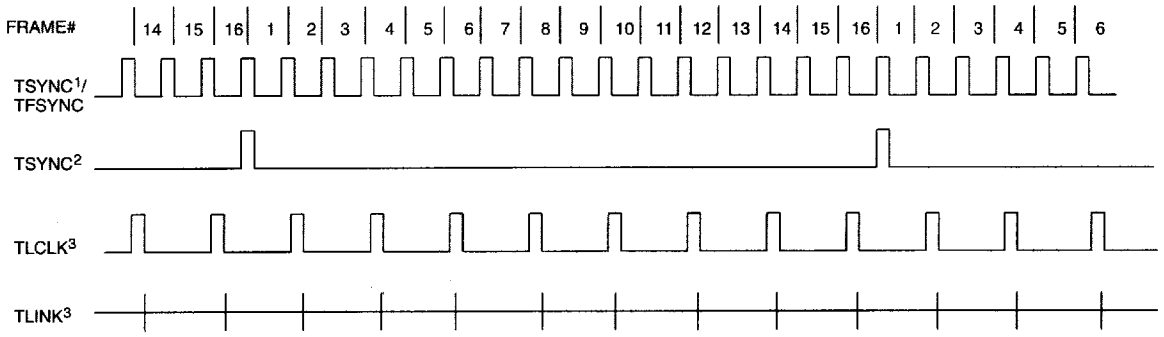
NOTE 1: DATA FROM THE E1 CHANNELS 1, 5, 9, 13, 17, 21, 25, AND 29 IS DROPPED (CHANNEL 2 FROM THE E1 LINK IS MAPPED TO CHANNEL 1 OF THE T1 LINK, ETC.) AND THE F-BIT POSITION IS ADDED (FORCED TO 1).
NOTE 2: RSYNC IS IN THE OUTPUT MODE (RCR1.5 = 0).
NOTE 3: RSYNC IS IN THE INPUT MODE (RCR1.5 = 1).
NOTE 4: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.

Figure 14-4. Receive Side 2.048MHz Boundary Timing (with Elastic Store Enabled)



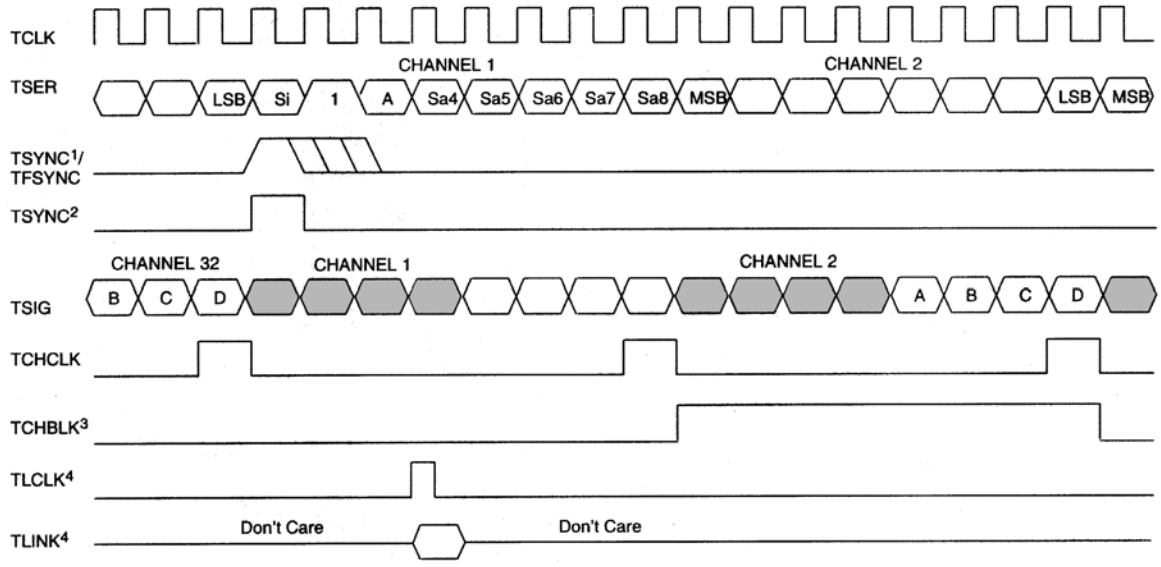
NOTE 1: RSYNC IS IN THE OUTPUT MODE (RCR1.5 = 0).
NOTE 2: RSYNC IS IN THE INPUT MODE (RCR1.5 = 1).
NOTE 3: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 1.
NOTE 4: RSIG NORMALLY CONTAINS THE CAS MULTIFRAME ALIGNMENT NIBBLE (0000) IN CHANNEL 1.

Figure 14-5. Transmit Side Timing



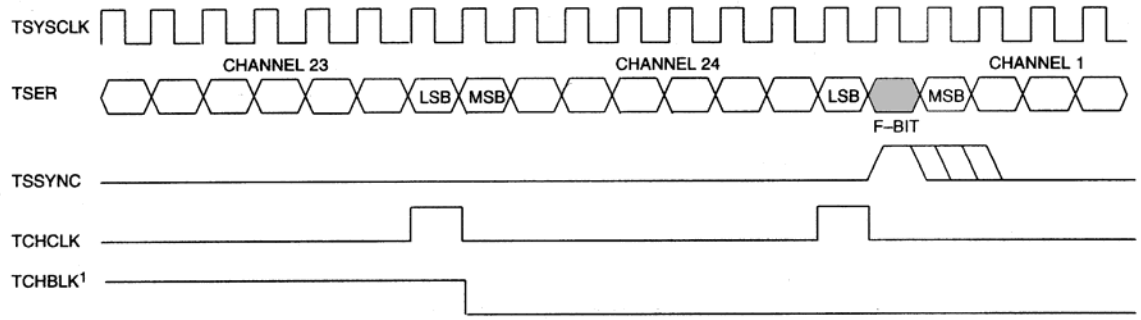
NOTE 1: TSYNC IN THE FRAME MODE (TCR1.1 = 0).
NOTE 2: TSYNC IN THE MULTIFRAME MODE (TCR1.1 = 1).
NOTE 4: TLINK IS PROGRAMMED TO SOURCE ONLY THE Sa4 BIT.
NOTE 5: THIS DIAGRAM ASSUMES BOTH THE CAS MF AND THE CRC4 BEGIN WITH THE ALIGN FRAME.

Figure 14-6. Transmit Side Boundary Timing



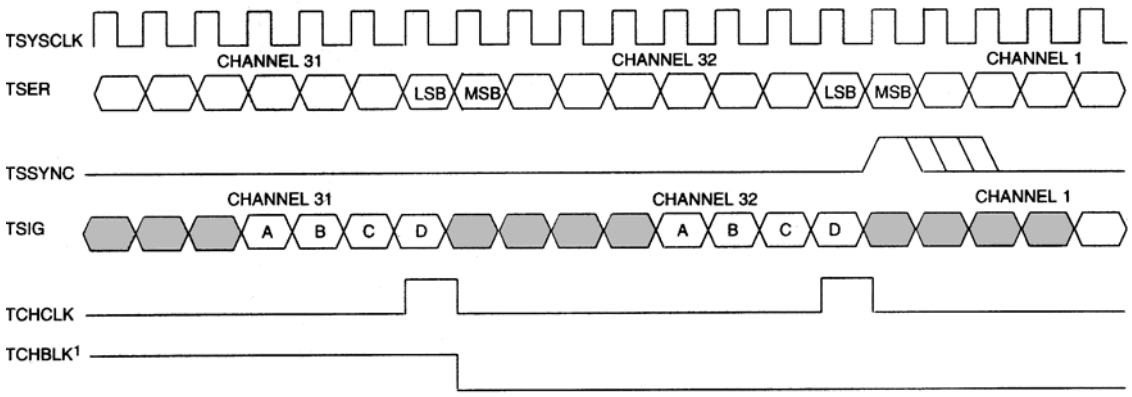
NOTE 1: TSYNC IS IN THE INPUT MODE (TCR1.0 = 0).
NOTE 2: TSYNC IS IN THE OUTPUT MODE (TCR1.0 = 1).
NOTE 3: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 2.
NOTE 4: TLINK IS PROGRAMMED TO SOURCE THE Sa4 BITS.
NOTE 5: THE SIGNALING DATA AT TSIG DURING CHANNEL 1 IS NORMALLY OVERWRITTEN IN THE TRANSMIT FORMATTER WITH THE CAS MULTIFRAME ALIGNMENT NIBBLE (0000).
NOTE 4: SHOWN IS A NON-ALIGN FRAME BOUNDARY.

Figure 14-7. Transmit Side 1.544MHz Boundary Timing (with Elastic Store Enabled)



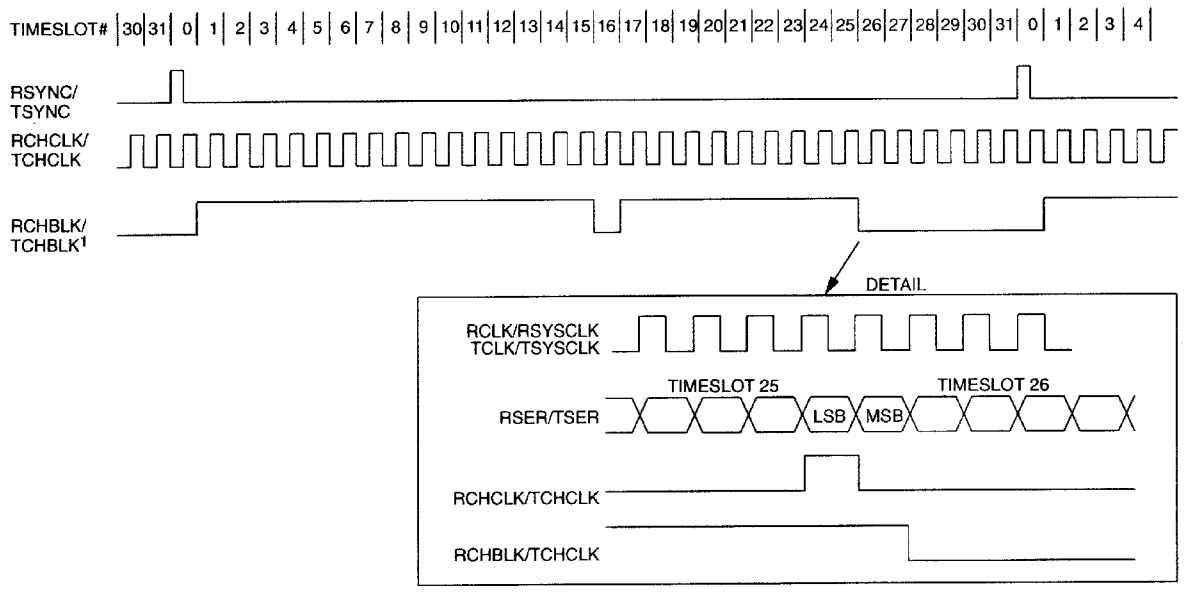
NOTE 1: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.
NOTE 2: THE F-BIT POSITION IS IGNORED BY THE DS2154.

Figure 14-8. Transmit Side 2.048MHz Boundary Timing (with Elastic Store Enabled)



NOTE 1: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 31.

Figure 14-9. G.802 Timing



NOTE 1: RCHBLK OR TCHBLK IS PROGRAMMED TO PULSE HIGH DURING TIME SLOTS 1 TO 15, 17, 25, AND DURING BIT 1 OF TIME SLOT 26.

Figure 14-10. Synchronization Flow Chart

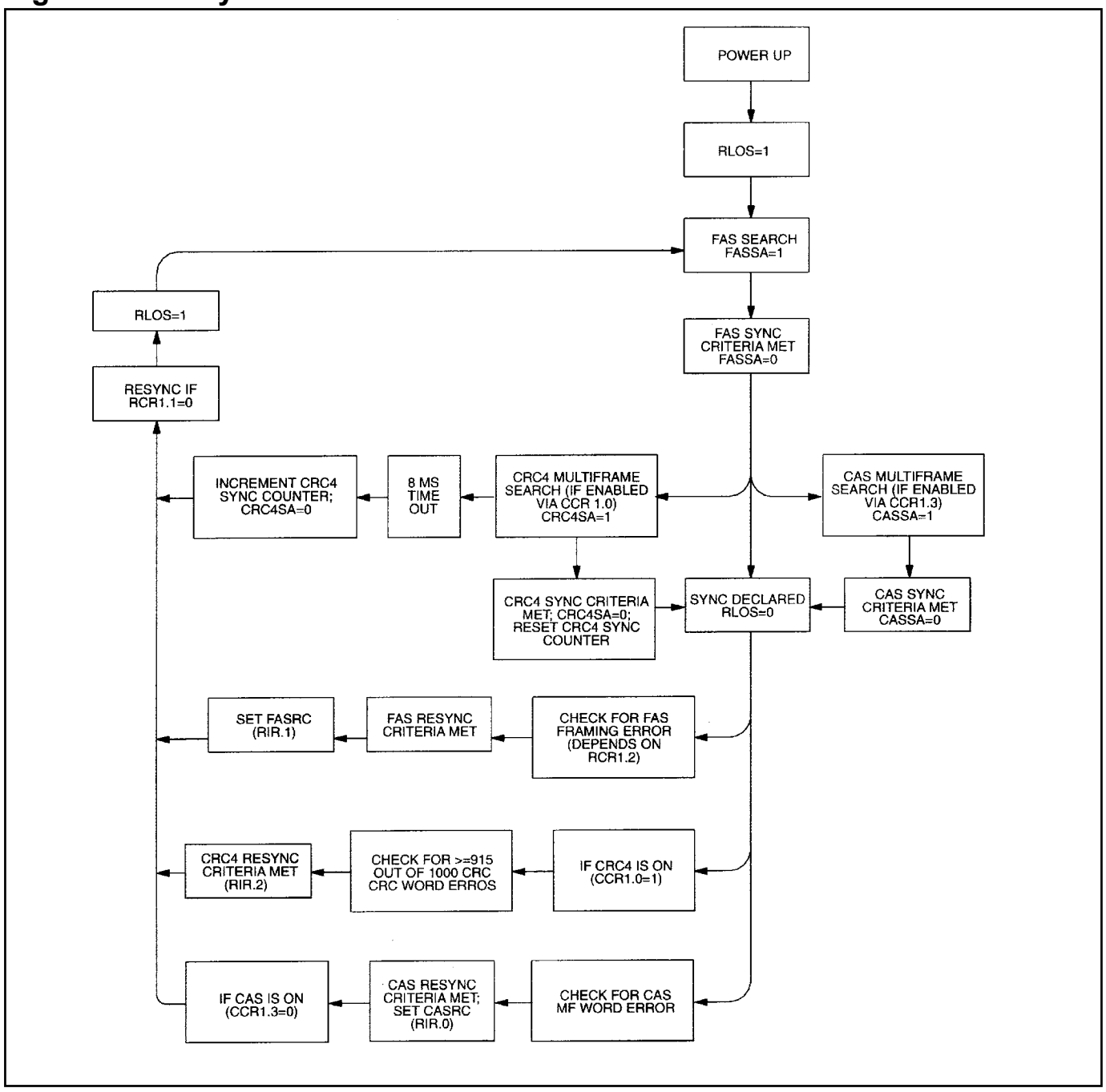
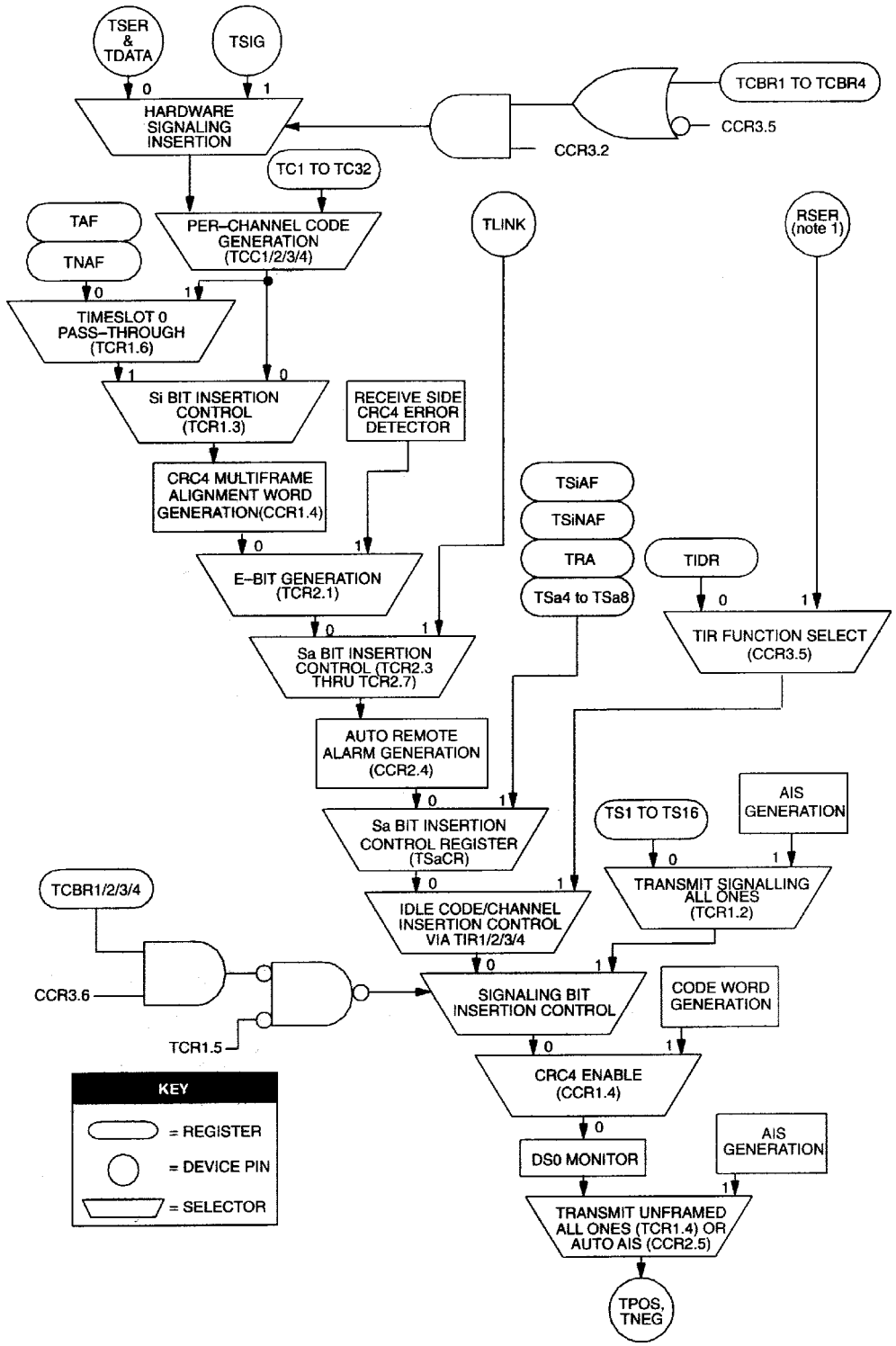


Figure 14-11. Transmit Data Flow



NOTE 1: TCLK SHOULD BE TIED TO RCLK AND TSYNC SHOULD BE TIED TO RFSYNC FOR DATA TO BE PROPERLY SOURCED FROM RSER.
NOTE 2: AUTO REMOTE ALARM IF ENABLED WILL ONLY OVERWRITE BIT 3 OF TIME SLOT 0 IN THE NON-ALIGN FRAMES IN THE ALARM NEEDS TO BE SENT.

15 DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-1.0V to +7.0V
Operating Temperature Range
Commercial……0°C to +70°C
Industrial……-40°C to +85°C
Storage Temperature……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Table 15-1. Recommended DC Operating Conditions

(T_A = 0°C to +70°C for DS2154L, T_A = -40°C to +85°C for DS2154LN.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD} + 0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.75		5.25	V	1

Table 15-2. Capacitance

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

Table 15-3. DC Characteristics

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2154L, T_A = -40°C to +85°C for DS2154LN.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current at 5V	I_{DD}		75		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. Applies to RVDD, TVDD, and DVDD.
2. TCLK = RCLK = TSYSCLK = RSYSCLK = 2.048MHz; outputs open circuited.
3. $0V < V_{IN} < V_{DD}$.
4. Applied to $\overline{INT}$ when tri-stated.

16 AC CHARACTERISTICS

Table 16-1. AC Characteristics—Multiplexed Parallel Port (MUX = 1)

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2154L, T_A = -40°C to +85°C for DS2154LN.)
(See Figure 16-1, Figure 16-2, and Figure 16-3.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS Low or $\overline{RD}$ High	PW_{EL}	100			ns	
Pulse Width, DS High or $\overline{RD}$ Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			20	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS High	t_{RWS}	50			ns	
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$ or $\overline{RD}$ active	t_{CS}	20			ns	
$\overline{CS}$ Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t_{ASL}	15			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time, DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ASED}	10			ns	
Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20		80	ns	
Data Setup Time	t_{DSW}	50			ns	

Figure 16-1. Intel Bus Read AC Timing (BTS = 0/MUX = 1)

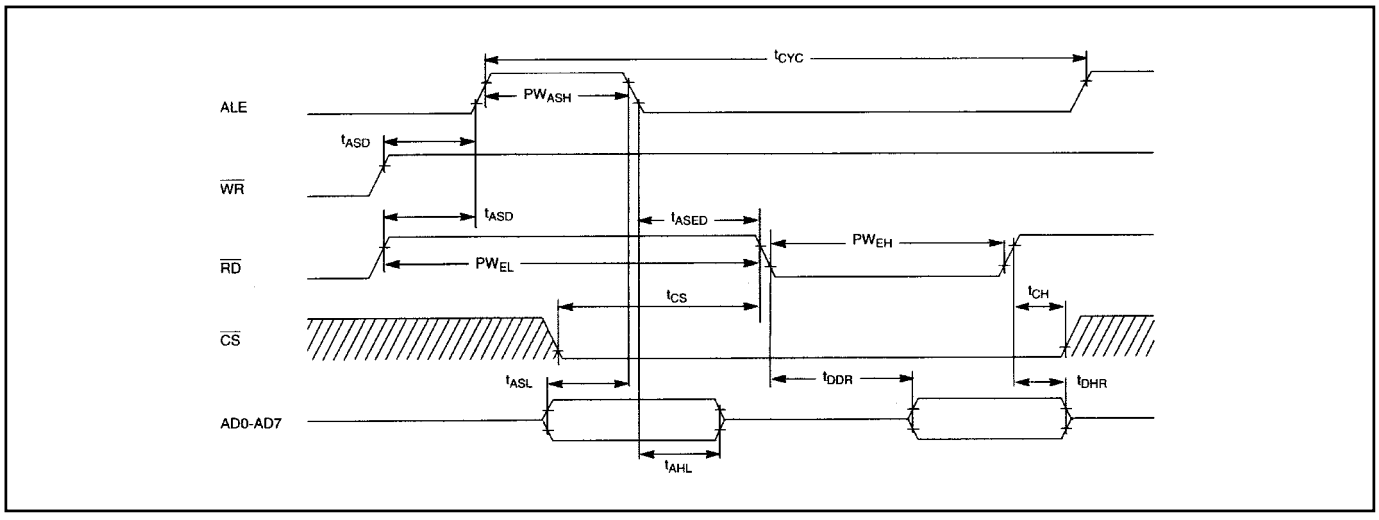


Figure 16-2. Intel Bus Write AC Timing (BTS = 0/MUX = 1)

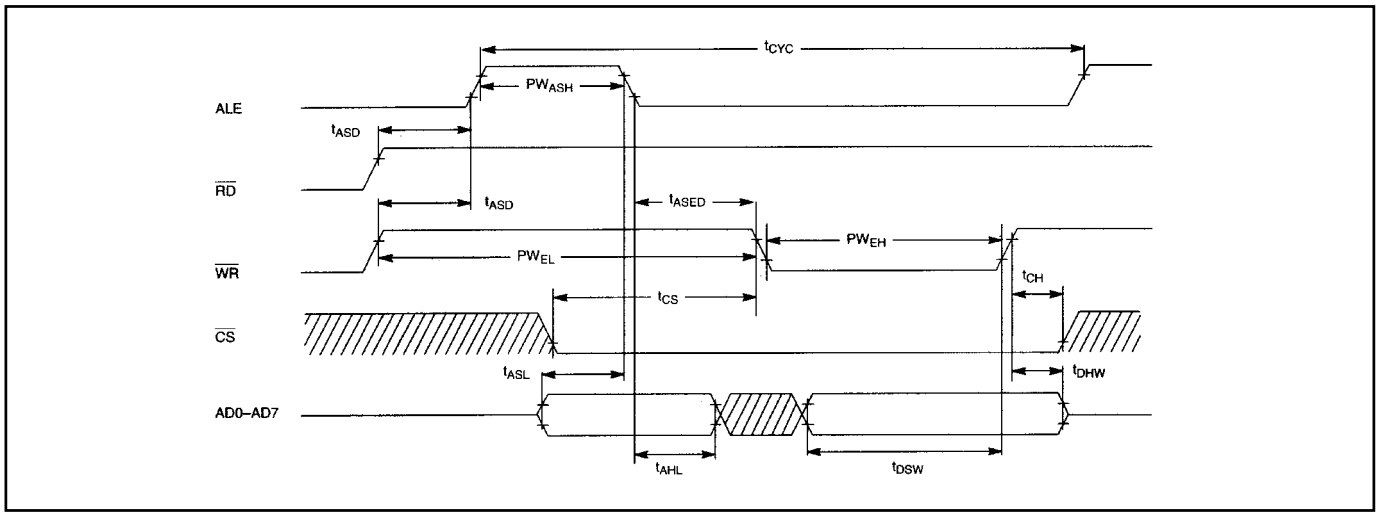


Figure 16-3. Motorola Bus AC Timing (BTS = 1/MUX = 1)

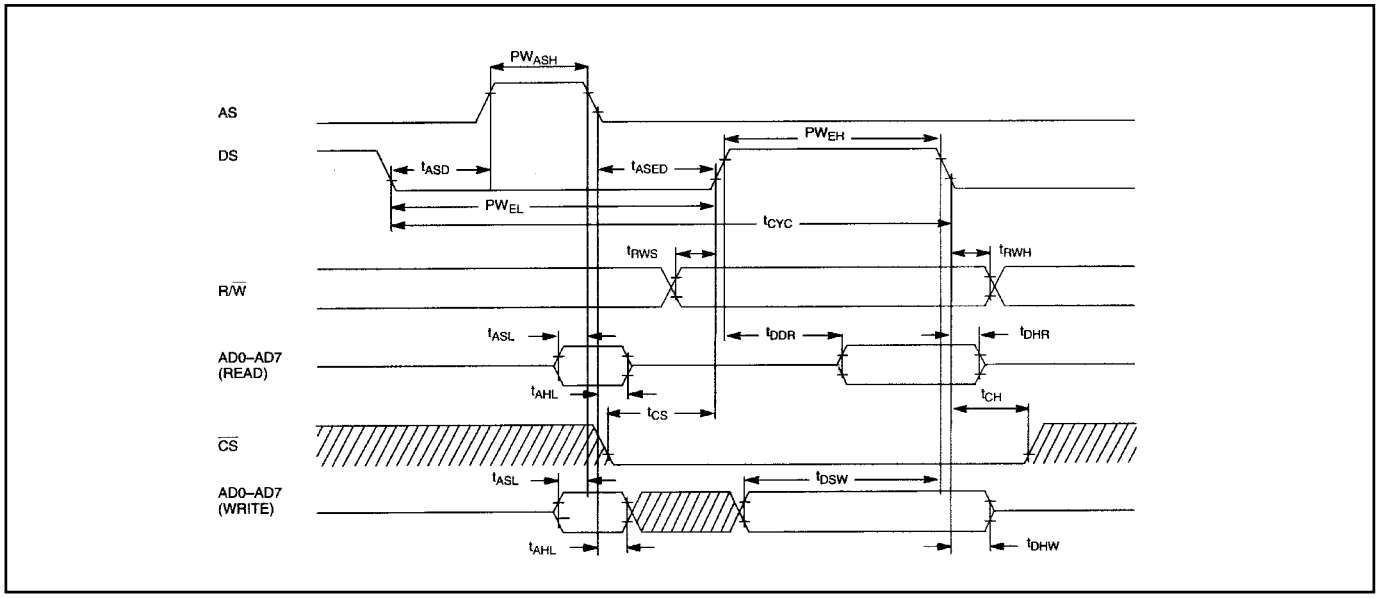


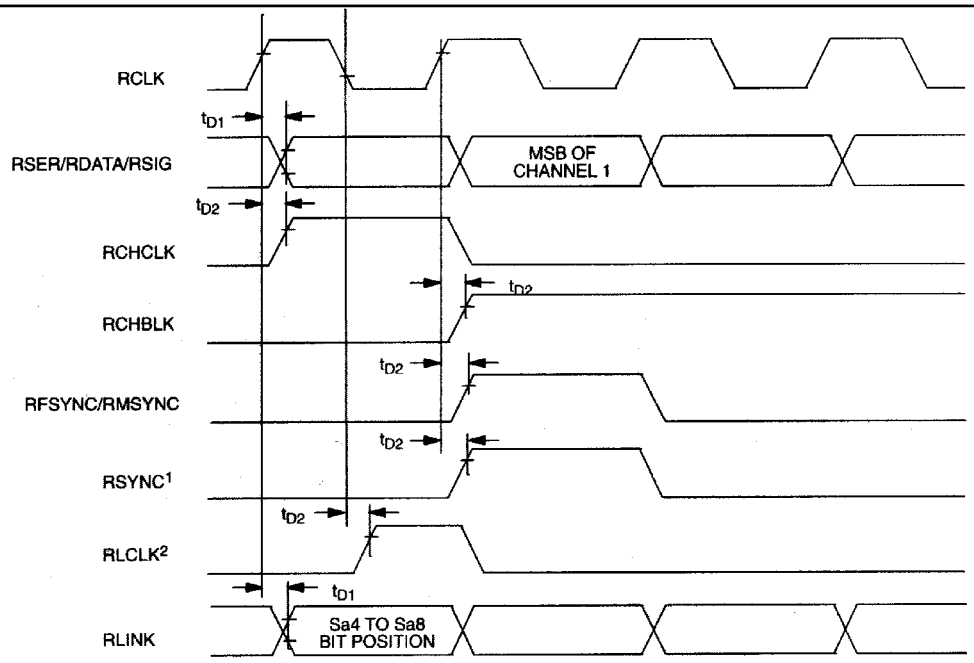
Table 16-2. AC Characteristics—Receive Side

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2154L, T_A = -40°C to +85°C for DS2154LN.)
(See Figure 16-4, Figure 16-5, and Figure 16-6.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLKO Period	t_{LP}		488		ns	
RCLKO Pulse Width	t_{LH}	200	244		ns	1
	t_{LL}	200	244		ns	1
RCLKO Pulse Width	t_{LH}	150	244		ns	2
	t_{CL}	150	244		ns	2
RCLKI Period	t_{CP}		488		ns	
RCLKI Pulse Width	t_{CH}	75			ns	
	t_{CL}	75			ns	
RSYSCLK Period	t_{SP}	122	648		ns	3
	t_{SP}	122	488		ns	4
RSYSCLK Pulse Width	t_{SH}	50			ns	
	t_{SL}	50			ns	
RSYNC Setup to RSYSCLK Falling	t_{SU}	20		t_{SH}-5	ns	
RSYNC Pulse Width	t_{PW}	50			ns	
RPOSI/RNEGI Setup to RCLKI Falling	t_{SU}	20			ns	
RPOSI/RNEGI Hold From RCLKI Falling	t_{HD}	20			ns	
RSYSCLK/RCLKI Rise and Fall Times	t_R, t_F			25	ns	
Delay RCLKO to RPOSO, RNEGO Valid	t_{DD}			50	ns	
Delay RCLK to RSER, RDATA, RSIG, RLINK Valid	t_{D1}			50	ns	
Delay RCLK to RCHCLK, RSYNC, RCHBLK, RFSYNC, RLCLK	t_{D2}			50	ns	
Delay RSYSCLK to RSER, RSIG Valid	t_{D3}			50	ns	
Delay RSYSCLK to RCHCLK, RCHBLK, RMSYNC, RSYNC	t_{D4}			50	ns	

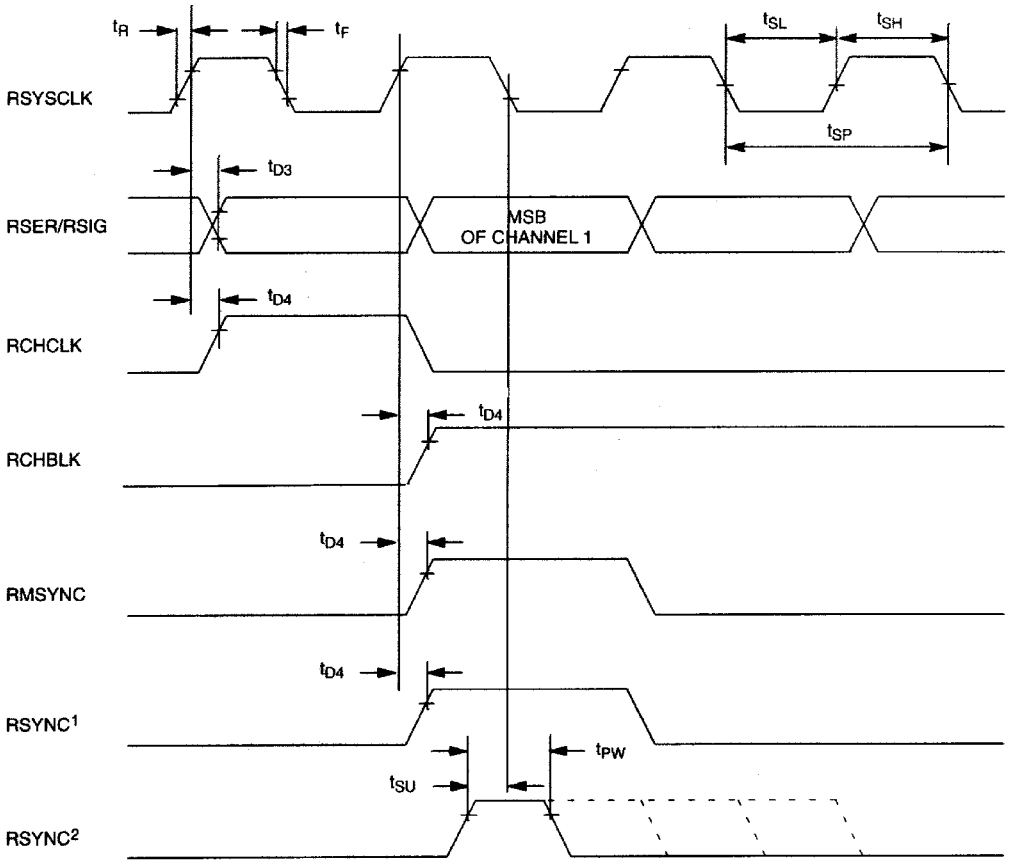
NOTES:
1) Jitter attenuator enabled in the receive path.
2) Jitter attenuator disabled or enabled in the transmit path.
3) RSYSCLK = 1.544MHz.
4) RSYSCLK = 2.048MHz.

Figure 16-4. Receive Side AC Timing



NOTE 1: RSYNC IS IN THE OUTPUT MODE (RCR1.5 = 0).
NOTE 2: RLCLK ONLY PULSES HIGH DURING Sa BIT LOCATIONS AS DEFINTED IN RCR2; NO RELATIONSHIP BETWEEN RLCLK AND RSYNC OR RFSYNC IS IMPLIED.

Figure 16-5. Receive System Side AC Timing



NOTE 1: RSYNC IS IN THE OUTPUT MODE (RCR1.5 = 0).
NOTE 2: RSYNC IS IN THE INPUT MODE (RCR1.5 = 1).

Figure 16-6. Receive Line Interface AC Timing

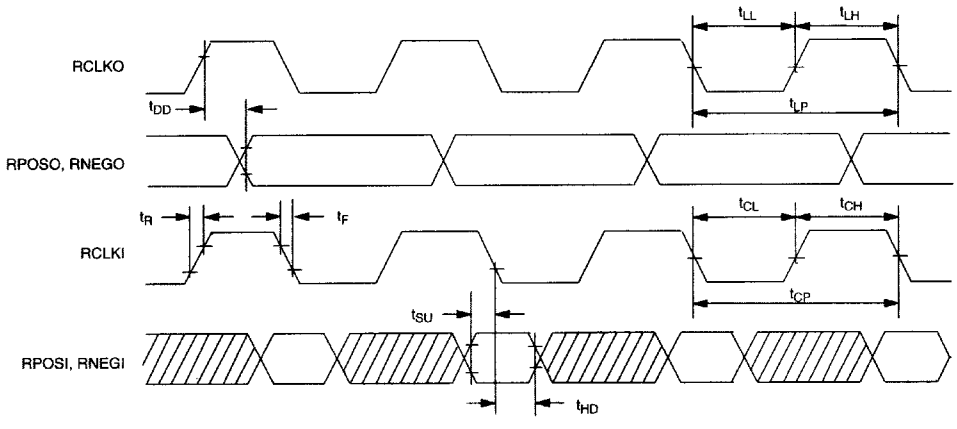


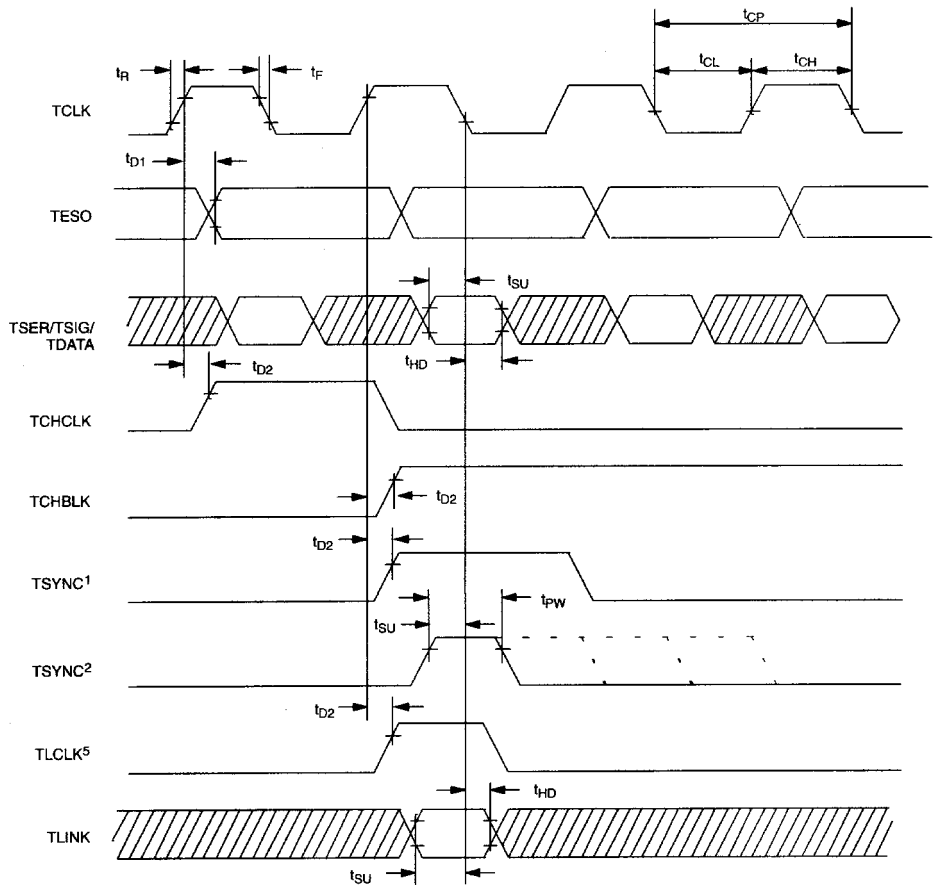
Table 16-3. AC Characteristics—Transmit Side

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2154L, T_A = -40°C to +85°C for DS2154LN.)
(See Figure 16-7, Figure 16-8, and Figure 16-9.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		488		ns	
TCLK Pulse Width	t_{CH}	75			ns	
	t_{CL}	75			ns	
TCLKI Period	t_{LP}		488		ns	
TCLKI Pulse Width	t_{LH}	75			ns	
	t_{LL}	75			ns	
TSYSCLK Period	t_{SP}	122	648		ns	1
	t_{SP}	122	448		ns	2
TSYSCLK Pulse Width	t_{SH}	50			ns	
	t_{SL}	50			ns	
TSYNC or TSSYNC Setup to TCLK or TSYSCLK Falling	t_{SU}	20		t_{CH}-5 or t_{SH}-5	ns	
TSYNC or TSSYNC Pulse Width	t_{PW}	50			ns	
TSER, TSIG, TDATA, TLINK, TPOSI, TNEGI Setup to TCLK, TSYSCLK, TCLKI Falling	t_{SU}	20			ns	
TSER, TSIG, TDATA, TLINK, TPOSI, TNEGI Hold from TCLK, TSYSCLK, TCLKI Falling	t_{HD}	20			ns	
TCLK, TCLKI, or TSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay TCLKO to TPOSO, TNEGO Valid	t_{DD}			50	ns	
Delay TCLK to TESO Valid	t_{D1}			50	ns	
Delay TCLK to TCHBLK, TCHBLK, TSYNC, TLCLK	t_{D2}			50	ns	
Delay TSYSCLK to TCHCLK, TCHBLK	t_{D3}			75	ns	

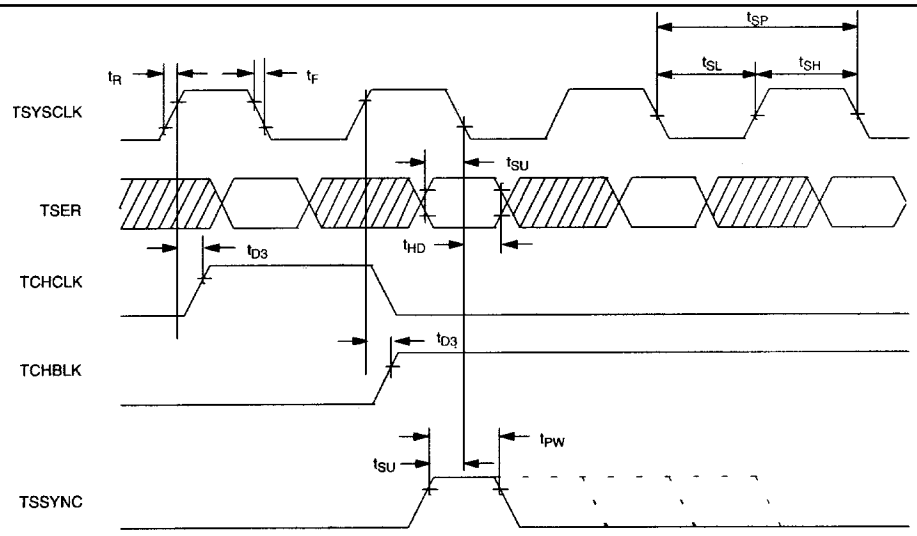
NOTES:
1) TSYSCLK = 1.544MHz.
2) TSYSCLK = 2.048MHz.

Figure 16-7. Transmit Side AC Timing



NOTE 1: TSYNC IS IN THE OUTPUT MODE (TCR1.0 = 1).
NOTE 2: TSYNC IS IN THE INPUT MODE (TCR1.0 = 0).
NOTE 3: TSER IS SAMPLED ON THE FALLING EDGE OF TCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS DISABLED.
NOTE 4: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS DISABLED.
NOTE 5: TLINK IS ONLY SAMPLED DURING Sa-BIT LOCATIONS AS DEFINED IN TCR2. NO RELATIONSHIP BETWEEN TLCLK/TLINK AND TSYNC IS IMPLIED.

Figure 16-8. Transmit System Side AC Timing



NOTE 1: TSER IS ONLY SAMPLED ON THE FALLING EDGE OF TSYSCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS ENABLED.
NOTE 2: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TSYSCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS ENABLED.

Figure 16-9. Transmit Line Interface Side AC Timing

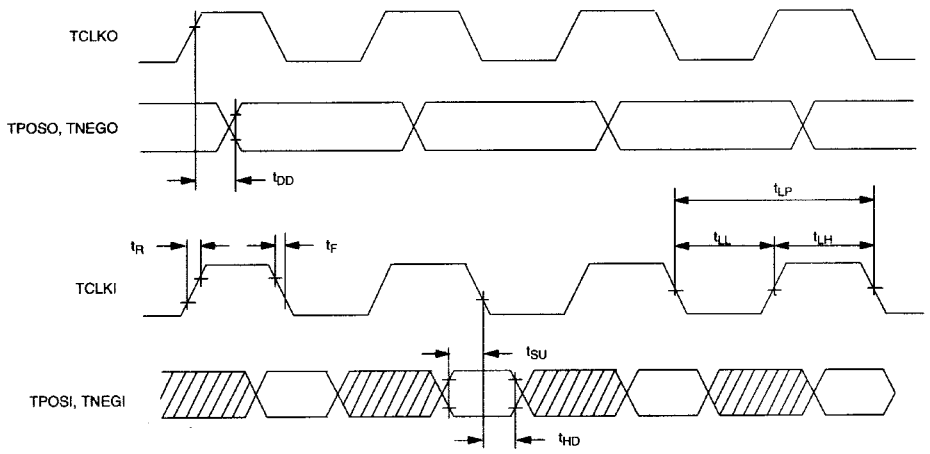


Table 16-4. AC Characteristics—Nonmultiplexed Parallel Port (MUX = 0)

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2154L, T_A = -40°C to +85°C for DS2154LN.)
(See Figure 16-10, Figure 16-11, Figure 16-12, and Figure 16-13.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Setup Time for A0 to A7 Valid to $\overline{CS}$ Active	t1	0			ns	
Setup Time for $\overline{CS}$ Active to Either $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Active	t2	0			ns	
Delay Time from Either $\overline{RD}$ or $\overline{DS}$ Active to Data Valid	t3			75	ns	
Hold Time from Either $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Inactive to $\overline{CS}$ Inactive	t4	0			ns	
Hold Time from $\overline{CS}$ Inactive to Data Bus Tri-State	t5	5		20	ns	
Wait Time from Either $\overline{WR}$ or $\overline{DS}$ Active to Latch Data	t6	75			ns	
Data Setup Time to Either $\overline{WR}$ or $\overline{DS}$ Inactive	t7	10			ns	
Data Hold Time to Either $\overline{WR}$ or $\overline{DS}$ Inactive	t8	10			ns	
Address Hold from Either $\overline{WR}$ or $\overline{DS}$ Inactive	t_9	10			ns	

Figure 16-10. Intel Bus Read AC Timing (BTS = 0/MUX = 0)

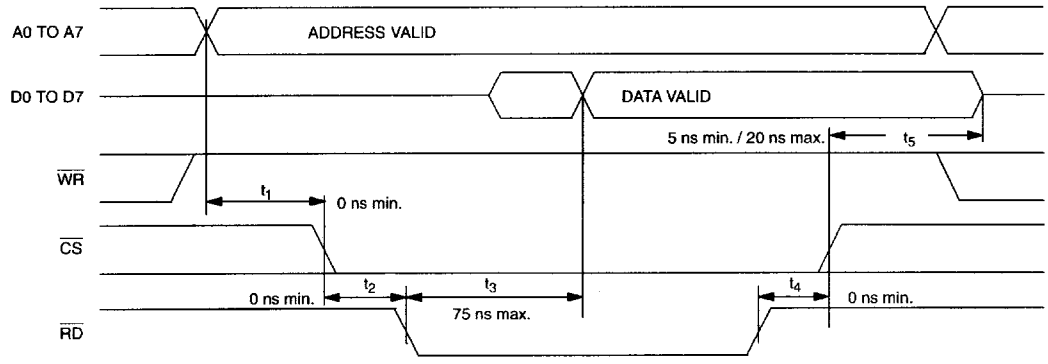


Figure 16-11. Intel Bus Write AC Timing (BTS=0/MUX=0)

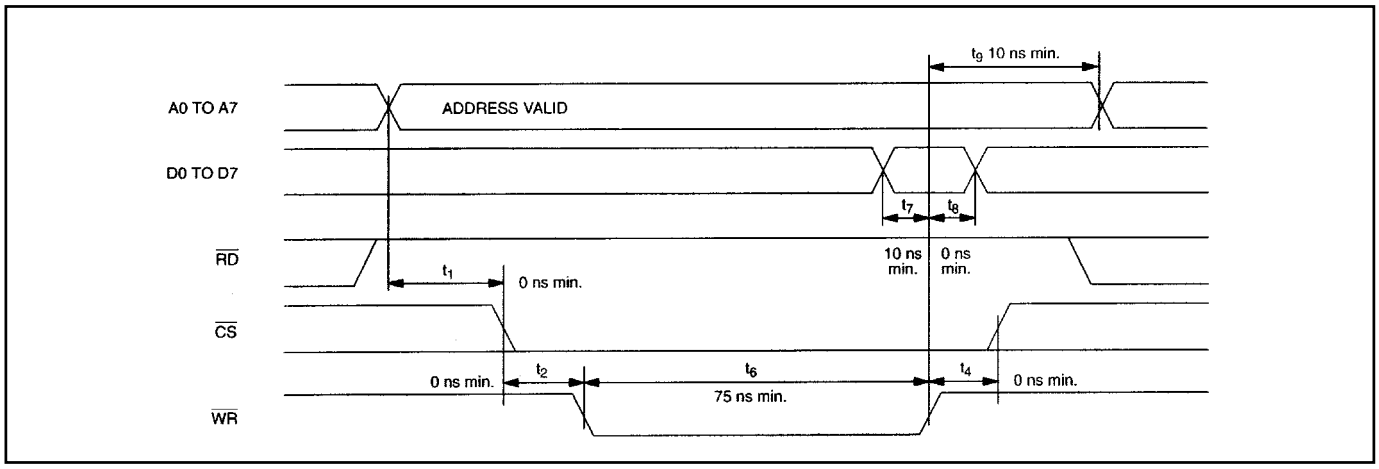


Figure 16-12. Motorola Bus Read AC Timing (BTS = 1/MUX = 0)

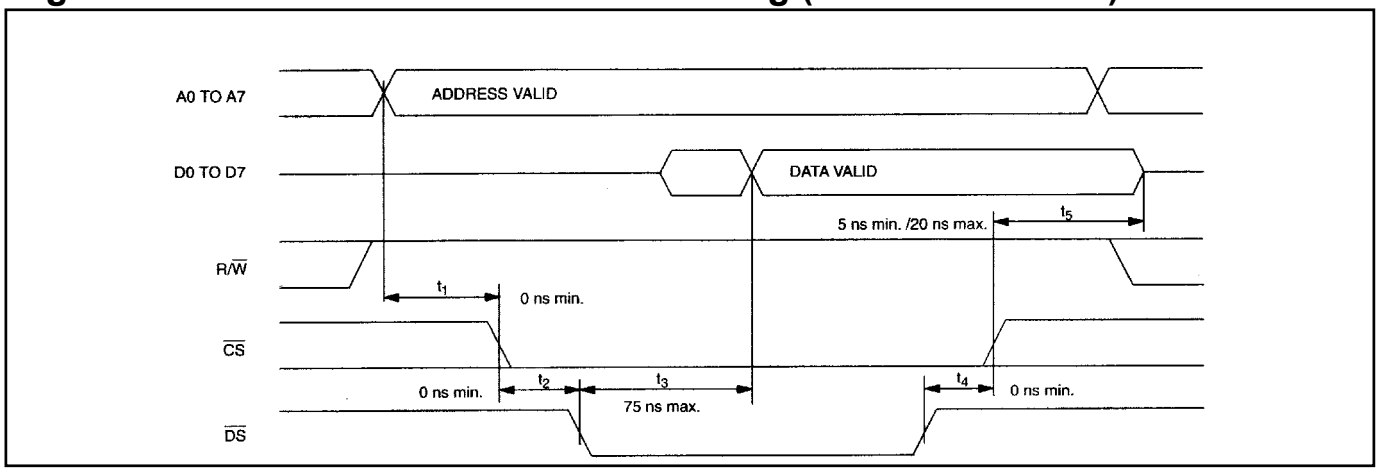
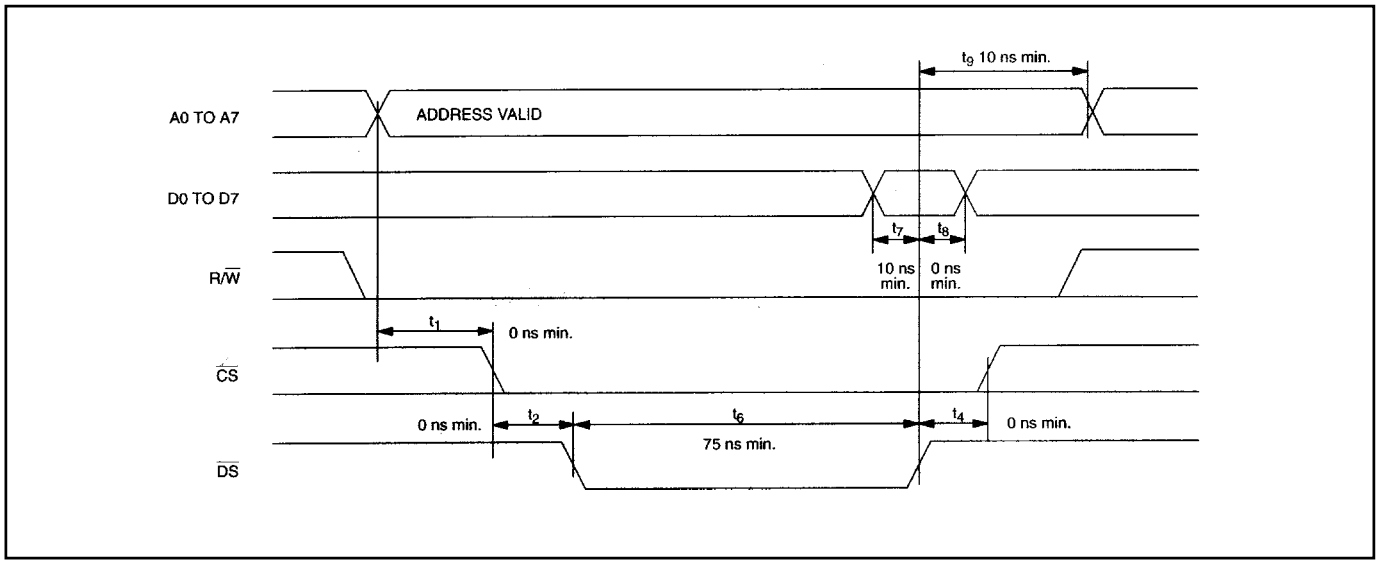


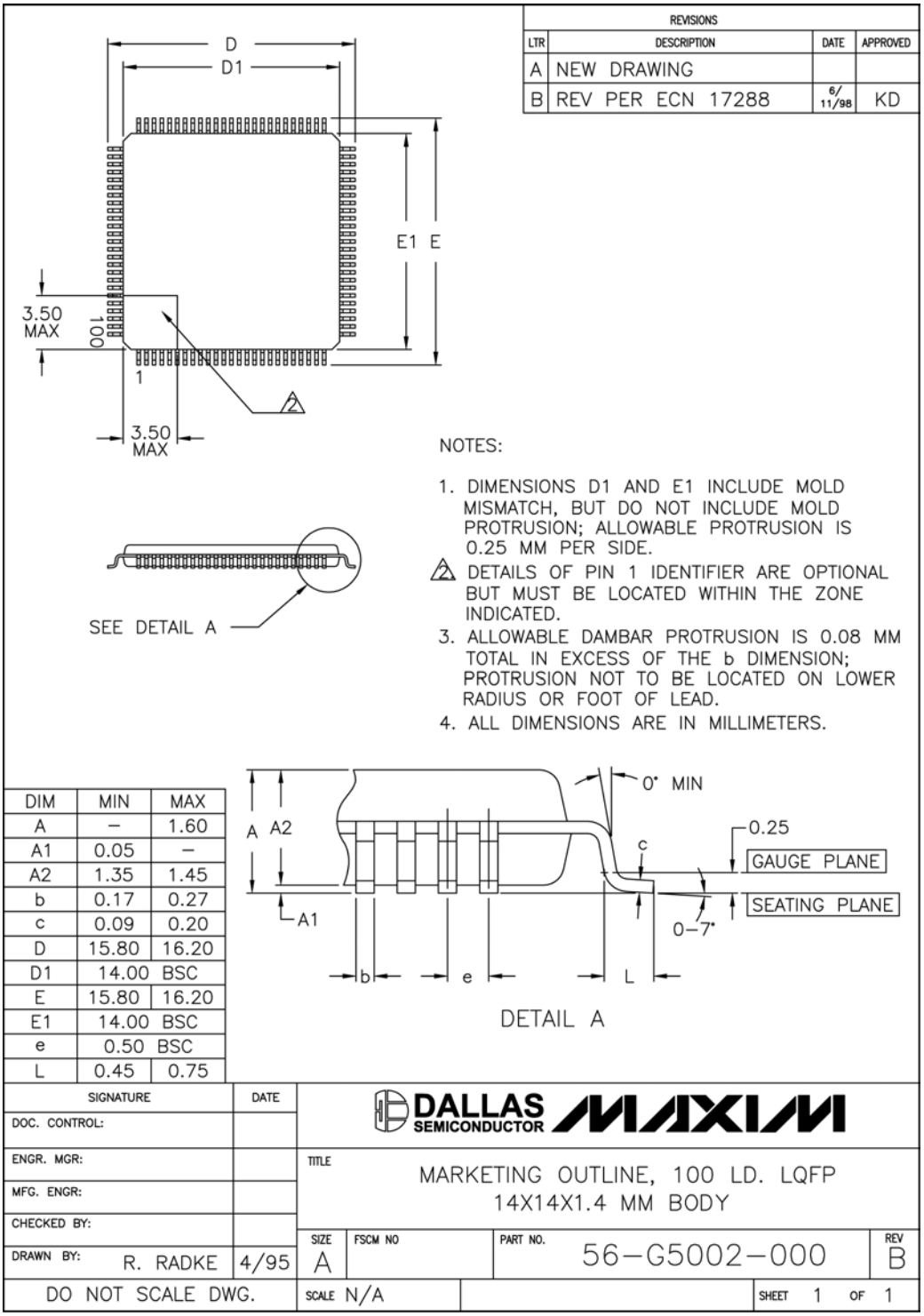
Figure 16-13. Motorola Bus Write AC Timing (BTS = 1/MUX = 0)



17 PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

17.1 100-Pin LQFP (56-G5002-000)



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