19-2485; Rev 1; 10/02

MAXIM

Triple-Output TFT LCD Power Supply with Fault Protection

General Description

The MAX1889 provides the three regulated output voltages required for active matrix, thin-film transistor liquid crystal displays (TFT LCDs). It combines a high-performance step-up regulator with two linear-regulator controllers and multiple levels of protection circuitry for a complete power-supply system.

The main DC-DC converter is a high-frequency (500kHz/1MHz), current-mode step-up regulator with an integrated N-channel power MOSFET that allows the use of ultra-small inductors and ceramic capacitors. With its high closed-loop bandwidth performance, the MAX1889 provides fast transient response to pulsed loads while operating with efficiencies over 85%. The positive and negative linear-regulator controllers post-regulate charge-pump outputs for TFT gate-on and gate-off supplies.

The MAX1889 has a unique input switch control that can replace the typical input fuse by disconnecting the load from the input supply when a fault is detected. The fault detector monitors all three regulated output voltages and can monitor current from the input supply as well. Additionally, the MAX1889 enters thermal shutdown when its overtemperature threshold is reached.

The MAX1889 undervoltage lockout is set at 2.5V (max) to allow the input supply to droop under pulsed load conditions while avoiding any unexpected behavior when its input voltage dips momentarily. Also, the built-in soft-start and cycle-by-cycle current limiting prevent input surge currents during power-up.

The MAX1889 is available in a 16-pin thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panel design.

Applications

Notebook Computer Displays

LCD Monitors

Car Navigation Displays

Features

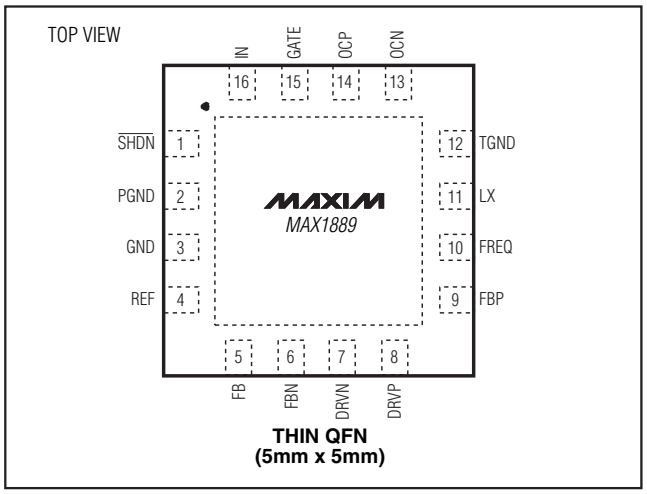
- **High-Performance Step-Up Regulator**
  - **Fast Transient Response**
  - **Current-Mode Control Architecture**
  - **Built-In High-Efficiency N-Channel Power MOSFET**
  - **Current-Limit Comparator**
  - **>85% Efficiency**
  - **Selectable Switching Frequency (500kHz/1MHz)**
  - **Internal Soft-Start**
- **Positive Linear-Regulator Controller**
- **Negative Linear-Regulator Controller**
- **Triple-Level Protection Against Smoke or Fire**
  - **Input Switch Replaces Input Fuse**
  - **Output Overload Detection with Timer Latch**
  - **Thermal Shutdown**
- **2.7V to 5.5V Input Operating Range**
- **Ultra-Small External Components**
- **1µA Shutdown Current (max)**
- **1mA Quiescent Current (max)**
- **Ultra-Thin 16-Pin QFN Package (0.8mm Maximum Thickness)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1889ETE	-40°C to +85°C	16 Thin QFN (5mm × 5mm)
MAX1889EGE*	-40°C to +85°C	16 QFN (5mm × 5mm)

** Future product—Contact factory for availability.*

Pin Configuration



THIN QFN (5mm x 5mm)

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Triple-Output TFT LCD Power Supply with Fault Protection

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, OCN, OCP,
FB, FBP, FBN, FREQ to GND .....-0.3V to +6V
PGND to GND.....±0.3V
LX to PGND .....-0.3V to +14V
DRVP to GND .....-0.3V to +30V
REF, GATE, TGND to GND.....-0.3V to (V_{IN} + 0.3V)
DRVN to GND .....(V_{IN} - 28V) to (V_{IN} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
16-Pin QFN (derate 19.2mW/°C above +70°C) 1538mW
Operating Temperature Range
MAX1889EGE .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, $\overline{SHDN}$ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range	V_{IN}			2.7		5.5	V
IN Undervoltage Lockout (UVLO) Threshold	V_{UVLO}	350mV typical hysteresis	V_{IN} rising	2.55	2.7	2.85	V
			V_{IN} falling	2.2	2.35	2.5	
IN Quiescent Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = 0V (Note 1)				1.0	mA
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V			0.1	1.0	µA
REF Output Voltage	V_{REF}	-2µA < I_{REF} < 50µA		1.231	1.250	1.269	V
Thermal Shutdown					160		°C
MAIN STEP-UP REGULATOR							
Main Output Voltage Range	V_{MAIN}			V_{IN}		13	V
Operating Frequency	f_{OSC}	V_{FREQ} = V_{IN}		0.85	1	1.15	MHz
		V_{FREQ} = 0V			500		kHz
Oscillator Maximum Duty Cycle				80	85	90	%
FB Regulation Voltage	V_{FB}	I_{LX} = 200mA, slope = 0 (Note 2)		1.229	1.242	1.254	V
FB Fault Trip Level		V_{FB} falling		0.95	1.0	1.05	V
Load Regulation		I_{MAIN} = 0 to full load			-1.6		%
Line Regulation		V_{IN} = 2.7V to 5.5V			0.2		%/V
FB Input Bias Current	I_{FB}	V_{FB} = 1.5V		-100		+100	nA
LX Switch On-Resistance	$R_{LX(ON)}$				250	450	mΩ
LX Leakage Current	I_{LX}	V_{LX} = 13V			0.01	20	µA
LX Current Limit	I_{LIM}			1.6	2.1	2.8	A
LX RMS Current Rating		Not tested				1.4	A
Soft-Start Period	t_{SS}				4096 / f_{OSC}		s
Soft-Start Step Size					V_{REF} /32		V
POSITIVE LINEAR-REGULATOR CONTROLLER							
FBP Regulation Voltage	V_{FBP}	I_{DRVP} = 0.2mA		1.213	1.25	1.288	V
FBP Fault Trip Level		V_{FBP} falling		0.96	1.0	1.04	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.25V		-50		+50	nA
FBP Effective Transconductance		V_{DRVP} = 10V, I_{DRVP} = 0.1mA to 2mA		75			mS

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, $\overline{SHDN}$ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBP Line Regulation		I_{DRVP} = 0.2mA, V_{IN} = 2.7V to 5.5V		1		mV
Bandwidth		(Note 3)	200			kHz
DRVP Sink Current	I_{DRVP}	V_{FBP} = 1.1V, V_{DRVP} = 10V	5			mA
DRVP Off-Leakage Current		V_{FBP} = 1.1V, V_{DRVP} = 28V		0.1	10	µA
NEGATIVE LINEAR-REGULATOR CONTROLLER						
FBN Regulation Voltage	V_{FBN}	I_{DRVN} = 0.2mA	95	125	155	mV
FBN Fault Trip Level		V_{FBN} rising	325	400	475	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0V	-50		+50	nA
FBN Effective Transconductance		V_{DRVN} = -10V, I_{DRVN} = 0.1mA to 2mA	75			mS
FBN Line Regulation		I_{DRVN} = 0.2mA, V_{IN} = 2.7V to 5.5V		1		mV
Bandwidth		(Note 2)	200			kHz
DRVN Sink Current	I_{DRVN}	V_{FBN} = 200mV, V_{DRVN} = -10V	5			mA
DRVN Off-Leakage Current		V_{FBP} = -0.1V, V_{DRVN} = -20V		0.1	10	µA
LOGIC SIGNAL ($\overline{SHDN}$)						
Input Low Voltage		100mV typical hysteresis, V_{IN} = 2.7V to 5.5V			0.4	V
Input High Voltage		V_{IN} = 2.7V to 5.5V	1.6			V
Input Current	$I_{\overline{SHDN}}$			0.01	1	µA
LOGIC SIGNAL (FREQ)						
Input Low Voltage		0.15 x V_{IN} typical hysteresis			0.3 x V_{IN}	V
Input High Voltage			0.7 x V_{IN}			V
Input Current	I_{FREQ}			0.01	1	µA
OVERCURRENT COMPARATOR						
Input Offset Voltage			-5		+5	mV
Input Bias Current	I_{OCN}, I_{OCP}	V_{OCN} = V_{OCP} = V_{IN}	-50		+50	nA
OCN, OCP Input Common-Mode Range			1.5		0.8 x V_{IN}	V
FAULT TIMER AND GATE DRIVER						
Fault Timer Period	t_{FAULT}	V_{FREQ} = 0V, 32768/f_{OSC}		64		ms
		V_{FREQ} = V_{IN}, 65536/f_{OSC}		64		
GATE Output Sink Current During Slew	I_{GATE}	V_{GATE} = 1.5V, during turn-on transition	6	12	18	µA
GATE Output Pulldown Resistance		V_{GATE} < 0.5V			200	Ω
GATE Output Pullup Resistance					200	Ω

Triple-Output TFT LCD Power Supply with Fault Protection

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, $\overline{SHDN}$ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = -40°C to +85°C**.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
IN Supply Range	V_{IN}		2.7	5.5	V
IN ULVO Threshold	V_{UVLO}	V_{IN} rising	2.55	2.85	V
		V_{IN} falling	2.2	2.5	
IN Quiescent Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = 0V (Note 1)		1.0	mA
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V		1.0	µA
REF Output Voltage	V_{REF}	-2µA < I_{REF} < 50µA	1.231	1.269	V
MAIN STEP-UP REGULATOR					
Main Output Voltage Range	V_{MAIN}		V_{IN}	13	V
Operating Frequency	f_{OSC}	V_{FREQ} = V_{IN}	0.75	1.25	MHz
Oscillator Maximum Duty Cycle			78	92	%
FB Regulation Voltage	V_{FB}	I_{LX} = 200mA, slope = 0 (Note 2)	1.215	1.260	V
FB Fault Trip Level		V_{FB} falling	0.96	1.04	V
Line Regulation		V_{IN} = 2.7V to 5.5V		0.45	%/V
FB Input Bias Current	I_{FB}	V_{FB} = 1.5V	-100	+100	nA
LX Switch On-Resistance	$R_{LX(ON)}$			450	mΩ
LX Current Limit	I_{LIM}		1.6	2.8	A
POSITIVE LINEAR-REGULATOR CONTROLLER					
FBP Regulation Voltage	V_{FBP}	I_{DRVP} = 0.2mA	1.213	1.288	V
FBP Fault Trip Level		V_{FBP} falling	0.96	1.04	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.25V	-50	+50	nA
FBP Effective Transconductance		V_{DRVP} = 10V, I_{DRVP} = 0.1mA to 2mA	60		mS
Bandwidth		(Note 2)	200		kHz
DRVP Sink Current	I_{DRVP}	V_{FBP} = 1.1V, V_{DRVP} = 10V	5		mA
NEGATIVE LINEAR-REGULATOR CONTROLLER					
FBN Regulation Voltage	V_{FBN}	I_{DRVN} = 0.2mA	95	155	mV
FBN Fault Trip Level		V_{FBN} rising	325	475	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0V	-50	+50	nA
FBN Effective Transconductance		V_{DRVN} = -10V, I_{DRVN} = 0.1mA to 2mA	60		mS
Bandwidth		(Note 2)	200		kHz
DRVN Sink Current	I_{DRVN}	V_{FBN} = 200mV, V_{DRVN} = -10V	5		mA
LOGIC SIGNAL ($\overline{SHDN}$)					
Input Low Voltage		100mV typical hysteresis		0.4	V
Input High Voltage			1.6		V
Input Current	$I_{\overline{SHDN}}$			1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, $\overline{SHDN}$ = IN, C_{REF} = 0.22µF, PGND = GND, **T_A = -40°C to +85°C**.) (Note 4)

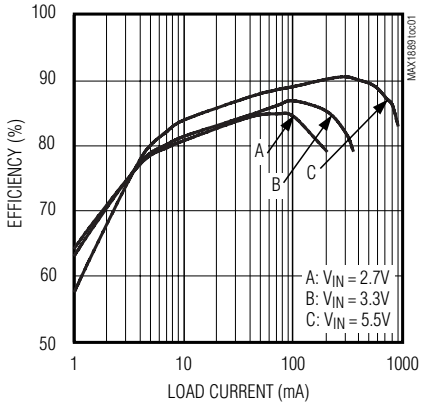
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC SIGNAL (FREQ)						
Input Low Voltage		0.15 x V_{IN} typical hysteresis			0.3 x V_{IN}	V
Input High Voltage			0.7 x V_{IN}			V
Input Current	I_{FREQ}				1	µA
OVERCURRENT COMPARATOR						
Input Offset Voltage			-5		+5	mV
Input Bias Current	I_{OCN}, I_{OCP}	V_{OCN} = V_{OCP} = V_{IN}	-50		+50	nA
OCN, OCP Input Common-Mode Range			1.5		0.8 x V_{IN}	V
FAULT TIMER AND GATE DRIVER						
GATE Output Sink Current	I_{GATE}	V_{GATE} = 1.5V, during turn-on transition	6		18	µA
GATE Output Pulldown Resistance		V_{GATE} < 0.5V			200	Ω
GATE Output Pullup Resistance					200	Ω

Note 1: Quiescent current does not include switching losses.
Note 2: FB regulation voltage is tested with no slope compensation ramp. Slope compensation needs to be included when selecting resisitors for setting the output voltage (see *Main Step-Up Regulator* and *Output Voltage Selection* sections).
Note 3: Guaranteed by design. Not production tested.
Note 4: Specifications to -40°C are guaranteed by design, not production tested.

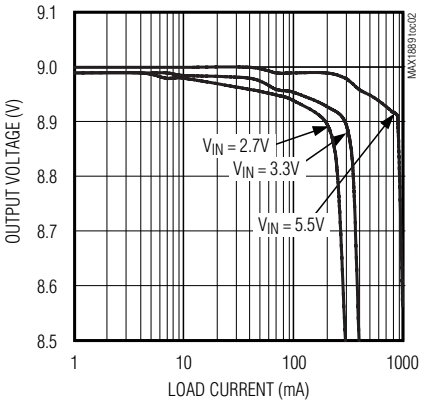
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = +3.3V, V_{MAIN} = +9V, V_{PL} = +20V, V_{NL} = -7V, $\overline{SHDN}$ = FREQ = IN, PGND = GND, T_A = +25°C, unless otherwise noted.)

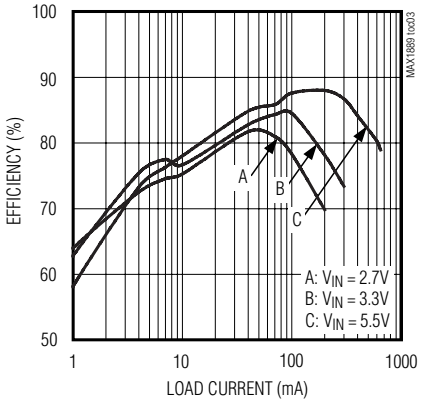
STEP-UP REGULATOR EFFICENCY vs. LOAD CURRENT (V_{MAIN} = 9V)



STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (V_{MAIN} = 9V)



STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 13V)

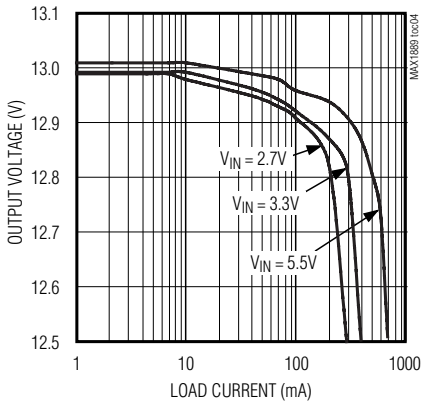


Triple-Output TFT LCD Power Supply with Fault Protection

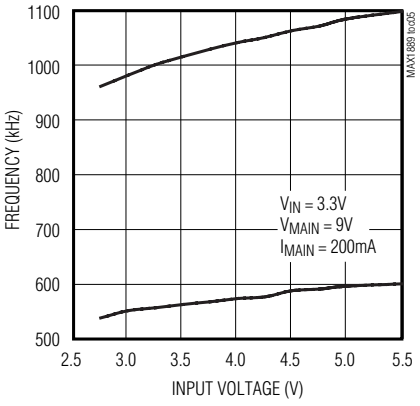
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, V_{MAIN} = +9V, V_{PL} = +20V, V_{NL} = -7V, $\overline{SHDN}$ = FREQ = IN, PGND = GND, T_A = +25°C, unless otherwise noted.)

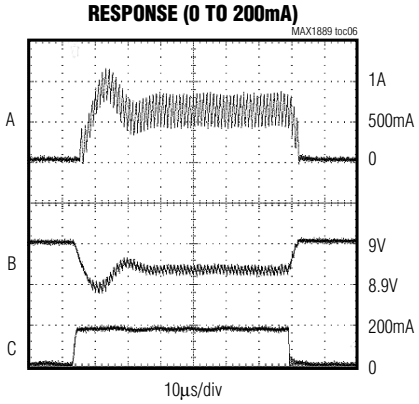
STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (V_{MAIN} = 13V)



STEP-UP REGULATOR SWITCHING FREQUENCY vs. INPUT VOLTAGE

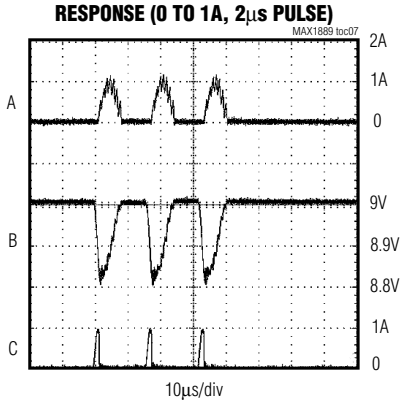


STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (0 TO 200mA)



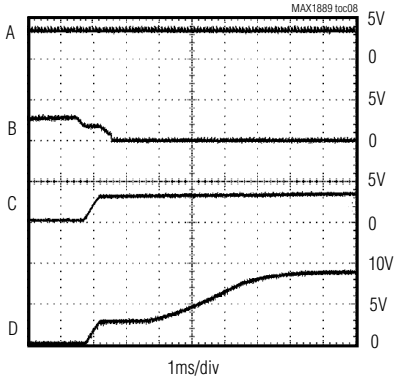
A: INDUCTOR CURRENT, 500mA/div
B: V_{MAIN} = 9V, 100mV/div, AC-COUPLED
C: I_{MAIN} = 0 TO 200mA, 200mA/div

STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (0 TO 1A, 2µs PULSE)



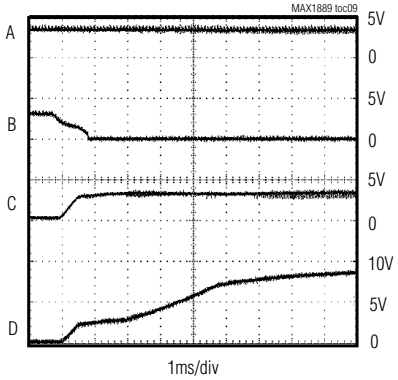
A: INDUCTOR CURRENT, 1A/div
B: V_{MAIN} = 9V, 100mV/div, AC-COUPLED
C: I_{MAIN} = 0 TO 1A, 1A/div

STEP-UP REGULATOR SOFT-START (10mA LOAD) FROM SLOW-RISING INPUT SUPPLY



A: V_{IN}, 5V/div
B: V_{GATE}, 5V/div
C: V_{C2}, 5V/div
D: V_{MAIN} = 9V, 5V/div

STEP-UP REGULATOR SOFT-START (200mA LOAD) FROM SLOW-RISING INPUT SUPPLY

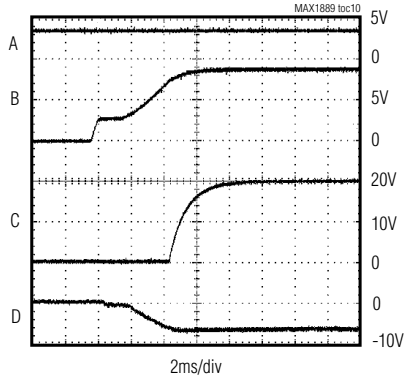


A: V_{IN}, 5V/div
B: V_{GATE}, 5V/div
C: V_{C2}, 5V/div
D: V_{MAIN} = 9V, 5V/div

Typical Operating Characteristics (continued)

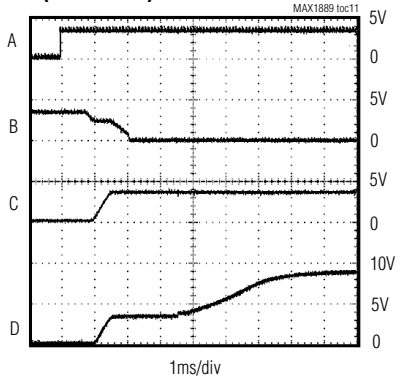
(Circuit of Figure 1, V_{IN} = +3.3V, V_{MAIN} = +9V, V_{PL} = +20V, V_{NL} = -7V, $\overline{SHDN}$ = FREQ = IN, PGND = GND, T_A = +25°C, unless otherwise noted.)

POWER-UP SEQUENCE FROM SLOW-RISING INPUT SUPPLY



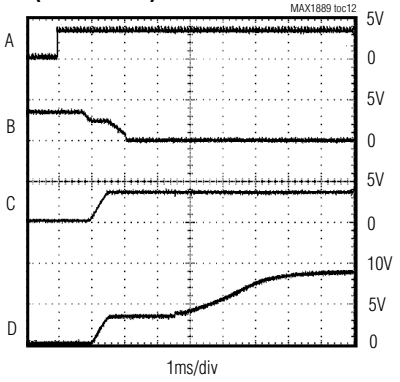
A: V_{IN}, 5V/div
B: V_{MAIN} = 9V, 5V/div
C: V_{PL} = 20V, 10V/div
D: V_{NL} = -7V, 10V/div

STEP-UP REGULATOR SOFT-START (10mA LOAD) USING $\overline{SHDN}$ CONTROL



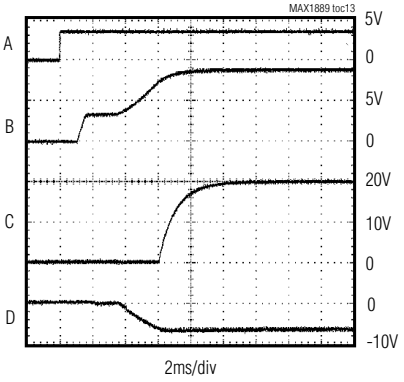
A: $V_{\overline{SHDN}}$, 5V/div
B: V_{GATE}, 5V/div
C: V_{C2}, 5V/div
D: V_{MAIN} = 9V, 5V/div

STEP-UP REGULATOR SOFT-START (200mA LOAD) USING $\overline{SHDN}$ CONTROL



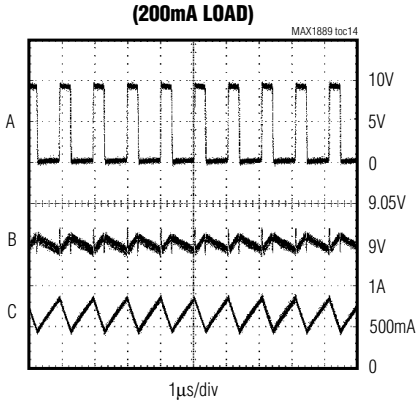
A: $V_{\overline{SHDN}}$, 5V/div
B: V_{GATE}, 5V/div
C: V_{C2}, 5V/div
D: V_{MAIN} = 9V, 5V/div

POWER-UP SEQUENCE USING $\overline{SHDN}$ CONTROL



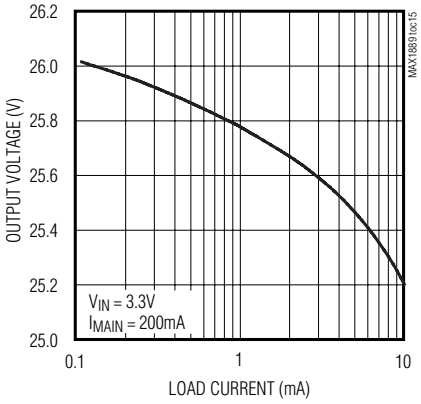
A: $V_{\overline{SHDN}}$, 5V/div
B: V_{MAIN} = 9V, 5V/div
C: V_{PL} = 20V, 10V/div
D: V_{NL} = -7V, 10V/div

STEP-UP REGULATOR NORMAL OPERATION (200mA LOAD)



A: V_{LX}, 5V/div
B: V_{MAIN} = 9V, 50mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 500mA/div

POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT

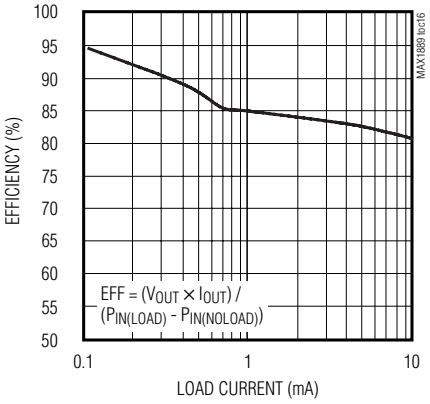


Triple-Output TFT LCD Power Supply with Fault Protection

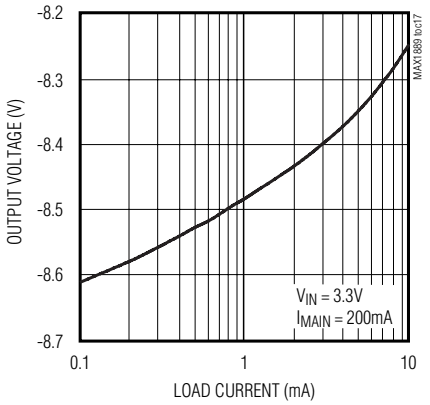
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, V_{MAIN} = +9V, V_{PL} = +20V, V_{NL} = -7V, $\overline{SHDN}$ = FREQ = IN, PGND = GND, T_A = +25°C, unless otherwise noted.)

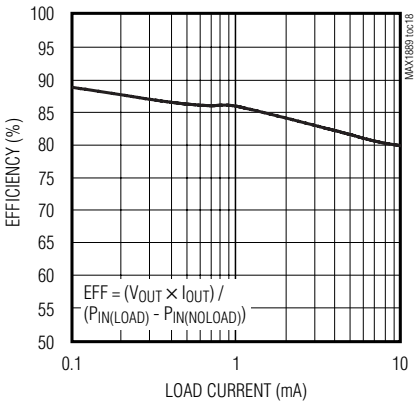
POSITIVE CHARGE-PUMP INCREMENTAL EFFICIENCY vs. LOAD CURRENT



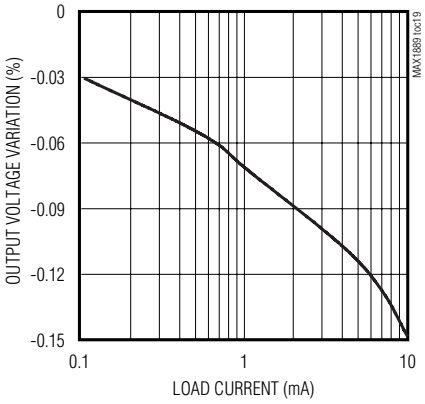
NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



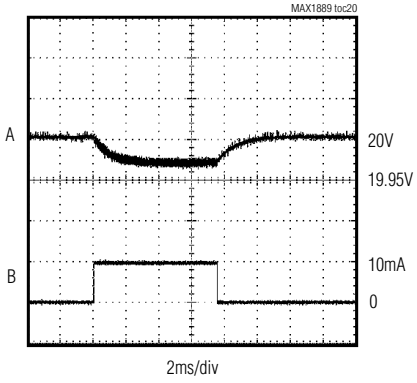
NEGATIVE CHARGE-PUMP INCREMENTAL EFFICIENCY vs. LOAD CURRENT



POSITIVE LINEAR-REGULATOR LOAD REGULATION

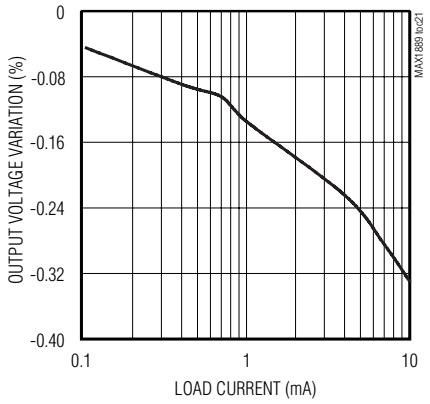


POSITIVE LINEAR-REGULATOR LOAD-TRANSIENT RESPONSE



A: V_{PL} = 20V, 50mV/div, AC-COUPLED
B: I_{PL} = 0 TO 10mA, 10mA/div

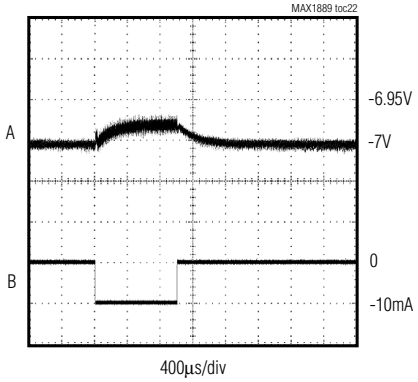
NEGATIVE LINEAR-REGULATOR LOAD REGULATION



Typical Operating Characteristics (continued)

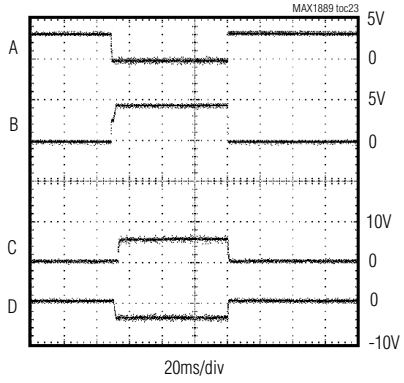
(Circuit of Figure 1, V_{IN} = +3.3V, V_{MAIN} = +9V, V_{PL} = +20V, V_{NL} = -7V, $\overline{SHDN}$ = FREQ = IN, PGND = GND, T_A = +25°C, unless otherwise noted.)

NEGATIVE LINEAR-REGULATOR LOAD-TRANSIENT RESPONSE



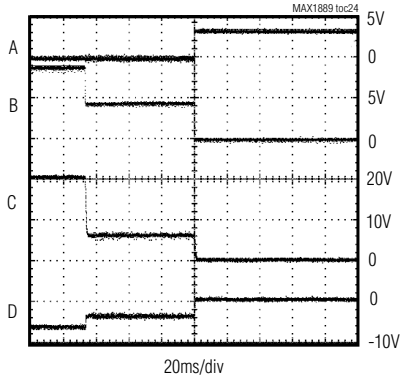
A: V_{NL} = -7V, 50mV/div, AC-COUPLED
B: I_{NL} = 0 TO -10mA, 10mA/div

OVERCURRENT PROTECTION RESPONSE TO OVERLOAD DURING STARTUP



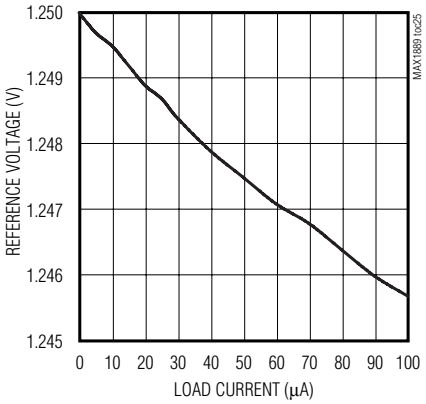
A: V_{GATE}, 5V/div
B: V_{MAIN}, 5V/div; I_{MAIN} = 1.5A
C: V_{PL}, 10V/div; I_{PL} = 10mA
D: V_{NL}, 10V/div; I_{NL} = 10mA

OVERCURRENT PROTECTION RESPONSE TO OVERLOAD DURING NORMAL OPERATION

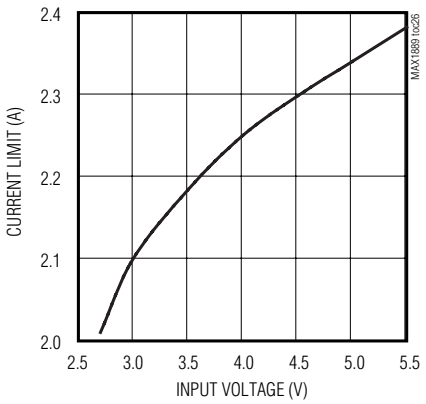


A: V_{GATE}, 5V/div
B: V_{MAIN} = 9V, 5V/div; I_{MAIN} = 200mA TO 1.5A
C: V_{PL} = 20V, 10V/div; I_{PL} = 10mA
D: V_{NL} = -7V, 10V/div; I_{NL} = 10mA

REFERENCE VOLTAGE vs. LOAD CURRENT



LX CURRENT LIMIT vs. INPUT VOLTAGE



Triple-Output TFT LCD Power Supply with Fault Protection

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Active-Low Shutdown Control Input. Pull $\overline{SHDN}$ below the 0.4V logic-low level to turn off all sections of the device and pull the GATE pin high. Pull $\overline{SHDN}$ above the 1.6V logic-high level to enable the device. Do not leave $\overline{SHDN}$ floating.
2	PGND	Power Ground. PGND is the source of the N-channel power MOSFET. Connect PGND to the analog ground (GND) at the device's pins.
3	GND	Analog Ground. Connect GND to the power ground (PGND) at the device's pins.
4	REF	Internal Reference Bypass Terminal. Connect a 0.22µF ceramic capacitor from REF to the analog ground (GND). External load capability is at least 50µA.
5	FB	Main Step-Up Regulator Feedback Input. FB regulates to 1.25V nominal. Connect FB to the center of a resistive voltage-divider between the main output (V_{MAIN}) and the analog ground (GND) to set the main step-up regulator output voltage. Place the resistive voltage-divider close to the pin.
6	FBN	Negative Linear-Regulator Feedback Input. FBN regulates to 125mV nominal. Connect FBN to the center of a resistive voltage-divider between the negative output (V_{NEG}) and the REF to set the negative linear-regulator output voltage. Place the resistive voltage-divider close to the pin.
7	DRVN	Negative Linear-Regulator Base Drive. Open drain of an internal P-channel MOSFET. Connect DRVN to the base of the external linear-regulator NPN pass transistor (see *Pass Transistor Selection* section).
8	DRVP	Positive Linear-Regulator Base Drive. Open drain of an internal N-channel MOSFET. Connect DRVP to the base of the external linear-regulator PNP pass transistor (see *Pass Transistor Selection* section).
9	FBP	Positive Linear-Regulator Feedback Input. FBP regulates to 1.25V nominal. Connect FBP to the center of a resistive voltage-divider between the positive output (V_{POS}) and the analog ground (GND) to set the positive linear-regulator output voltage. Place the resistive voltage-divider close to the pin.
10	FREQ	Frequency Select Input. Pull FREQ above logic-high level ($0.7 \times V_{IN}$) to set the frequency to 1MHz and pull FREQ below logic-low level ($0.3 \times V_{IN}$) to set the frequency to 500kHz. Do not leave FREQ floating.
11	LX	Switching Node. Drain of the internal N-channel power MOSFET for the main step-up regulator.
12	TGND	Internal connection. Connect this pin to ground.
13	OCN	Overcurrent Comparator Inverting Input. OCN connects to the center tap of a resistive voltage-divider connected to the drain of the input protection P-channel MOSFET (see the *Input Overcurrent Protection* section). If unused, connect OCN to REF.
14	OCP	Overcurrent Comparator Noninverting Input. OCP is connected to the center tap of a resistive voltage-divider that sets the input overcurrent threshold (see the *Input Overcurrent Protection* section). If unused, connect OCP to GND.
15	GATE	Gate Driver Output to the External P-Channel MOSFET (see the *Input Overcurrent Protection* section). If unused, leave GATE open.
16	IN	Supply Input. The supply voltage powers all the control circuitry. The input voltage range is from 2.7V to 5.5V. Bypass with a 0.1µF ceramic capacitor between IN and GND, as close to the pins as possible.

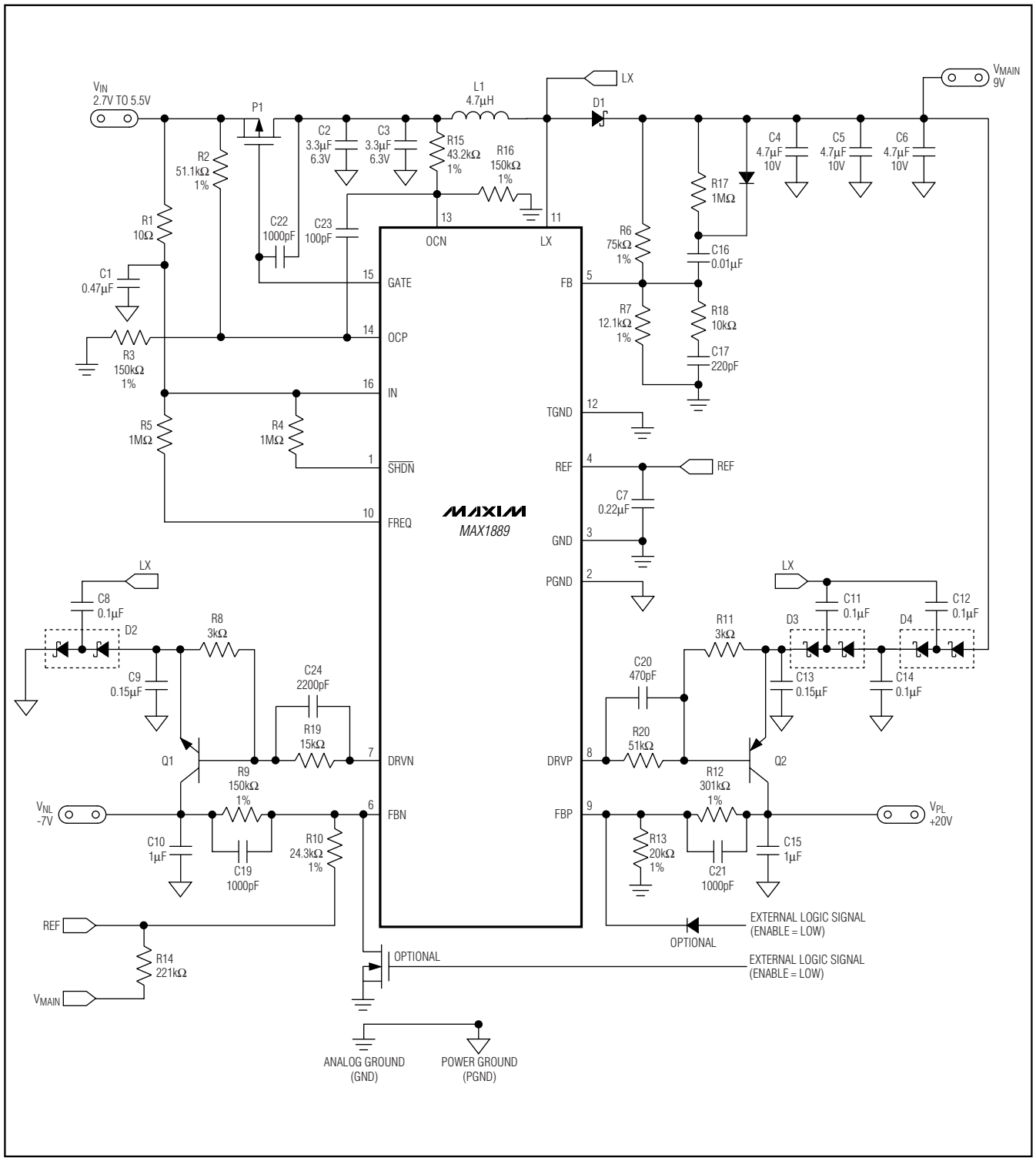


Figure 1. Standard Application Circuit

Triple-Output TFT LCD Power Supply with Fault Protection

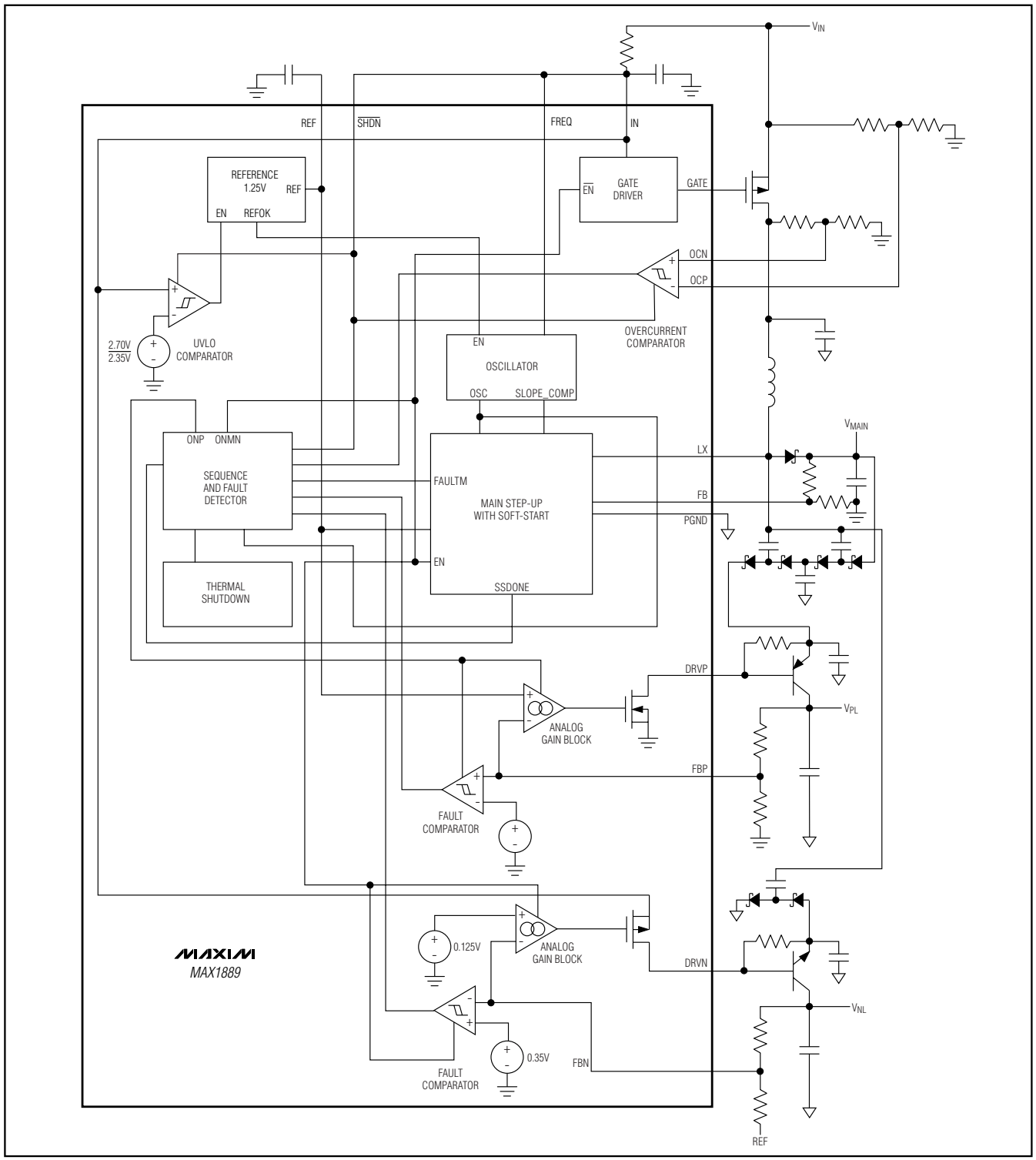


Figure 2. MAX1889 System Functional Diagram

Table 1. Component List

DESIGNATION	DESCRIPTION
C2, C3	3.3µF, 6.3V X5R ceramic capacitors (0805) Taiyo Yuden JMK212BJ335MG
C4, C5, C6	4.7µF, 10V X7R ceramic capacitors (1210) Taiyo Yuden LMK352BJ475MF
D1	1.0A, 30V Schottky diode (S-flat) Toshiba CRS02
D2, D3, D4	200mA, 25V dual-series Schottky diodes (SOT23) Fairchild BAT54S
D5	250mA, 75V switching diode (SOT23) Central Semiconductor CMPD914
L1	6.8µH, 1.3A inductor Coilcraft LPO2506IB-682
P1	2.4A, 20V P-channel MOSFET (3-pin SuperSOT) Fairchild FDN304P
Q1	200mA, 40V NPN bipolar transistor (SOT23) Fairchild MMBT3904
Q2	200mA, 40V PNP bipolar transistor (SOT23) Fairchild MMBT3906

Standard Application Circuit

The standard application circuit (Figure 1) of the MAX1889 generates +9V, +20V, and -7V outputs for TFT LCD displays. The input voltage is from 2.7V to 5.5V. Table 1 lists the recommended component options and Table 2 lists the component suppliers.

Detailed Description

The MAX1889 contains a high-performance, step-up switching regulator, two low-cost linear-regulator controllers, and multiple levels of protection circuitry. Figure 2 shows the system functional diagram of the device. The output voltage of the main step-up converter (V_{MAIN}) can be set from V_{IN} to 13V with an external resistive voltage-divider. The high switching frequency (500kH/1MHz) of the main step-up converter and current-mode control provide fast transient response and allow the use of low-profile inductors and ceramic capacitors. The internal power MOSFET minimizes the external component count while achieving high efficiency by incorporating a lossless current-sensing technology.

The switching node (LX) can generate both positive and negative voltage supplies by driving charge-pump stages of capacitors and diodes. The user can use as many charge-pump stages as needed to generate supply voltages of more than +30V and -15V. The positive and negative linear-regulator controllers postregulate the charge-pump supply voltages and allow users to program power-up sequencing as well.

The unique input switch control of the MAX1889 senses the current drawn from the input power supply by monitoring the voltage drop across the input P-channel MOSFET and latches off if an overcurrent condition lasts for more than the fault timer period. In addition, all three outputs are monitored for fault conditions that last longer than the fault latch timer. If the junction temperature of the IC exceeds +160°C, the device goes into a latched shutdown state.

Main Step-Up Regulator

The main step-up regulator switches at 1MHz (or 500kHz) and employs a current-mode control architecture to maximize loop bandwidth to provide fast-transient response to pulsed loads found in source drivers for TFT LCD panels. Also, the high switching frequency allows the use of low-profile inductors and capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in soft-start function reduce the number of external components required while controlling inrush current.

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Coilcraft	847-639-6400	847-639-1469	www.coilcraft.com
Fairchild	408-822-2000	408-822-2102	www.fairchildsemi.com
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com

Triple-Output TFT LCD Power Supply with Fault Protection

Depending on the input-to-output voltage ratio, the regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

On the rising edge of the internal clock, the controller sets a flip-flop, which turns on the N-channel MOSFET (Figure 3). The input voltage is applied across the inductor. The inductor current ramps up linearly, storing energy in a magnetic field. Once the sum of the feedback voltage error-amplifier output, slope-compensation, and current-feedback signals trip the multi-input PWM comparator, the MOSFET turns off, and the flip-flop resets. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

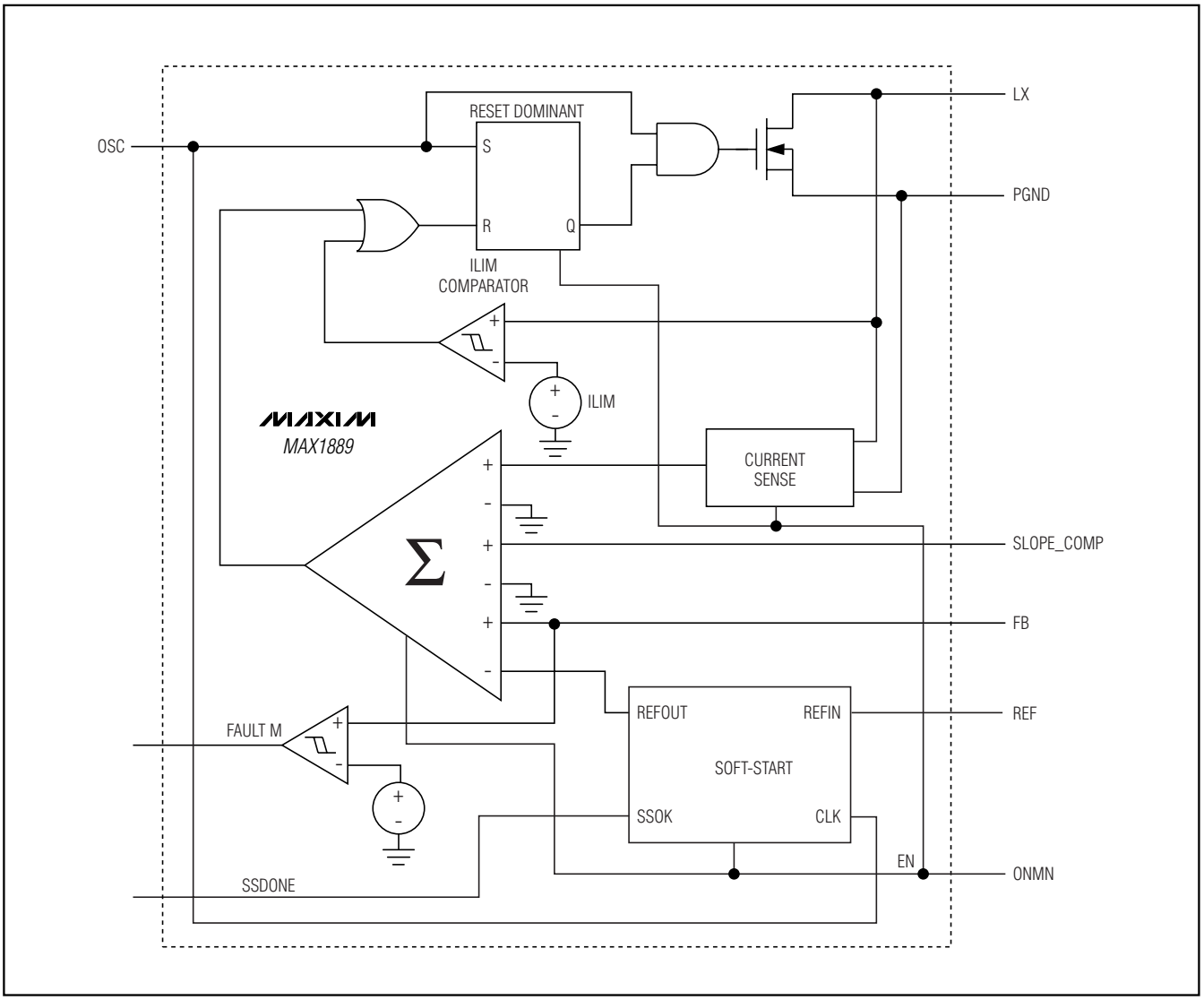


Figure 3. Main Step-Up Regulator Functional Diagram

Positive Linear-Regulator Controller

The positive linear regulator provides the positive high voltage for the TFT LCD gate drivers. The high voltage can be produced using a charge-pump circuit as shown in Figure 1. Use as many stages as necessary to obtain the required output voltage (see the *Selecting the Number of Charge-Pump Stages* section). The positive linear-regulator controller is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 3kΩ base-to-emitter resistor to post-regulate the charge-pump output (Figure 1). The regulator controller is designed to be stable with an output capacitor of 0.1µF or more.

To enable the regulator using an external control signal, apply the logic-control input in series with a signal diode (Figure 1). Additional delay can be added with external circuitry.

Note that the voltage rating of the DRVP output is 28V. If higher voltages are present, an external cascode NPN transistor should be used with the emitter connected to DRVP, the base to V_{MAIN}, and the collector to the base of the PNP.

Negative Linear-Regulator Controller

The negative linear regulator provides the negative voltage required to supply gate drivers in TFT LCD panels. The negative voltage can be produced using a charge pump circuit as shown in Figure 1. Use as many stages as necessary to obtain the required output voltage (see the *Selecting the Number of Charge-Pump Stages* section). The negative linear-regulator controller is an analog gain block with an open-drain P-channel output. It drives an external NPN pass transistor with a 3kΩ base-to-emitter resistor to postregulate the charge-pump output (Figure 1). The regulator controller is designed to be stable with an output capacitor of 0.1µF or more.

The negative linear regulator is enabled as soon as the main step-up regulator is enabled. To enable the regulator using an external control signal, apply the logic-control input through an open-drain output or an N-channel MOSFET (Figure 1). Additional delay can be added with external circuitry (see the *Applications Information* section).

Note that the voltage rating of the DRVN output is V_{IN} - 28V. If higher voltages are present, an external cascode PNP transistor should be used with the emitter connected to DRVN, the base to GND, and the collector to the base of the NPN.

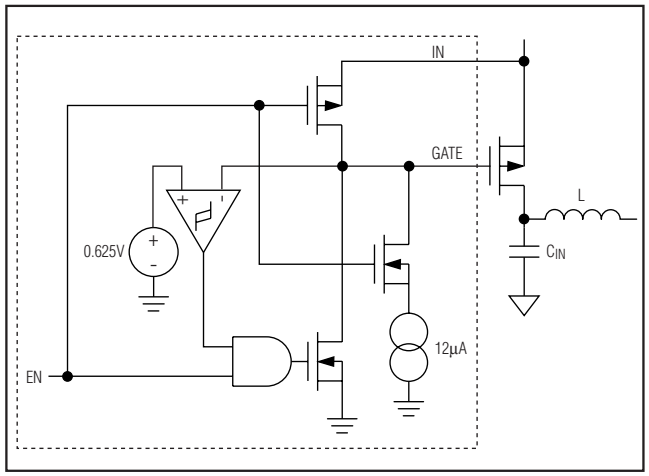


Figure 4. External Input P-Channel MOSFET Switch Control

Undervoltage Lockout (UVLO)

The UVLO comparator of the MAX1889 compares the input voltage at the IN pin with the UVLO threshold (2.7V rising, 2.35V falling, typ) to ensure that the input voltage is high enough for reliable operation. The 350mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO threshold, the controller enables the reference block. Once the reference is above 1.05V, an internal 12µA current source pulls the GATE pin low and turns on an external P-channel MOSFET switch (P1, Figure 1) that connects the input supply to the regulator. When the input voltage falls below the UVLO threshold, the controller sets the fault latch and pulls GATE high with an internal 100Ω switch to turn off P1 quickly (Figure 4).

Reference Voltage (REF)

The reference output is nominally 1.25V, and can source at least 50µA (see the *Typical Operating Characteristics*). Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND.

Oscillator Frequency (FREQ)

The internal oscillator frequency is pin programmable. Connect FREQ to ground for 500kHz operation and to V_{IN} for 1MHz operation. Note that the soft-start period scales with the oscillator frequency (see the *Soft-Start* section).

Shutdown ($\overline{SHDN}$)

A logic-low signal on the $\overline{SHDN}$ pin disables all device functions including the reference. When shut down, the supply current drops to 0.1µA (typ) to maximize battery life. The output capacitance, feedback resistors, and load current determine the rate at which each output voltage decays. A logic-high signal on the $\overline{SHDN}$ pin activates the MAX1889 (see the *Power-Up Sequencing* section). Do not leave the pin floating. If unused, connect $\overline{SHDN}$ to IN. Toggling $\overline{SHDN}$ or cycling IN clears the fault latch.

Triple-Output TFT LCD Power Supply with Fault Protection

Power-Up Sequencing and Inrush Current Control

Once $\overline{SHDN}$ is high, the MAX1889 enables the UVLO circuitry and compares the input voltage with the UVLO rising threshold (2.7V, typ). If the input voltage exceeds the UVLO rising threshold, the reference is enabled. When the reference voltage ramps up above 1.05V (typ), the MAX1889 enables the oscillator and turns on the external P-channel MOSFET P1 (Figure 1) by pulling GATE low. GATE is pulled down with a 12µA current source. Add a capacitor from the gate of P1 to its drain to slow down the turn-on rate of the MOSFET, and reduce inrush current. Once GATE reaches around 0.6V, an internal N-channel MOSFET turns on and pulls GATE to ground in order to maximize the enhancement of the external P-channel MOSFET. As P1 fully turns on, the main step-up regulator powers up with soft-start (see the *Soft-Start* section). The negative linear regulator is enabled at the same time as the main step-up regulator. The positive linear regulator is enabled after the soft-start routine is completed. The fault detection timer begins after the main step-up regulator has finished its soft-start period.

Soft-Start

The soft-start of the main step-up regulator (Figure 3) is achieved by ramping up the reference voltage of the multi-input PWM comparator in 4096 oscillator clock cycles. The 4096 clock cycles correspond to 4.096ms for 1MHz operation and 8.192ms for 500kHz operation. The reference of the PWM comparator comes from a 5-bit DAC that generates 32 steps when the reference ramps up from 0V to its final value. This soft-start method allows a gradual increase of the output voltage to reduce the input surge current (see the startup waveforms in the *Typical Operating Characteristics*). The average input current is given as:

$$I_{IN_AVG} = \frac{V_{MAIN}^{2} \times C_{OUT}}{V_{IN} \times t_{SS} \times \eta}$$

where V_{MAIN} is the main step-up regulator output voltage, V_{IN} is the input voltage, C_{OUT} is the main step-up regulator output capacitor, η is the efficiency of the step-up regulator, and t_{SS} is the soft-start period (4.096ms for 1MHz operation and 8.192ms for 500kHz operation).

Input Overcurrent Protection

The high-side overcurrent comparator of the MAX1889 provides input overcurrent protection when it is used together with the external P-channel MOSFET switch P1 (Figure 1). Connect resistive voltage-dividers from the source and drain of P1 to GND to set the overcurrent threshold. The center taps of the dividers are connected to the overcurrent comparator inputs (OCN and OCP) See the *Setting the Input Overcurrent Threshold* section for information on calculating resistor values. An overcurrent event activates the fault-protection circuitry.

Fault Protection

Once the soft-start routine is completed, if the output of the main regulator or either linear regulator is below its respective fault-detection threshold, or the input overcurrent comparator pulls high, the MAX1889 activates the fault timer. If the fault condition still exists after the 64ms fault-timer duration, the MAX1889 sets the fault latch, which shuts down all the outputs except the reference, which remains active. After removing the fault condition, toggle $\overline{SHDN}$ (below 0.4V) or cycle the input voltage (below 2.2V) to clear the fault latch and reactivate the device.

Thermal Shutdown

The thermal shutdown feature limits total power dissipation in the MAX1889. When the junction temperature (T_J) exceeds +160°C, a thermal sensor sets the fault latch (Figure 2), which shuts down all the outputs except the reference, allowing the device to cool down. Once the device cools down by 15°C, toggle $\overline{SHDN}$ (below 0.4V) or cycle the input voltage (below 2.2V) to clear the fault latch and reactivate the device.

Design Procedure

Main Step-Up Regulator

Output Voltage Selection

Adjust the output voltage by connecting a resistive voltage-divider from the output (V_{MAIN}) to GND with the center tap connected to FB (Figure 1). Select R7 in the 10kΩ to 50kΩ range. Calculate R6 with the following equations:

$$R6 = R7\left[(V_{MAIN} / V_{FB}) - 1\right]$$

where

$$V_{FB} = 1.242V - (D \times 20mV) \text{ and } D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

For example, at V_{IN} = 3V, V_{MAIN} = 9V, D ≈ 0.66, and V_{FB} = 1.229V.

V_{MAIN} can range from V_{IN} to 13V.

Inductor Selection

The minimum inductance value, peak current rating, series resistance, and size are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. For most applications, values between 3.3µH and 20µH work best with the MAX1889's switching frequencies.

The maximum load current, input voltage, output voltage, and switching frequency determine the inductor value. For a given load current, higher inductor value results in lower peak current and, thus, less output ripple, but degrades the transient response and possibly increases the size of the inductor. The equations provided here include a constant defined as LIR, which is the ratio of the peak-to-peak inductor current ripple to the average DC inductor current. For a good compromise between the size of the inductor, power loss, and output voltage ripple, select an LIR of 0.3 to 0.5. The inductance value is then given by:

$$L = \left(\frac{V_{IN(TYP)}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN(TYP)}}{I_{MAIN(MAX)} f_{OSC}}\right)\left(\frac{1}{LIR}\right)\eta$$

where η is the efficiency, f_{OSC} is the oscillator frequency (see the *Electrical Characteristics*), and I_{MAIN} includes the primary load current and the input supply currents for the charge pumps. Considering the typical application circuit, the maximum average DC load current ($I_{MAIN(MAX)}$) is 200mA with a 9V output. Based on the above equations, and assuming 85% efficiency and a switching frequency of 1MHz, the inductance value is 9.4µH for an LIR of 0.3. The inductance value is 5.6µH for an LIR of 0.5. The inductance in the standard application circuit is chosen to be 6.8µH.

The inductor's peak current rating should be higher than the peak inductor current throughout the normal operating range. The peak inductor current is given by:

$$I_{PEAK} = \left(\frac{I_{MAIN(MAX)} V_{MAIN}}{V_{IN(MIN)}}\right)\left(1 + \frac{LIR}{2}\right)\left(\frac{1}{\eta}\right)$$

Under fault conditions, the inductor current can reach the internal LX current limit (see the *Electrical Characteristics*). However, soft saturation inductors and the controller's fast current-limit circuitry protect the device from failure during such a fault condition.

The inductor's DC resistance can significantly affect efficiency due to conduction losses in the inductor. The power loss due to the inductor's series resistance (P_{LR}) can be approximated by the following equation:

$$P_{LR} = I_{(LAVG)}^2 R_L \cong \left(\frac{I_{MAIN} \times V_{MAIN}}{V_{IN}}\right)^2 R_L$$

where $I_{L(AVG)}$ is the average inductor current and R_L is the inductor's series resistance. For best performance, select inductors with resistance less than the internal N-channel MOSFET's on-resistance (0.25Ω typ). To minimize radiated noise in sensitive applications, use a shielded inductor.

Output Capacitor

The output capacitor affects the circuit stability and output voltage ripple. A 10µF ceramic capacitor works well in most applications. Depending on the output capacitor chosen, feedback compensation may be required or desirable to increase the loop-phase margin or increase the loop bandwidth for transient response (see the *Feedback Compensation* section).

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohm ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}, \text{ and}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Step-Up Regulator Compensation

The loop stability of a current-mode step-up regulator can be analyzed using a small-signal model. In continuous conduction mode (CCM), the loop-gain transfer function consists of a dominant pole, a high-frequency pole, a right-half-plane (RHP) zero, and an ESR zero. In the case of ceramic output capacitors, the ESR zero is at a very high frequency.

Triple-Output TFT LCD Power Supply with Fault Protection

Therefore, the dominant pole and the RHP zero determine the loop response of the step-up regulator. The frequency of the dominant pole is:

$$f_{P_DOMINANT} = \frac{1}{2\pi R_L C}$$

where R_L is the load resistance and C is the output capacitor. The frequency of the RHP zero is:

$$f_{Z_RHP} = \left(1\text{-}D\right)^2 \frac{R_L}{2\pi L}$$

where D is the duty cycle, L is the inductance, and the DC gain is given by:

$$A_{DC} = 20\log\left(\frac{R1}{R1+R2} \times \frac{(1-D)}{R_{CS}} \times R_L\right)$$

where R_{CS} is the internal current-sense resistor, and R1 and R2 are the feedback divider resistors in Figure 5.

However, adding lead or lag compensation (Figure 5) can be useful to adjust the trade-off between stability and transient response. If greater phase margin is needed for stability, and lower bandwidth is acceptable, add a pole-zero pair by connecting an RC network from the FB pin to ground (lag compensation). Conversely, if higher bandwidth is required for faster transient response, and lower phase margin is acceptable, add a zero-pole pair to the loop by connecting an RC network from the FB pin to the main output (lead compensation).

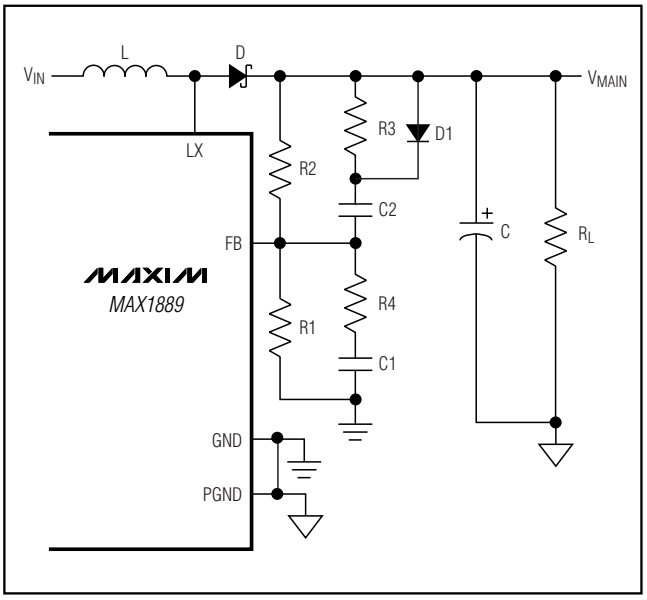


Figure 5. External Compensation

The frequencies of the pole and zero for the lag compensation are:

$$f_{P_FB} = \frac{1}{2\pi\left(R4\frac{R1\times R2}{R1+R2}\right)C1}$$

$$f_{Z_FB} = \frac{1}{2\pi R4 \times C1}$$

The frequencies of the zero and pole for the lead compensation are:

$$f_{Z_FF} = \frac{1}{2\pi\left(R2+R3\right)\times C2}$$

$$f_{P_FF} = \frac{1}{2\pi\left(R3+\frac{R1\times R2}{R1+R2}\right)C2}$$

The compensation resistors R3 and R4 change the AC gain affecting the loop bandwidth and phase margin at crossover. Reducing the bandwidth too much (FB compensation) harms the transient response, while increasing it too much harms phase margin and stability. As a rule, start with R3 (or R4) approximately equal to half of R1 (or R2). In a typical application, the compensation capacitors C1 and C2 can be in the range between 100pF to 1000pF. Then, check the stability by monitoring the transient response waveform when a pulsed load is applied to the output.

Using Compensation for Improved Soft-Start

The digital soft-start of the main step-up regulator limits the average input current during startup. In order to smooth out each step of the digital soft-start, add a low-frequency lead compensation network (Figure 5). The network effectively spreads out the switching pulses and lowers the peak inductor currents.

The smoothing network is active only during soft-start when the output voltage rises. Positive changes in the output are instantaneously coupled to the FB pin through D1 and feed-forward capacitor C2. This arrangement generates a smoothly rising output voltage. When the output voltage reaches regulation, C2 charges up through R3 and D1 turns off. In most applications, the lead compensation is not needed and can be disabled by making R3 large. With R3 > R2, the pole and the zero in the compensation network are very close to one another and cancel out.

Input Capacitor

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the device. Two 3.3µF ceramic capacitors are used in the standard application circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator typically runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the standard applications circuit. Ensure a low noise supply at the IN pin by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (see R1, C1 in Figure 1).

Rectifier Diode

The MAX1889's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 1A Schottky diode complements the internal MOSFET well.

Input P-Channel MOSFET

Select the input P-channel MOSFET based on the current rating, voltage rating, gate threshold, and on-resistance. The MOSFET must be able to handle the peak input current (see the *Inductor Selection* section). The drain-to-source voltage rating of the input MOSFET should be higher than the maximum input voltage. Because the MOSFET conducts the full input current, the on-resistance should be low enough for higher efficiency. Use a low-threshold MOSFET to ensure that the switch is fully enhanced at lowest input voltages.

Setting the Input Overcurrent Threshold

The high-side comparator of the MAX1889 provides input overcurrent protection when used in conjunction with an external P-channel MOSFET P1. The accuracy of the overcurrent threshold is affected by many factors, including comparator offset, resistor tolerance, input voltage range, and variations in MOSFET $R_{DS(ON)}$. The input overcurrent comparator is only intended to protect against catastrophic failures. This function is similar to an input fuse.

To minimize the impact of the comparator's input offset on the current-sense accuracy, the sense voltage should be close to the upper limit of the common-mode range, which extends up to 80% of the input voltage. The resistive voltage-divider (R3/R4), combined with the on-state resistance of P1, sets the overcurrent threshold. The center of R3/R4 is connected to the inverting input (OCN) as shown in Figure 6.

If the comparator and resistors are ideal, the threshold is at the current where both inputs are equal:

$$V_{IN} \times \frac{R2}{R1+R2} = \left(V_{IN} - I_{L(MAX)} \times R_{DS(MAX)}\right) \times \frac{R4}{R3+R4}$$

$I_{L(MAX)}$ is the average inductor current at maximum load condition and minimum input voltage, and given by:

$$I_{L(MAX)} = \frac{V_{OUT}}{\eta \times V_{IN(MIN)}} \times I_{LOAD(MAX)}$$

where η is the efficiency of the main step-up regulator. If the step-up regulator's minimum input voltage is 2.7V, output voltage is 9V and maximum load current is 0.3A. Assuming 80% efficiency, the maximum average inductor current is:

$$I_{L(MAX)} = \frac{9V}{0.8 \times 2.7V} \times 0.3A = 1.25A$$

$R_{DS(MAX)}$ is the maximum on-state drain-to-source resistance of P1. The maximum $R_{DS(ON)}$ at +25°C can be found in the MOSFET data sheet, but that number does not include the temperature coefficient.

Since the temperature coefficient for the resistance is 0.5%/°C, $R_{DS(MAX)}$ can be calculated with the following equation:

$$R_{DS(MAX)} = R_{DS_25°C} \times \left[1 + 0.005 \times \left(T_J - 25\right)\right]$$

where T_J is the actual MOSFET junction temperature in normal operation due to ambient temperature rise and self-heating caused by power dissipation. As an example, consider Fairchild FDN304P, which has a maximum $R_{DS(ON)}$ at room temperature of 70mΩ.

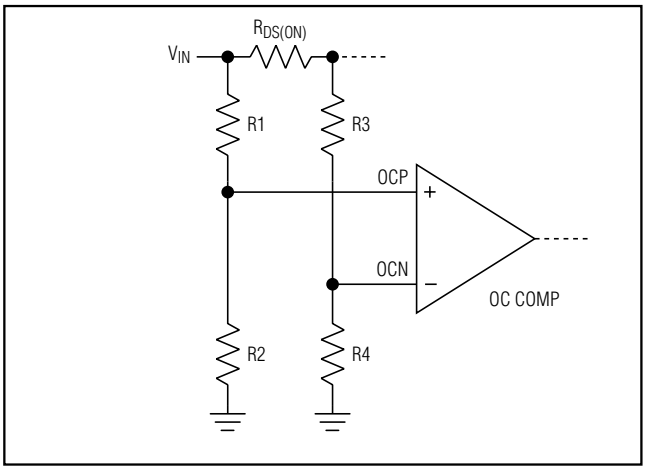


Figure 6. Setting the Overcurrent Threshold

Triple-Output TFT LCD Power Supply with Fault Protection

If the junction temperature is +100°C, the maximum on-state resistance overtemperature is:

$$R_{DS(MAX)} = 70m\Omega \times \left[1 + 0.005 \times (100 - 25)\right] = 100m\Omega$$

For given R1 and R2 values, the ideal ratio of R3/R4 can be determined:

$$\frac{R3}{R4} = \frac{R1 + R2}{R2} \times \frac{V_{IN} - I_{PEAK(MAX)} \times R_{DS(MAX)}}{V_{IN}} - 1$$

To consider the effect of resistor tolerance, comparator offset, and input voltage variation, the minimum threshold equation is:

$$V_{IN(MIN)} \times \frac{R2 \times (1+\varepsilon)}{R1 \times (1-\varepsilon) + R2 \times (1+\varepsilon)} + 5mV =$$
$$\left(V_{IN(MIN)} - I_{L(MAX)} \times R_{DS(MAX)}\right) \times \frac{R4 \times (1-\varepsilon)}{R3 \times (1+\varepsilon) + R4 \times (1-\varepsilon)}$$

where $V_{IN(MIN)}$ is the minimum expected value of the input voltage, ε is the tolerance of the resistors and the 5mV is the worst-case input offset voltage of the comparator. To simplify the equation, define a constant k as follows:

$$k = \frac{1-\varepsilon}{1+\varepsilon}$$

The minimum threshold equation becomes:

$$V_{IN(MIN)} \times \frac{R2}{k \times R1 + R2} + 5mV =$$
$$\left(V_{IN(MIN)} - I_{L(MAX)} \times R_{DS(MAX)}\right) \times \frac{k \times R4}{R3 + k \times R4}$$

Solving for R3/R4 yields:

$$\frac{R3}{R4} = k \times \left(\frac{V_{IN(MIN)} - I_{L(MAX)} \times R_{DS(MAX)}}{V_{IN(MIN)} \times \frac{R2}{R2 + k \times R1} + 5mV} - 1 \right)$$

The R3/R4 ratio guarantees the required minimum level for $I_{L(MAX)}$. The typical overcurrent threshold is given by:

$$I_{TH_TYP} = \frac{V_{IN(TYP)}}{R_{DS(TYP)}} \times \left[1 - \frac{R2 \times (R3 + R4)}{R4 \times (R1 + R2)}\right]$$

The following example shows how to apply the above equations in the design. If 1% resistors are used, then ε = 0.01. To set V_{OCP} to be around 75% of V_{IN}, select R1 = 51.1kΩ and R2 = 150kΩ. Assume that the minimum input voltage is 2.7V and the typical input voltage is 3.3V, the average inductor current at maximum load is 1.25A, and the maximum $R_{DS(ON)}$ of P1 is 100mΩ:

$$k = \frac{1 - 0.01}{1 + 0.01} = 0.9802$$

$$\frac{R3}{R4} = 0.9802 \times \left(\frac{2.7V - 1.25A \times 0.1\Omega}{2.7V \times \frac{150k\Omega}{150k\Omega + 0.9802 \times 51.1k\Omega} + 0.005V} - 1 \right)$$
$$= 0.2637$$

If R4 =150kΩ, then R3 = 39.2kΩ. The typical overcurrent threshold is:

$$I_{TH_TYP} = \frac{3.3V}{0.047\Omega} \times \left[1 - \frac{150k\Omega \times (39.2k\Omega + 150k\Omega)}{150k\Omega \times (51.1k\Omega + 150k\Omega)}\right]$$
$$= 4.15A$$

Charge Pumps

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meets the output requirement.

The number of positive charge-pump stages is given by:

$$N_{POS} = \frac{V_{PL} + V_{DROPOUT} - V_{MAIN}}{V_{MAIN} - 2 \times V_D}$$

where N_{POS} is the number of positive charge-pump stages, V_{PL} is the positive linear-regulator output, V_{MAIN} is the main step-up regulator output, V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 2V.

The number of negative charge-pump stages is given by:

$$N_{NEG} = \frac{-V_{NL} + V_{DOPOUT}}{V_{MAIN} - 2 \times V_D}$$

where N_{NEG} is the number of negative charge-pump stages, V_{NL} is the negative linear-regulator output, V_{MAIN} is the main step-up regulator output, V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 2V.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{MAIN} and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to V_{IN} or another available supply.

If the first charge-pump stage is powered from V_{IN}, then the above equations become:

$$N_{POS} = \frac{V_{PL} + V_{DROPOUT} - V_{IN}}{V_{MAIN} - 2 \times V_D}$$

$$N_{NEG} = \frac{-V_{NL} + V_{DROPOUT} + V_{IN}}{V_{MAIN} - 2 \times V_D}$$

Flying Capacitor

Increasing the flying capacitor (C_X) value increases the output current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and the diode impedance limit the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > N \times V_{MAIN}$$

where N is the stage number in which the flying capacitor appears, and V_{MAIN} is the main output voltage. For example, the two-stage positive charge pump in the typical application circuit (Figure 1) where V_{MAIN} = 9V contains two flying capacitors. The flying capacitor in the first stage (C14) requires a voltage rating over 9V. The flying capacitor in the second stage (C13) requires a voltage rating over 18V.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT} \geq \frac{I_{LOAD}}{2 f_{OSC} V_{RIPPLE}}$$

where V_{RIPPLE} is the peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diodes

Use Schottky diodes with a current rating equal to or greater than two times the average charge-pump input current.

Linear-Regulator Controllers

Output Voltage Selection

Adjust the positive linear-regulator output voltage by connecting a resistive voltage-divider from V_{PL} to GND with the center tap connected to FBP (Figure 1). Select R13 in the range of 10kΩ to 30kΩ.

Calculate R12 with the following equation:

$$R12 = R13 [(V_{PL} / V_{FBP}) - 1]$$

where V_{FBP} = 1.25V.

Adjust the negative linear-regulator output voltage by connecting a resistive voltage-divider from V_{NL} to REF with the center tap connected to FBN (Figure 1). Select R10 in the range of 10kΩ to 30kΩ. Calculate R9 with the following equation:

$$R9 = R10 [(V_{FBN} - V_{NL}) / (V_{REF} - V_{FBN})]$$

where V_{FBN} = 125mV, V_{REF} = 1.25V. Note that REF is only guaranteed to source 50µA. Using a resistor less than 20kΩ for R10 results in higher bias current than REF can supply. Connecting another resistor (R14) from V_{MAIN} to REF (Figure 1) can solve this problem because the main output can supply part of the resistor's (R10) bias current. Use the following equation to determine the value of R14:

$$R14 = \frac{V_{MAIN} - V_{REF}}{\left(\frac{V_{REF} - V_{FBN}}{R10}\right) - 40\mu A}$$

Drawing only 40µA from REF leaves the remaining 10µA for other purposes.

Pass Transistor Selection

The pass transistor must meet specifications for current gain (β), input capacitance, collector-emitter saturation voltage, and power dissipation.

Triple-Output TFT LCD Power Supply with Fault Protection

The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = \left(I_{DRV} - \frac{V_{BE}}{R_{BE}} \right) \beta_{MIN}$$

where I_{DRV} is the minimum base-drive current, and R_{BE} is the pullup resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the *Stability Requirements* section), so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current are not recommended. The transistor's input capacitance and input resistance also create a second pole, which could be low enough to make the output unstable when heavily loaded.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator supports. Alternatively, the package's power dissipation could limit the usable maximum input-to-output voltage differential. The maximum power dissipation capability of the transistor's package and mounting must exceed the actual power dissipation in the device. The power dissipation equals the maximum load current times the maximum input-to-output voltage differential:

$$P = I_{LOAD(MAX)}(V_{LDOIN} - V_{LDOOUT}) = I_{LOAD(MAX)}V_{CE}$$

During startup, the LDO outputs are below their respective setpoints, and the base drive to the pass transistors is a maximum. The large drive currents can cause the charge-pump outputs to collapse. If the charge-pump loading is objectionable, base resistors can be added between the drive outputs (DRVN and DRVP) and the pass transistors (Figure 7). These resistors limit the maximum drive current and prevent discharging the charge pump's output capacitors. Select the minimum base drive current to meet the maximum required LDO output current:

$$I_{DRIVE(MIN)} = \frac{I_{LDOOUT(MAX)}}{\beta_{MIN}}$$

The resistance required to guarantee this base current is:

$$R_{BASE} \le \frac{V_{LDOIN(MAX)} - V_{BE}}{I_{DRIVE(MIN)}} = \frac{\beta_{MIN}\left(V_{LDOIN(MAX)} - V_{BE}\right)}{I_{LDOOUT(MAX)}}$$

As a consequence of adding the base resistors, a voltage change at DRVN and DRVP accompanies changes in drive current. This voltage change can be coupled through parasitic capacitance to the LDO feedback pins. If the rate of voltage change is sufficiently large, it can cause instability.

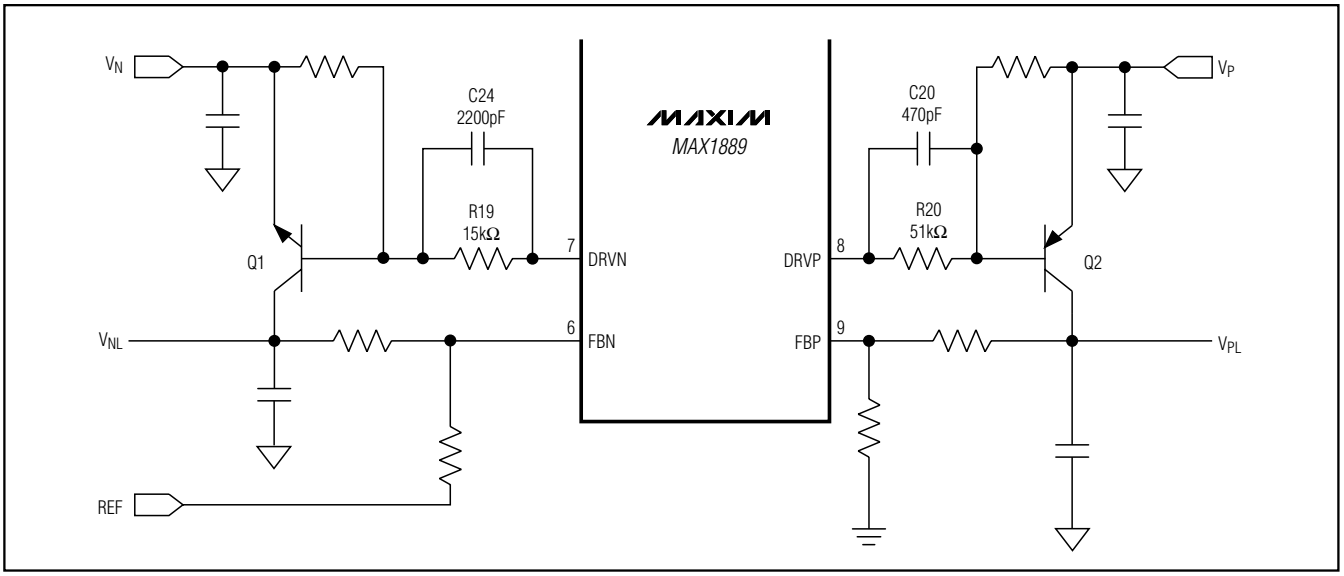


Figure 7. Limiting LDO Drive Current During Startup

To avoid excessive voltage coupling, a small capacitor can be added in parallel with the base resistor. The resulting RC time constant should be between 5µs to 50µs.

Stability Requirements

The MAX1889 linear-regulator controllers use an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the base-emitter resistor, and the output capacitor determine the loop stability. If the output capacitor and pass transistor are not properly selected, the linear regulator can be unstable.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V(LDO)} = \left(\frac{5.5}{V_T}\right)\left[1+\left(\frac{I_{BIAS}h_{FE}}{I_{LOAD}}\right)\right]V_{REF}$$

where V_T is 26mV at room temperature, and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). This bias resistor is typically 3kΩ, providing 0.23mA of current, biasing the LDO near its regulation voltage setpoint.

The output capacitor and the load resistance create the dominant pole in the system. The pass transistor's input capacitance creates a second pole in the system. Additionally, the output capacitor's ESR generates a zero.

To achieve stable operation, use the following equations to verify that the linear regulator is properly compensated:

1) First, determine the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE(CLDO)} = \frac{1}{2\pi C_{LDO}R_{LOAD}} = \frac{I_{LOAD(MAX)}}{2\pi C_{LDO}V_{LDO}}$$

The unity gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V(LDO)}\, f_{POLE(CLDO)}$$

2) Next, determine the second pole set by the base-to-emitter capacitance (including the transistor's input capacitance), the transistor's input resistance, and the base-to-emitter pullup resistor:

$$f_{POLE(CBE)} = \frac{1}{2\pi C_{BE}(R_{BE} \,||\, R_{IN})} = \frac{R_{BE}I_{LOAD} + V_T h_{FE}}{2\pi C_{BE}R_{BE}V_T h_{FE}}$$

3) A third pole is set by the linear regulator's feedback resistance and the capacitance (including stray capacitance) between FB_ and GND (for the positive LDO) and FBN and GND (for the negative LDO) (Figure 8):

$$f_{POLE(FB)_POS} = \frac{1}{2\pi C_{FB}(R12 \,||\, R13)}$$

$$f_{POLE(FB)_NEG} = \frac{1}{2\pi C_{FB}(R9 \,||\, R10)}$$

4) If the second and third poles occur well after unity-gain crossover, the linear regulator remains stable:

$$f_{POLE(CBE)} > 2f_{POLE(CLDO)}A_{V(LDO)}$$

However, if the ESR zero occurs before the unity-gain crossover, cancel the zero with the feedback pole by changing circuit components such that:

$$f_{POLE(FB)} \approx \frac{1}{2\pi C_{OUT}R_{ESR}}$$

For most applications where ceramic capacitors are used, the ESR zero always occurs after the crossover.

A capacitor connected between the output and the feedback node improves the transient response, reduces the noise coupled into the feedback loop, and maintains the correct regulation point (Figure 8).

Output Capacitor Selection

Typically, more output capacitance provides the best solution, since this also reduces the output voltage drop immediately after a load transient. Connect at least a 0.1µF capacitor between the linear regulator's output and ground, as close to the external pass transistor as possible. Depending on the selected pass transistor, larger capacitor values may be required for stability (see the *Stability Requirements* section). Furthermore, the output capacitor's ESR affects stability. Use output capacitors with an ESR less than 200mΩ to ensure stability and optimum transient response. Once the minimum capacitor value for stability is determined, verify that the linear regulator's output does not contain excessive noise. Although adequate for stability, small capacitor values can provide too much bandwidth, making the linear regulator sensitive to noise. Larger capacitor values reduce the bandwidth, thereby reducing the regulator's noise sensitivity. If noise on the ground reference causes the design to be marginally stable for the negative linear regulator, bypass the negative output back to its reference voltage. This technique reduces the differential noise on the output.

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Applications Information

PC Board Layout

Careful PC board layout is extremely important for proper operation. Use the following guidelines for good PC board layout:

1) Minimize the area of high-current loops by placing the input capacitors, inductor, output diode, and output capacitors less than 0.2in (5mm) from the LX and PGND pins. Connect these components with traces as wide as possible. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create islands for the analog ground (GND), power ground (PGND), and linear regulator ground. Star-connect them to the backside pad of the device. The REF bypass capacitor and both feedback dividers should be connected to the analog ground island (GND). The step-up regulator's input and output capacitors, and the charge-pump components should be a wide power ground plane. The power ground plane should be connected to the power ground pin (PGND) with a wide trace. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. All the other ground connections, such as the IN pin bypass capacitor and the linear regulator output capacitors, should be star-connected to the backside of the device with wide traces. Make no other connections between these separate ground planes.
3) Place IN pin and REF pin bypass capacitors as close to the device as possible.
4) Place all feedback voltage-divider resistors as close to their respective feedback pins as possible. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX or the switching nodes in the charge pumps.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of LX node while keeping it wide and short. Keep the LX node away from feedback nodes (FB, FBP, and FBN) and analog ground. Use DC traces as shield if necessary.

Refer to the MAX1889 evaluation kit for an example of proper board layout.

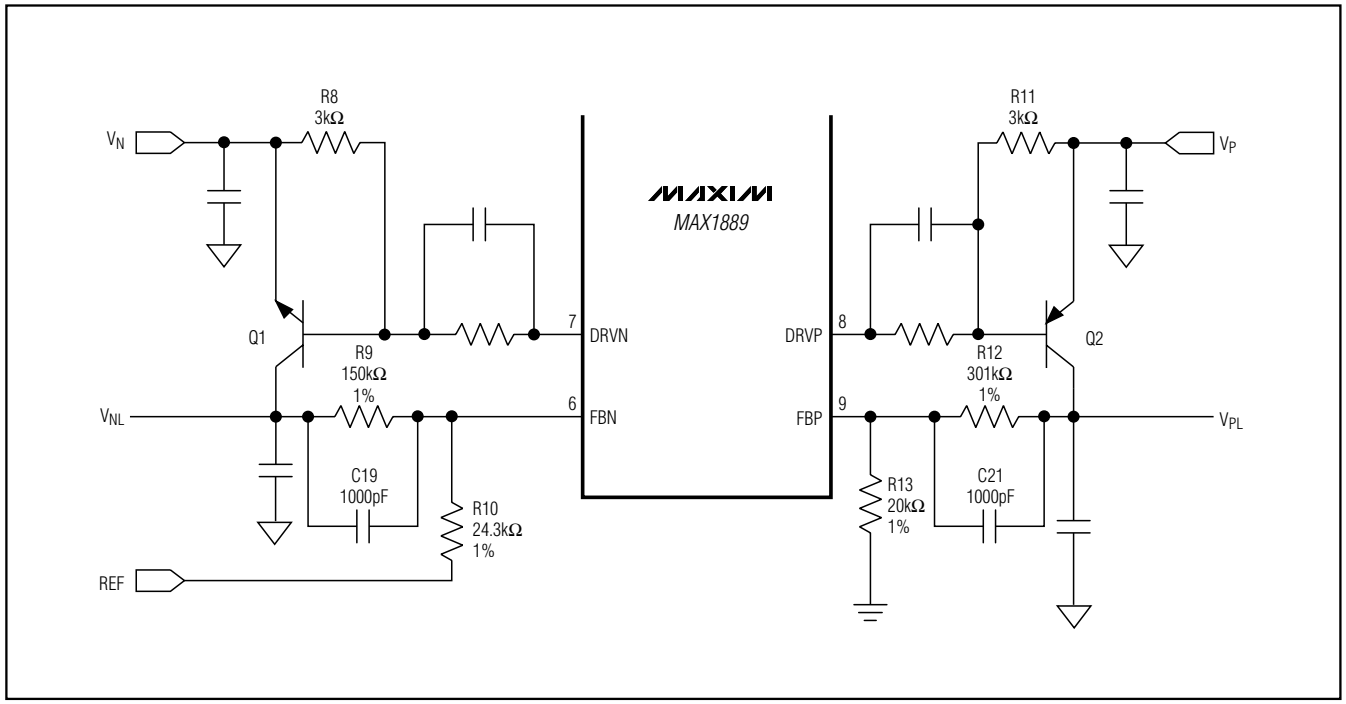


Figure 8. LDO Compensation

Additional Application Circuits

Operation with Output Voltage >13V

The maximum output voltage of the step-up regulator is 13V, which is limited by the absolute maximum rating of the internal power MOSFET. To achieve higher output voltage, an external N-channel MOSFET can be cascoded with the internal FET (Figure 9). Since the gate of the external FET is biased from the input supply, use a logic-level FET to ensure that the FET is fully enhanced at the minimum input voltage. The current rating of the FET needs to be higher than the internal current limit.

Changing Power-Up Sequence

The power-up sequencing of the linear regulators can be controlled using external delays. Figure 10 shows an application where the negative linear-regulator output powers up with a certain delay after the positive linear regulator reaches regulation. The resistors R1, R2, and the capacitor C form an RC network that provides the power-up delay. The time constant of this RC network is:

$$\tau = \frac{R1 \times R2}{R1 + R2} C$$

Select the ratio of R1 and R2 so that:

$$V_N \frac{R2}{R1+R2} + V_{PL} \frac{R1}{R1+R2} = 0$$

or:

$$\frac{R1}{R2} = -\frac{V_N}{V_{PL}}$$

With this R1/R2 ratio, the power-up delay can be calculated as:

$$\tau_D = \tau \ln \left(\frac{V_{PL} \frac{R1}{R1+R2}}{V_D - 0.125V} \right)$$

where V_D is the forward voltage drop of the diode and 0.125V is the FBN regulation point.

As a design example, assume the positive linear-regulator output V_{PL} is +20V, the negative charge-pump output V_N is -9V, and the required power-up delay time t_D is 4ms:

$$\frac{R1}{R2} = \frac{9}{20}$$

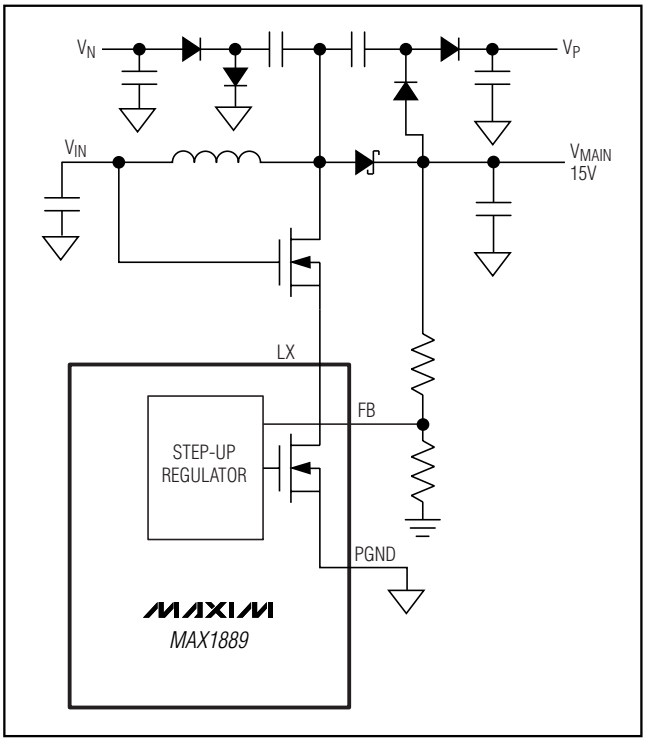


Figure 9. Operation with Output Voltage >13V Using Cascoded MOSFET

The required RC time constant is:

$$\tau = \frac{4ms}{\ln \left(\frac{20 \frac{9}{20+9}}{0.7 - 0.125} \right)} = 1.68ms$$

Choose C = 0.1µF, then R1//R2 = 16.8kΩ. Use standard resistor values: R1 = 56kΩ and R2 = 24kΩ.

Disabling Input MOSFET Switch

If the input protection MOSFET is not needed, disable the input overcurrent comparator by connecting the OCP pin to ground, the OCN pin to V_{IN}. Leave the GATE pin floating (Figure 11).

Generating Gamma Reference Voltage

The reference voltage for the Gamma correction resistor string can be produced using the linear-regulator controller. If the voltage difference between the main boost voltage (V_{MAIN}) and the Gamma reference voltage is 400mV or greater, the emitter of the PNP pass transistor should be connected to V_{MAIN}.

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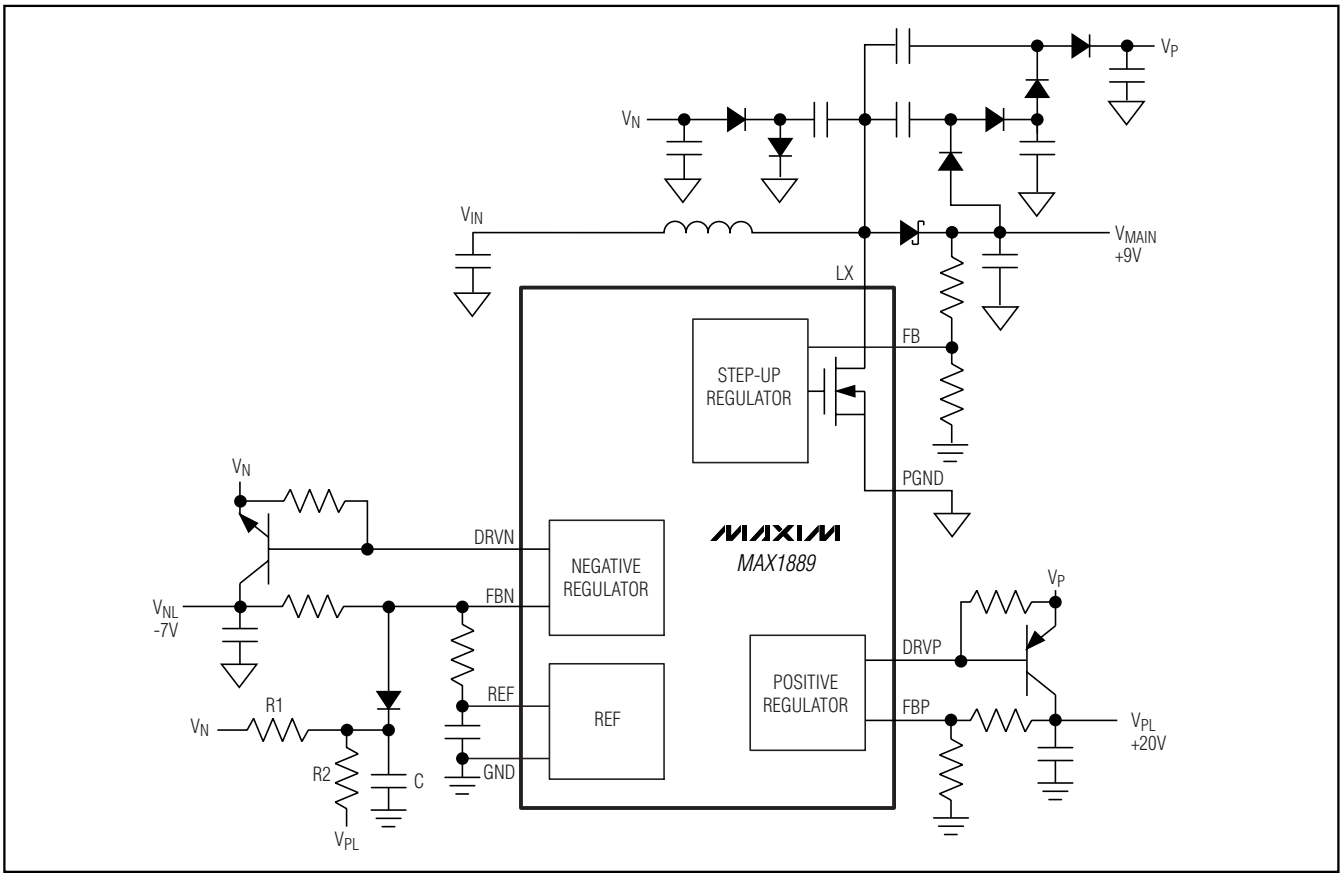


Figure 10. Controlling Power-Up Sequence with External Delay

If the voltage difference is less than 400mV, then the emitter of the PNP should be connected to a high supply voltage. The V_P output has two charge-pump stages added to V_{MAIN}. The emitter of the PNP can be connected to the output of the first stage as shown in Figure 12. For higher efficiency, the first charge-pump stage can be connected to V_{IN} rather than V_{MAIN}, as this reduces the power loss.

Chip Information

TRANSISTOR COUNT: 2396

PROCESS: BiCMOS

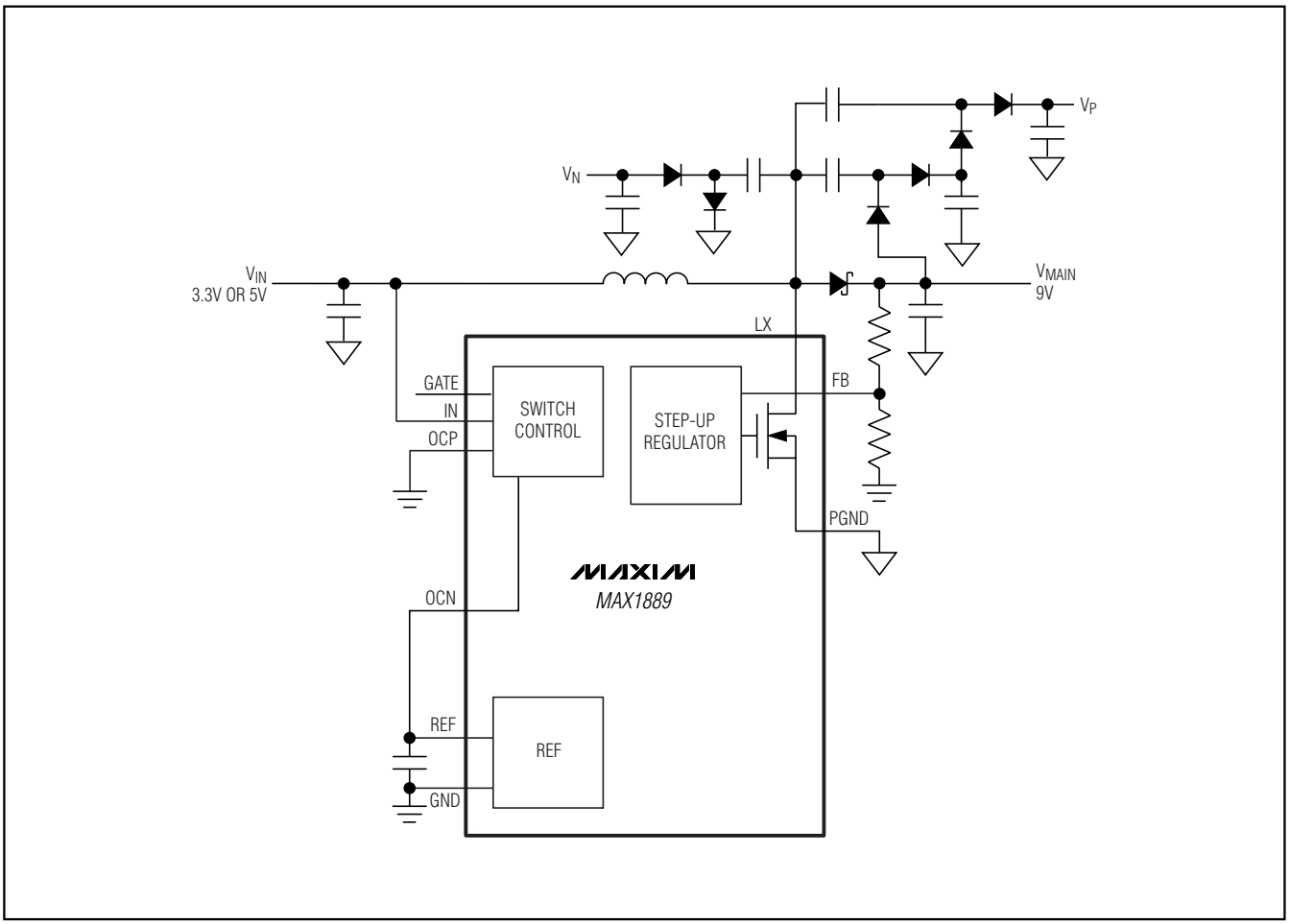


Figure 11. Disabling Input Protection MOSFET Switch

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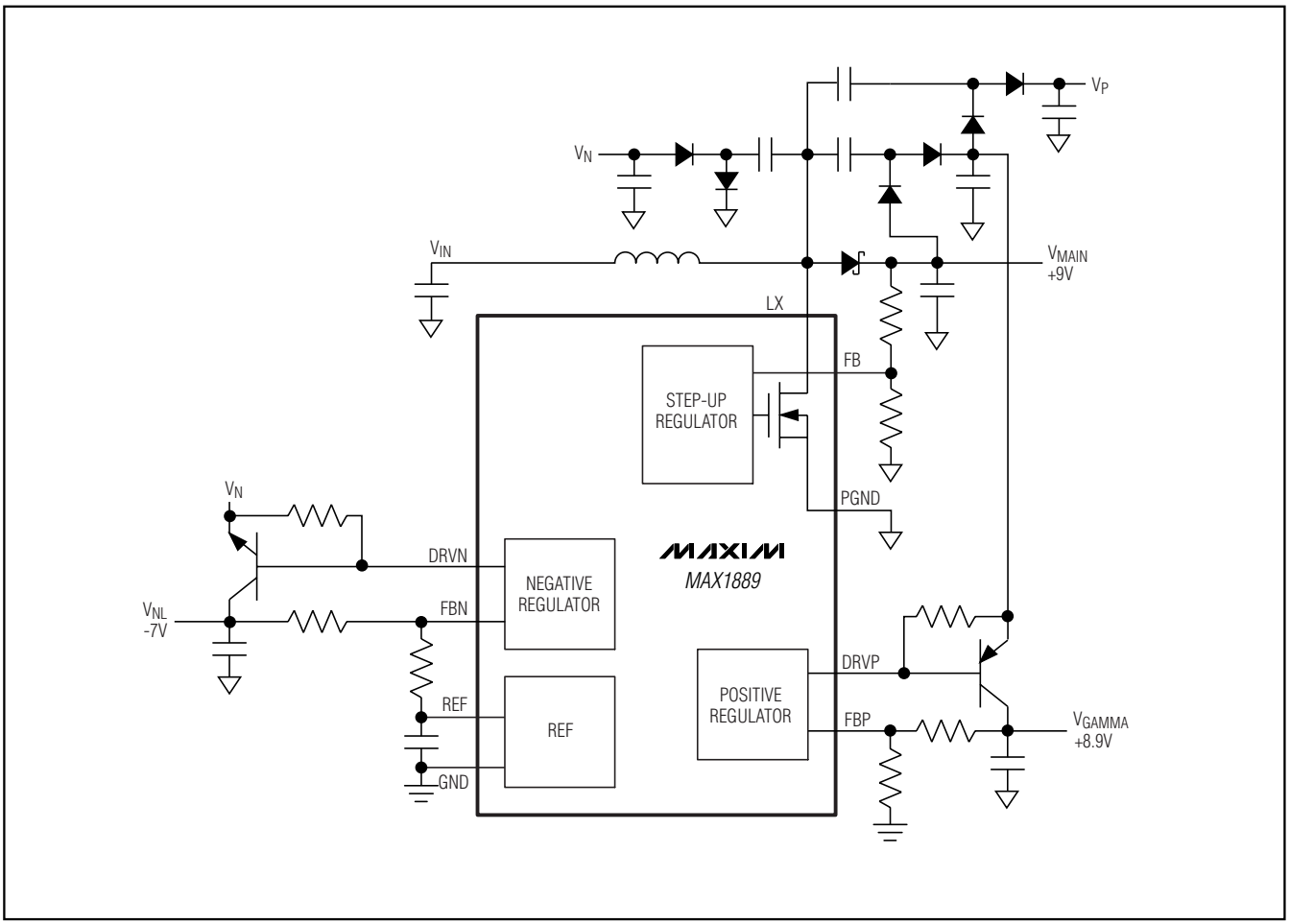
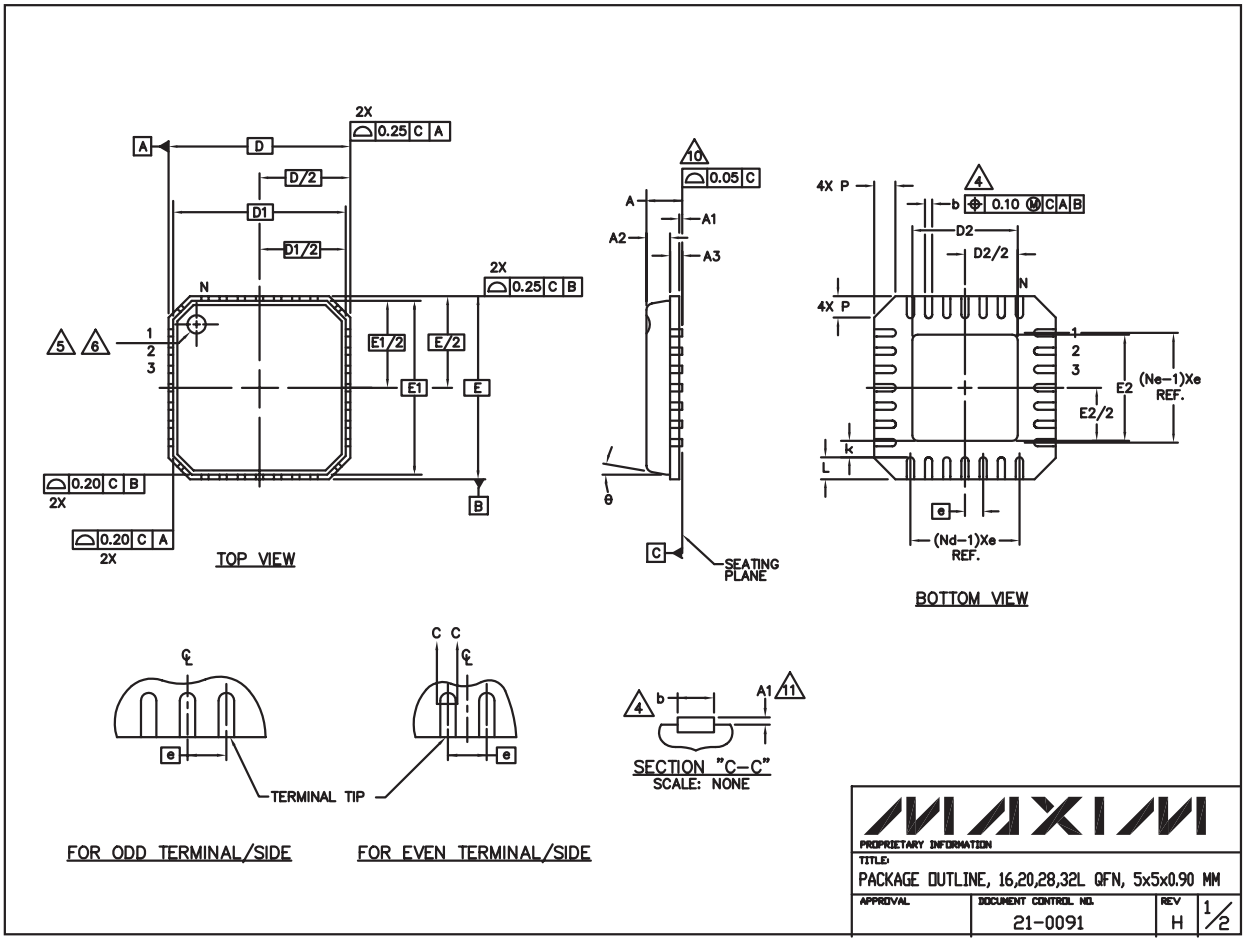


Figure 12. Generating Gamma Reference Voltage

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L QFN.EPS



Triple-Output TFT LCD Power Supply with Fault Protection

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

MAXIM

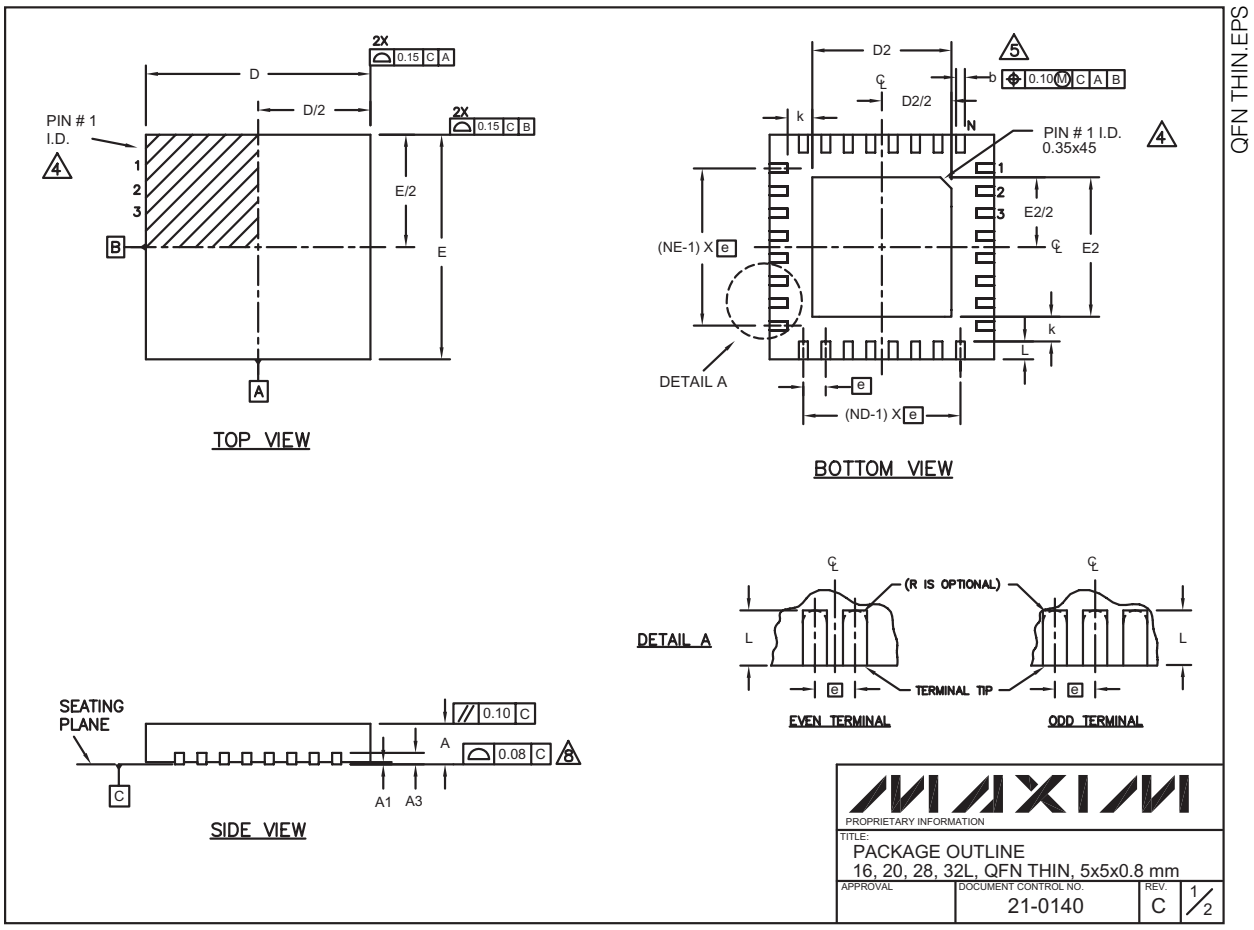
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	H	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Triple-Output TFT LCD Power Supply with Fault Protection

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	C	2/2

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