ADS8323EVM

This user's guide describes the characteristics, operation, and use of the ADS8323 16-bit, 500-kHz, parallel analog-to-digital converter evaluation board. A complete circuit description, a schematic diagram, and bill of materials are included.

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1 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this document by its title and literature number. Updated documents can also be obtained through the TI Web site at http://www.ti.com.

Data Sheets:	Literature Number:
ADS8323	SBAS224
THS4031	SLOS224
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC541	SCLS261

2 EVM Overview

2.1 Features

- Full-featured evaluation board for the ADS8323 16-bit, 500-kHz, single-channel, parallel interface analog-to-digital converter.
- Onboard signal conditioning
- Input and output digital buffers
- Onboard decoding for stacking multiple EVMs

3 Introduction

The ADS8323EVM is a single-channel, analog-to-digital converter evaluation board based on the ADS8323 16-bit, 500-kHz, parallel interface analog-to-digital converter (ADC). Typical power dissipation is 85 mW at a 500-kHz throughput rate and 5-V supply. The device uses a parallel interface.

The EVM incorporates an operational amplifier configured as buffer to ensure a low-noise input to the ADC. This EVM also buffers all the digital input and output signals, effectively isolating the converter from the parallel bus.

The ADS8323EVM Revision B has been redesigned to include a power connector and to allow for sharing the parallel bus with another EVM. The parallel interface is therefore significantly changed from ADS8323EVM Revision A.

4 Analog Interface

The full-scale analog input range for the analog-to-digital (A/D) converter is from 0 V up to twice the reference voltage. A buffer circuit is located between the analog inputs applied at connector J1 and the converter input pins.

Connector J1 is the analog connector. The inverting analog input signal can be applied to pin 1 of connector J1. The noninverting analog input signal should be shorted to pin 2 of connector J1. Jumper W4 selects the input source to the ADS8323 inverting input. It is factory-set to short across W4 pins 2-3 for single-ended mode operation. This configuration applies the on-chip internal reference voltage to the inverting input of the ADC, making the common-mode voltage 2.5 V. If W4 is shorted across pins 1-2, then the inverting input channel is shorted through the buffer circuit from J1, pin 1.

Table 1. Analog Input Connector

Description	Signal Name	Connector.Pin#		Signal Name	Description
Inverting input	(–)	J1.1	J1.2	(+)	Noninverting input
Reserved	N/A	J1.3	J1.4	N/A	Reserved
Reserved	N/A	J1.5	J1.6	N/A	Reserved
Reserved	N/A	J1.7	J1.8	N/A	Reserved

Table 1. Analog Input Connector (continued)

Description	Signal Name	Connector.Pin#		Signal Name	Description
Pin tied to ground	AGND	J1.9	J1.10	N/A	Reserved
Pin tied to ground	AGND	J1.11	J1.12	N/A	Reserved
Reserved	N/A	J1.13	J1.14	N/A	Reserved
Pin tied to ground	AGND	J1.15	J1.16	N/A	Reserved
Pin tied to ground	AGND	J1.17	J1.18	N/A	Reserved
Reserved	N/A	J1.19	J1.20	REF+	External reference input

The factory recommends that the analog input to any SAR-type converter be buffered and low-pass filtered. The recommended circuit is shown in Figure 1. This circuit was tested to ensure that the ac specifications listed in the data sheet of the converter could be met, given a quality input signal.

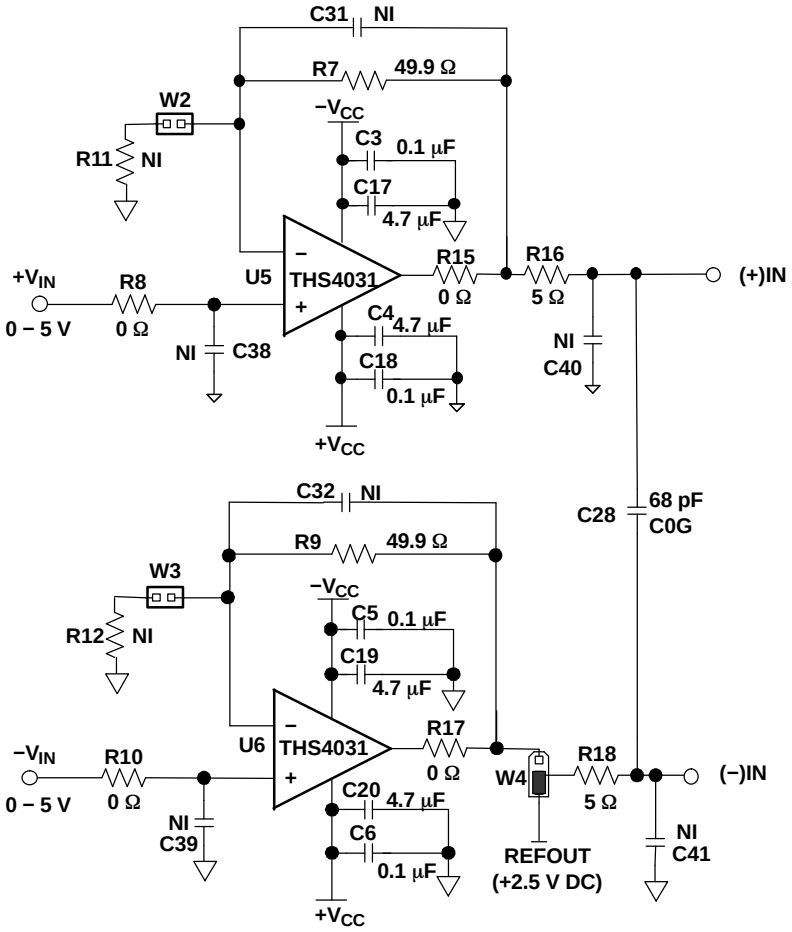

Figure 1. ADS8323 Input Buffer Circuit

4.1 Reference

The ADS8323EVM can be configured to use its on-chip reference, or external reference voltage applied at J1 pin 20 via W1. The EVM is shipped with the on-chip reference (REFout) shorted to REFin of the converter.

Table 2. Jumper Setting

Reference Designator	Description	Jumper Settings	
		1-2	2-3
W1	Short REFout (on-chip reference) to REFin pin	**Installed**(1)	
	Short external reference to REFin		Installed
W2	Short R11 to U4 pin 2	Installed	N/A
W3	Short R12 to U6 pin 2	Installed	N/A
W4	Short U6 output to –IN	Installed	
	Short REFout to –IN		**Installed** (1)
W5	Set A[2..0]=0x1 generates $\overline{RD}$ signal	**Installed**(1)	
	Set A[2..0]=0x2 generates $\overline{RD}$ signal		Installed
W6	Set A[2..0]=0x3 generates $\overline{CONVST}$ signal	**Installed**(1)	
	Set A[2..0]=0x4 generates $\overline{CONVST}$ signal		Installed
W7	Short $\overline{DC\_CS}$ to A/D chip select	**Installed**(1)	*N/A*

(1) Factory-installed setting

5 Digital Interface

The ADS8323EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW-110-22-F-D-VS-K , TSM-110-01-T-DV-P, SSW-116-22-S-D-VS , and TSM-116-01-T-D-V-P provide a convenient dual-row header/socket combination at J1, J2, and J3. Consult Samtec at http://www.samtec.com or 1-800-SAMTEC-9 for mating connector options.

Parallel Control J2 allows the user to plug the EVM into the 5-6K Interface Board to interface directly to TMS320C5000 and TMS320C6000 series of DSPs. See Table 3 for the J2 connector pinout.

Table 3. Pinout for Parallel Control Connector J2

Connector.Pin(1)	Signal	Description
J2.1	$\overline{DC\_CS}$	Daughtercard Select pin
J2.3		
J2.5		
J2.7	A0	Address line from processor
J2.9	A1	Address line from processor
J2.11	A2	Address line from processor
J2.13		
J2.15		
J2.17	CLK	ADC conversion Clock
J2.19	BUSY	Busy signal from converter. W4 must be shorted.

(1) All even-numbered pins of J2 are tied to DGND.

The Read ($\overline{RD}$), Conversion Start ($\overline{CONVST}$) signals to the converter can be assigned to two different addresses in memory via jumper settings. This allows for the stacking of up to two ADS8323EVMs in processor memory. See Table 2 for jumper settings. The evaluation module ships with the Chip Select ($\overline{CS}$) line of the converter shorted to daughtercard Chip Select signal and the $\overline{RD}$ and $\overline{CONVST}$ signals shorted to decoder outputs one and three, respectively.

The data bus is available at connector J3; see Table 4 for pinout information.

Table 4. Data Bus Connector J3

Connector.Pin[(1)]	Signal	Description
J3.1	D0	Buffered data bit 0 (LSB)
J3.3	D1	Buffered data bit 1
J3.5	D2	Buffered data bit 2
J3.7	D3	Buffered data bit 3
J3.9	D4	Buffered data bit 4
J3.11	D5	Buffered data bit 5
J3.13	D6	Buffered data bit 6
J3.15	D7	Buffered data bit 7
J3.17	D8	Buffered data bit 8
J3.19	D9	Buffered data bit 9
J3.21	D10	Buffered data bit 10
J3.23	D11	Buffered data bit 11
J3.25	D12	Buffered data bit 12
J3.27	D13	Buffered data bit 13
J3.29	D14	Buffered data bit 14
J3.31	D15	Buffered data bit 15 (MSB)

(1) All even-numbered pins of J3 are tied to DGND.

This evaluation module provides direct access to all the analog-to-digital converter control signals via connector J4, see Table 5.

Table 5. Converter Control Connector J4

Connector.Pin[(1)]	Signal	Description
J4.1	$\overline{CS}$	Chip Select pin. Active low
J4.3	$\overline{RD}$	Read Pin. Active low
J4.5	$\overline{CONVST}$	Convert start pin. Active low
J4.7	BYTE	BYTE mode pin. Used for 8-bit buses
J4.9	CLK	Conversion clock
J4.11	BUSY	Converter Status Output. High when a conversion is in progress

(1) All even-numbered pins of J4 are tied to DGND.

6 Power Supplies

The EVM accepts four power supplies.

- A dual ±Vs dc supply for the dual supply operational amplifiers. Recommend ±12-Vdc supply.
- A single +5-Vdc supply for analog section of the board (A/D).
- A single +5-Vdc supply for digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

1. Wire in voltages at test points on the EVM. See Table 6.

Table 6. Power Supply Test Points

Test Point	Signal	Description
TP16	+5VD	Apply +5 Vdc.
TP13	+5VA	Apply +5 Vdc.

Table 6. Power Supply Test Points (continued)

Test Point	Signal	Description
TP14	+VA	Apply +12 Vdc. Positive supply for amplifier
TP15	–VA	Apply –12 Vdc. Negative supply for amplifier

2. Use the power connector J5 and derive the voltages elsewhere. The pinout for this connector is shown in Table 7

Table 7. Power Connector, J1, Pinout

Signal	Power Connector – J5		Signal
+VA(+12V)	1	2	–VA(–12V)
+5VA	3	4	N/C
N/C	5	6	AGND
N/C	7	8	N/C
N/C	9	10	+5VD

7 Using the EVM

The ADS8323EVM serves three functions as a reference design, a prototype board, and as a test platform for the software engineer to develop code.

As a reference design, the ADS8323EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier and digital buffers. The EVM analog input circuit is optimized for 100-kHz sine wave; therefore, users may need to adjust the resistor and capacitor values of the A/D input RC circuit. In ac-type applications where signal distortion is a concern, polypropylene or low-cost SMT C0G ceramic capacitors should be used in the signal path. In applications where the input is multiplexed, the A/D input resistor and capacitor may need to be adjusted or possibly removed altogether.

As a prototype board, the buffer circuit consists of a standard 8-pin SOIC amplifier and resistor pads to adjust to various inverting and noninverting configurations. The EVM comes installed with a dual-supply amplifier, which allows the user to take advantage of the full input voltage range of the converter. For applications that require signal supply operation and smaller input voltage range, the THS4031 can be replaced with the single-supply amplifier like OPA300 or OPA355. Be sure to short the negative supply pin to ground in that case. Positive supply voltage can be applied via test point TP14 or connector J5, pin 1.

As a software test platform, connectors J1, J2, and J3 plug into the parallel interface connectors of the 5-6K Interface Board. The 5-6K Interface Board sits on the 'C5000 and 'C6000 digital signal processor starter kit (DSK). The ADS8323EVM is then mapped into the processor's memory space. This board also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitalization by the ADS8323 analog-to-digital converter. See the 5-6K Interface Board User's Guide (SLAU104) for more information.

For the software engineer, the ADS8323EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-in. headers and sockets to wire into prototype boards. The user needs only to provide three address lines (A2, A1, and A0) and address valid line ($\overline{DC\_CS}$) , and clock to connector J2. To choose which address combinations will generate $\overline{RD}$ and $\overline{CONVST}$, set jumpers as shown in Table 2. If address decoding is not required, the EVM provides direct access to converter data bus via J3 and control via J4.

Appendix A ADS8323EVM Bill of Materials

Table A-1 contains a complete bill of materials for the ADS8323EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or send an E-mail to dataconvapps@list.ti.com for questions regarding this EVM.

Table A-1. Bill of Materials

Item No.	Qty	Value	Reference Designators	Footprint	Mfg	Mfg's Part Number	Description
1	5	10 kΩ	R1 R2 R3 R4 R19	603	Panasonic - ECG or alternate	ERJ-3EKF1002V	RES 10.0 kΩ 1/16W 1% 0603 SMD
2	1	511 Ω	R5	1206	Panasonic - ECG or alternate	ERJ-8ENF5110V	RES 511 Ω 1/8W 5% 0805 SMD
3	4	NI	R6 R11 R12 R13	1206	Not Installed	Not Installed	1/4 W 1206 Chip resistor
4	2	49.9 Ω	R7 R9	805	Panasonic - ECG or alternate	ERJ-6ENF49R9V	RES 49.9 Ω 1/10W 1% 0805 SMD
5	4	0	R8 R10 R15 R17	805	Panasonic - ECG or alternate	ERJ-6GEY0R00V	RES 0.0 Ω 1/8W 5% 0805 SMD
6	1	0	R14	1206	Panasonic - ECG or alternate	ERJ-8GEY0R00V	RES 0.0 Ω 1/4W 5% 1206 SMD
7	2	5	R16 R18	805	Yageo America or alternate	9C08052A4R99FGHFT	RES 49.9 Ω 1/8W 1% 0805 SMD
8	7	4.7uF	C1 C2 C3 C4 C19 C20 C23	805	TDK Corporation	C3216X7R1E475M	CAP CER 4.7 µF 25V X7R 20% 1206
9	9	0.1 µF	C5 C6 C7 C8 C17 C18 C42 C43 C44	805	TDK Corporation	C2012X7R1E104K	CAP CER 0.01 µF 25V X7R 10% 0805
10	5	0.1uF	C9 C10 C24 C25 C26	1206	TDK Corporation	C3216X7R2A104M	CAP CER 0.1 µF 100V X7R 20% 1206
11	4	0.01uF	C11 C12 C21 C22	805	TDK Corporation	C2012X7R2A103K	CAP CER 10000 pF 100V X7R 10%0805
12	3	0.01uF	C13 C14 C34	1206	TDK Corporation	C3216C0G1H103J	CAP CER 10000 pF 50V C0G 5% 1206
13	8	NI	C15 C16 C31 C32 C38 C39 C40 C41	805	Not Installed	Not Installed	Multilayer Ceramic
14	1	68 pF	C28	805	Murata Electronics North America	GRM2195C2A680JZ01D	CAP CER 68 pF 100V 5% C0G 0805
15	3	10 µF	C33 C36 C37	1206	TDK Corporation	C3216X5R1C106M	CAP CER 10 µF 16V X5R 20% 1206
16	1	10 µF	C35	805	TDK Corporation	C2012Y5V1A106Z	CAP CER 10 µF 10V Y5V 0805
17	1	0.1uF	C27	603	TDK Corporation	C1608X7R1E104K	CAP CER 0.10 µF 25V X7R 10% 0603
18	1	100	RP1	CTS_742	CTS Corporation	742C163101JTR	RES Array 100 Ω 16TRM 8RES SMD
19	2	1K	RP2 RP3	CTS_742	CTS Corporation	742C163102JTR	RES Array 1 kΩ 16TERM 8RES SMD
20	1		D1	LED-1206	Chicago Miniature Lamp Inc	CMD15-21VYC/TR8	Yellow Lumex SM LED
21	4		FL1 FL2 FL3 FL4	NFM51R	Murata-Erie	NFM60R10T471	T-type EMI chip filter
22	1	1	U1	20-TSSOP(PW)	Texas Instruments	SN74AHCT541PWR	Octal Buffer and Driver
23	1	DUT	U2	32-TQFP	Texas Instruments	ADS8323YB	ADS8323 16-bit 500 KSPS A/D
24	2		U5 U6	8-SOP(D)	Texas Instruments	THS4031IDR	100-MHz Low-noise high-speed amplifier
25	2		U7 U8	20-TSSOP(PW)	Texas Instruments	SN74AHC245PWR	Octal Bus Transceiver, 3-State
26	1		U11	16-TSSOP(PW)	Texas Instruments	SN74AHC138PWR	3-Line To 8-Line Decoder / Demultiplexer
27	2	10X2X.1	J1 J2	10×2×0.1_SMT_PLUG_&_SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT Plug - bottom side of PWB
28	2				Samtec	TSM-110-01-T-D-V-P	0.025" SMT Plug - Top Side of PWB
29	1	32 Pin_IDC	J3	16×2×0.1_SMT_PLUG_&_SOCKET	Samtec	TSM-116-01-T-D-V-P	0.025" SMT Plug - Top Side of PWB
30	1				Samtec	SSW-116-22-S-D-VS	0.025" SMT socket - bottom side of PWB
31	1	6×2×0.1	J4	6×2×0.1_SMT_PLUG_&_SOCKET	Samtec	TSM-106-01-T-D-V-P	0.025" SMT Plug - top side of PWB
32	1	5×2×0.1	J5	5X2X0.1_SMT_SOCKET	Samtec	TSM-105-01-T-D-V-P	0.025" SMT Plug - top side of PWB
33	1				Samtec	SSW-105-22-S-D-VS	0.025" SMT socket - bottom side of PWB

Table A-1. Bill of Materials (continued)

Item No.	Qty	Value	Reference Designators	Footprint	Mfg	Mfg's Part Number	Description
34	4		W1 W4 W5 W6	3pos_jump	Samtec	TSW-103-07-L-S	3 Position Jumper_0.1" spacing
35	3		W2 W3 W7	2pos_jump	Samtec	TSW-102-07-L-S	2 Position Jumper_0.1" spacing
36	10	TP_0.025	TP1 TP3 TP5 TP7 TP9 TP10 TP13 TP14 TP15 TP16	test_point2	Keystone Electronics	5000K–ND	Test point PC MINI 0.040"D Red
37	6	TP_0.025	TP2 TP4 TP6 TP8 TP11 TP12	test_point2	Keystone Electronics	5001K–ND	Test point PC MINI 0.040"D Black

Appendix B ADS8323EVM Layout

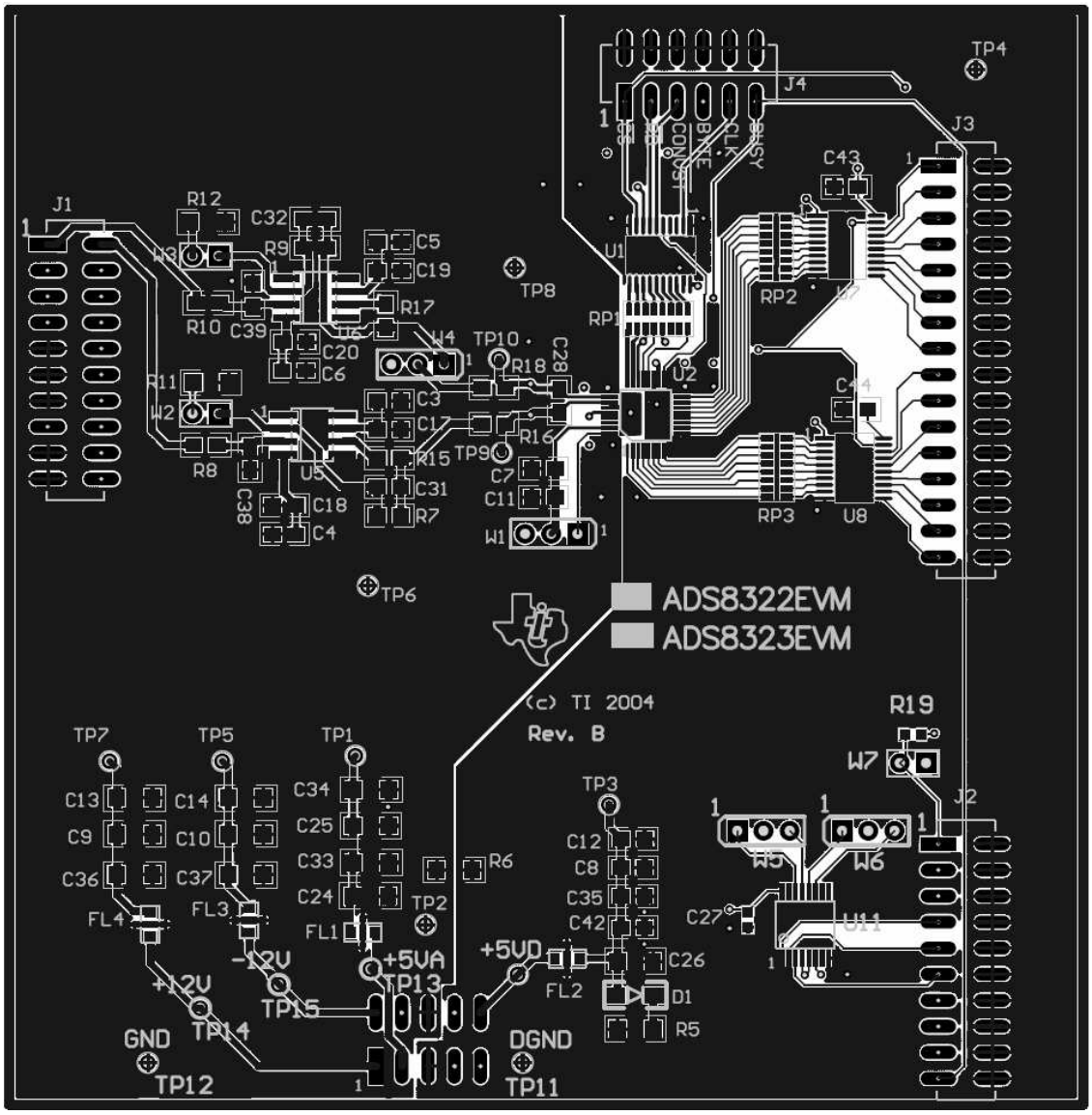

Figure B-1. Top Layer – Layer 1

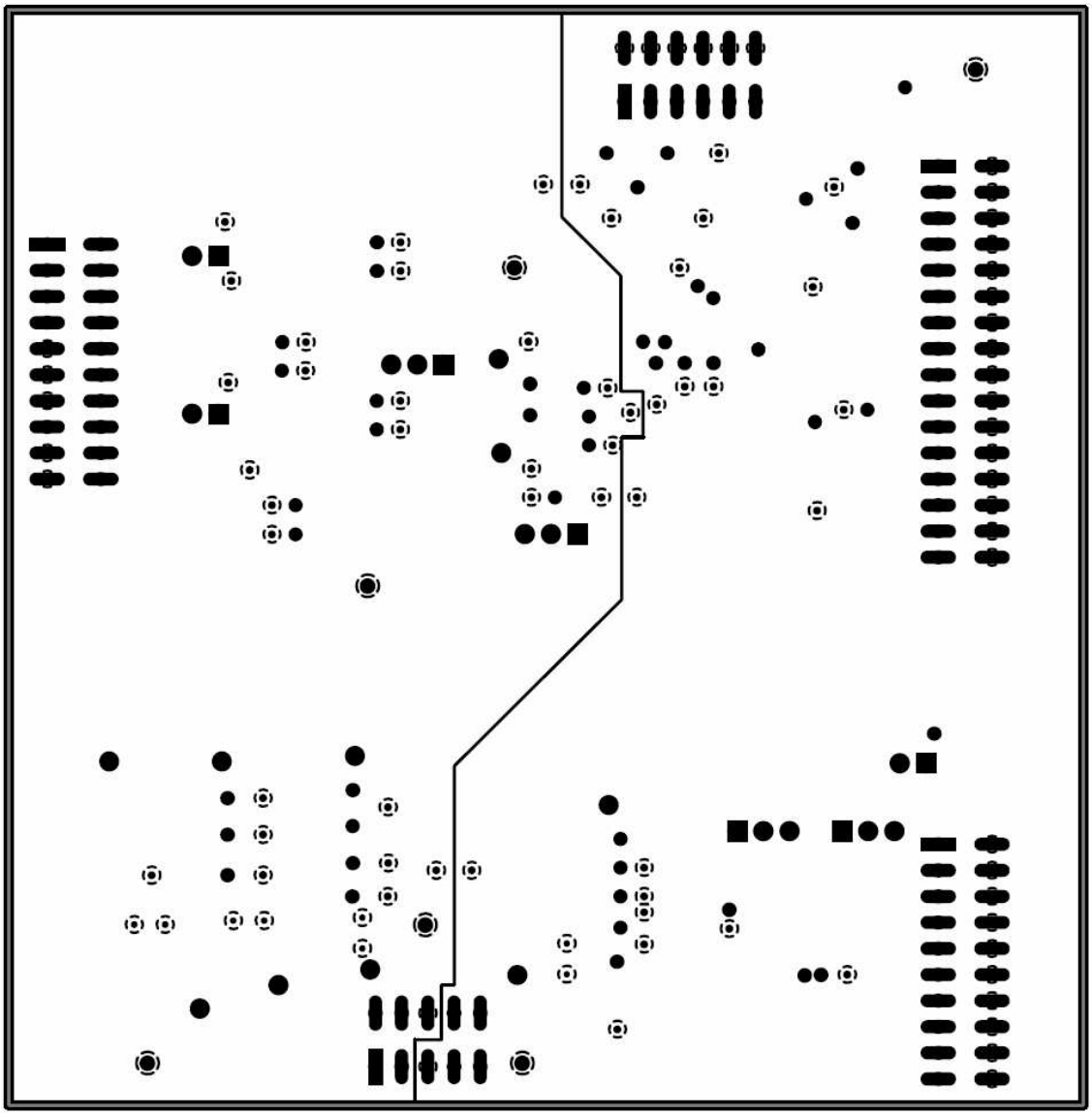

Figure B-2. Ground Plane – Layer 2

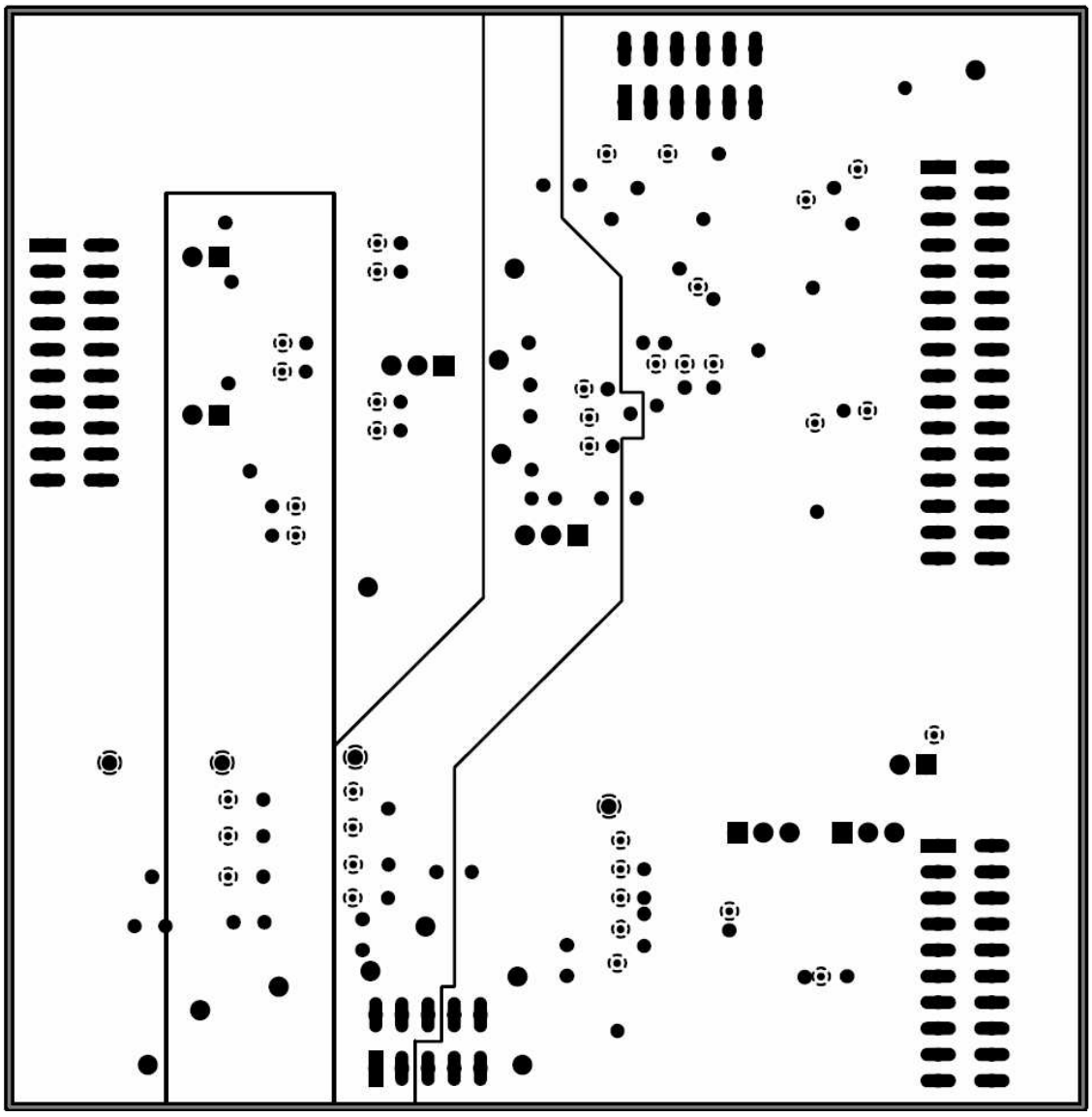

Figure B-3. Power Plane – Layer 3

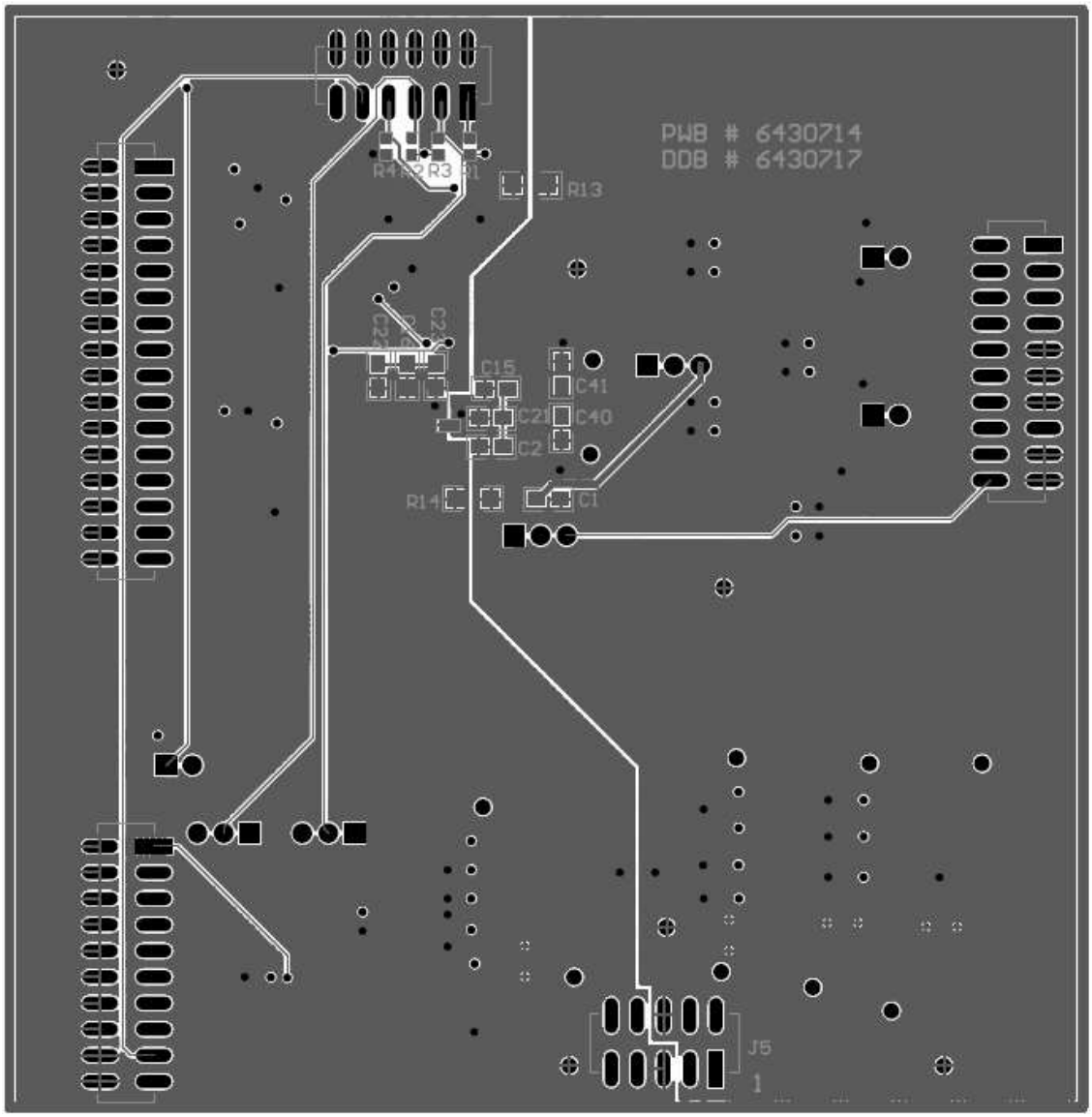

Figure B-4. Bottom Layer – Layer 4

Appendix C ADS8323EVM Schematic

See attachment for schematic drawings.

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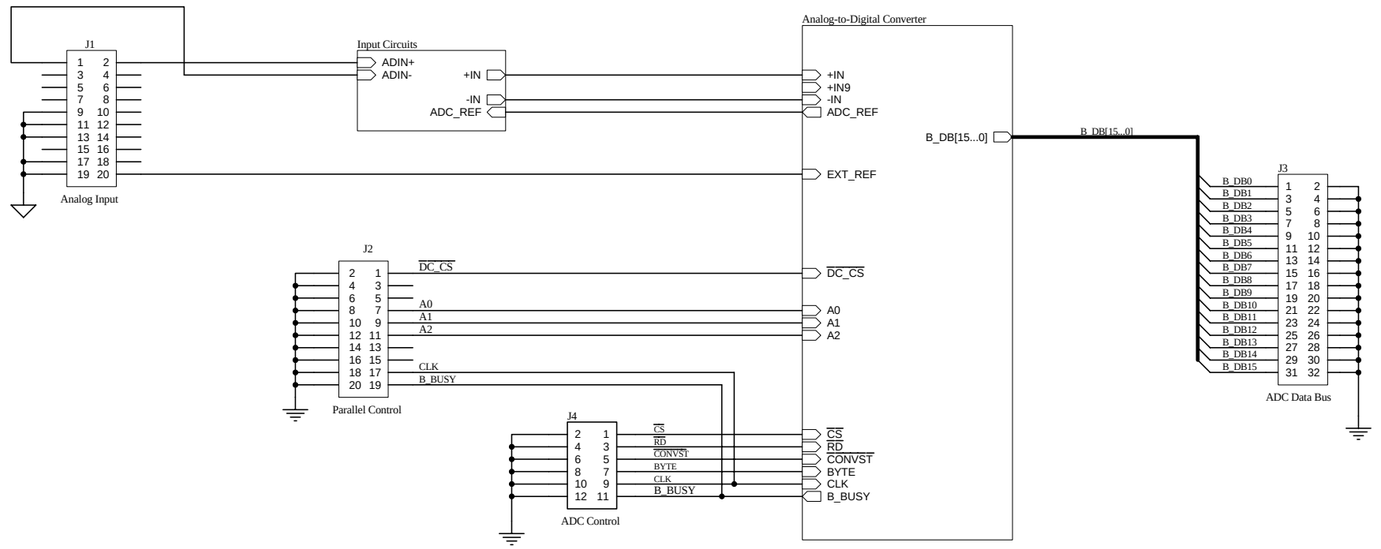

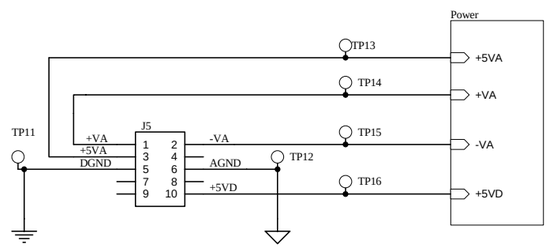

Engineer:	L. Philipose
Drawn By:	L. Philipose
FILE:	block diagram.Sch

TEXAS INSTRUMENTS

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TITLE: ADS8323EVM Block Diagram

DOCUMENT CONTROL #:	REV:
6430717	B

DATE:	SIZE:	SHEET:	OF:
17-Nov-2004		1	4

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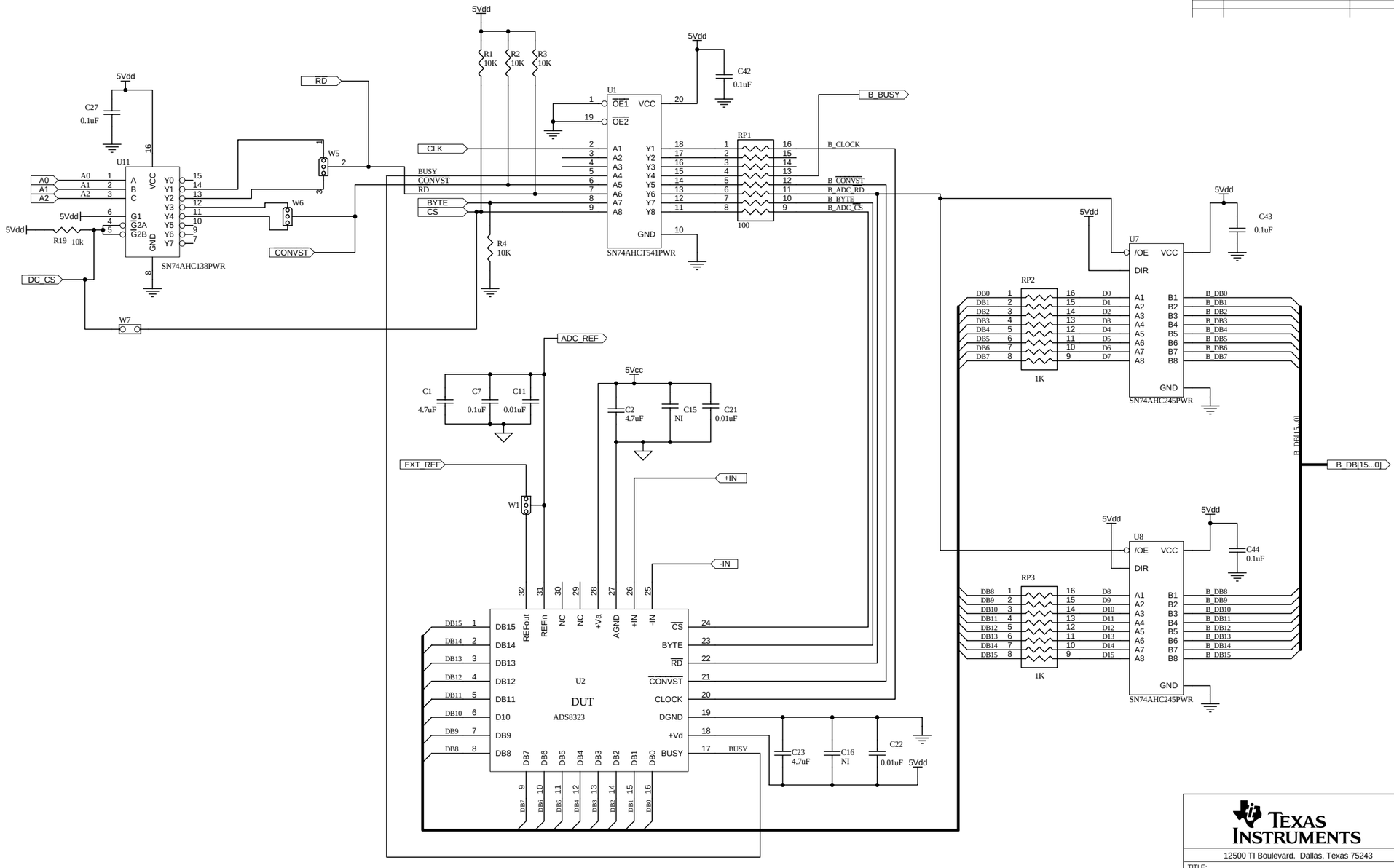

Engineer:	
Drawn By:	
FILE: Analog-to-Digital Converter	

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

TITLE: Converter and Digital Buffer

DOCUMENT CONTROL #:	REV:
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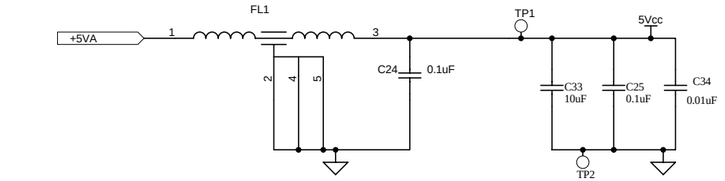

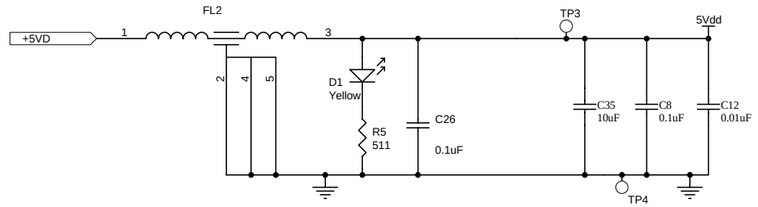

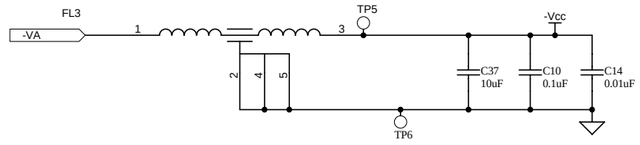

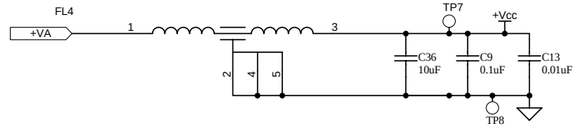

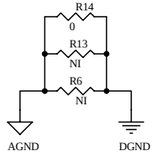

Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	Power

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

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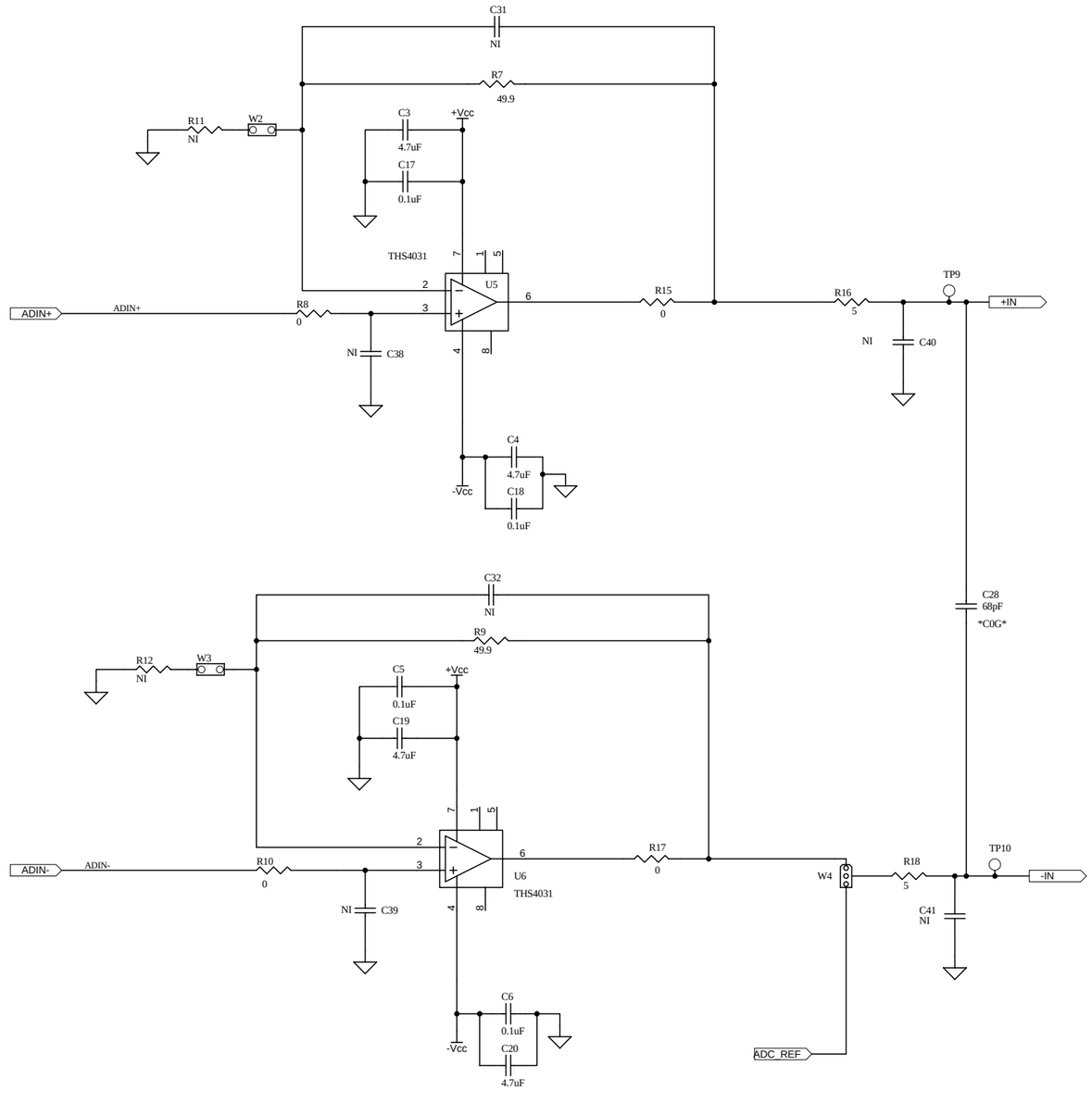

Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	Input Circuits

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

TITLE: Input Buffer

DOCUMENT CONTROL #: 6430717 | REV: B

DATE: 17-Nov-2004 | SIZE: | SHEET: 4 OF: 4

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