

Negative Output Flyback Pulse Width Modulator

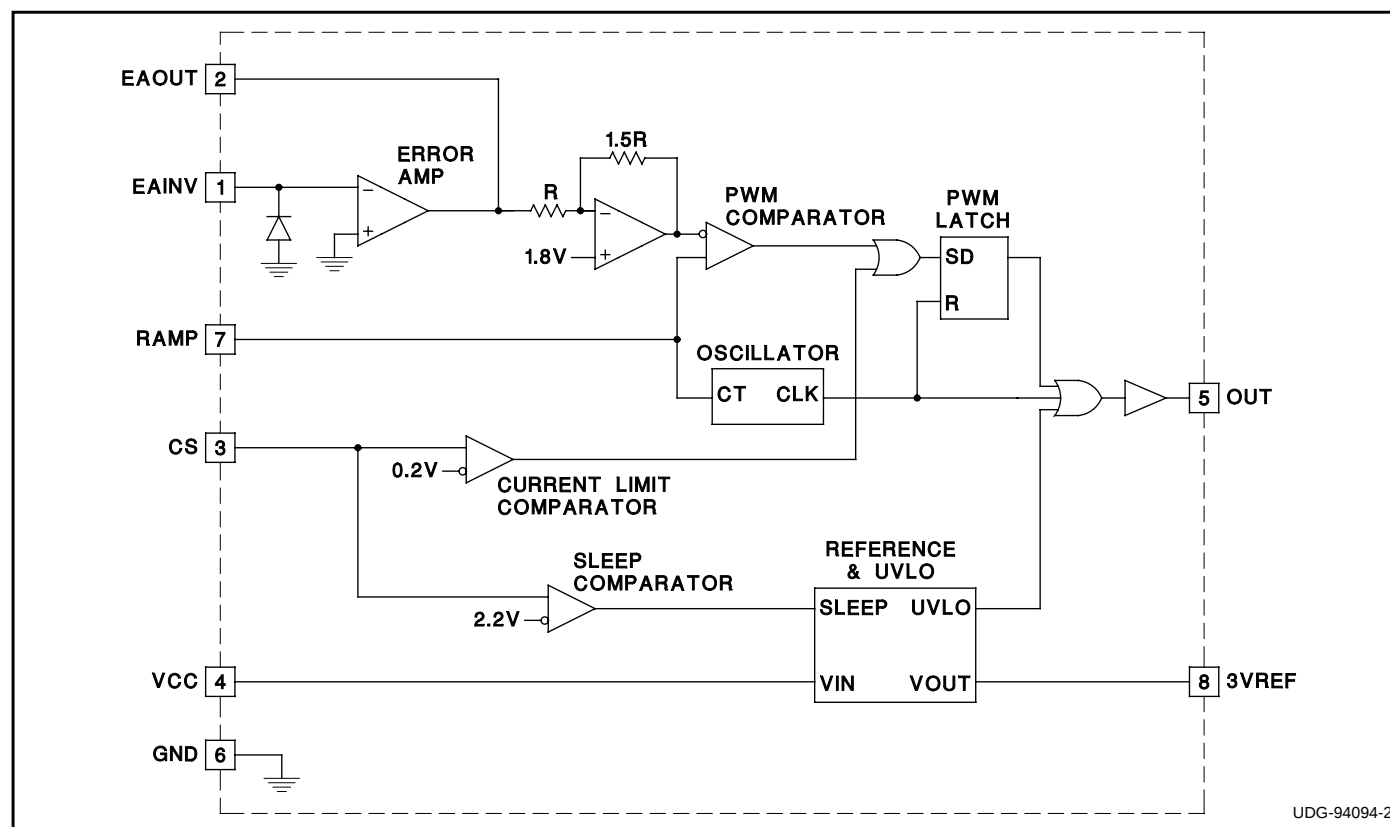
FEATURES

- Simple Single Inductor Flyback PWM for Negative Voltage Generation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50 μ A Sleep Mode Current

DESCRIPTION

The UC3572 is a negative output flyback pulse width modulator which converts a positive input voltage to a regulated negative output voltage. The chip is optimized for use in a single inductor negative flyback switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3572 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Output current can be sensed and limited to a user determined maximum value. The UVLO circuit turns the chip off when the input voltage is below the UVLO threshold. In addition, a sleep comparator interfaces to the UVLO circuit to turn the chip off. This reduces the supply current to only 50 μ A, making the UC3572 ideal for battery powered applications.

BLOCK DIAGRAM



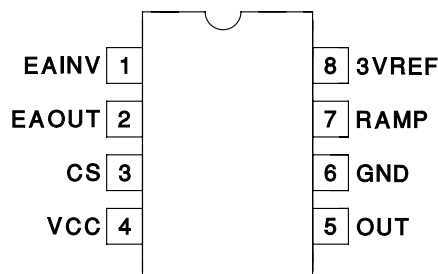
ABSOLUTE MAXIMUM RATINGS

VCC	35V
EAINV	-0.6V to VCC
IEAOUT	25mA
RAMP	-0.3V to 4V
CS	-0.3V to VCC
Iout	-0.7A to 0.7A
I3VREF	15mA
Storage Temperature	-65°C to +150°C
Junction Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (TOP VIEW)
D, N or J Packages



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1572	-55°C to +125°C	J
UC2572	-40°C to +85°C	D, N or J
UC3572	0°C to +70°C	D or N

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I3VREF = 0V to -5mA		1	10	mV
Oscillator Section					
Frequency	VCC = 5V to 30V	85	100	115	kHz
Error Amp Section					
EAINV	EAOUT = 2V	-10	0	10	mV
	IEANV = -1mA		-0.2	-0.9	V
IEAINV	EAOUT = 2V		-0.2	-1.0	μA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = -100mV	3.6	4	4.4	V
EAOUT Low	EAINV = 100mV		0.1	0.2	V
IEAOUT	EAINV = -100mV, EAOUT = 2V	-350	-500		μA
	EAINV = 100mV, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	TJ = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold		0.185	0.205	0.225	V
Input Bias Current	CS = 0		-0.4	-1	μA
CS Propagation Delay			300		nS

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drive Output Section					
OUT High Saturation	I _{OUT} = 0		0	0.3	V
	I _{OUT} = -10mA		0.7	1.5	V
	I _{OUT} = -100mA		1.5	2.5	V
OUT Low Saturation	I _{OUT} = 10mA		0.1	0.4	V
	I _{OUT} = 100mA		1.5	2.2	V
Rise Time	T _J = 25°C, C _{LOAD} = 1nF + 3.3 Ohms		30	80	nS
Fall Time	T _J = 25°C, C _{LOAD} = 1nF + 3.3 Ohms		30	80	nS
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = +100mV, VCC = 5V to 30V		92	96	%
Minimum Duty Cycle	EAINV = -100mV, VCC = 5V to 30V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	45	55	65	%/V
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
IVCC	VCC = 5V, 30V		9	15	mA
	VCC = 30, CS = 3V		50	150	μA

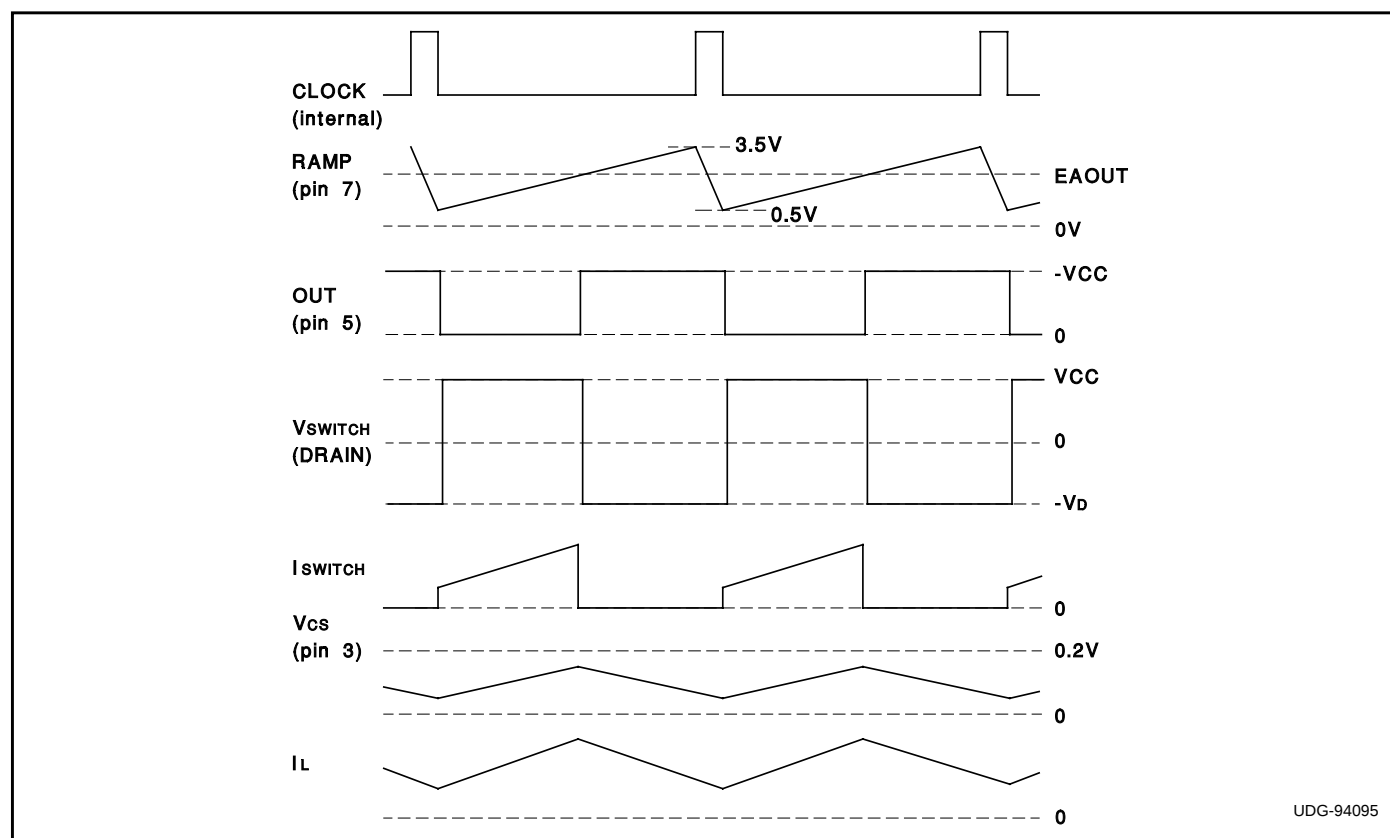


Figure 1. Typical waveforms.

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor to GND.

CS: Current limit sense pin. Connect to a ground referenced current sense resistor in series with the flyback inductor. OUT will be held high (PMOS switch off) if CS exceeds 0.2V.

EAINV: Inverting input to error amplifier. Summing junction for 3VREF and VOUT sense. The non-inverting input of the error amplifier is internally connected to GND. This pin will source a maximum of 1mA.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

OUT: Gate drive for external PMOS switch connected between Vcc and the flyback inductor. OUT drives the gate of the PMOS switch between Vcc and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \cdot C_{RAMP}}$$

Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75 to 30V. Bypass with a 1μF capacitor.

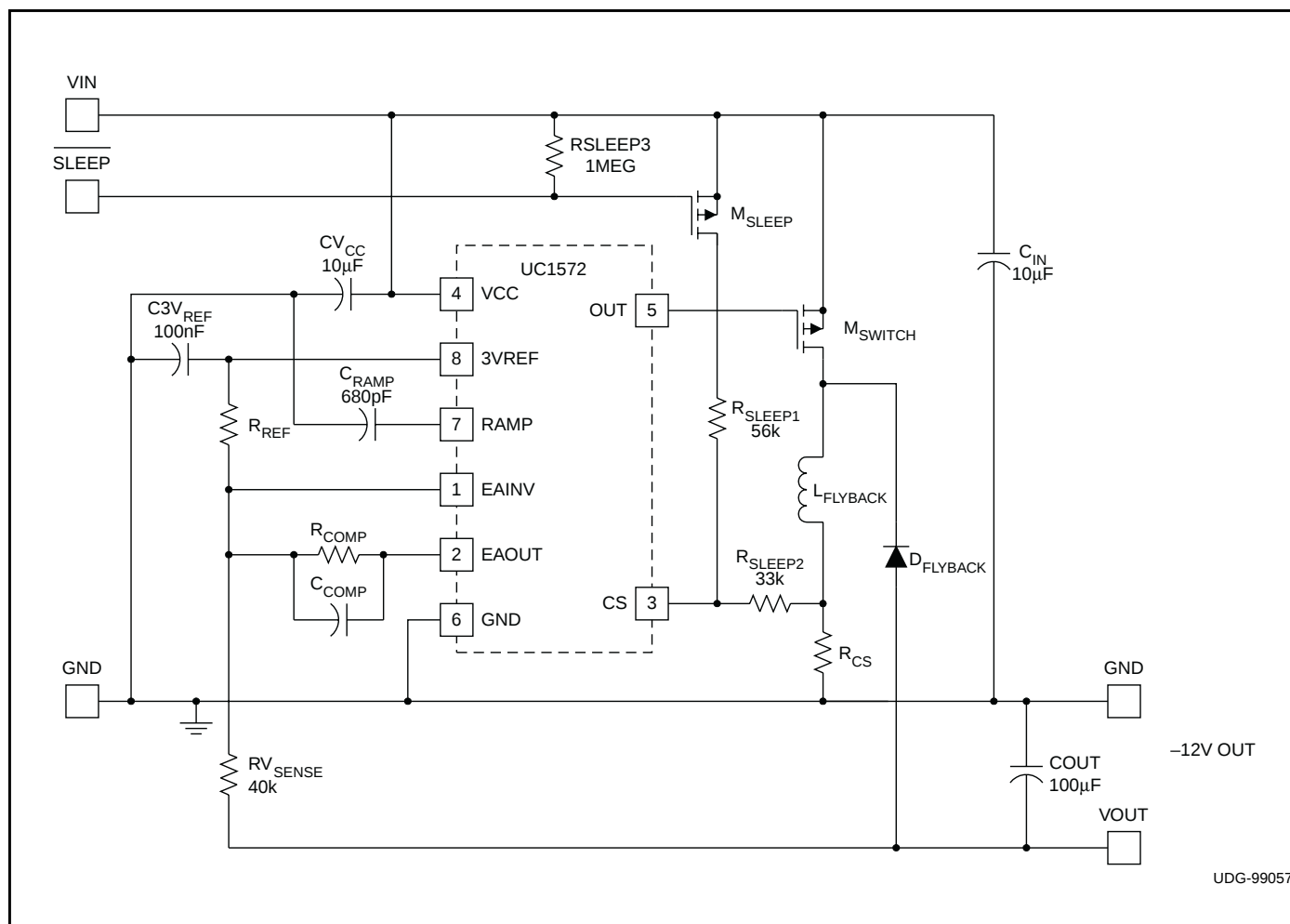


Figure 2. Typical application: +5V to -12V flyback converter.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC1572J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI
UC2572D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2572DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2572DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2572DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2572N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2572NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3572D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3572DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3572DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3572DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3572N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3572NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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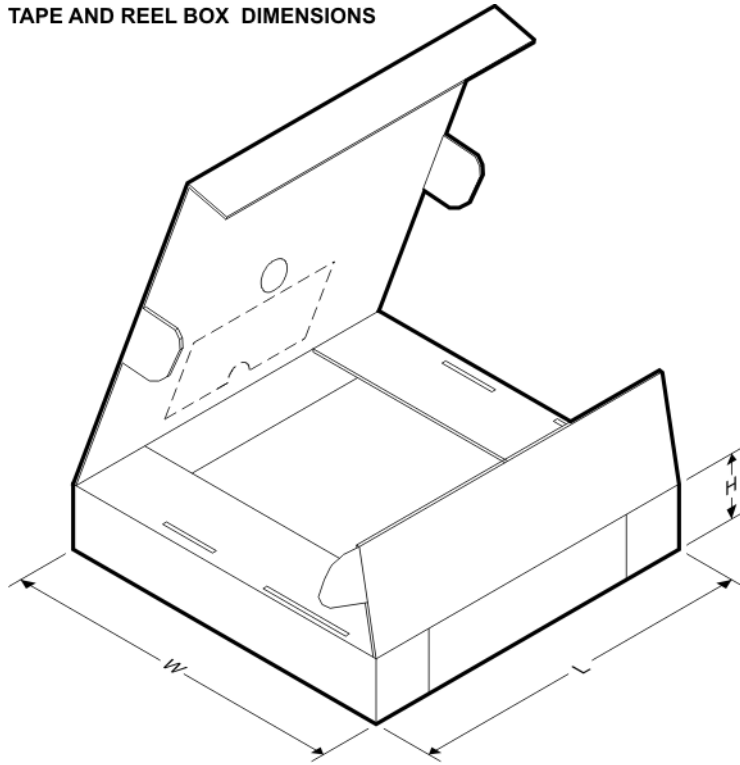
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2572DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3572DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2572DTR	SOIC	D	8	2500	340.5	338.1	20.6
UC3572DTR	SOIC	D	8	2500	340.5	338.1	20.6

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