Ordering number : ENA2017B

LV5694P

Bi-CMOS IC

System Power Supply IC for Automotive Infotainment Multiple Output Linear Voltage Regulator

ON Semiconductor®

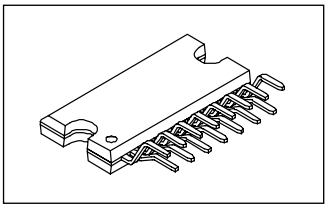
http://onsemi.com

Overview

The LV5694P is a multiple output linear regulator IC, which allows reduction of quiescent current. The LV5694P is specifically designed to address automotive infotainment systems power supply requirements. The LV5694P integrates 5 linear regulator outputs, 2 high side power switches, over current protection, overvoltage protection and thermal shutdown circuitry.

Function

- Low consumption current:
  50μA (typ, only V_{DD} output is in operation)
- 5 systems of regulator output
  V_{DD} for microcontroller:
  output voltage: 5.0V/3.3V (always ON),
  maximum output current: 300mA
  For SWD5V: output voltage: 5V,
  maximum output current: 500mA
  For CD: output voltage: 7.6V/8.1V,
  maximum output current: 2000mA
  For illumination: output voltage: 9.0V,
  maximum output current: 500mA
  For audio: output voltage: 8.45V,
  maximum output current: 800mA
- 2 lines of high side switch with interlock V_{CC}
  AMP: Maximum output current: 500mA, voltage difference between input and output: 0.5V
  ANT: Maximum output current: 350mA, voltage difference between input and output: 0.5V
- Overcurrent protector
- Overvoltage protector: Typ 36V (All outputs are turned off)
- Overheat protector: Typ 175°C
- PchLDMOS is used in power output block



HZIP15J

(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

Semiconductor Components Industries, LLC, 2014
March, 2014

32014NK/71112SY/30712SY 20120203-S00001 No.A2017-1/14

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{CC} max			36	V
Power dissipation	Pd max	IC unit	Ta ≤ 25°C	1.5	W
		At using Al heat sink		5.6	W
		At infinity heat sink		32.5	W
Peak voltage	V_{CC} peak	Regarding Bias wave, refer to below the pulse.		50	V
Junction temperature	Tj max			150	°C
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Conditions	Ratings	Unit
Power supply voltage rating 1	V_{DD} output, SWD output	7 to 16	V
Power supply voltage rating 2	ILM output	10.8 to 16	V
Power supply voltage rating 3	Audio output, CD output	10 to 16	V
Power supply voltage rating 4	ANT output, AMP output	7.5 to 16	V

* $V_{CC}1$ should be as follows: $V_{CC}1 > V_{CC}-0.7V$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, $V_{CC} = V_{CC}1 = 14.4V$ (*2)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
$V_{CC}1$ input voltage	$V_{CC}1$		V_{CC}-0.7V		16	V
Current drain	I_{CC}	V_{DD} no load, CTRL1/2/3 =「L/L/L」		50	100	μA
CTRL1/2/3 Input						
Low input voltage	$V_{IL}1$		-	-	0.3	V
Middle1 input voltage	$V_{IM}1$		0.9	1.18	1.45	V
Middle2 input voltage	$V_{IM}2$		1.85	2.10	2.4	V
High input voltage	$V_{IH}1$		2.95	3.29	5.5	V
Input impedance	$R_{IH}1$	Input voltage ≤ 3.3V	280	400	520	kΩ
IKCD/IKV_{DD} Input						
Low input voltage	$V_{IL}2$		-	-	0.7	V
High input voltage	$V_{IH}2$	IKCD IKV_{DD}	V_{CC}-0.7V $V_{CC}1$-0.7V	-	-	V
V_{DD} output (5V/3.3V)						
Output voltage	V_O11	I_O1 = 200mA, IKV_{DD}=$V_{CC}1$	4.75	5.0	5.25	V
	V_O12	I_O1 = 200mA, IKV_{DD}=GND	3.16	3.3	3.45	V
Output current	I_O1	$V_O11 \geq 4.70V$, $V_O12 \geq 3.10V$	300			mA
Line regulation	$\Delta V_{OLN}1$	$7.5V < V_{CC}1 < 16V$, I_O1 = 200mA		30	70	mV
Load regulation	$\Delta V_{OLD}1$	$1mA < I_O1 < 200mA$		70	150	mV
Dropout voltage 1	$V_{DROP}1$	I_O1 = 200mA (V_{DD} output 5V)		0.8	1.6	V
Dropout voltage 2	$V_{DROP}1'$	I_O1 = 100mA (V_{DD} output 5V)		0.4	0.8	V
Ripple rejection	$R_{REJ}1$	f = 120Hz, I_O1 = 200mA	30	40		dB
Short circuit current	I_S1	V_O11, V_O12 = 0	50	150	340	mA

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
AUDIO (8.45V) Output ; CTRL2 =⌈M1 or H⌋						
Output voltage	V_O3	I_O3 = 650mA	8.16	8.45	8.7	V
Output current	I_O3	$V_O3 \geq 8.0V$	800			mA
Line regulation	$\Delta V_{OLN}3$	$10V < V_{CC} < 16V$, I_O3 = 650mA		30	90	mV
Load regulation	$\Delta V_{OLD}3$	$1mA < I_O3 < 650mA$		100	200	mV
Dropout voltage 1	$V_{DROP}3$	I_O3 = 650mA		0.7	1.2	V
Dropout voltage 2	$V_{DROP}3'$	I_O3 = 200mA		0.2	0.35	V
Ripple rejection	$R_{REJ}3$	f = 120Hz, I_O3 = 650mA	40	50		dB
Short circuit current	I_S3	V_O3 = 0	120	250	550	mA
ILM (9V) Output ; CTRL1 =⌈M1 or H⌋						
Output voltage	V_O4	I_O4 = 350mA	8.7	9.0	9.3	V
Output current	I_O4	$V_O4 \geq 8.6V$	500			mA
Line regulation	$\Delta V_{OLN}4$	$10.8V < V_{CC} < 16V$, I_O4 = 350mA		40	100	mV
Load regulation	$\Delta V_{OLD}4$	$1mA < I_O4 < 350mA$		70	150	mV
Dropout voltage 1	$V_{DROP}4$	I_O4 = 350mA		1.0	1.5	V
Dropout voltage 2	$V_{DROP}4'$	I_O4 = 200mA		0.3	0.6	V
Ripple rejection	$R_{REJ}4$	f = 120Hz, I_O4 = 350mA	40	50		dB
Short circuit current	I_S4	V_O4 = 0	100	200	400	mA
AMP_HS-SW; CTRL3 =⌈M2 or H⌋						
Output voltage	V_O5	I_O5 = 500mA		V_{CC}-0.5	V_{CC}-1.0	V
Output current	I_O5	$V_O5 \geq V_{CC}$-1.0V	500			mA
Short circuit current	I_S5	V_O5 = 0	120	250	500	mA
ANT_HS-SW; CTRL3 =⌈M1 or H⌋						
Output voltage	V_O6	I_O6 = 500mA		V_{CC}-0.5	V_{CC}-1.0	V
Output current	I_O6	$V_O6 \geq V_{CC}$-1.0V	350			mA
Short circuit current	I_S6	V_O6 = 0	100	200	450	mA
SWD5V; CTRL2 =⌈M2 or H⌋						
Output voltage	V_O7	I_O7 = 350mA	4.75	5.0	5.25	V
Output current	I_O7	$V_O7 \geq 4.7V$	500			mA
Line regulation	$\Delta V_{OLN}7$	$10V < V_{CC} < 16V$, I_O7 = 350mA		30	70	mV
Load regulation	$\Delta V_{OLD}7$	$1mA < I_O7 < 350mA$		70	150	mV
Dropout voltage	$V_{DROP}7$	I_O7 = 350mA		0.8	1.6	V
Ripple rejection	$R_{REJ}7$	f = 120Hz, I_O7 = 350mA	40	50		dB
Short circuit current	I_S7	V_O7 = 0	100	200	450	mA
CD(7.6/8.1V output); CTRL1 =⌈M2 or H⌋						
Output voltage	V_O81	I_O8 = 1300mA, IKCD=GND	7.2	7.6	8.0	V
	V_O82	I_O8 = 1300mA, IKCD=V_{CC}	7.7	8.1	8.5	V
Output current	I_O8	$V_O81 \geq 7.1V$, $V_O82 \geq 7.5V$	2000			mA
Line regulation	$\Delta V_{OLN}8$	$10.5V < V_{CC} < 16V$, I_O8 = 1300mA		40	100	mV
Load regulation	$\Delta V_{OLD}8$	$10mA < I_O8 < 1300mA$		70	200	mV
Dropout voltage 1	$V_{DROP}8$	I_O8 = 1300mA		1.3	1.5	V
Dropout voltage 2	$V_{DROP}8'$	I_O8 = 350mA		0.35	0.7	V
Ripple rejection	$R_{REJ}8$	f = 120Hz, I_O8 = 1300mA	40	50		dB
Short circuit current	I_S8	V_O81 = 0, V_O82 = 0	300	550	1000	mA
Over voltage detection						
Over voltage detection voltage	V_{OVP}	V_{CC}, All output stop	34	36	38	V

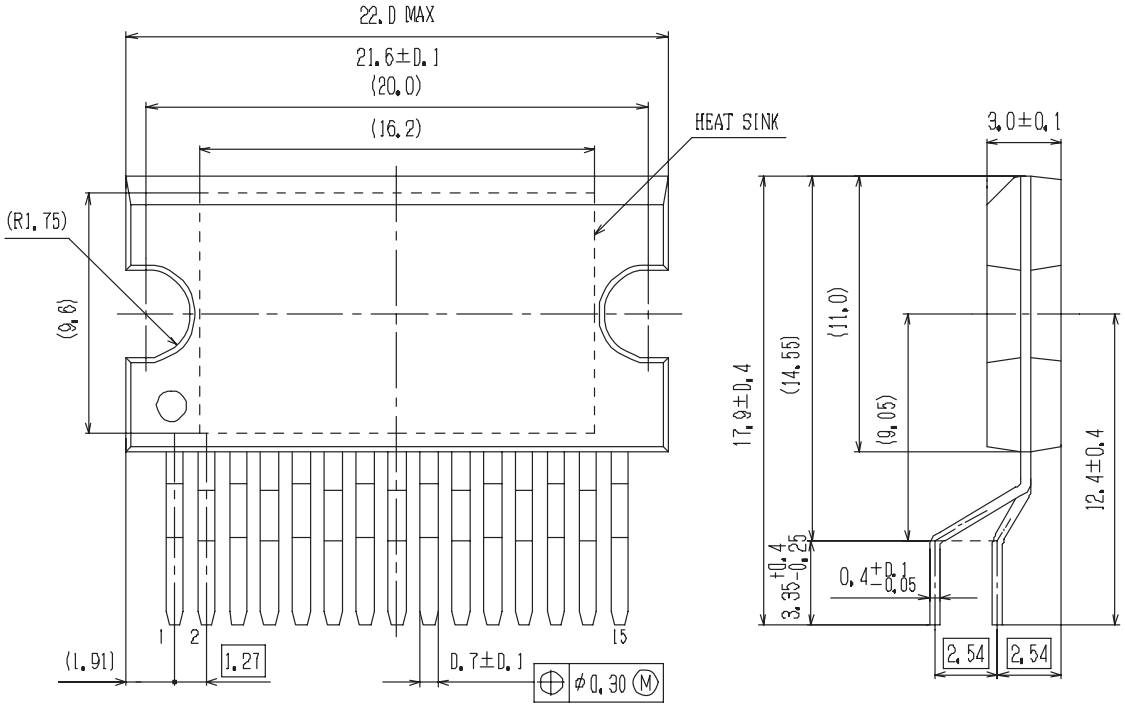
*2: The entire specification has been defined based on the tests performed under the conditions where Tj and Ta (=25°C) are almost equal. There tests were performed with pulse load to minimize the increase of junction temperature (Tj).

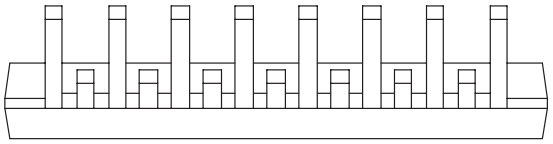
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Package Dimensions

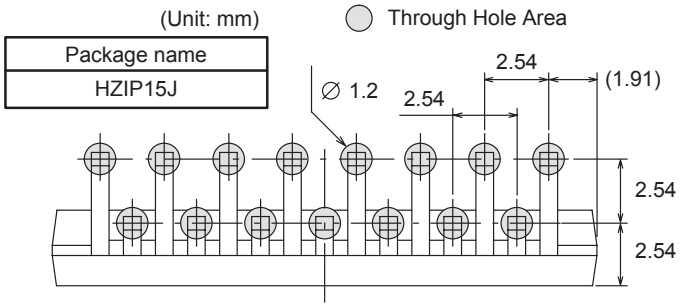
unit : mm

HZIP15J
CASE 945AC
ISSUE A





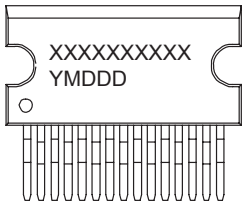
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

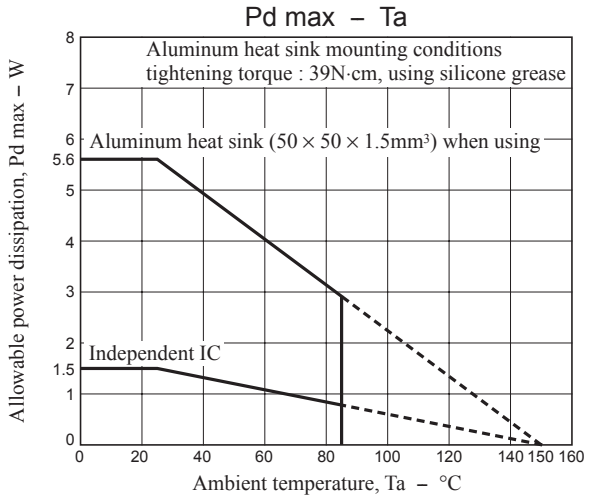
GENERIC MARKING DIAGRAM*



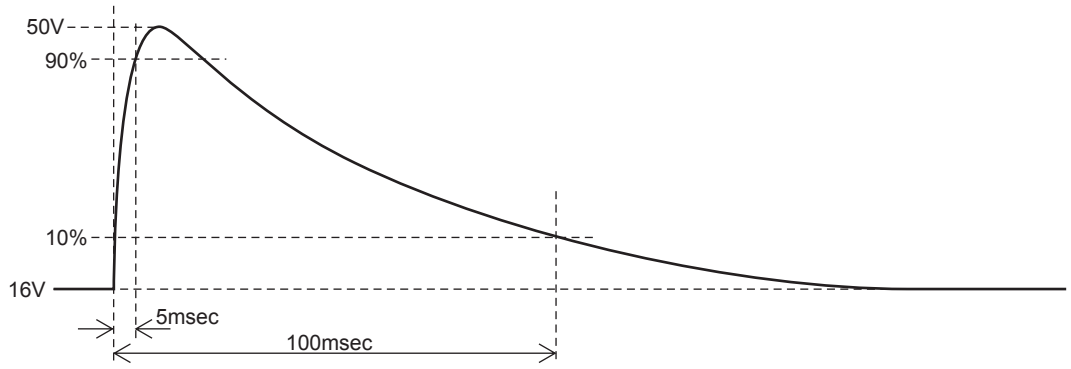
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

• Allowable power dissipation derating curve



• Waveform applied during surge test

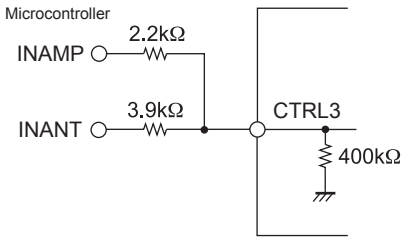


CTRL Pin Output Truth Table (each output is controllable by 4-value input)

INAMP	INANT	CTRL3	AMP	ANT
L	L	L	OFF	OFF
L	H	M1	OFF	ON
H	L	M2	ON	OFF
H	H	H	ON	ON

CTRL2	SWD5V	AUDIO
L	OFF	OFF
M1	OFF	ON
M2	ON	OFF
H	ON	ON

CTRL1	CD	ILM
L	OFF	OFF
M1	OFF	ON
M2	ON	OFF
H	ON	ON



(Warning) Usage of CTRL pin

When CTRL pin transits between L and M2, since it passes M1, ILM/AUDIO/ANT is turned on for a moment. Likewise, when CTRL pin transits between H and M1, since it passes M2, ILM/AUDIO/ANT is turned off for a moment.

To avoid operation failure by the above factors, please refer to (1) and (2) as shown below for precaution.

- Do not connect parasitic capacitor to CTRL as much as possible.
- If use of capacitor for CTRL is required, keep the resistance value as low as possible.
  (Recommendation level: 2.2kΩ / 3.9kΩ)
- Make sure that the output load capacitor has enough marjin against the voltage fluctuation due to instantaneous ON/OFF.

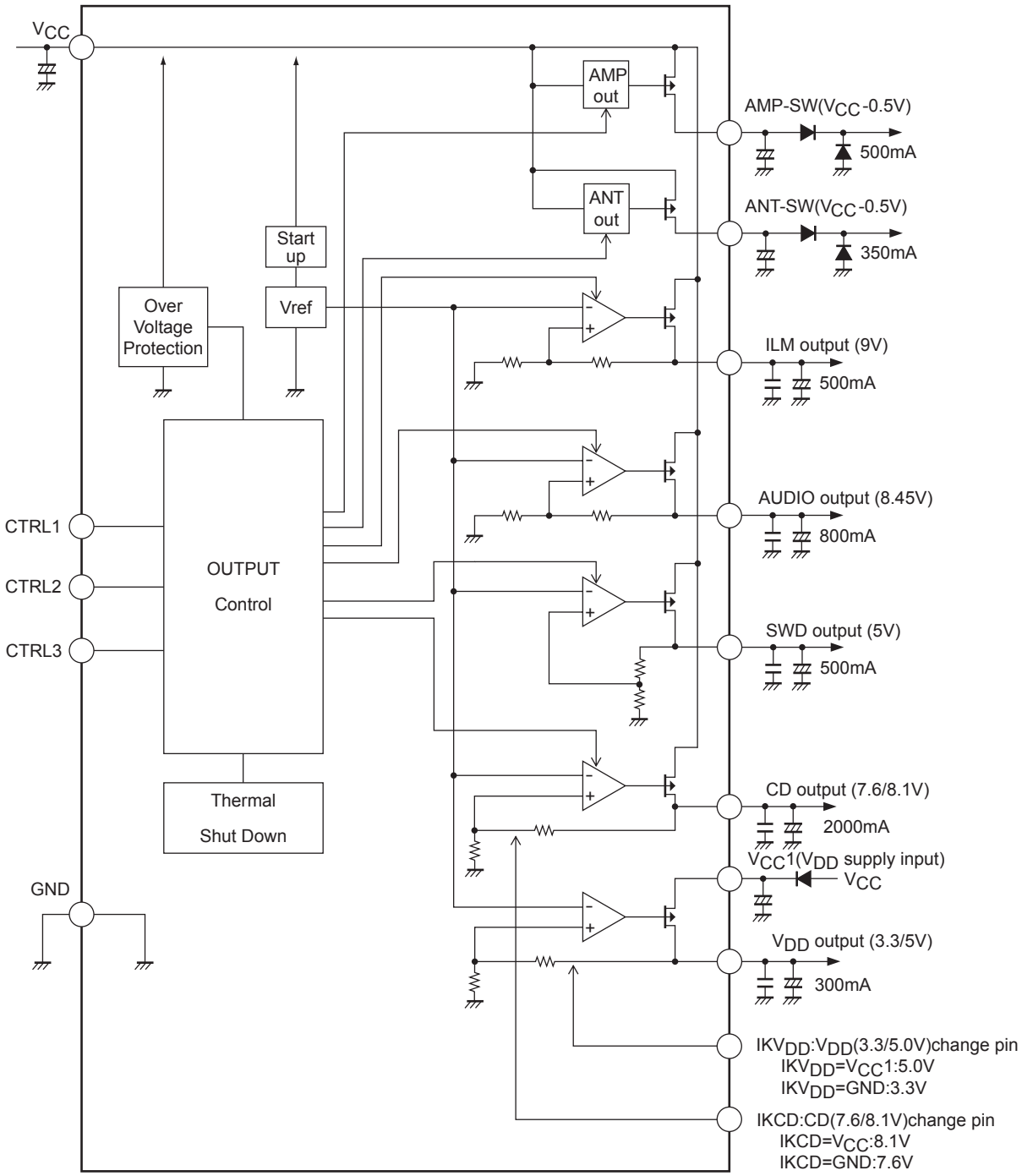
(1) The time until a reaction occurs in output after shifting from CTRL ON to OFF (typ)

OFF → ON time	27°C
CTRL1 → ILM	0.95μs
CTRL2 → AUDIO	1.33μs
CTRL3 → ANT	2.86μs

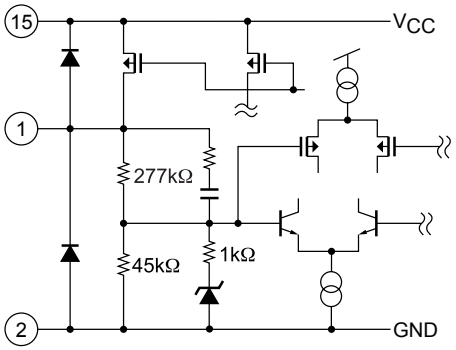
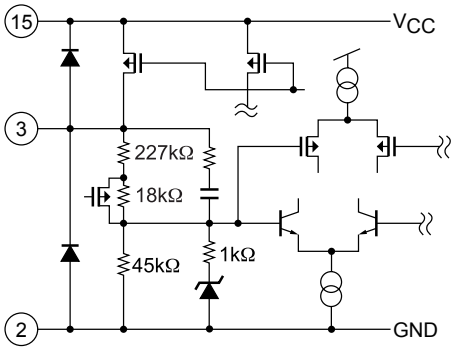
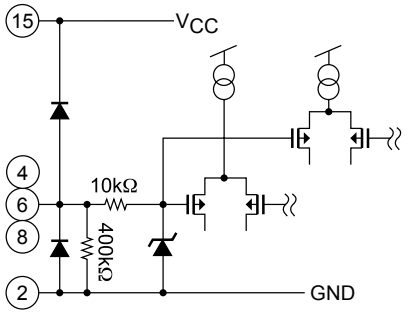
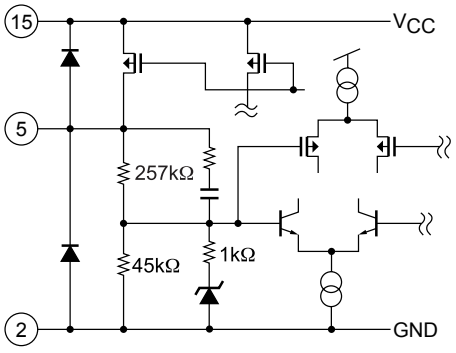
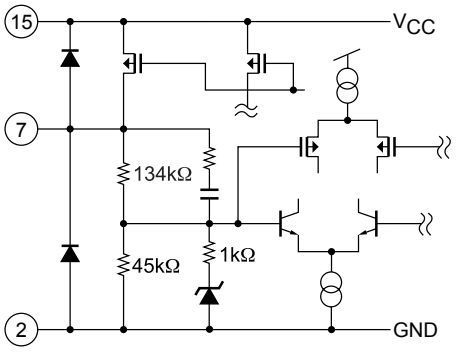
Due to quality fluctuation of the ICs in manufacturing process, the above-mentioned time can be shortened by 10 to 20%.

(2) The time until output starts to react after shifting from CTRL ON→OFF control (typ):
All output: 200ns to 300ns

● Block Diagram

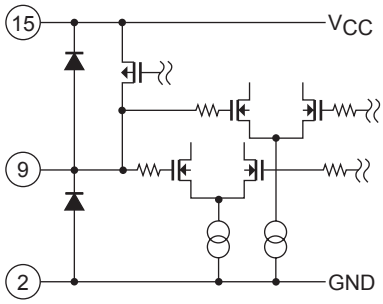
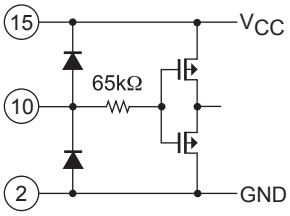
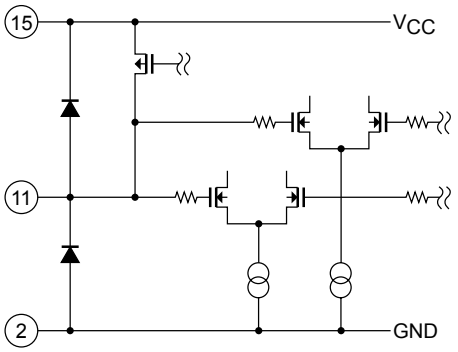
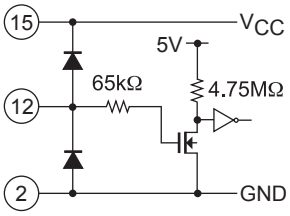
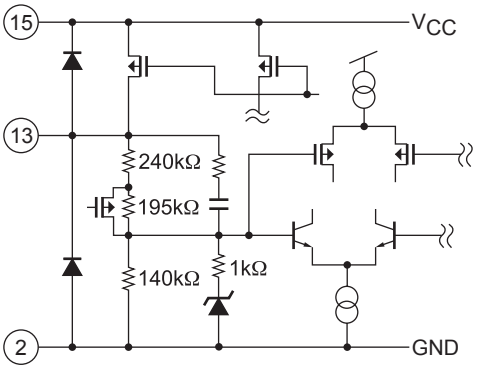
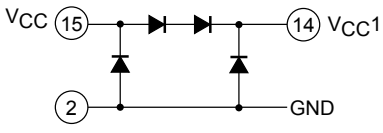


Pin Function

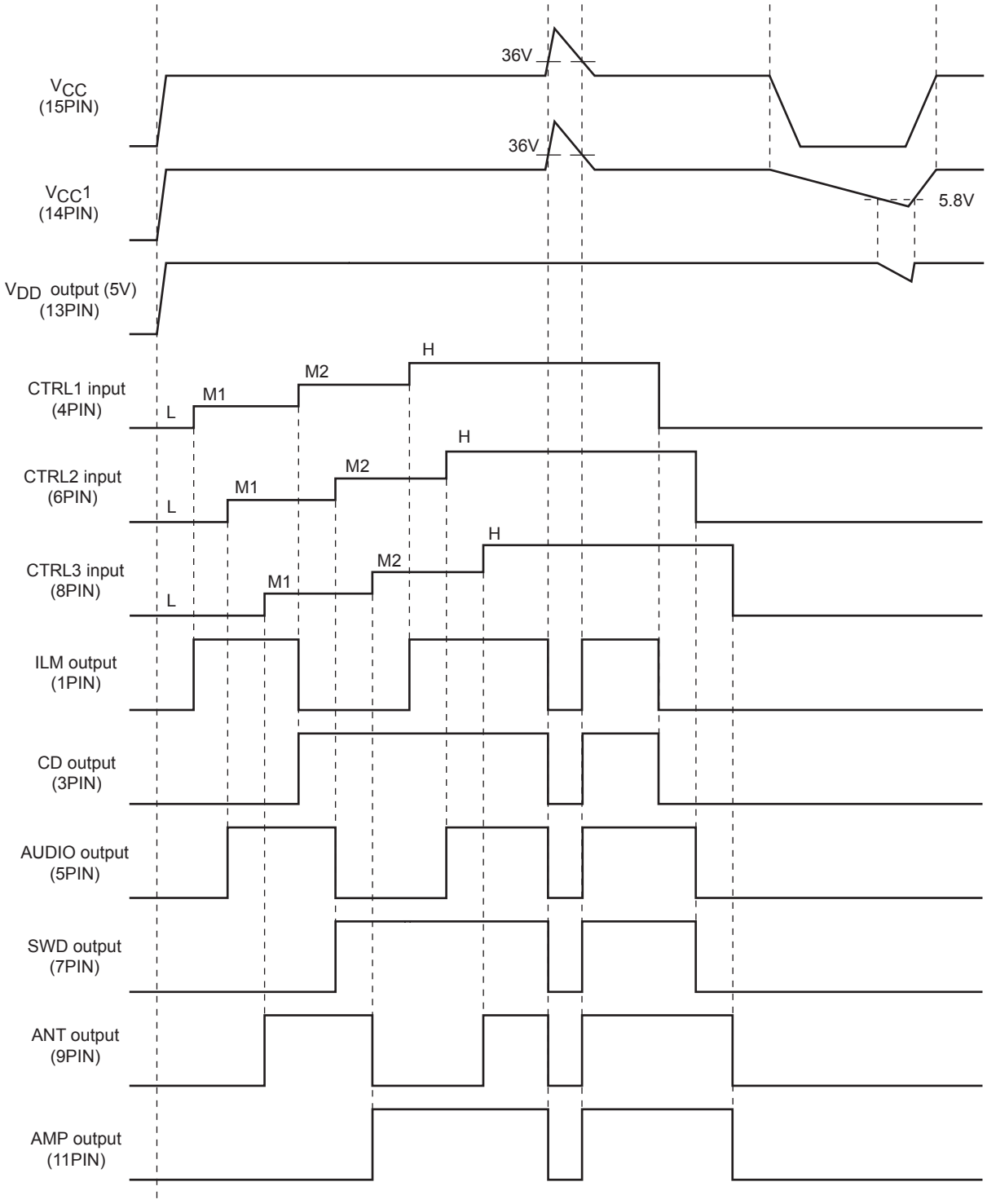
Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL1 = M1, H 9V/0.5A	
2	GND	GND pin	
3	CD	CD output pin ON when CTRL1 = M2, H 8.1V/2A (IKCD=V_{CC}) 7.6V/2A (IKCD=GND)	
4 6 8	CTRL1 CTRL2 CTRL3	CTRL1/2/3 input pin Four value input	
5	AUDIO	AUDIO output pin ON when CTRL2 = M1, H 8.45V/0.8A	
7	SWD	SWD output pin ON when CTRL2 = M2, H 5V/0.5A	

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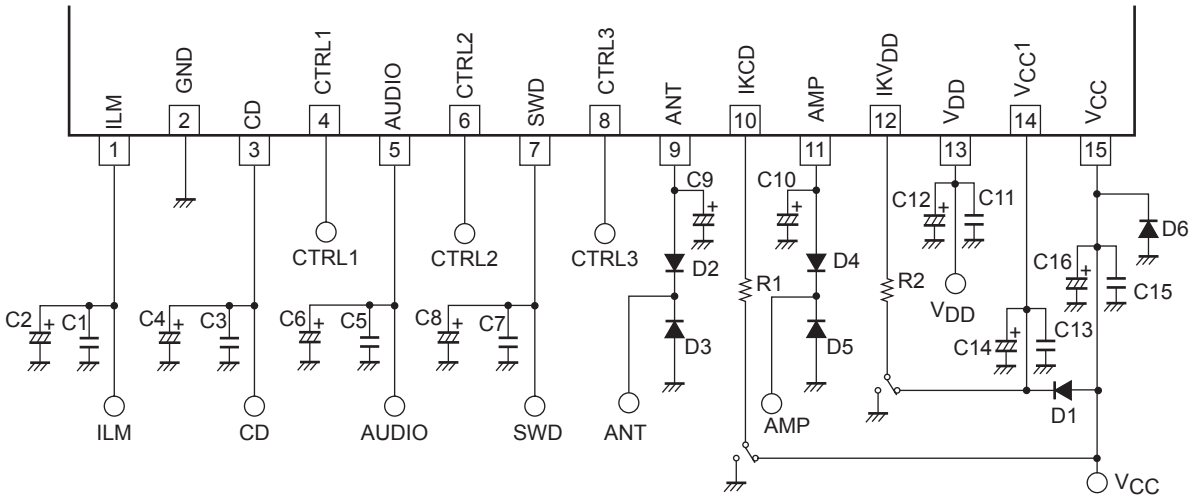
Pin No.	Pin name	Description	Equivalent Circuit
9	ANT	ANT output pin ON when CTRL3 = M1, H V_{CC}-0.5V/350mA	
10	IKCD	CD voltage control input pin	
11	AMP	AMP output pin ON when CTRL2 = M2, H V_{CC}-0.5V/500mA	
12	IKV_{DD}	V_{DD} voltage control input pin V_{CC}1/GND	
13	V_{DD}	V_{DD} output pin 5.0V/0.3A (IKV_{DD} = V_{CC}1) 3.3V/0.3A (IKV_{DD} = GND)	
14	V_{CC}1	V_{DD} power supply pin	
15	V_{CC}	Power supply pin	

Timing Chart



*The above values are obtained when typ.

Applied circuit example



Peripheral parts list

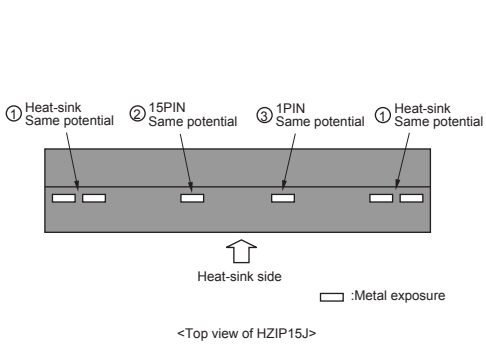
Name of part	Description	Recommended value	Remarks
C2, C4, C6, C8, C12	Output stabilization capacitor	10μF or more*	Electrolytic capacitor
C1, C3, C5, C7, C11	Output stabilization capacitor	0.22μF or more*	Ceramic capacitor
C14, C16	Power supply bypass capacitor	100μF or more	These capacitors must be placed near the V_{CC} and GND pins.
C13, C15	Oscillation prevention capacitor	0.22μF or more	
C9, C10	AMP/ANT output stabilization capacitor	2.2μF or more	
R1, R2	Resistance for protection	10 to 100kΩ	
D1	Diode for prevention of backflow		Meeting the specifications of the rush electric current in a true use state
D2, D3, D4, D5	Diode for internal element protection	SB1003M3	
D6	Diode for internal element protection	SB1003M3	When a minus number surge is applied

* : Make sure that the capacitors of the output pins are 10μF or higher and meets the condition of ESR is 0.001 to 10Ω (ceramic capacitor alone can be used.), in which voltage/ temperature fluctuation and unit differences are taken into consideration. Moreover, RF characteristics of electrolytic capacitor should be sufficient.

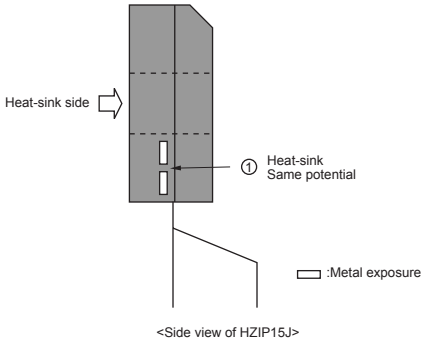
Caution for implementing LV5694P to a system board

The package of LV5694P is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin 15 and pin 1, respectively. (2) (=pin 15) is the V_{CC} pin and (3) (=pin 1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and V_{CC}. The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can connect each other.

- HZIP15J outline

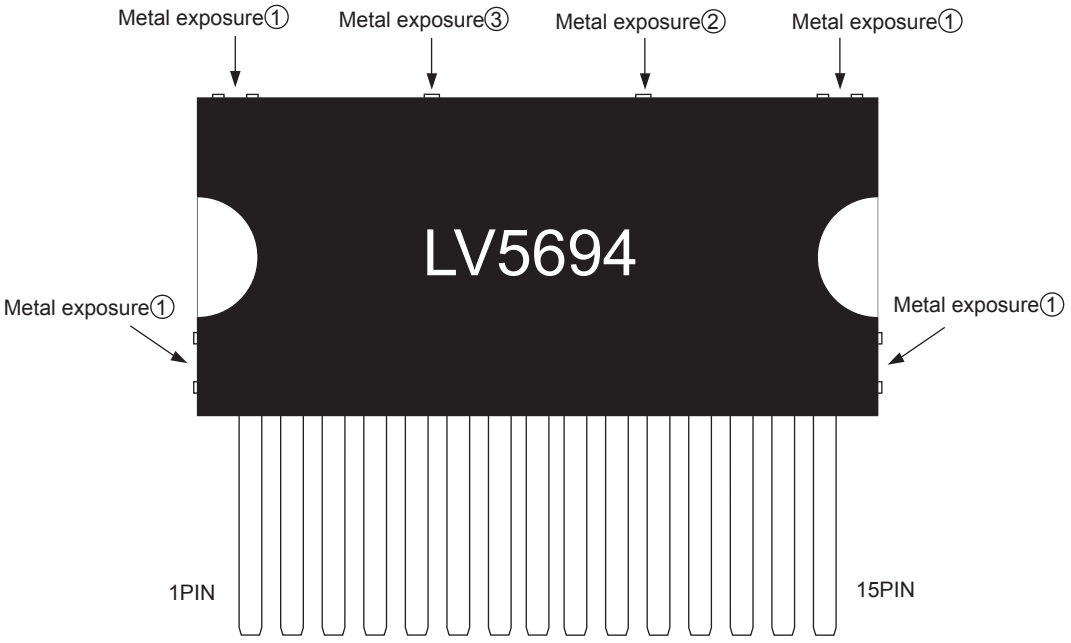


<Top view of HZIP15J>



<Side view of HZIP15J>

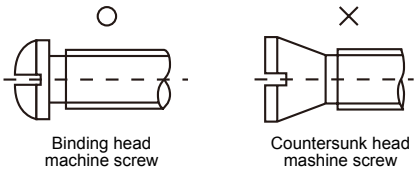
- Frame diagram (LV5694P) *In the system power supply other than LV5694P, pin assignment may differ.



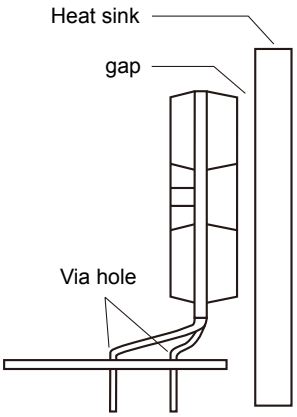
HZIP15J Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.



b. Heat sink attachment
- · Use flat-head screws to attach heat sinks.
- · Use also washer to protect the package.
- · Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
- · If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- · Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- · Take care a position of via hole .
- · Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- · Verify that there are no press burrs or screw-hole burrs on the heat sink.
- · Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- · Twisting must be limited to under 0.05 mm.
- · Heat sink and semiconductor device are mounted in parallel. Take care of electric or compressed air drivers
- · The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.



c. Silicone grease
- · Spread the silicone grease evenly when mounting heat sinks.
- · Our company recommends YG-6260 (Momentive Performance Materials Japan LLC)

d. Mount
- · First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- · When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

e. When mounting the semiconductor device to the heat sink using jigs, etc.,
- · Take care not to allow the device to ride onto the jig or positioning dowel.
- · Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

f. Heat sink screw holes
- · Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- · When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- · When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5694P-E	HZIP15J (Pb-Free)	20 / Fan-Fold

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