LPC83x

32-bit ARM® Cortex®-M0+ microcontroller; up to 32 KB flash and 4 KB SRAM; 12-bit ADC

Rev. 1.2 — 4 April 2018 Product data sheet

1. General description

The LPC83x are an ARM Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 30 MHz. The LPC83x support up to 32 KB of flash memory and 4 KB of SRAM.

The peripheral complement of the LPC83x includes a CRC engine, one I^{2}C-bus interface, one USART, up to two SPI interfaces, one multi-rate timer, self-wake-up timer, and SCTimer/PWM, a DMA, one 12-bit ADC, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 29 general-purpose I/O pins.

For additional documentation related to the LPC83x parts, see Section 18.

2. Features and benefits

- System:
  - ARM Cortex-M0+ processor (revision r0p1), running at frequencies of up to 30 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - AHB multilayer matrix.
  - Serial Wire Debug (SWD) with four break points and two watch points. JTAG boundary scan (BSDL) supported.
  - Macro Trace Buffer (MTB).
- Memory:
  - Up to 32 KB on-chip flash programming memory with 64 Byte page write and erase. Code Read Protection (CRP) supported.
  - 4 KB SRAM.
- ROM API support:
  - Boot loader.
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 29 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and digital filter. GPIO direction control supports independent set/clear/toggle of individual bits.
  - High-current source output driver (20 mA) on four pins.
  - High-current sink driver (20 mA) on two true open-drain pins.

- GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
- Switch matrix for flexible configuration of each I/O pin function.
- CRC engine.
- DMA with 18 channels and 8 trigger inputs.

- Timers:
  - SCTimer/PWM with up to 4 capture inputs and 4 match output functions for timing and PWM applications.
  - Four channel Multi-Rate Timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Self-Wake-up Timer (WKT) clocked from either the IRC, a low-power, low-frequency internal oscillator, or an external clock input in the always-on power domain.
  - Windowed Watchdog timer (WWDT).
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 1.2 Msamples/s. The ADC supports two independent conversion sequences.
- Serial peripherals:
  - One USART interface with pin functions assigned through the switch matrix and one fractional baud rate generator.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - One I^2C-bus interface. Supports Fast-mode Plus with 1 Mbit/s data rates on the open-drain pins and listen mode.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1.5 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input, or the internal RC oscillator.
  - Clock output function with divider that can reflect all internal clock sources.
- Power control:
  - Power consumption in active mode as low as 90 uA/MHz in low-current mode using the IRC as the clock source.
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from Deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect (BOD).

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- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Operating temperature range -40 °C to +85 °C.
- Available in a TSSOP20 and HVQFN33 (5x5) package.

3. Applications

- Sensor gateways
- Industrial
- Gaming controllers
- 8/16-bit applications
- Consumer
- Climate control
- Simple motor control
- Portables and wearables
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC834M101FHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC832M101FDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I^2C	SPI	ADC channels	GPIO	Package
LPC834M101FHI33	32	4	1	1	2	12	29	HVQFN33
LPC832M101FDH20	16	4	1	1	2	5	16	TSSOP20

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5. Marking

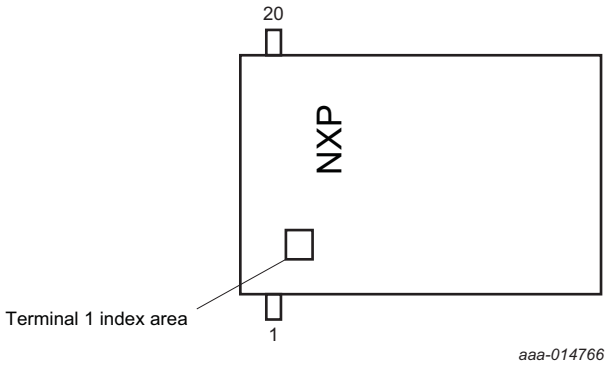

Fig 1. TSSOP20 package marking

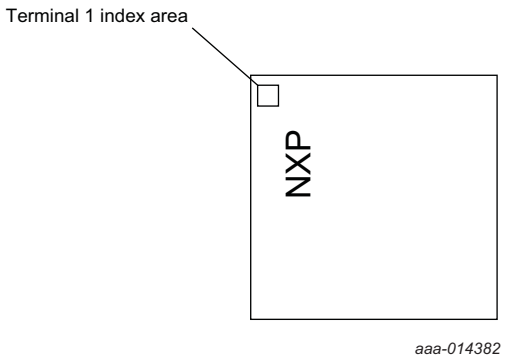

Fig 2. HVQFN33 package marking

The HVQFN33 packages typically have the following top-side marking:

83xF

xx xx

yywwxR

The TSSOP20 packages typically have the following top-side marking:

LPC83x

Mx01F

xxxxxxxx

zzywwxR

In the last line, field ‘y’ or ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year. Field ‘R’ states the chip revision.

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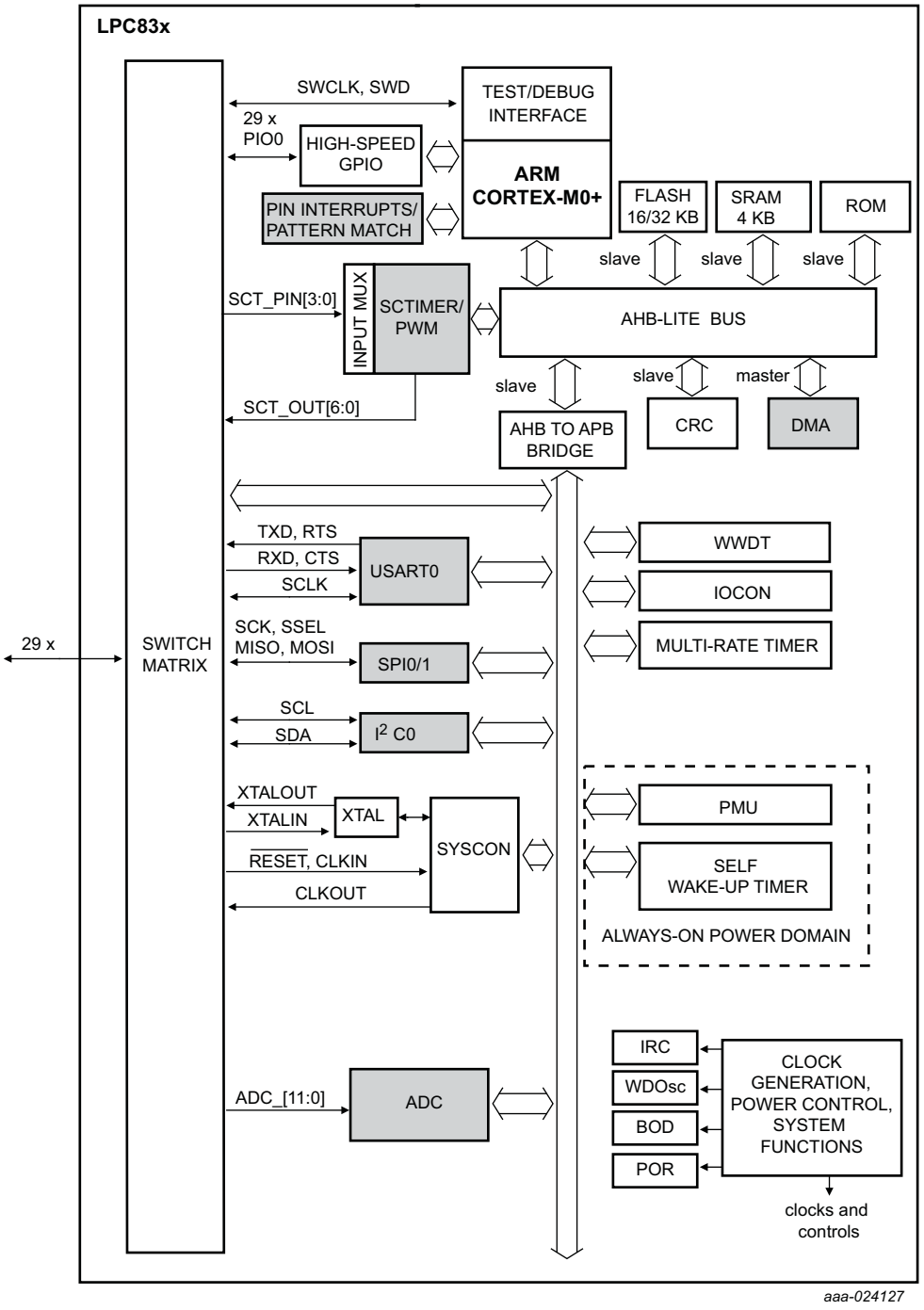
6. Block diagram



Gray-shaded blocks show peripherals that can provide hardware triggers or fixed DMA requests for DMA transfers.

Fig 3. LPC83x block diagram

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7. Pinning information

7.1 Pinning

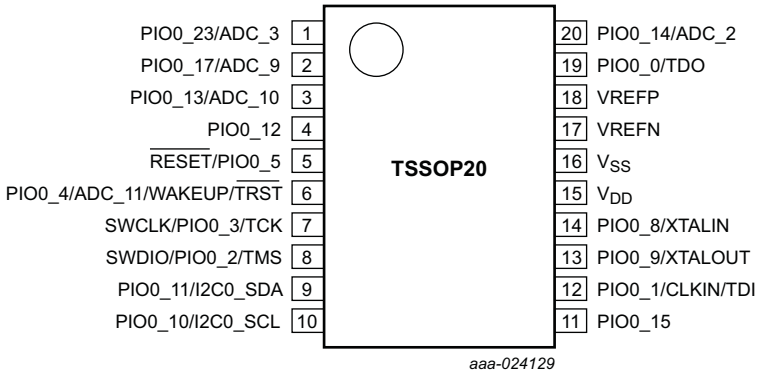

Fig 4. Pin configuration TSSOP20 package

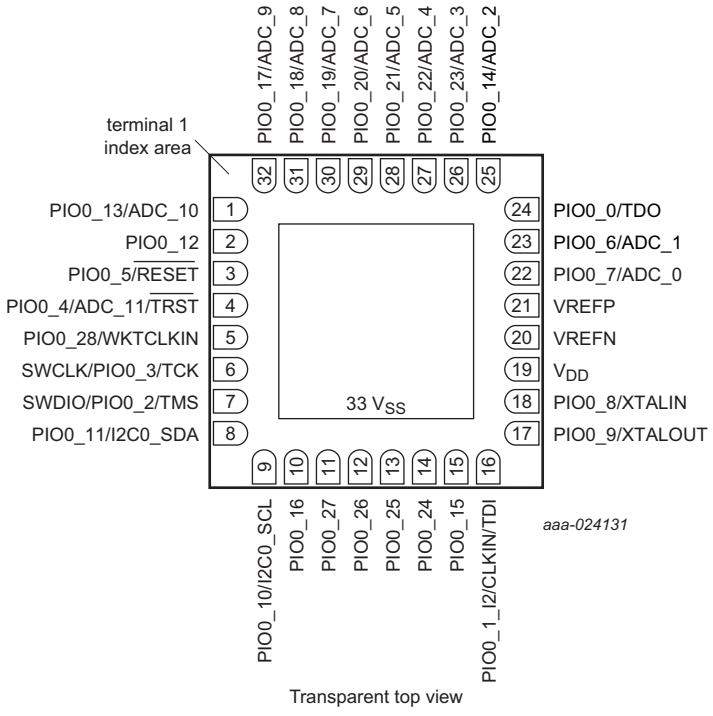

Fig 5. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table Table 3 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable through the switch matrix between GPIO and the ADC, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

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Movable function for the I²C, USART, SPI, and SCTimer/PWM pin functions can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If the part must wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 3. Pin description

Symbol	TSSOP20	HVQFN33		Reset state[1]	Type	Description
PIO0_0/ TDO	19	24	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In ISP mode, this is the U0_RXD pin. In boundary scan mode: TDO (Test Data Out).
PIO0_1/ CLKIN/TDI	12	16	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
					I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	8	7	[4]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
					I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	7	6	[4]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
					IO	**PIO0_3 —** General-purpose port 0 input/output 3.
PIO0_4/ADC_11/ TRSTN/WAKEUP	6	4	[3]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). In ISP mode, this pin is the U0_TXD pin. This pin triggers a wake-up from Deep power-down mode. If the part must wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. This pin should be pulled HIGH externally before entering Deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit Deep power-down mode and wakes up the part.
					A	**ADC_11 —** ADC input 11.

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Table 3. Pin description

Symbol	TSSOP20	HVQFN33		Reset state[1]	Type	Description
$\overline{\text{RESET}}$/PIO0_5	5	3	[7]	I; PU	IO	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed and the Deep power-down mode is not used.
					I	**PIO0_5 —** General-purpose port 0 input/output 5.
PIO0_6/ADC_1	-	23	[10]	I; PU	IO	**PIO0_6 —** General-purpose port 0 input/output 6.
					A	**ADC_1 —** ADC input 1.
PIO0_7/ADC_0	-	22	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
					A	**ADC_0 —** ADC input 0.
PIO0_8/XTALIN	14	18	[8]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
					A	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	17	[8]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
					A	**XTALOUT —** Output from the oscillator circuit.
PIO0_10/I2C0_SCL	10	9	[6]	Inactive	I; F	**PIO0_10 —** General-purpose port 0 input/output 10 (open-drain).
						I2C0_SCL — Open-drain I^2C-bus clock input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_11/I2C0_SDA	9	8	[6]	Inactive	I; F	**PIO0_11 —** General-purpose port 0 input/output 11 (open-drain).
						I2C0_SDA — Open-drain I^2C-bus data input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_12	4	2	[4]	I; PU	IO	**PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_13/ADC_10	3	1	[2]	I; PU	IO	**PIO0_13 —** General-purpose port 0 input/output 13.
					A	**ADC_10 —** ADC input 10.
PIO0_14/ADC_2	20	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
					A	**ADC_2 —** ADC input 2.

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Table 3. Pin description

Symbol	TSSOP20	HVQFN33		Reset state[1]	Type	Description
PIO0_15	11	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	-	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9	2	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
					A	**ADC_9 —** ADC input 9.
PIO0_18/ADC_8	-	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
					A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	-	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
					A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	-	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
					A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	-	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
					A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	-	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
					A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3	1	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
					A	**ADC_3 —** ADC input 3.
PIO0_24	-	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24.
PIO0_25	-	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25.
PIO0_26	-	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	-	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	-	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
V_{DD}	15	19		-	-	Supply voltage for the I/O pad ring, the core voltage regulator, and the analog peripherals.
V_{SS}	16	33[11]		-	-	Ground.
VREFN	17	20		-	-	ADC negative reference voltage.
VREFP	18	21		-	-	ADC positive reference voltage. Must be equal or lower than V_{DD}.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 14.5 “Pin states in different power modes”. For termination on unused pins, see Section 14.4 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. This pin is active in Deep power-down mode and includes a 20 ns glitch filter (active in all power modes). In Deep power-down mode, pulling the WAKEUP pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low-power oscillator is enabled for waking up the part from Deep power-down mode. See Table 17 “Dynamic characteristics: WKTCLKIN pin” for the WKTCLKIN input.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

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[6] True open-drain pin. I²C-bus pins compliant with the I²C-bus specification for I²C standard mode, I²C Fast-mode, and I²C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[7] See Figure 9 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured for XTALIN and XTALOUT, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The WKTCLKIN function is enabled in the DPDCTRL register in the PMU.

[10] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[11] Thermal pad for HVQFN33.

Table 4. Movable functions (assign to pins PIO0_0 to PIO0_28 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0_CTS}}$	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL0	I/O	Slave select 0 for SPI0.
SPI0_SSEL1	I/O	Slave select 1 for SPI0.
SPI0_SSEL2	I/O	Slave select 2 for SPI0.
SPI0_SSEL3	I/O	Slave select 3 for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL0	I/O	Slave select 0 for SPI1.
SPI1_SSEL1	I/O	Slave select 1 for SPI1.
SCT_PIN0	I	Pin input 0 to the SCT input multiplexer.
SCT_PIN1	I	Pin input 1 to the SCT input multiplexer.
SCT_PIN2	I	Pin input 2 to the SCT input multiplexer.
SCT_PIN3	I	Pin input 3 to the SCT input multiplexer.
SCT_OUT0	O	SCT Output 0.
SCT_OUT1	O	SCT Output 1.
SCT_OUT2	O	SCT Output 2.
SCT_OUT3	O	SCT Output 3.
SCT_OUT4	O	SCT Output 4.
SCT_OUT5	O	SCT Output 5.

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Table 4. Movable functions (assign to pins PIO0_0 to PIO0_28 through switch matrix)

Function name	Type	Description
ADC_PINTRIG0	I	ADC external pin trigger input 0.
ADC_PINTRIG1	I	ADC external pin trigger input 1.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

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8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC83x contain up to 32 KB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC83x contain a total of 4 KB on-chip static RAM data memory.

8.4 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.

8.5 Memory map

The LPC83x incorporates several distinct memory regions. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

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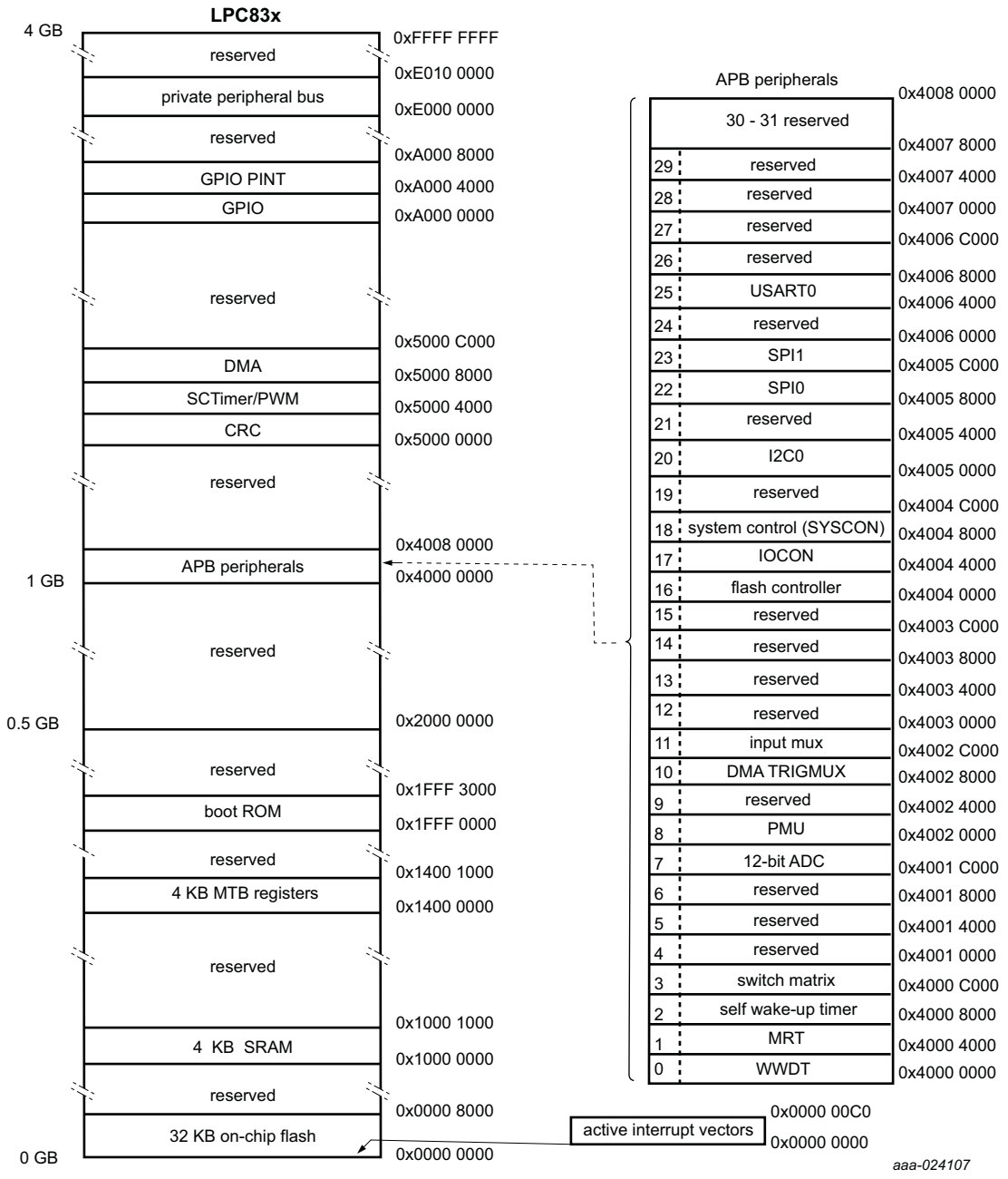

Fig 6. LPC83x Memory mapping

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8.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.6.1 Features

- Nested Vectored Interrupt Controller is a part of the ARM Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC83x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Supports NMI.

8.6.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.7 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 3 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 8 “LPC83x clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

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8.8.1 Standard I/O pad configuration

Figure 7 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

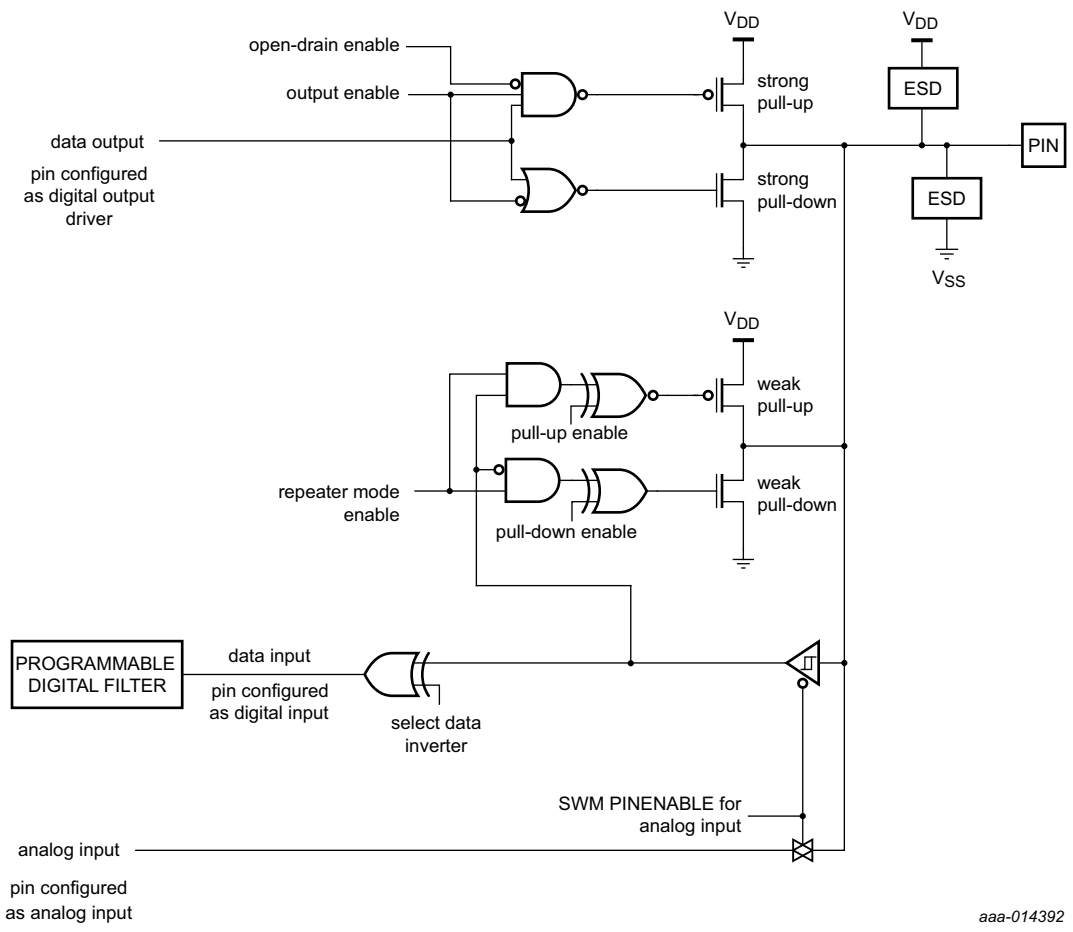

Fig 7. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCTimer/PWM, and I^2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

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Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC83x use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and $\overline{\text{RESET}}$/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_10 and PIO0_11.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 7).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

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8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC83x from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be also programmed to generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.
  - The pattern match engine does not facilitate wake-up.

8.12 DMA controller

The DMA controller can access all memories and the USART, SPI, I2C, and ADC peripherals using DMA requests or triggers. DMA transfers can also be triggered by internal events like the ADC interrupts, the pin interrupts (PININT0 and PININT1), the SCTimer DMA requests, and the DMA trigger outputs.

8.12.1 Features

- 18 channels with each channel connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events or by two pin interrupts. Each DMA channel can select one trigger input from 8 sources.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with two entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

8.12.2 DMA trigger input MUX (TRIGMUX)

Each DMA trigger is connected to a programmable multiplexer which connects the trigger input to one of multiple trigger sources. Each multiplexer supports the same trigger sources: the ADC sequence interrupts, the SCTimer/PWM DMA request lines, and pin interrupts PININT0 and PININT1, and the outputs of the DMA triggers 0 and 1 for chaining DMA triggers.

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8.13 USART0

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.13.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except the open-drain pins.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.

8.14 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.14.1 Features

- Maximum data rates of up to 30 Mbit/s in master mode and up to 18 Mbit/s in slave mode for SPI functions connected to all digital pins except the open-drain pins.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

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Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.15 I²C-bus interface (I²C0)

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master.

The I²C0-bus functions are fixed-pin functions. The true open-drain pins provide the electrical characteristics to support the full I²C-bus specification (see Ref. 1).

8.15.1 Features

- I²C0 supports Fast-mode Plus with data rates of up to 1 Mbit/s in addition to standard and fast modes on two true open-drain pins.
- True open-drain pins provide fail-safe operation: When the power to an I²C-bus device is switched off, the SDA and SCL pins connected to the I²C0-bus are floating and do not disturb the bus.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

8.16 SCTimer/PWM

The SCTimer/PWM can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to eight different programmable states, which can change under the control of events, to provide complex timing patterns.

The inputs to the SCT are multiplexed between movable functions from the switch matrix and internal connections such as the ADC threshold compare interrupt, and the ARM core signals ARM_TXEV and DEBUG_HALTED. The signal on each SCT input is selected through the INPUT MUX.

All outputs of the SCT are movable functions and are assigned to pins through the switch matrix. One SCT output can also be selected as one of the ADC conversion triggers.

8.16.1 Features

- Each SCTimer/PWM supports:
  - Eight match/capture registers.
  - Eight events.

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  - Eight states.
  - Four inputs. Each input is configurable through an input multiplexer to use one of four external pins (connected through the switch matrix) or one of four internal sources. The maximum input signal frequency is 25 MHz.
  - Six outputs. Connected to pins through the switch matrix.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to eight match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.16.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, and the ARM core signals ARM_TXEV and DEBUG_HALTED.

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8.17 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.17.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.18 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

8.18.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

8.19 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

8.19.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the IRC. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in Deep power-down mode.

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- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.20 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources.

The ADC includes a hardware threshold compare function with zero-crossing detection.

Remark: For best performance, select VREFP and VREFN at the same voltage levels as V_{DD} and V_{SS}. When selecting VREFP and VREFN different from VDD and VSS, ensure that the voltage midpoints are the same:

$(VREFP-VREFN)/2 + VREFN = V_{DD}/2$

8.20.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 1.2 MSamples/s.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (not to exceed V_{DD} voltage level).
- Burst conversion mode for single or multiple inputs.
- Hardware calibration mode.

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8.21 Clocking and power control

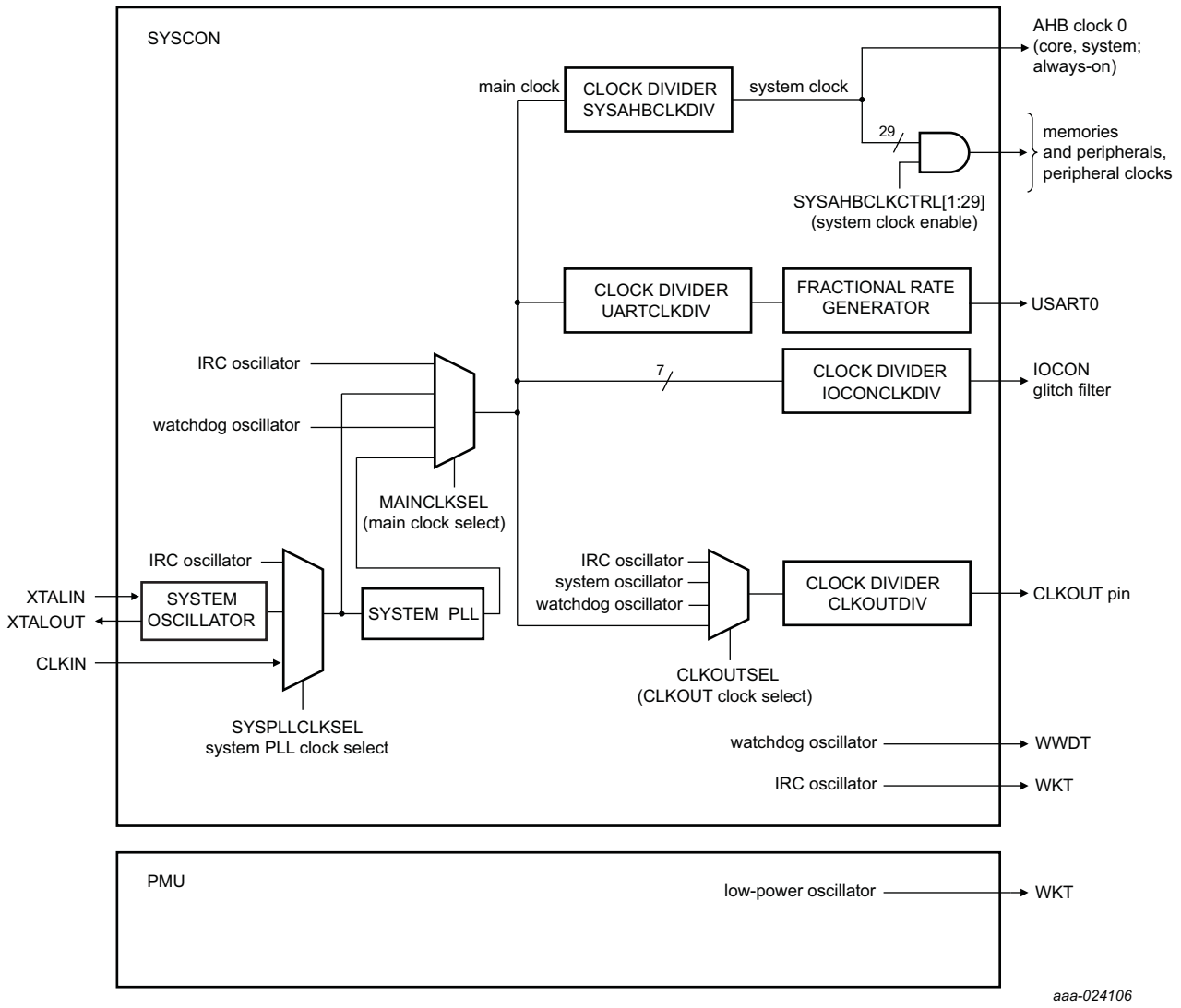

Fig 8. LPC83x clock generation

8.21.1 Crystal and internal oscillators

The LPC83x include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self-wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

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Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC83x operates from the IRC until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 8 for an overview of the LPC83x clock generation.

8.21.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and then the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC83x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.21.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.21.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz (± 40% accuracy) oscillator serves as the clock input to the WKT. This oscillator can be configured to run in all low-power modes.

8.21.2 Clock input

An external clock source can be supplied on the selected CLKIN pin directly to the PLL input. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 8 “Static characteristics, supply pins” and Table 16 “Dynamic characteristics: I/O pins[1]”.

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal (see Section 14.1).

The maximum frequency for both clock signals is 25 MHz.

8.21.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within

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its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is nominally 100 μs.

8.21.4 Clock output

The LPC83x features a clock output function that routes the IRC, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

8.21.5 Wake-up process

The LPC83x begin operation at power-up by using the IRC as the clock source allowing chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL are needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

8.21.6 Power control

The LPC83x supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.21.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.21.6.2 Deep-sleep mode

In Deep-sleep mode, the LPC83x core is in Sleep mode and all peripheral clocks and all clock sources are off except for the IRC and watchdog oscillator or low-power oscillator if selected. The IRC output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC83x can wake up from Deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

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Any interrupt used for waking up from Deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

8.21.6.3 Power-down mode

In Power-down mode, the LPC83x is in Sleep mode and all peripheral clocks and all clock sources are off except for watchdog oscillator or low-power oscillator if selected. In addition, all analog blocks and the flash are shut down. In Power-down mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC83x can wake up from Power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from Power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.21.6.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the self-wake-up timer if enabled. Four general-purpose registers are available to store information during Deep power-down mode. The LPC83x can wake up from Deep power-down mode via the WAKEUP pin, or without an external signal by using the time-out of the self-wake-up timer (see Section 8.19).

The LPC83x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

8.22 System control

8.22.1 Reset

Reset has four sources on the LPC83x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

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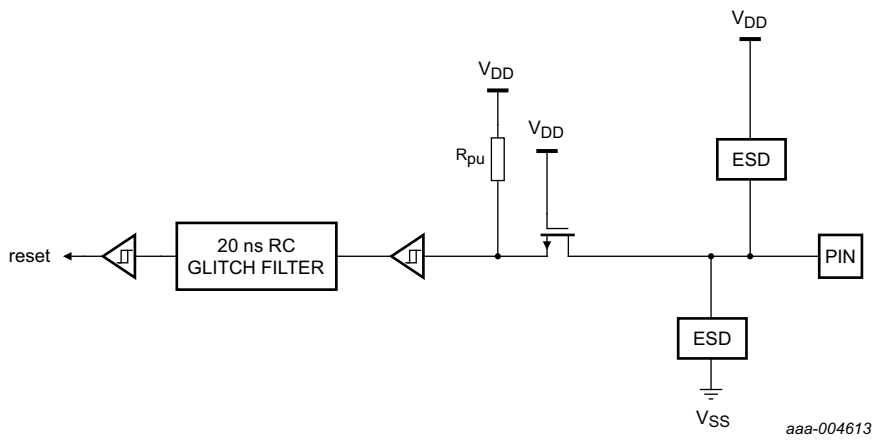

Fig 9. Reset pad configuration

8.22.2 Brownout detection

The LPC83x includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

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8.22.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION	
⚠	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled.

8.22.4 APB interface

The APB peripherals are located on one APB bus.

8.22.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.

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8.23 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC83x.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC83x is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 3).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

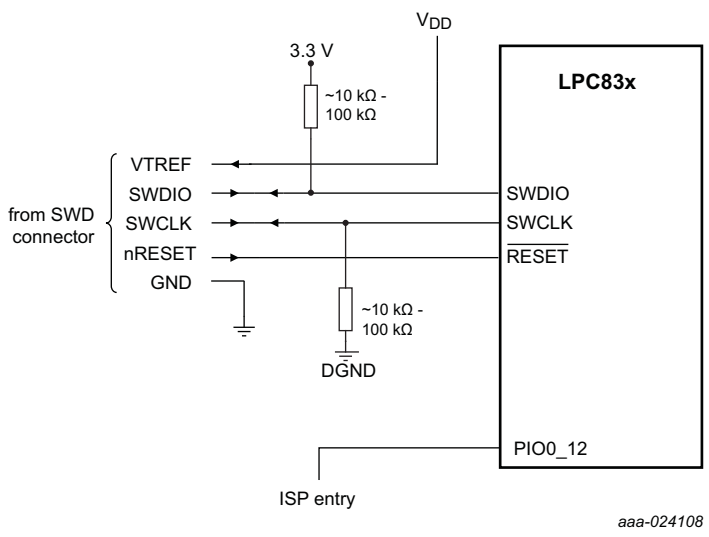

Fig 10. Connecting the SWD pins to a standard SWD connector

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9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		−0.5	V_{DD}	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq$ 1.8 V	[3][4]	−0.5	+5.5	V
		on I2C open-drain pins PIO0_10, PIO0_11	[5]	−0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage		[7][8][9]	−0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[9]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[10]	-	3500	V
		charged device model; HVQFN33 package		-	1200	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 7) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_10 and PIO0_11 and except the 3 V tolerant pin PIO0_6.

[4] Including the voltage on outputs in 3-state mode.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] V_{DD} present or not present.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[9] Dependent on package type.

[10] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 6. Thermal resistance

Symbol	Parameter	Conditions	Max/min	Unit
HVQFN33 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	40 +/- 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	114 +/- 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		18 +/- 15 %	°C/W

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11. Static characteristics

11.1 General operating conditions

Table 7. General operating conditions

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	30	MHz
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP		2.4	-	V_{DD}	V
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	1.8	1.95	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		I^2C-bus pins (PIO0_10 and PIO0_11)	[2]	-	-	2.5	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

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11.2 Supply pins

Table 8. Static characteristics, supply pins

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	1.85	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	1.04	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][3][6][7][9]	-	3.95	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][6][7][9]	-	3.2	-	mA
		Sleep mode					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	1.35	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	0.8	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][3][9][6][7]	-	2.55	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][9][6][7]	-	2.1	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[2][3][10]	-	158	300	μA
		T_{amb} = 85 °C		-	-	400	μA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C	[2][3][10]	-	1.6	10	μA
		T_{amb} = 85 °C		-	-	50	μA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; 10 kHz low-power oscillator and self-wake-up timer (WKT) disabled T_{amb} = 25 °C	[2][11]	-	0.2	1	μA
		T_{amb} = 85 °C		-	-	4	μA

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Table 8. Static characteristics, supply pins *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; 10 kHz low-power oscillator and self-wake-up timer (WKT) enabled		-	1.1	-	μA
		Deep power-down mode; V_{DD} = 3.3 V; external clock input WKTCLKIN @ 10 kHz with self-wake-up timer enabled		-	0.4	-	μA
		Deep power-down mode; V_{DD} = 3.3 V; external clock input WKTCLKIN @ 32 kHz with self-wake-up timer enabled		-	0.7	-	μA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC enabled; system oscillator disabled; system PLL enabled.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] All oscillators and analog blocks turned off.

[11] WAKEUP pin pulled HIGH externally.

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11.3 Electrical pin characteristics

Table 9. Static characteristics, electrical pin characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, $\overline{RESET}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_12	[4] [6]	0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		$V_{DD} - 0.4$	-	-	V
		I_{OH} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		-	-	0.4	V
		I_{OL} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V $\leq V_{DD} \leq$ 3.6 V		4	-	-	mA
		1.8 V $\leq V_{DD}$ < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V $\leq V_{DD} \leq$ 3.6 V		4	-	-	mA
		1.8 V $\leq V_{DD}$ < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[7]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[7]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V $\leq V_{DD} \leq$ 3.6 V		15	50	85	μA
		1.8 V $\leq V_{DD}$ < 2.0 V		10	50	85	
		$V_{DD} < V_I$ < 5 V		0	0	0	μA
High-drive output pin configured as digital pin (PIO0_2, PIO0_3, PIO0_12, PIO0_16)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA

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Table 9. Static characteristics, electrical pin characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_I	input voltage	$V_{DD} \geq 1.8$ V	[4] [6]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.4	-	-	V
		I_{OH} = 12 mA; 1.8 V <= V_{DD} < 2.5 V		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		$V_{OH} = V_{DD}$ − 0.4 V; 1.8 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[7]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[8]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[8]	−10	−50	−85	μA
		$V_{DD} < V_I$ < 5 V		0	0	0	μA
I²C-bus pins (PIO0_10 and PIO0_11)							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as standard mode pins 2.5 V <= V_{DD} < 3.6 V		3.5	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as Fast-mode Plus pins; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		16	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[9]	-	2	4	μA
		V_I = 5 V		-	10	22	μA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Based on characterization. Not tested in production.

[3] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[4] Including voltage on outputs in 3-state mode.

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[5] V_{DD} supply voltage must be present.

[6] 3-state outputs go into 3-state mode in Deep power-down mode.

[7] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[8] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 11.

[9] To V_{SS}.

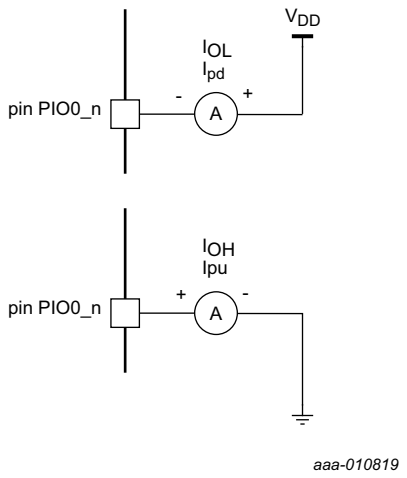

Fig 11. Pin input/output current measurement

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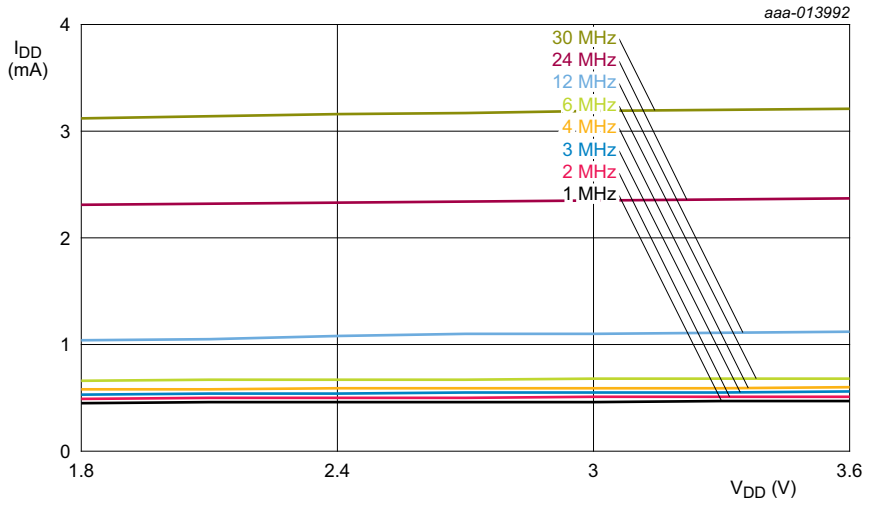
11.4 Power consumption

Power measurements in Active, Sleep, Deep-sleep, and Power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: external clock; IRC, PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: system oscillator enabled; PLL enabled.

Fig 12. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD}

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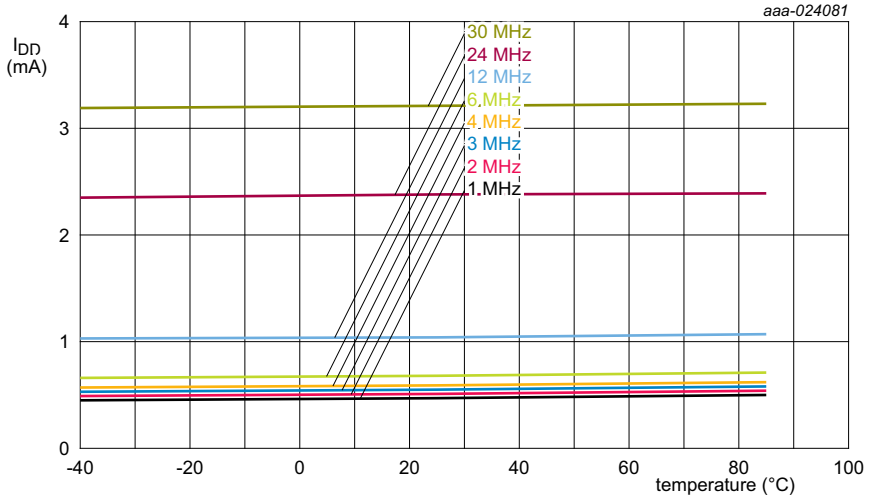

Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: external clock; IRC, PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: system oscillator enabled; PLL enabled.

Fig 13. Active mode: Typical supply current I_{DD} versus temperature

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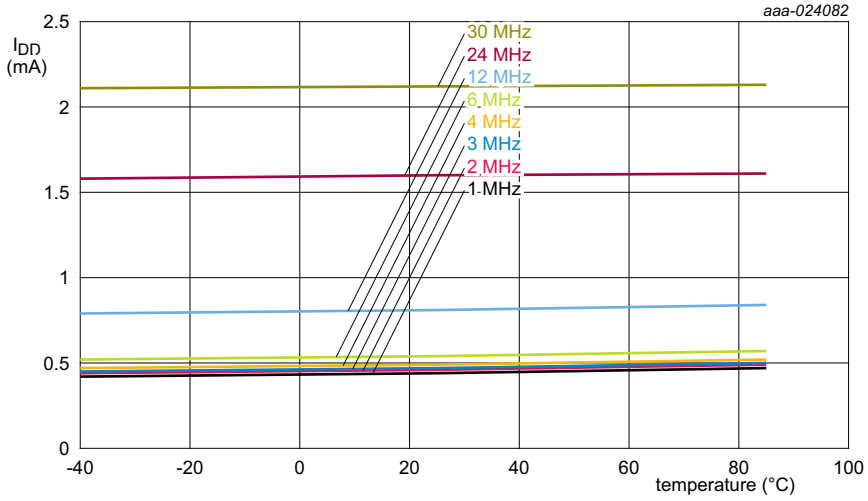


Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

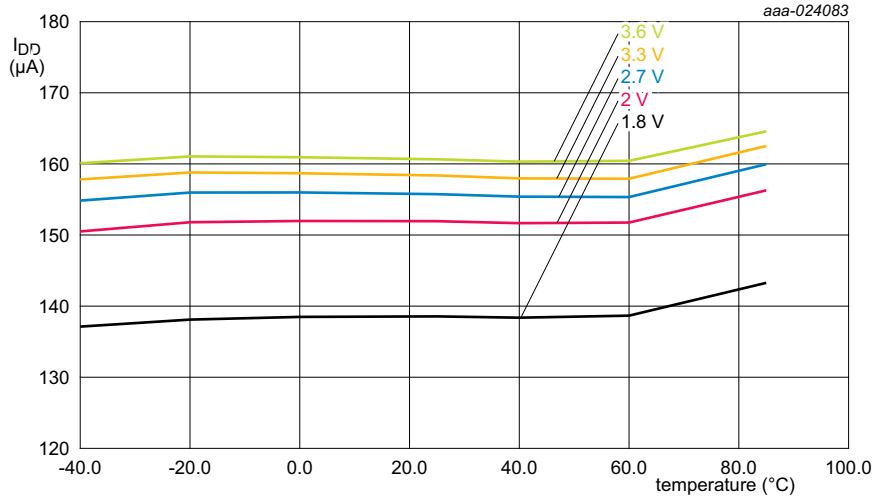
1 MHz - 6 MHz: external clock; IRC, PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: system oscillator enabled; PLL enabled.

Fig 14. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 15. Deep sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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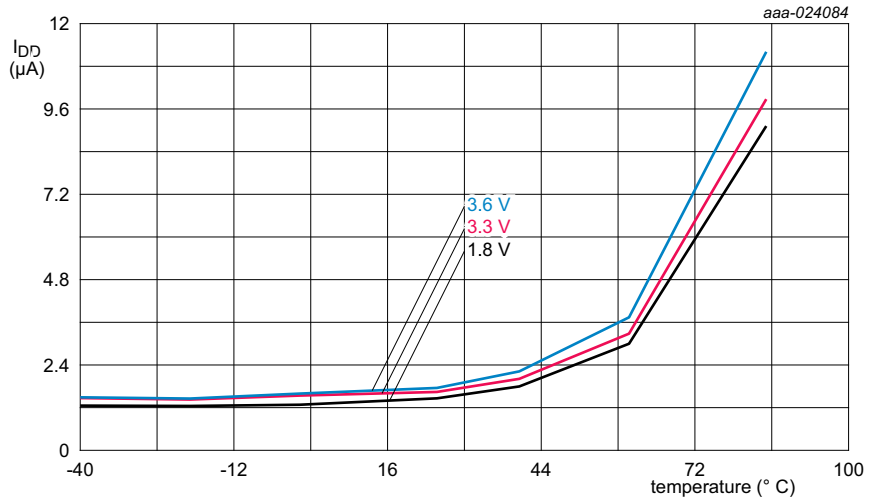
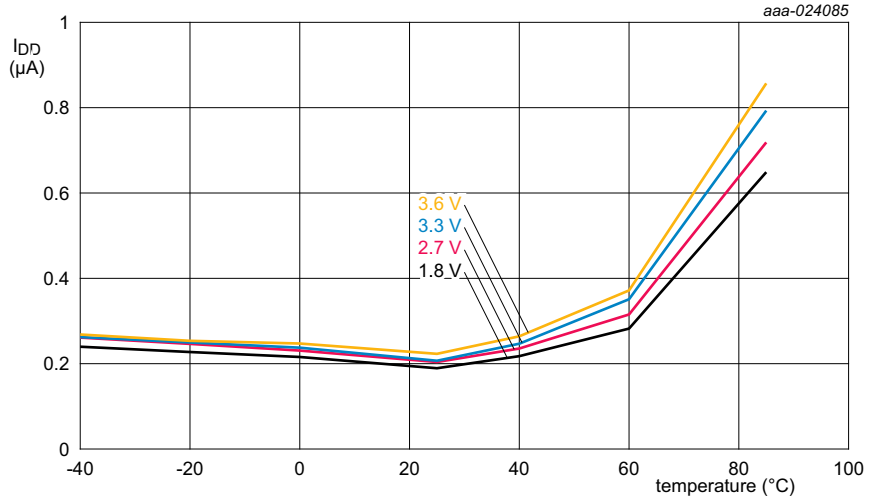


Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Power down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



WKT not running.

Fig 17. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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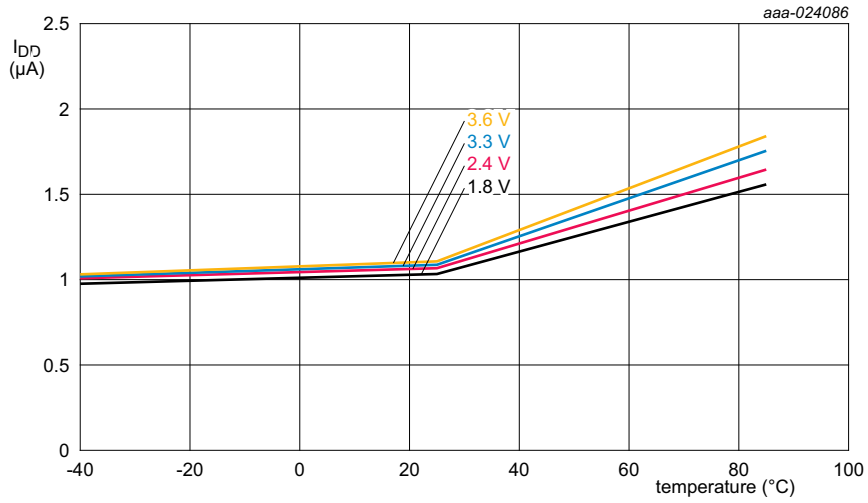
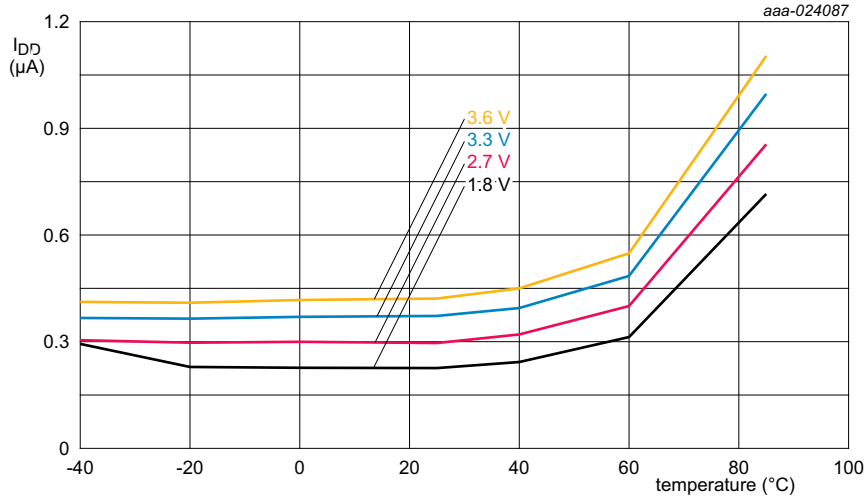


WKT running with internal 10 kHz low-power oscillator.

Fig 18. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (internal clock)



WKT running with external 10 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 10 kHz input clock)

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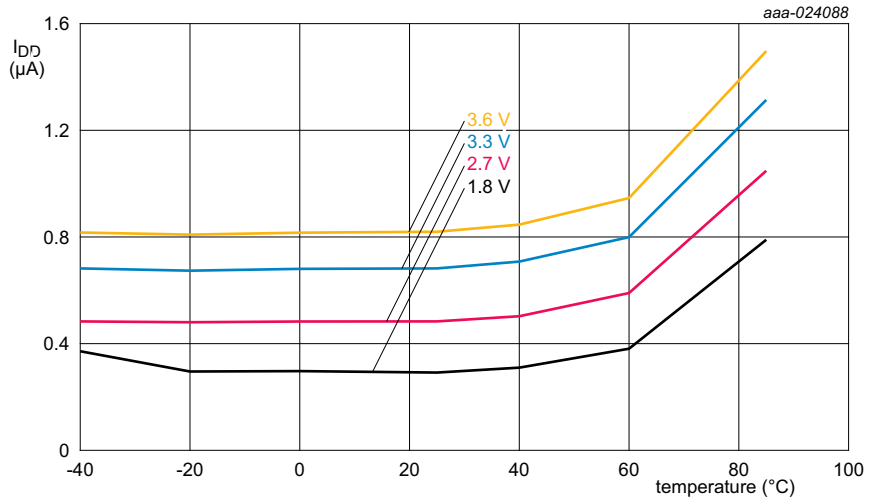
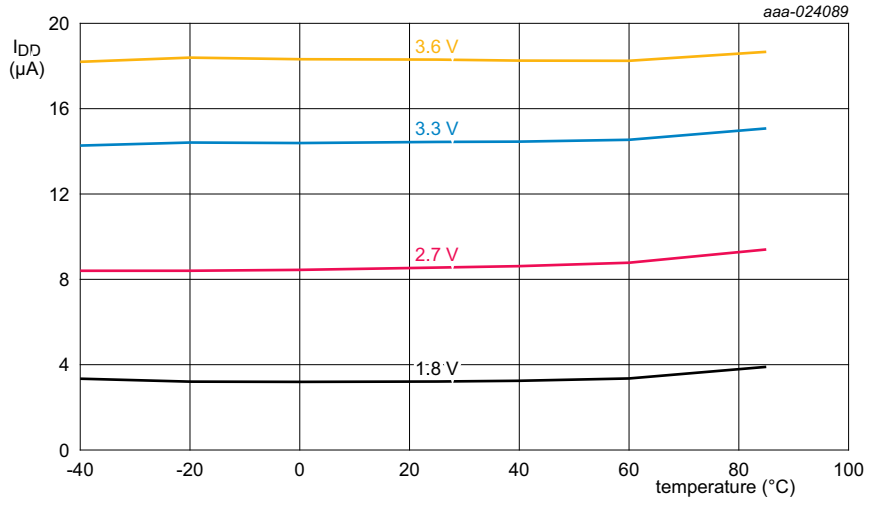


WKT running with external 32 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 20. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 32 kHz input clock)



WKT running with external 1 MHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 21. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 1 MHz input clock)

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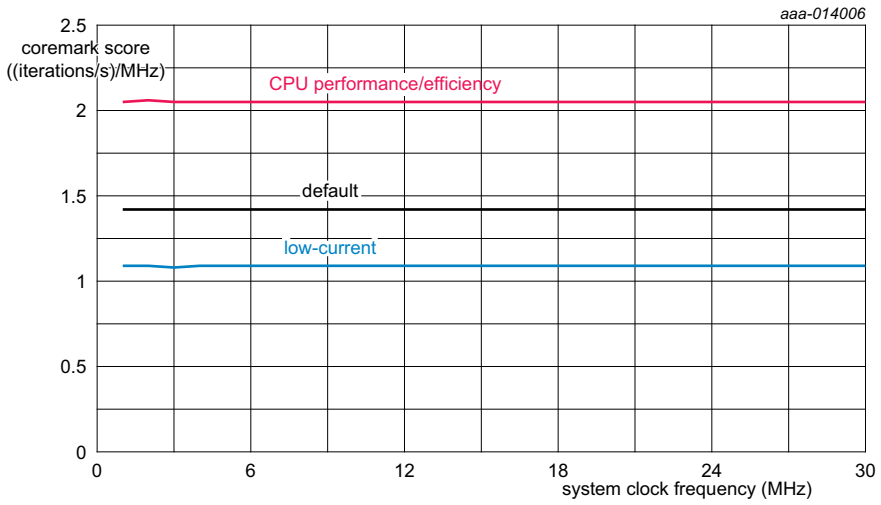
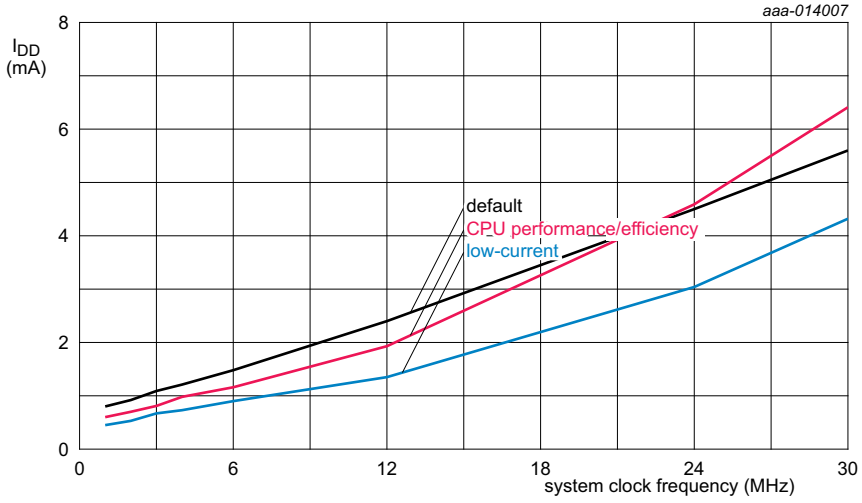
11.5 CoreMark data



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCTimer/PWM disabled in the SYSAHBCLKCTRL register; BOD disabled; internal pull-up resistors enabled. Measured with Keil uVision 5.10.

1 MHz - 6 MHz: external clock; IRC, PLL disabled.12 MHz: IRC enabled; PLL disabled. 24 MHz: IRC enabled; PLL enabled.30 MHz: system oscillator enabled; PLL enabled.

Fig 22. CoreMark score



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCTimer/PWM disabled in the SYSAHBCLKCTRL register; BOD disabled; internal pull-up resistors enabled. Measured with Keil uVision 5.10.

1 MHz - 6 MHz: external clock; IRC, PLL disabled.12 MHz: IRC enabled; PLL disabled.24 MHz: IRC enabled; PLL enabled.30 MHz: system oscillator enabled; PLL enabled.

Fig 23. Active mode: CoreMark power consumption I_{DD}

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11.6 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG. and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 30 MHz.

Table 10. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
IRC	261	-	-	System oscillator running; PLL off; independent of main clock frequency; IRC output disabled.
System oscillator at 12 MHz	274	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator	2	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	39	-	-	Independent of main clock frequency.
Main PLL	-	301	-	-
CLKOUT	-	67	150	Main clock divided by 4 in the CLKOUTDIV register.
ROM	-	27	68	-
GPIO + pin interrupt/pattern match	-	95	233	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	59	145	-
IOCON	-	45	110	-
SCTimer/PWM	-	168	411	-
MRT	-	89	220	-
WWDT	-	29	71	-
I2C0	-	54	132	-
SPI0	-	55	136	-
SPI1	-	55	136	-
USART0	-	50	124	-

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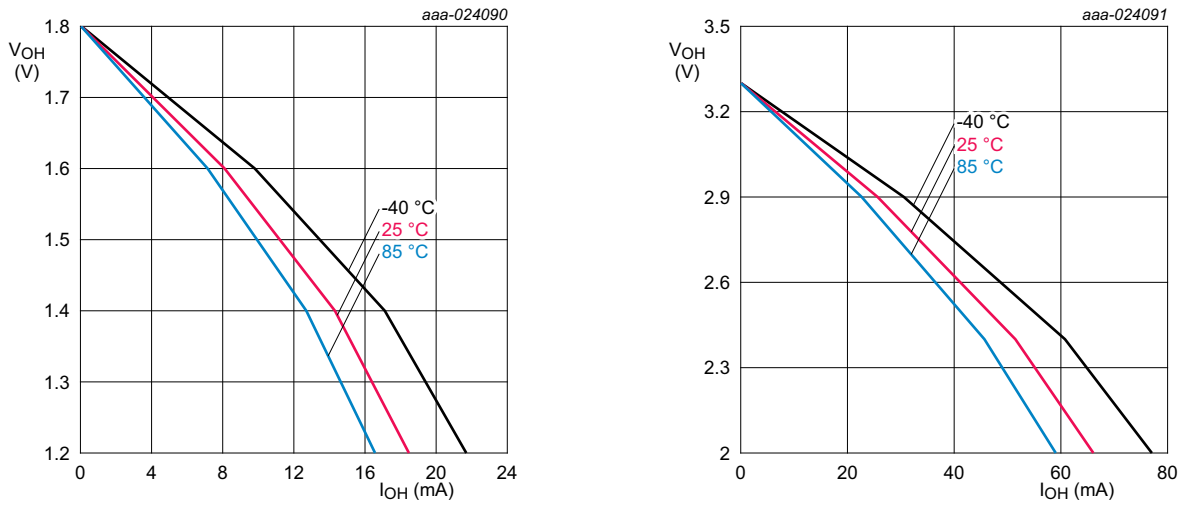
Table 10. Power consumption for individual analog and digital blocks *...continued*

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
ADC	-	57	141	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	57	141	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	1990	2070	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
DMA	-	324	793	
CRC	-	34	85	-

11.7 Electrical pin characteristics



Conditions: V_{DD} = 1.8 V; on pin PIO0_12.

Conditions: V_{DD} = 3.3 V; on pin PIO0_12.

Fig 24. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

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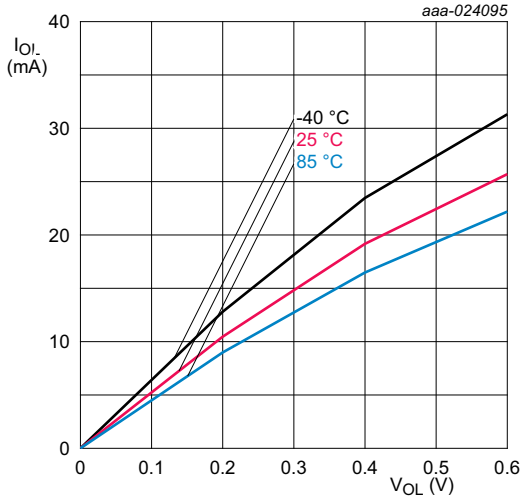
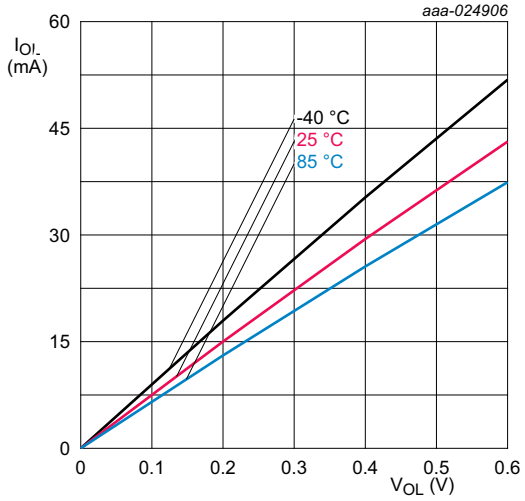
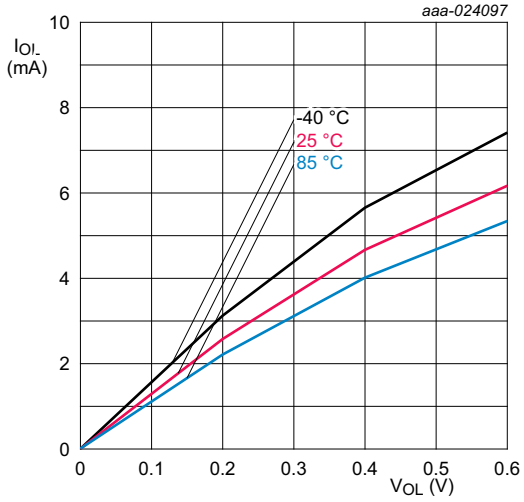


Conditions: V_{DD} = 1.8 V; on pins PIO0_10 and PIO0_11.

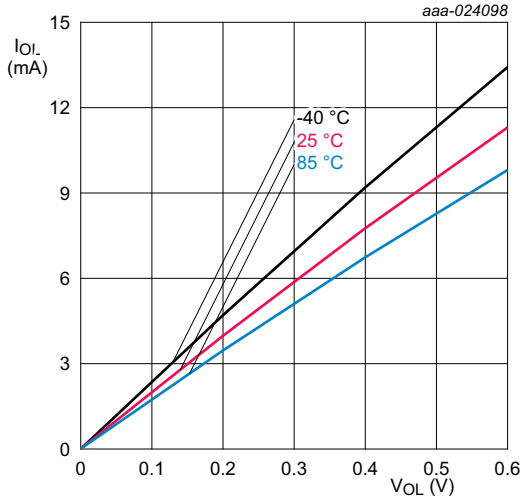


Conditions: V_{DD} = 3.3 V; on pins PIO0_10 and PIO0_11.

Fig 25. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.



Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 26. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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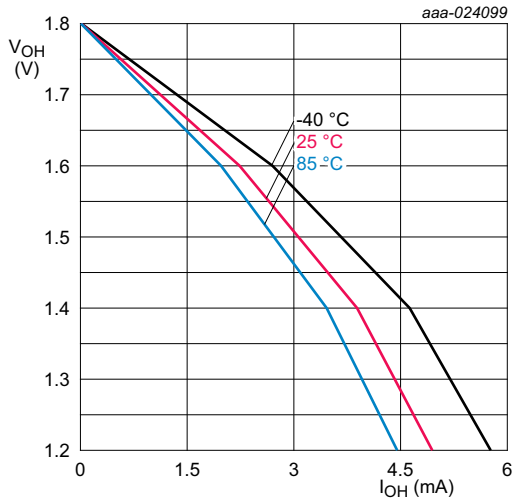
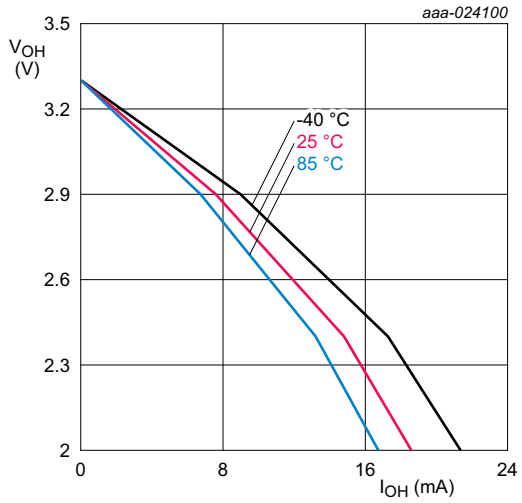
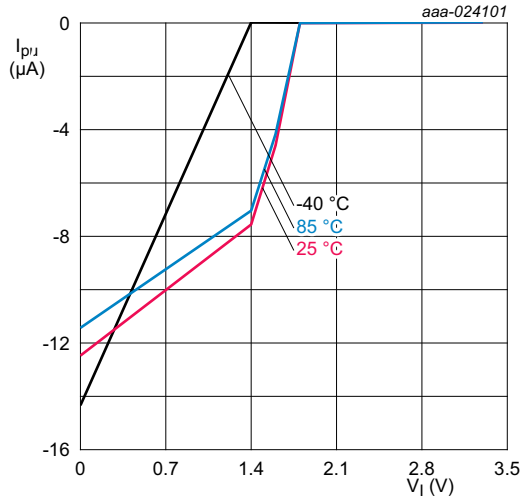


Conditions: V_{DD} = 1.8 V; standard port pins.

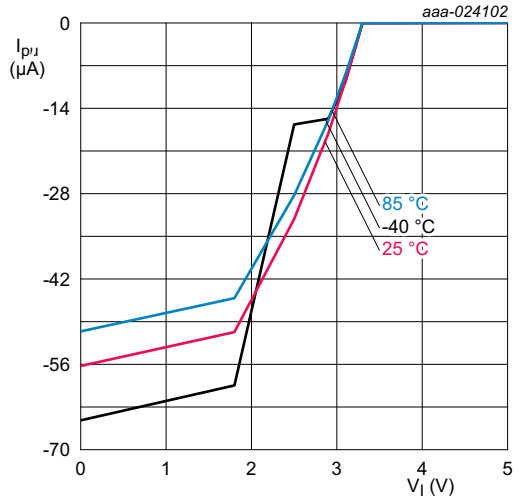


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 27. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical pull-up current I_{PU} versus input voltage V_I

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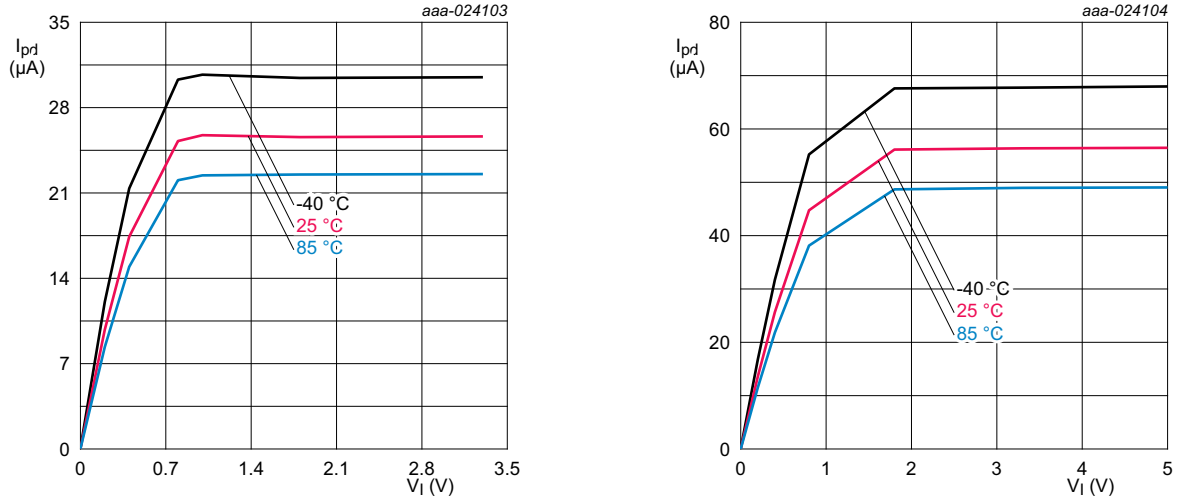

Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 29. Typical pull-down current I_{PD} versus input voltage V_I

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12. Dynamic characteristics

12.1 Power-up ramp conditions

Table 11. Power-up characteristics

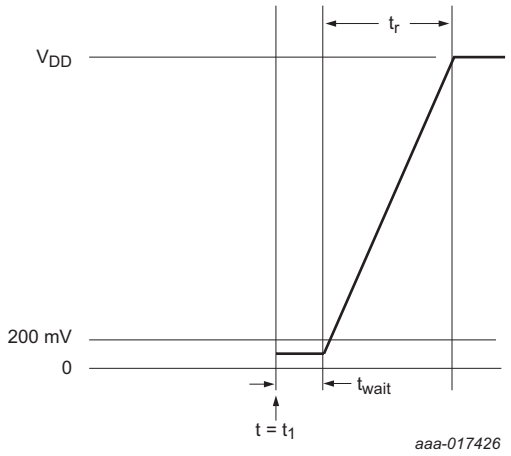
T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	at t = t_1: 0 < V_I ≤ 200 mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2][3]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	200	mV

[1] See Figure 30.

[2] The wait time specifies the time the power supply must be at levels below 200 mV before ramping up. See the LPC83x errata sheet.

[3] Based on characterization, not tested in production.



Condition: 0 < V_I ≤ 200 mV at start of power-up (t = t_1)

Fig 30. Power-up ramp

12.2 Flash/EEPROM memory

Table 12. Flash characteristics

T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	1000	-	-	cycles

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Table 12. Flash characteristics

T_{amb} = −40 °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ret}	retention time	powered		10	20	-	years
		not powered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. T_{amb} <= +85 °C.

12.3 External clock for the oscillator in slave mode

Remark: The input voltage on the XTALIN and XTALOUT pins must be ≤ 1.95 V (see Table 7). For connecting the oscillator to the XTAL pins, also see Section 12.3.

Table 13. Dynamic characteristic: external clock (XTALIN input)

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency	1	-	25	MHz
$T_{cy(clk)}$	clock cycle time	40	-	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

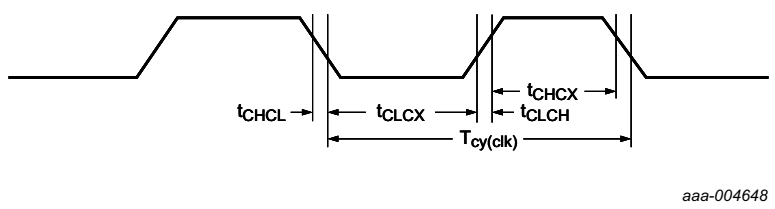

Fig 31. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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12.4 Internal oscillators

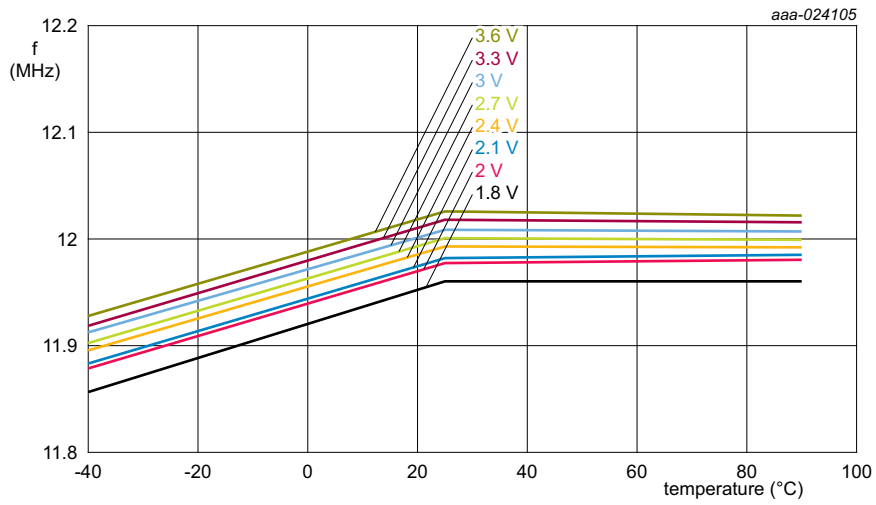
Table 14. Dynamic characteristics: IRC

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.82	12	12.18	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1.5 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1.5 % accuracy specification for voltages below 2.7 V.

Fig 32. Typical Internal RC oscillator frequency versus temperature

Table 15. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

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12.4.1 I/O pins

Table 16. Dynamic characteristics: I/O pins[1]

T_{amb} = –40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.4.2 WKTCLKIN pin (wake-up clock input)

Table 17. Dynamic characteristics: WKTCLKIN pin

T_{amb} = –40 °C to +85 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Max	Unit
f_{clk}	clock frequency	deep power-down mode and power-down mode	[1]	-	1	MHz
		deep-sleep, sleep, and active mode	[1]	-	10	MHz
t_{CHCX}	clock HIGH time	-		50	-	ns
t_{CLCX}	clock LOW time	-		50	-	ns

[1] Assuming a square-wave input clock.

12.4.3 SCTimer/PWM

Table 18. SCTimer/PWM output dynamic characteristics

T_{amb} = –40 °C to +85 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated skew (over process, voltage, and temperature) of any two SCTimer/PWM output signals routed to standard I/O pins; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	4	ns

12.4.4 I²C-bus

Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = –40 °C to +85 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns

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Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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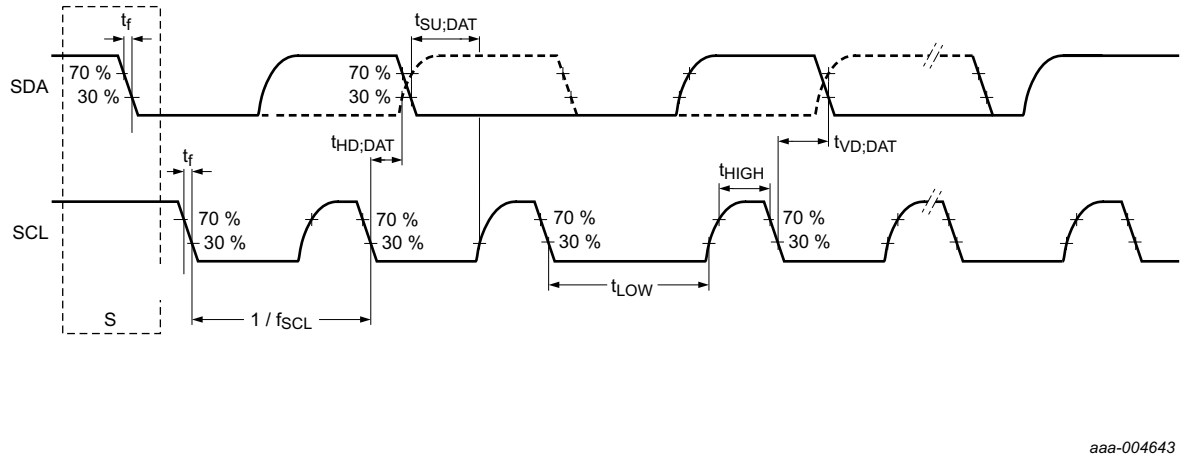

Fig 33. I²C-bus pins clock timing

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12.4.5 SPI interfaces

In master mode, the maximum supported bit rate is limited by the maximum system clock to 30 Mbit/s. In slave mode, assuming a set-up time of 3 ns for the external device and neglecting any PCB trace delays, the maximum supported bit rate is 1/(2 x (26 ns + 3 ns)) = 17 Mbit/s at 3.0 V <= VDD <= 3.6 V and 13 Mbit/s at 1.8 V <= VDD < 3.0 V. The actual bit rate depends on the delays introduced by the external trace and the external device.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 20. SPI dynamic characteristics

T_{amb} = −40 °C to +85 °C; C_L = 20 pF; input slew = 1 ns. Simulated parameters sampled at the 30 % and 70 % level of the rising or falling edge; values guaranteed by design. Delays introduced by the external trace or external device are not considered.

Symbol	Parameter	Conditions	Min	Max	Unit
SPI master					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	2	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	6	-	ns
$t_{v(Q)}$	data output valid time	1.8 V <= V_{DD} <= 3.6 V	-3	4	ns
SPI slave					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	2	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	4	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	26	ns
		1.8 V <= V_{DD} < 3.0 V	0	35	ns

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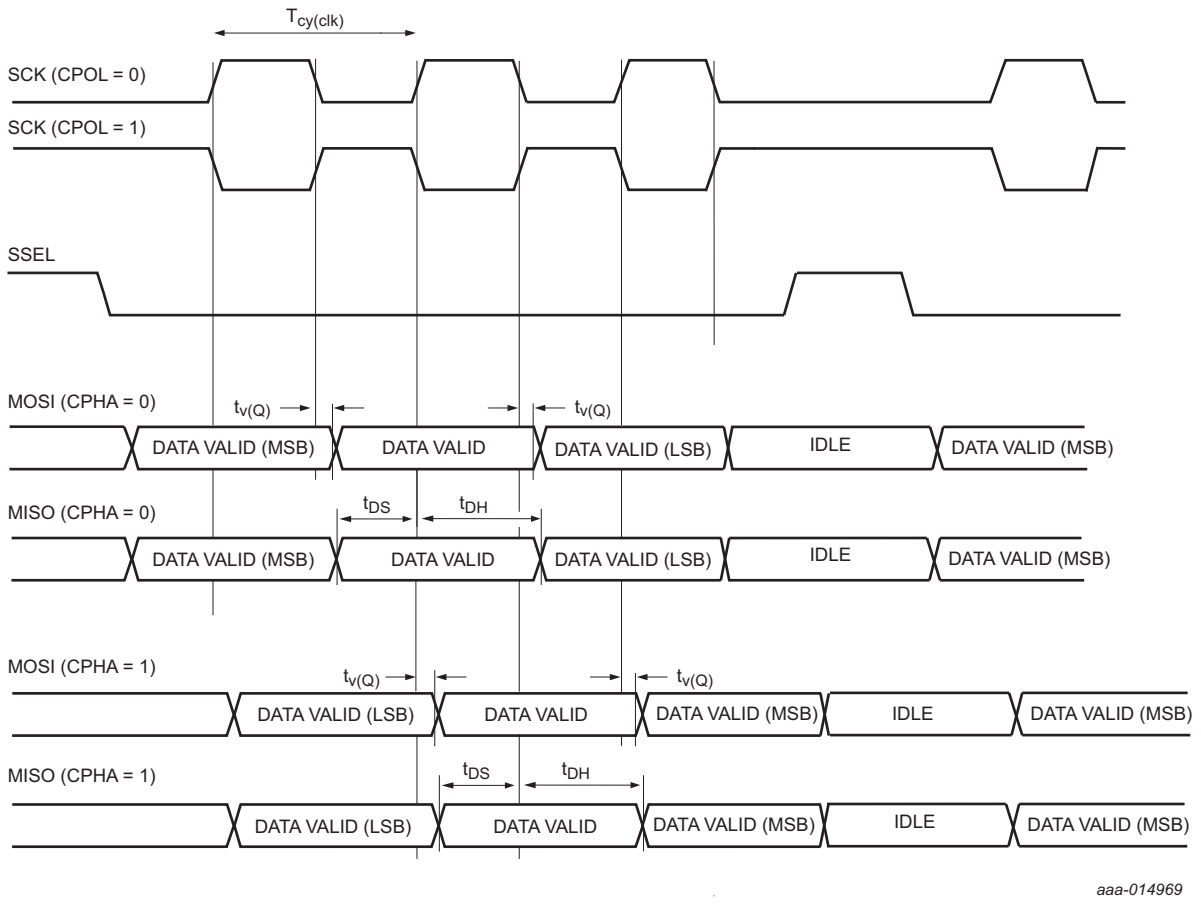

$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider.

Fig 34. SPI master timing

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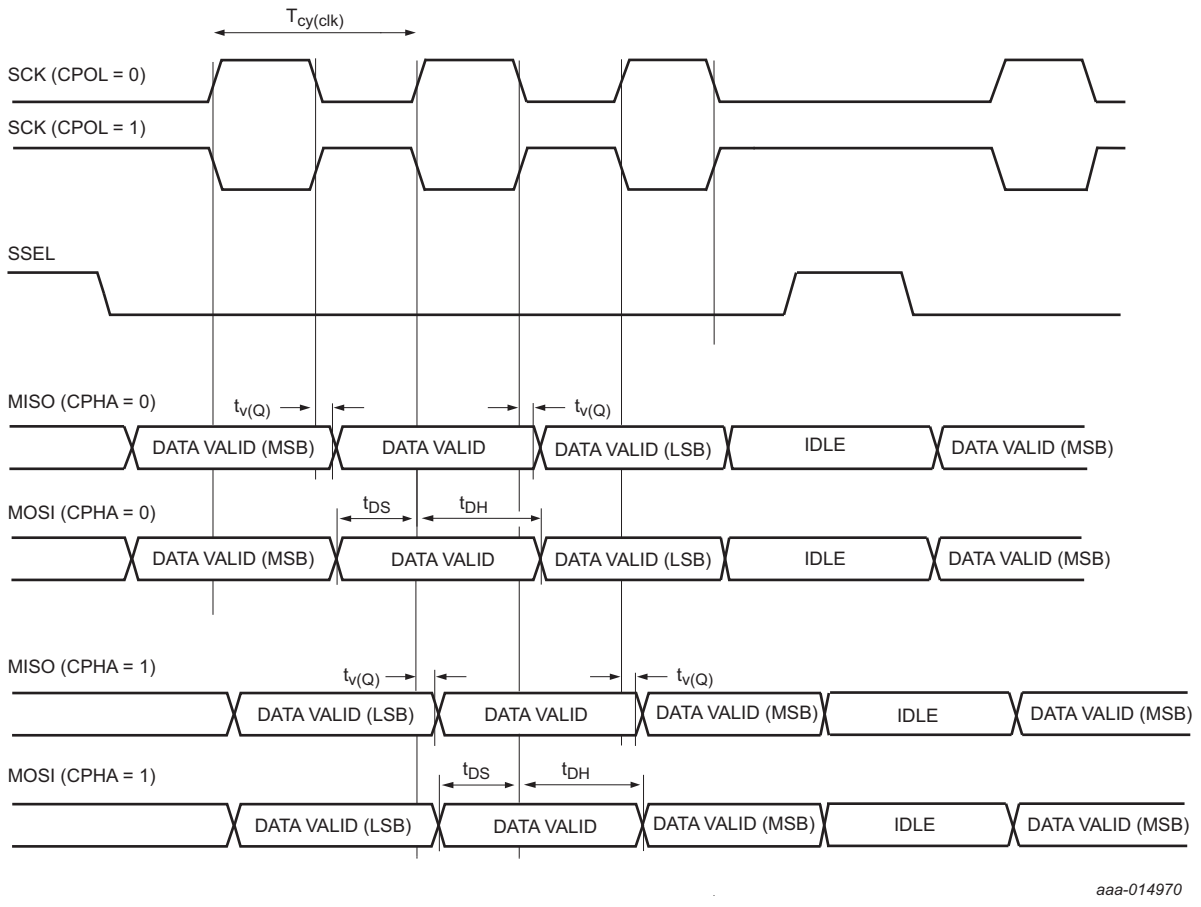

Fig 35. SPI slave timing

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12.4.6 USART interface

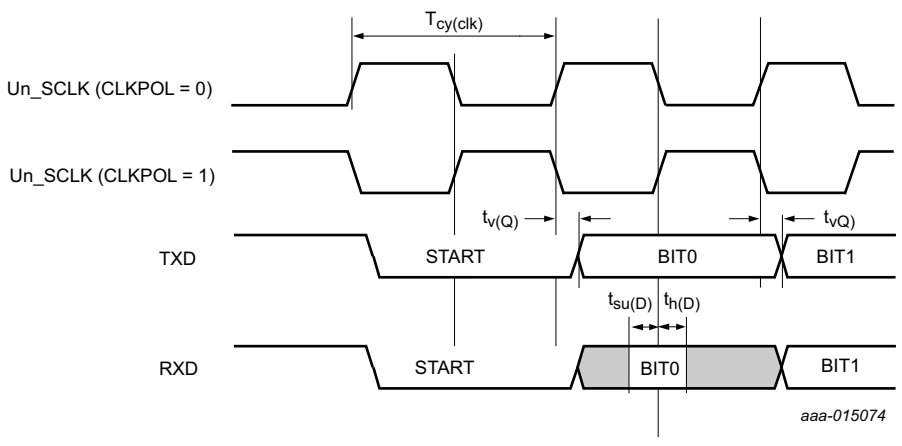
The maximum USART bit rate is 10 Mbit/s in synchronous mode master mode and 10 Mbit/s in synchronous slave mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 21. USART dynamic characteristics

T_{amb} = −40 °C to +85 °C; 1.8 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	31	-	ns
		1.8 V <= V_{DD} < 3.0 V	37		
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		0	5	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		6	-	ns
$t_{h(D)}$	data input hold time		2	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	28	ns
		1.8 V <= V_{DD} < 3.0 V	0	37	ns



In master mode, $T_{cy(clk)}$ = U_PCLK/BRGVAL.

Fig 36. USART timing

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13. Characteristics of analog peripherals

13.1 BOD

Table 22. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.40	-	V
		interrupt level 2					
		assertion		-	2.54	-	V
		de-assertion		-	2.68	-	V
		interrupt level 3					
		assertion		-	2.85	-	V
		de-assertion		-	2.95	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.20	-	V
		reset level 2					
		assertion		-	2.34	-	V
		de-assertion		-	2.49	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.78	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL. Interrupt level 0 is reserved.

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13.2 ADC

Table 23. 12-bit ADC static characteristics

T_{amb} = −40 °C to +85 °C unless noted otherwise; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DD}; VREFN = V_{SS}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
V_{ref}	reference voltage	on pin VREFP		2.4	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	0.32	pF
$f_{clk(ADC)}$	ADC clock frequency	2.7 V <= V_{DD} <= 3.6 V	[2]	-	-	30	MHz
		2.4 V <= V_{DD} < 2.7 V	[3]	-	-	25	MHz
f_s	sampling frequency	2.7 V <= V_{DD} <= 3.6 V	[2]	-	-	1.2	Msamples/s
		2.4 V <= V_{DD} < 2.7 V	[3]	-	-	1	Msamples/s
E_D	differential linearity error	T_{amb} = 85 °C	[5][4]	-	+/- 2.5	-	LSB
$E_{L(adj)}$	integral non-linearity	T_{amb} = 85 °C	[6][4]	-	+/- 2.5	-	LSB
E_O	offset error	T_{amb} = 85 °C	[7][4]	-	+/- 4.5	-	LSB
$V_{err(fs)}$	full-scale error voltage	1.2 Msamples/s; T_{amb} = 85 °C	[8][4]	-	+/- 0.5	-	%
Z_i	input impedance	f_s = 1.2 Msamples/s	[1][9] [10]	0.1	-	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels. See Figure 37.

[2] In the ADC TRM register, set VRANGE = 0 (default).

[3] In the ADC TRM register, set VRANGE = 1 (default).

[4] Based on characterization. Not tested in production.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 38.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 38.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 38.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 38.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0.1 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 8 for C_{io}.

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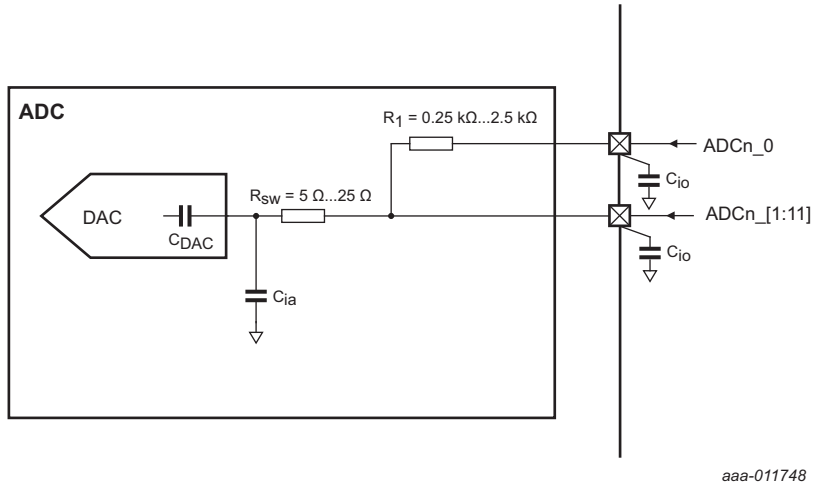

Fig 37. ADC input impedance

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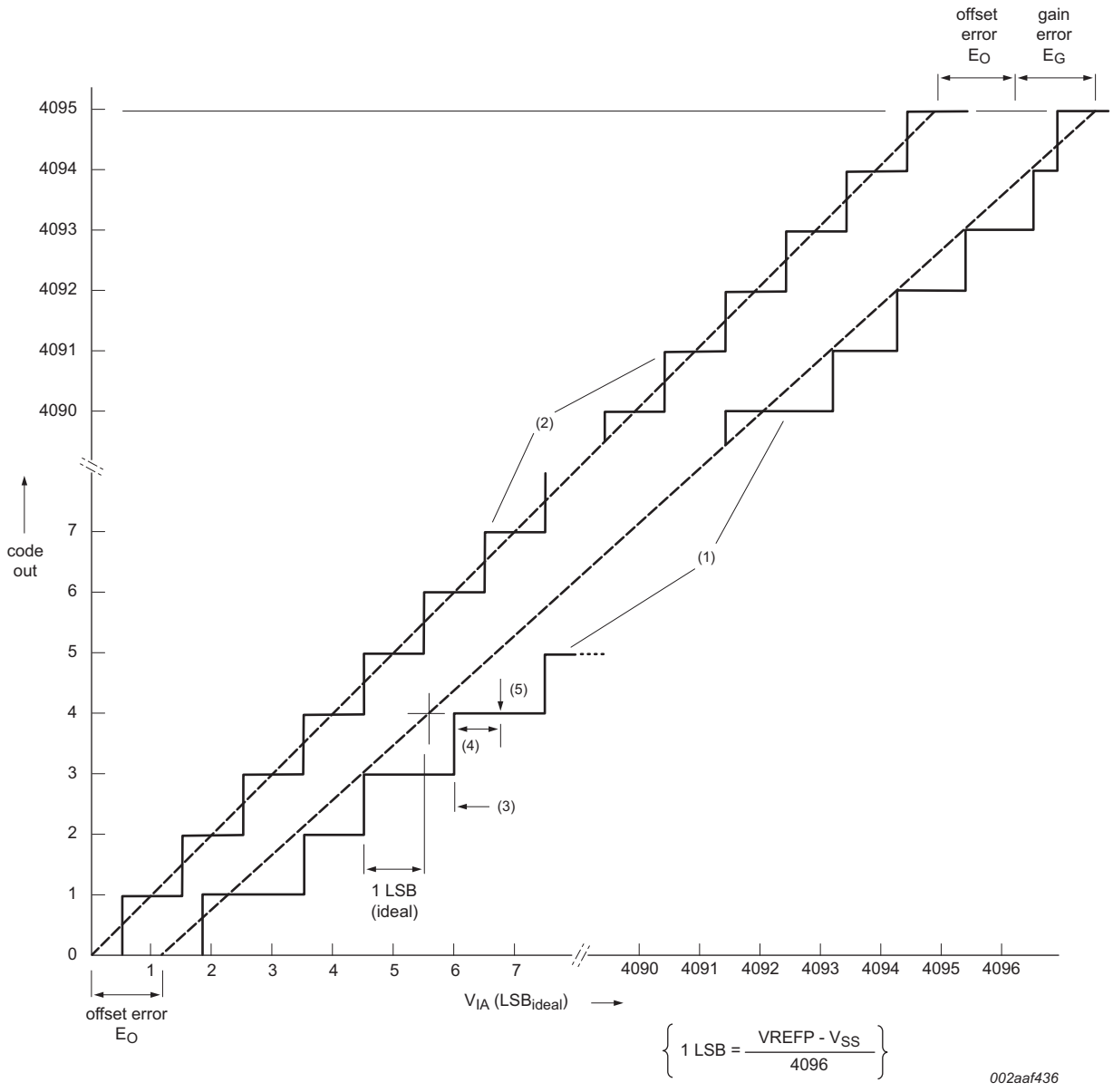

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 38. 12-bit ADC characteristics

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14. Application information

14.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended to couple the input through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

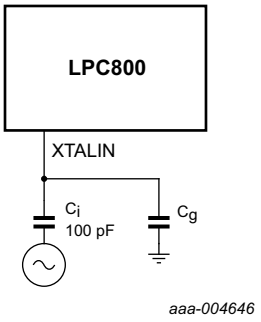

Fig 39. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled with a capacitor of 100 pF (Figure 39), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 40 and in Table 24 and Table 25. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 40 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 24).

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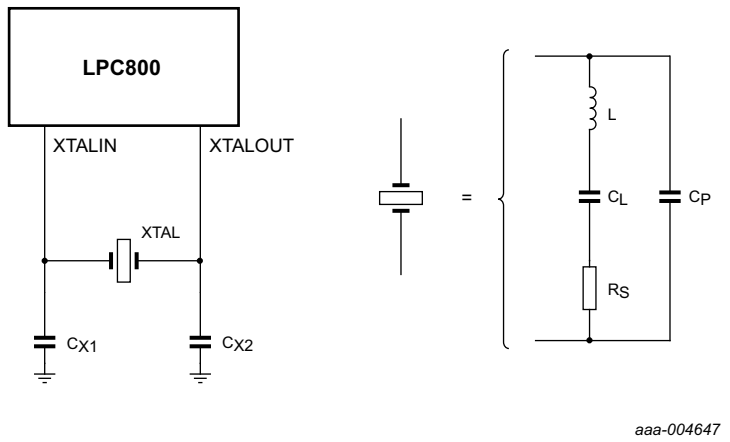

Fig 40. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 24. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 25. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.2 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

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order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller according to the increase in parasitics of the PCB layout.

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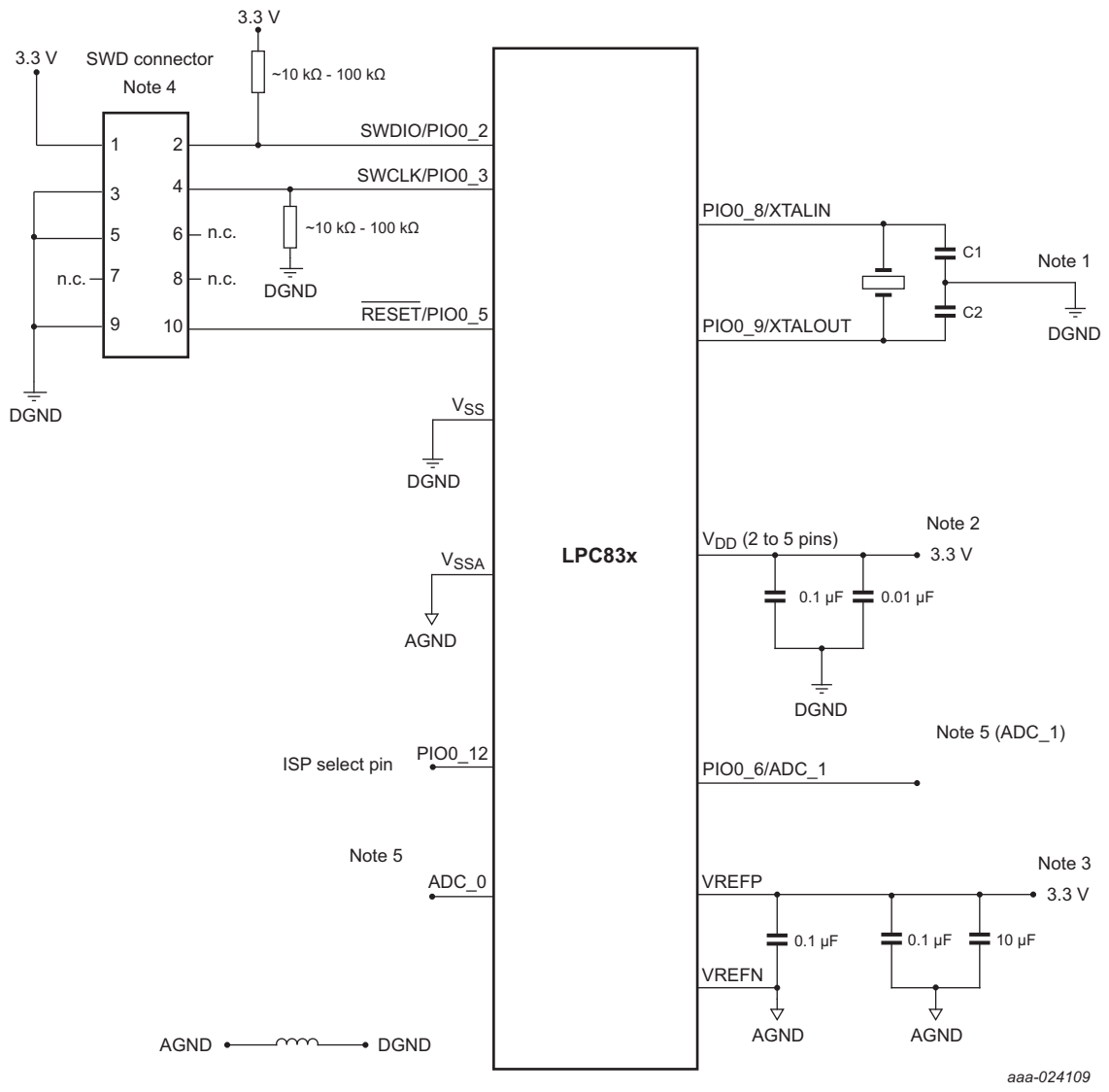
14.3 Connecting power, clocks, and debug functions

Figure 41 shows the basic board connections used to power the LPC83x, connect the external crystal, and provide debug capabilities via the serial wire port.



(1) See Section 14.1 "XTAL input" for the values of C1 and C2.

(2) Position the decoupling capacitors of 0.1 μF and 0.01 μF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 μF as close as possible to the VREFN and V_{DD} pins. The 10 μF bypass capacitor filters the power line. Tie VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 2.

Fig 41. Power, clock, and debug connections

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14.4 Termination of unused pins

Table 26 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 26. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_5	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether Deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

14.5 Pin states in different power modes

Table 27. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_4, PIO0_5 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
PIO0_16/ WAKEUP	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

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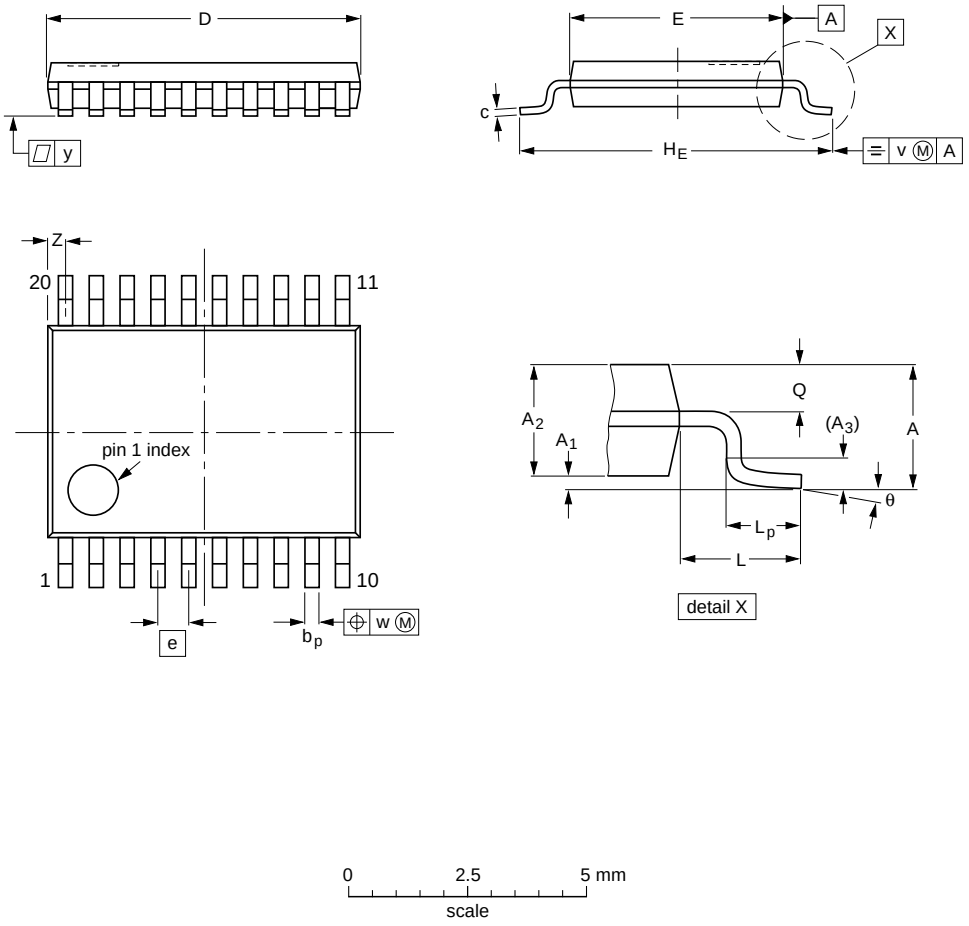
15. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 42. Package outline SOT360-1 (TSSOP20)

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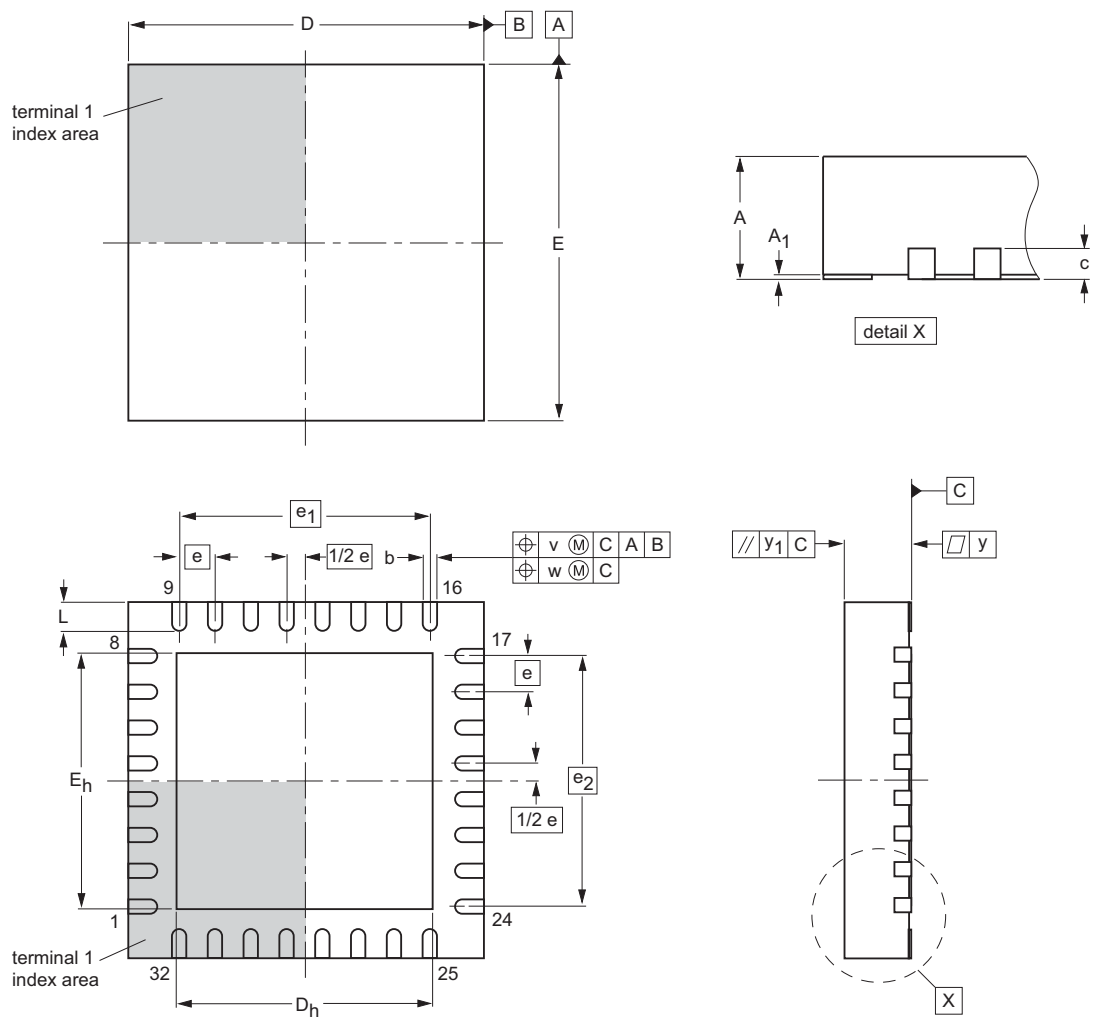
HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit(1)		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max		0.05	0.30		5.1	3.75	5.1	3.75				0.5				
	nom	0.85			0.2					0.5	3.5	3.5		0.1	0.05	0.05	0.1
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 43. Package outline (HVQFN33 5x5)

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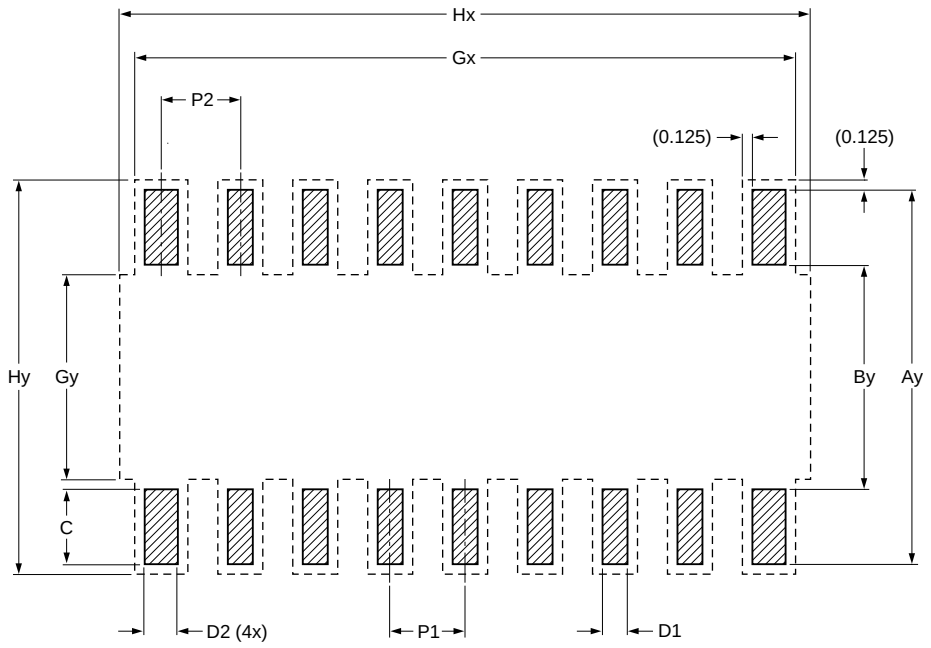
16. Soldering

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 44. Reflow soldering of the TSSOP20 package

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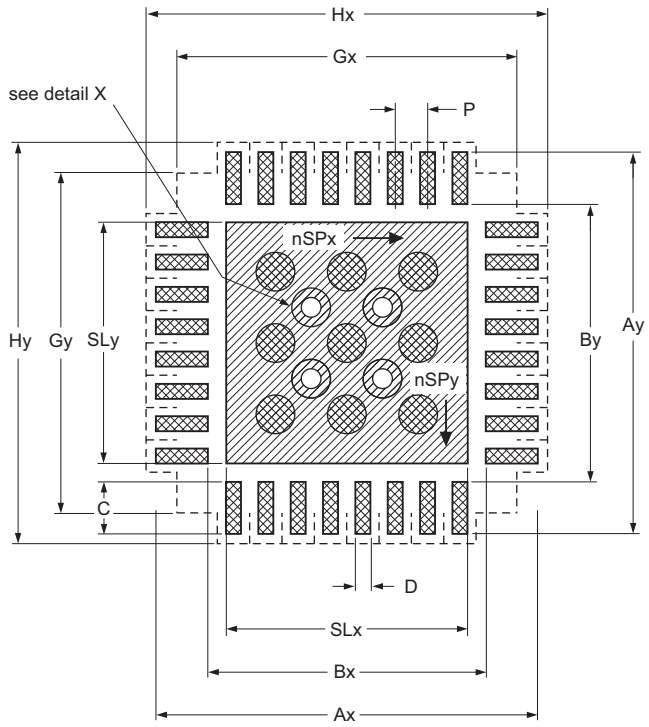
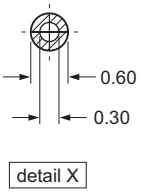
Footprint information for reflow soldering of HVQFN33 package





solder land

solder paste

occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 45. Reflow soldering of the HVQFN33 package (5x5)

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17. Abbreviations

Table 28. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] I2C-bus specification *UM10204*.

[2] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

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19. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC83X v.1.2	20180404	Product data sheet	201804004I	LPC83X v.1.1
Modifications:	• Updated table note 2 of Section 12.1 “Power-up ramp conditions”.			
LPC83X v.1.1	20161003	Product data sheet	-	LPC83X v.1
Modifications:	• Updated Section 2 “Features and benefits”: DMA with 18 channels and 8 trigger inputs. • Updated features of Section 8.12 “DMA controller”: DMA with 18 channels and 8 trigger inputs. • Added text to Table 4 “Movable functions (assign to pins PIO0_0 to PIO0_28 through switch matrix)”: – SPI0_SSEL1 Slave select 0 for SPI1. Slave select 1 for SPI0. – SPI0_SSEL2 Slave select 0 for SPI2. Slave select 2 for SPI0. – SPI0_SSEL3 Slave select 0 for SPI3. Slave select 3 for SPI0. • Changed the cross reference in the remark of Section 12.3 “External clock for the oscillator in slave mode” to Table 7 “General operating conditions”. • Updated Figure 2 “HVQFN33 package marking”. Removed the number 14 from the inner block. • Updated table note section 2 in Table 5 “Limiting values” to make the reference to Table 7 “General operating conditions”.			
LPC83X v.1	20160805	Product data sheet	-	-

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20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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