

Quick Start Guide

SJA1124EVB

Evaluation Board for SJA1124 SPI to Quad-LIN Bridge

Arduino™ UNO footprint-compatible LIN Communication Shield

GET TO KNOW THE SJA1124 EVALUATION BOARD

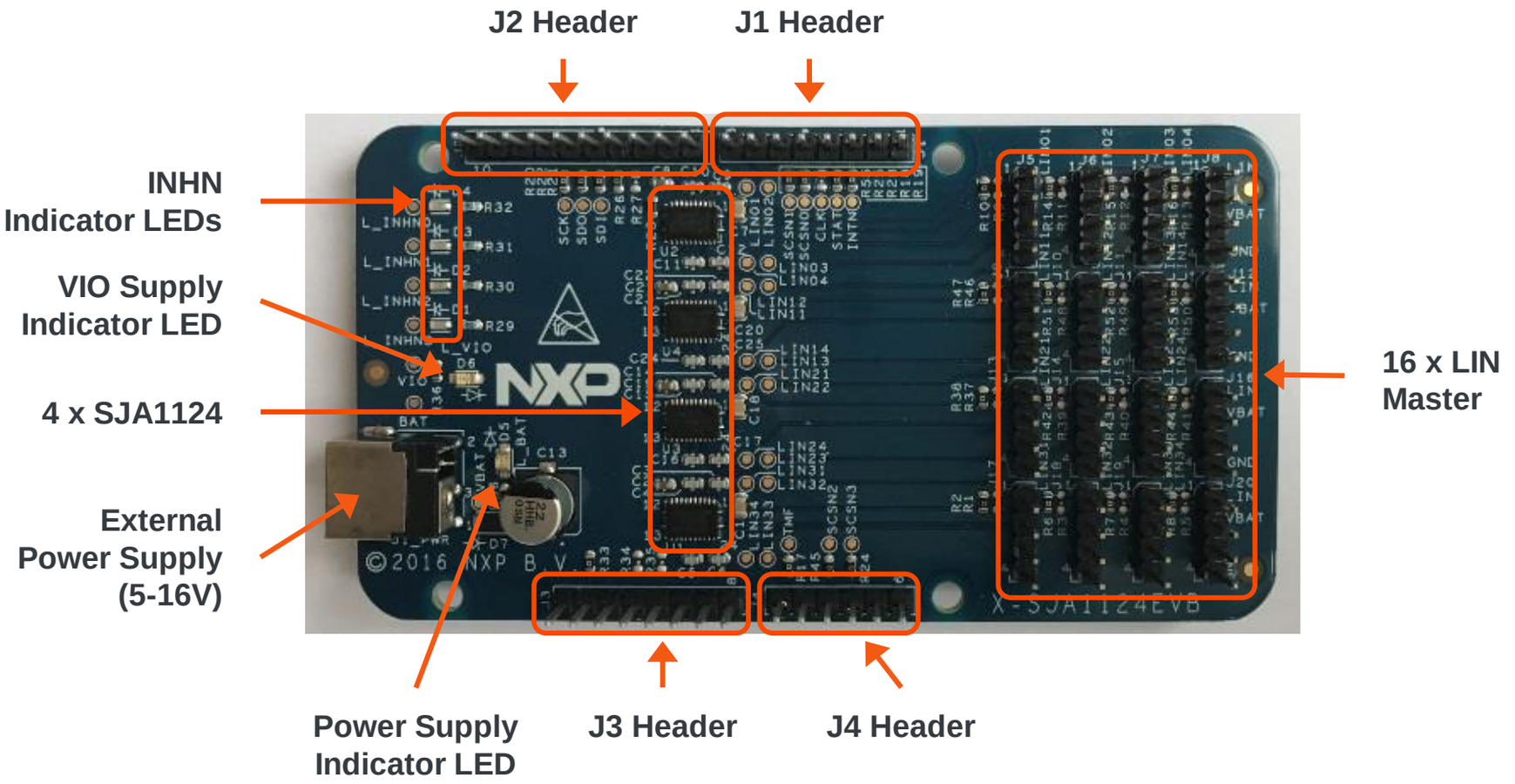


Figure 1: Front side of SJA1124EVB

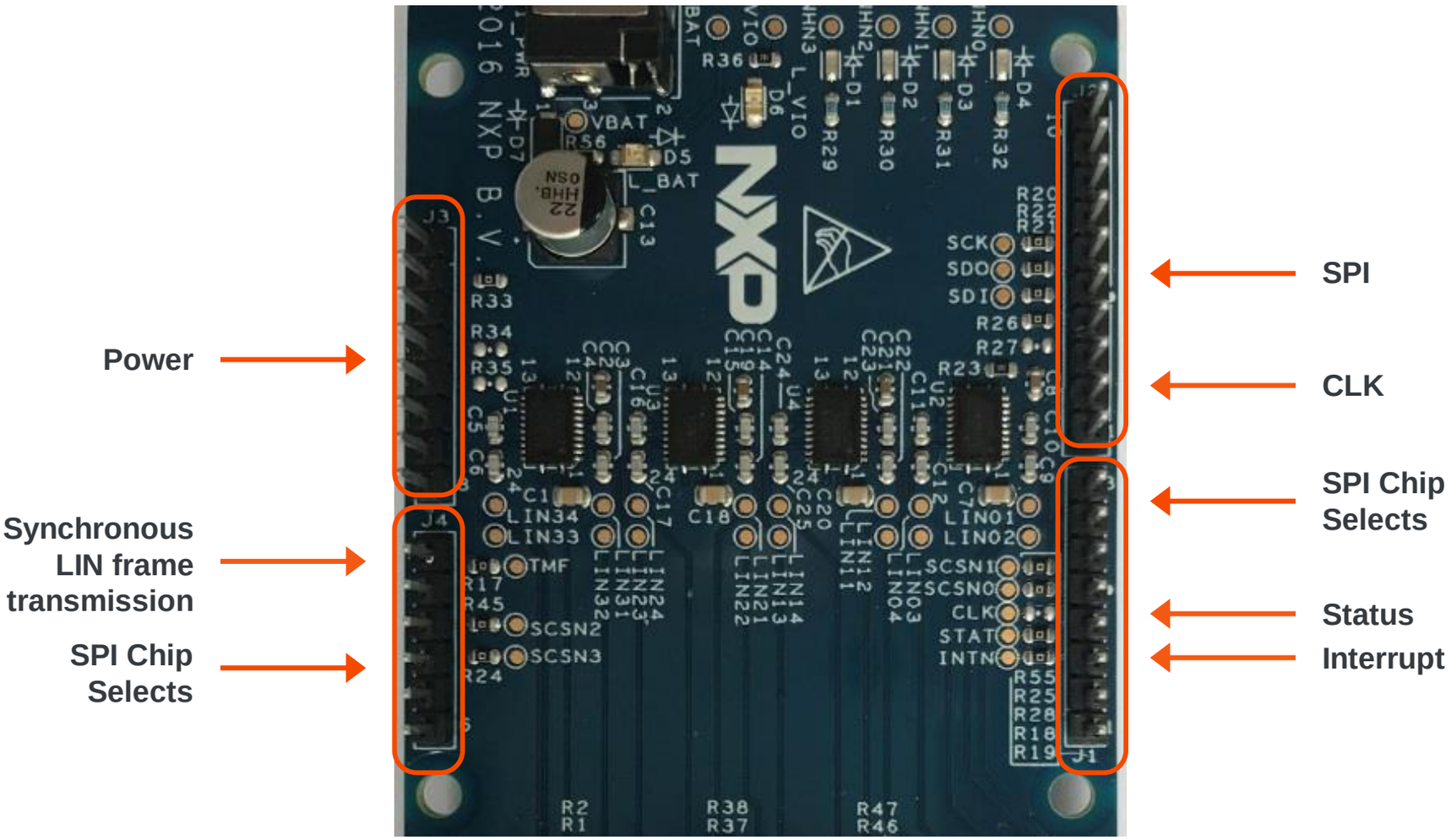
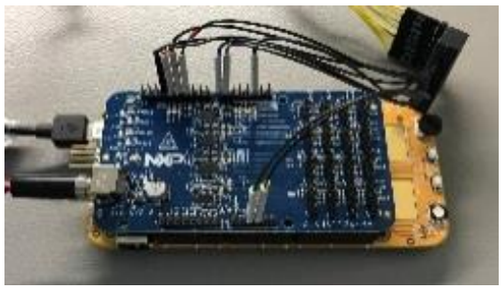


Figure 2: SJA1124EVB footprint

SJA1124EVB

Arduino™ UNO footpint-compatible shield



The SJA1124 EVB has the standard-based form factor compatible with Arduino™ UNO pin layout, that enables rapid prototyping with a wide range of microcontroller development boards.

Example: SJA1124EVB + S32K144EVB

FEATURES

- 4 x SJA1124A
- SPI to LIN bridge
- Supports 16 x LIN master channel connectors
- Arduino™ UNO footprint-compatible shield
- Easy access to I/O header pins
- Power LED indicator
- VIO LED indicator
- INHN LED indicators
- Small form factor

MICROCONTROLLER BOARD COMPATIBILITY

- S32K14xEVB
- DEVKIT-MPC574x
- DEVKIT-S12x
- FRDM-KEAx
- etc.

STEP-BY-STEP INSTRUCTIONS

This section describes how to use the SJA1124 evaluation board as a hardware plug-in board (shield) that supports up to 16 LIN master connections when plugged on existing microcontroller development boards.

1 Verification of Supply Setting

The supply connector pin mapping of J3 Header must be checked against microcontroller board supply connector. VBAT is the power supply voltage (max 16V). VDD (3.3V / 5V), P3V3 (3.3V) and P5V0 (5V) are reference voltages. Otherwise SJA1124 and other components on the boards can be damaged.

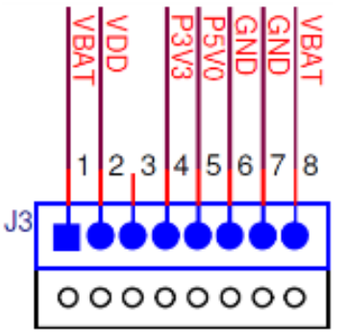


Figure 3: J3 Header (supply connector)

STEP-BY-STEP INSTRUCTIONS (cont.)

2 Digital Interface Voltage Setting

For adaptation to the digital interface levels of the connected microcontroller provides the SJA1124 a VIO reference voltage pin. Default SJA1124EVB setting for VIO pin mapping is J3-3 (VDD).

As alternative J3-4 (P3V3) or J3-4 (P5V0) can be used by populating a zero-ohm resistor to the appropriate placeholder. See Figure 4.

Note: Only one placeholder of R33, R34 and R35 shall be populated with a zero-ohm resistor. Otherwise different voltage sources are shorted and damage on the microcontroller development boards might occur.

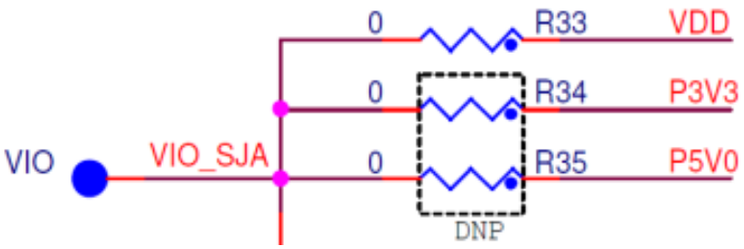


Figure 4: VIO pin mapping configuration options

3 Reference Clock Setting

For the baud rate generators a reference clock CLK (0.4 … 10 MHz) must be provided. Default SJA1124EVB setting for CLK pin mapping is J2-2 (CLK1_SJA).

As alternative J2-1 (CLK2_SJA) or J1-5 (CLK3_SJA) can be used by populating a zero-ohm resistor to the appropriate placeholder. See Figure 5.

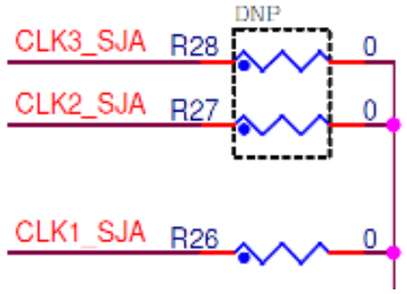


Figure 5: CLK pin mapping configuration options

J1 HEADER – DEFAULT SETTING

J1 Header	Resistor	Default Setting	Signal	Description
J1-1	-	-	-	Not connected
J1-2	-	-	-	Not connected
J1-3	R19	0	INTN_SJA	Shared SJA1124 interrupt output
J1-4	R18	0	STAT_SJA	Shared SJA1124 SPI status output
J1-5	R28	open	CLK3_SJA	Alternative SJA1124 clock reference
J1-6	-	-		Not connected
J1-7	R25	0	SCSN_SJA0	SJA1124 SPI chip select input #0
J1-8	R55	0	SCSN_SJA1	SJA1124 SPI chip select input #1

J2 HEADER – DEFAULT SETTING

J2 Header	Resistor	Default Setting	Signal	Description
J2-1	R27	open	CLK2_SJA	Alternative SJA1124 clock reference
J2-2	R26	0	CLK1_SJA	SJA1124 clock reference
J2-3	-	-	-	Not connected
J2-4	R21	0	SDI_SJA	Shared SJA1124 SPI slave data input
J2-5	R22	0	SDO_SJA	Shared SJA1124 SPI slave data output
J2-6	R20	0	SCK_SJA	Shared SJA1124 SPI slave clock input
J2-7	-	-	GND	Ground
J2-8	-	-	-	Not connected
J2-9	-	-	-	Not connected
J2-10	-	-	-	Not connected

J3 HEADER – DEFAULT SETTING

J3 Header	Resistor	Default Setting	Signal	Description
J3-1	-	-	VBAT	Power supply
J3-2	R33	0	VDD	SJA1124 VIO reference voltage
J3-3	-	-	-	Not connected
J3-4	R34	open	P3V3	Alternative SJA1124 VIO reference voltage
J3-5	R35	open	P5V0	Alternative SJA1124 VIO reference voltage
J3-6	-	-	GND	Ground
J3-7	-	-	GND	Ground
J3-8	-	-	VBAT	Power supply

J4 HEADER – DEFAULT SETTING

J4 Header	Resistor	Default Setting	Signal	Description
J4-1	R17	0	TMF_SJA	Shared SJA1124 transmit frame input
J4-2	-	-	-	Not connected
J4-3	R45	0	SCSN_SJA2	SJA1124 SPI chip select input #2
J4-4	R24	0	SCSN_SJA3	SJA1124 SPI chip select input #3
J4-5	-	-	-	Not connected
J4-6	-	-	-	Not connected

J1 PWR HEADER – POWER SUPPLY

J1 PWR Header	Signal	Description
J1PWR-1	VBAT	Power supply
J1PWR-2	GND	Ground
J1PWR-3	GND	Ground

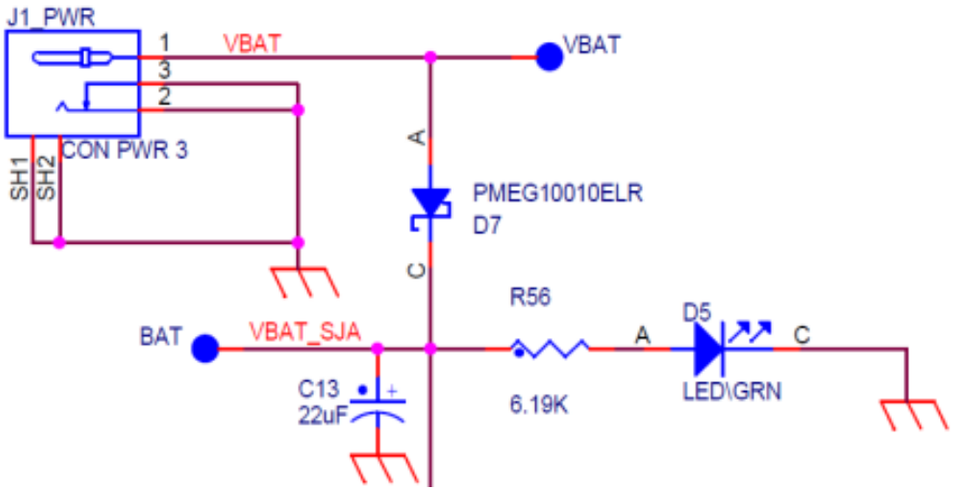


Figure 8: Power supply circuit

J5 – J20 HEADER – LIN BUS

Jx Header (J5 – J20)	Resistor	Default Setting	Signal	Description
Jx-1	Rx	0	LINx	LIN bus
Jx-2	-	-	VBAT	Power supply
Jx-3	-	-	-	Not connected
Jx-4	-	-	GND	Ground

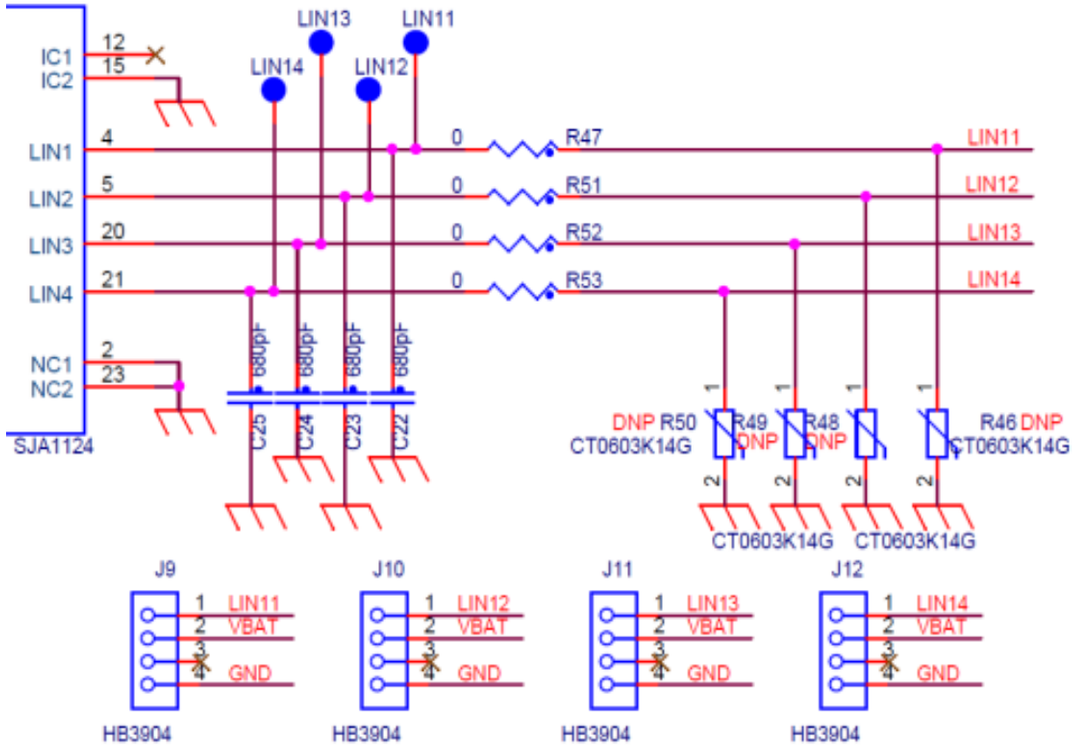


Figure 8: LIN circuit at SJA1124

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WARRANTY

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Get Started

Download example software and documentation from NXP DocStore (NDA required) www.docstore.nxp.com.

In-Vehicle Networking → LIN → SJA1124

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