NTUD3127C

Small Signal MOSFET

20 V, 200 mA / −180 mA, Complementary, 1.0 x 1.0 mm SOT−963 Package

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Features

- Complementary MOSFET Device
- 1.5 V Gate Voltage Rating
- Ultra Thin Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics.
- These are Pb−Free Devices

Applications

- Load Switch with Level Shift
- Optimized for Power Management in Ultra Portable Equipment

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
P−Channel −20 V	5.0 Ω @ −4.5 V	−0.18 A
	7.0 Ω @ −2.5 V	
	10 Ω @ −1.8 V	
	14 Ω @ −1.5 V	
N−Channel 20 V	3.0 Ω @ 4.5 V	0.20 A
	4.0 Ω @ 2.5 V	
	6.0 Ω @ 1.8 V	
	10 Ω @ 1.5 V	

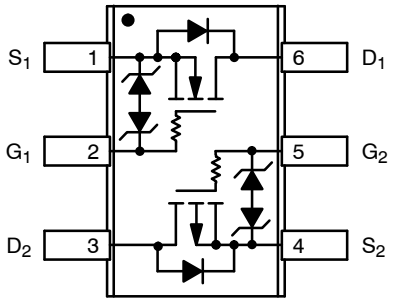
MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±8	V
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	160	mA
		T_A = 85°C		115	
	t ≤ 5 s	T_A = 25°C		200	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C		−140	
		T_A = 85°C		−100	
	t ≤ 5 s	T_A = 25°C		−180	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	125	mW
	t ≤ 5 s			200	
Pulsed Drain Current	N−Channel	t_p = 10 μs	I_{DM}	800	mA
	P−Channel			−600	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode) (Note 2)			I_S	200	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

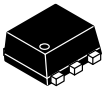
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz. Cu.
2. Pulse Test: pulse width ≤300 μs, duty cycle ≤2%

PINOUT: SOT−963

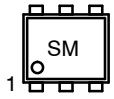


Top View



SOT−963
CASE 527AA

MARKING DIAGRAM



S = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NTUD3127CT5G	SOT−963 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State, Minimum Pad (Note 3)	$R_{\theta JA}$	1000	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 3)		600	

3. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz. Cu.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	N/P	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = −250 μA	−20			
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 5.0 V	T_J = 25°C			50	nA
				T_J = 85°C			200	
		P	V_{GS} = 0 V, V_{DS} = −5.0 V	T_J = 25°C			−50	
				T_J = 85°C			−200	
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25°C			100	nA
		P	V_{GS} = 0 V, V_{DS}= −16 V				−100	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±5.0 V				100	nA
		P					−100	
ON CHARACTERISTICS (Note 4)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.4		1.0	V
		P		I_D = −250 μA	−0.4		−1.0	
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V, I_D = 100 mA			1.5	3.0	Ω
		P	V_{GS} = −4.5V, I_D = −100 mA			4.0	5.0	
		N	V_{GS} = 2.5 V, I_D = 50 mA			2.0	4.0	
		P	V_{GS} = −2.5V, I_D = −50 mA			5.0	7.0	
		N	V_{GS} = 1.8 V, I_D = 20 mA			3.0	6.0	
		P	V_{GS} = −1.8V, I_D = −20 mA			6.5	10	
		N	V_{GS} = 1.5 V, I_D = 10 mA			4.0	10	
		P	V_{GS} = −1.5 V, I_D = −10 mA			7.5	14	
		N	V_{GS} = 1.2 V, I_D = 1.0 mA			5.5		
		P	V_{GS} = −1.2 V, I_D = −1.0 mA			11.5		
Forward Transconductance	g_{FS}	N	V_{DS} = 5.0 V, I_D = 125 mA			0.35		S
		P	V_{DS} = −5.0 V, I_D = −125 mA			0.26		
CHARGES, CAPACITANCES AND GATE RESISTANCE								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V V_{DS} = 15 V			9.0		pF
Output Capacitance	C_{OSS}					3.0		
Reverse Transfer Capacitance	C_{RSS}					2.2		
Input Capacitance	C_{ISS}	P	f = 1 MHz, V_{GS} = 0 V V_{DS} = −15 V			12		
Output Capacitance	C_{OSS}					2.7		
Reverse Transfer Capacitance	C_{RSS}					1.0		

4. Switching characteristics are independent of operating junction temperatures

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	N/P	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 4)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 200 mA, R_G = 2.0 Ω			15		ns
Rise Time	t_r					24		
Turn−Off Delay Time	$t_{d(OFF)}$					90		
Fall Time	t_f					60		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −180 mA, R_G = 2.0 Ω			20		
Rise Time	t_r					37		
Turn−Off Delay Time	$t_{d(OFF)}$					112		
Fall Time	t_f					97		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, I_S = 10 mA	T_J = 25°C		0.60	1.0	V
		P	V_{GS} = 0 V, I_S = −10 mA			−0.65	−1.0	

4. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES – N–CHANNEL

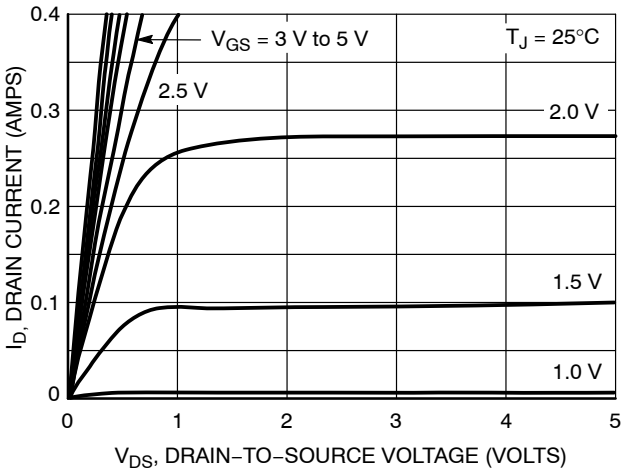


Figure 1. On–Region Characteristics

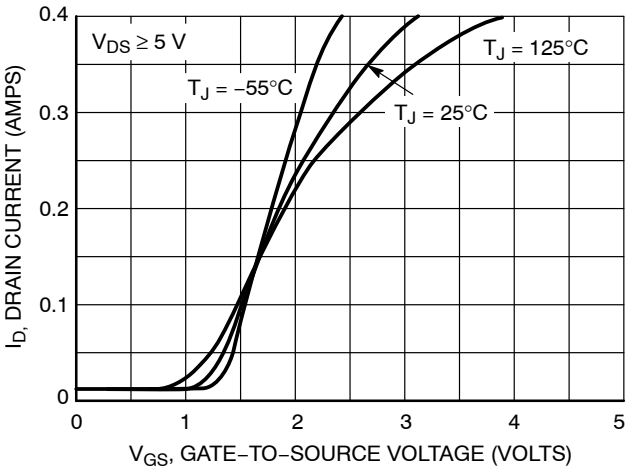


Figure 2. Transfer Characteristics

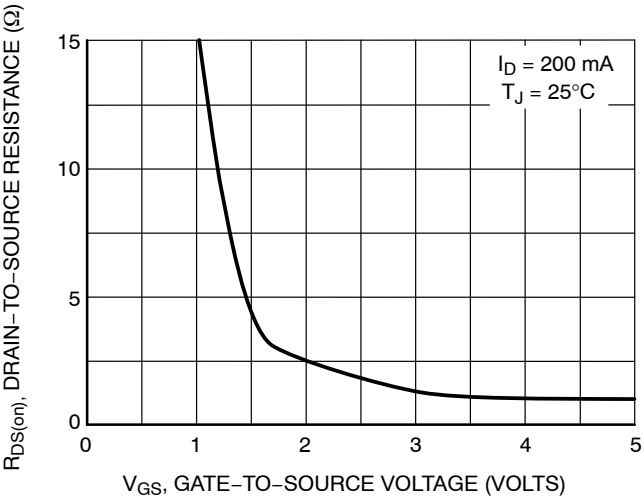


Figure 3. On–Resistance vs. Gate Voltage

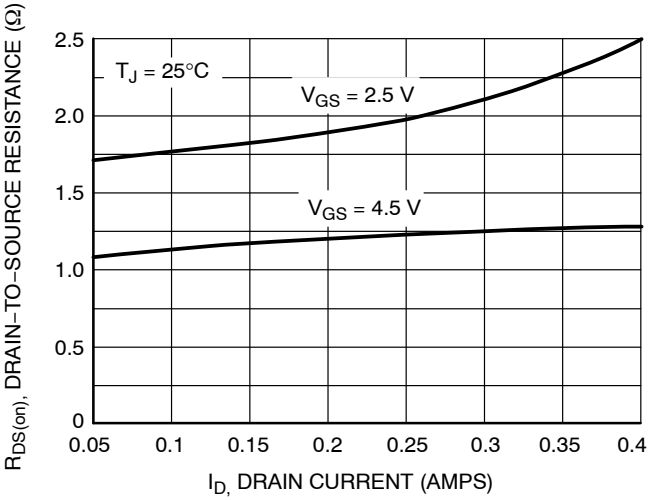


Figure 4. On–Resistance vs. Drain Current and Gate Voltage

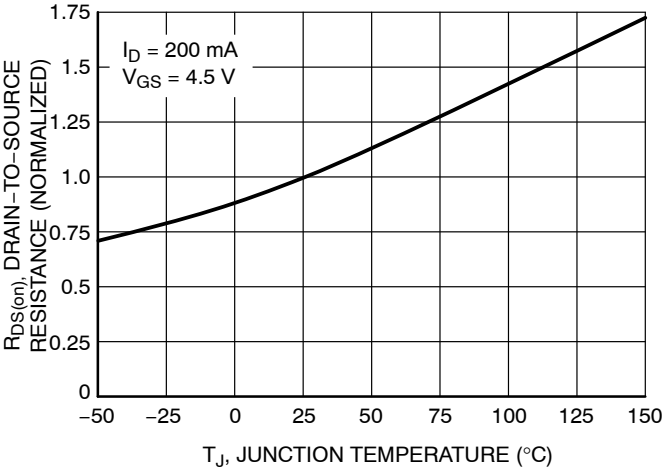


Figure 5. On–Resistance Variation with Temperature

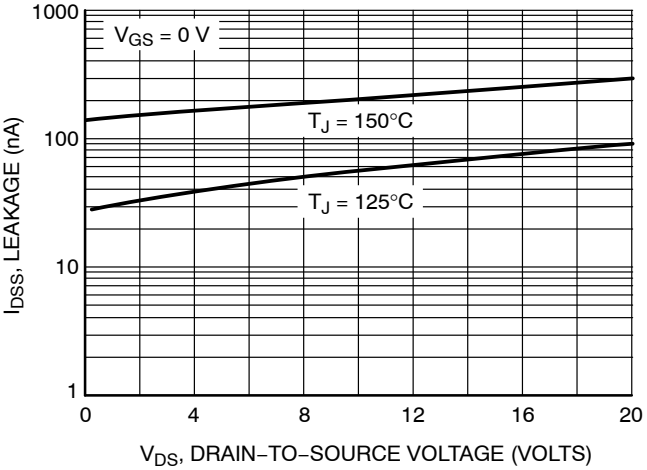


Figure 6. Drain–to–Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES – N–CHANNEL

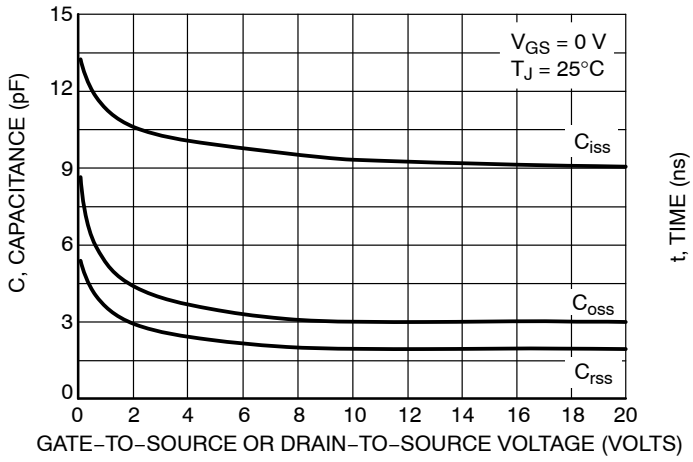


Figure 7. Capacitance Variation

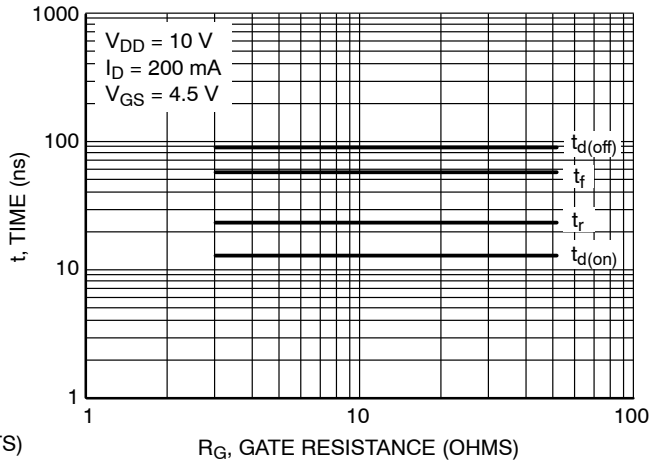


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

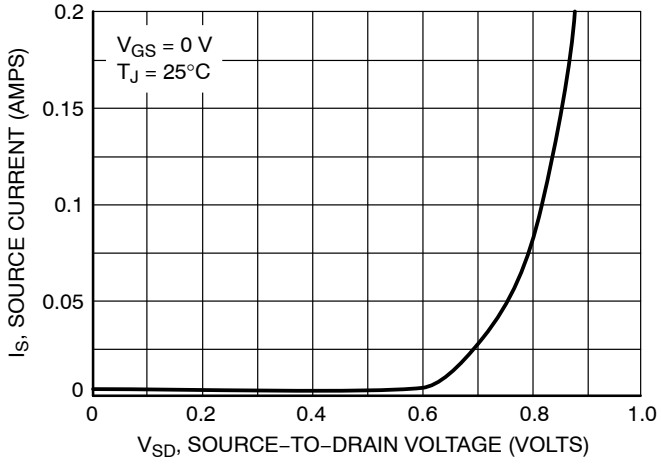


Figure 9. Diode Forward Voltage vs. Current

TYPICAL PERFORMANCE CURVES – P–CHANNEL

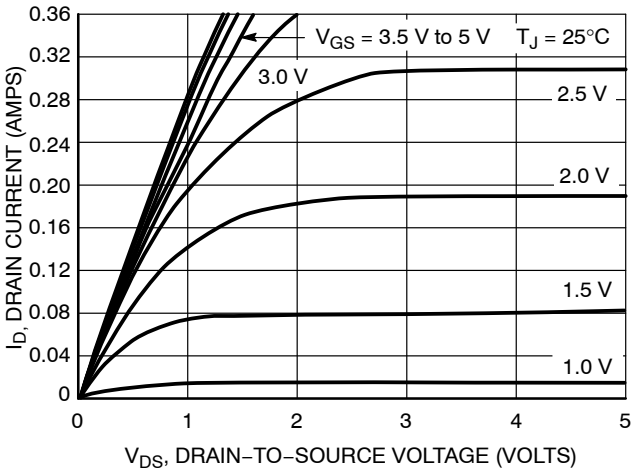


Figure 10. On–Region Characteristics

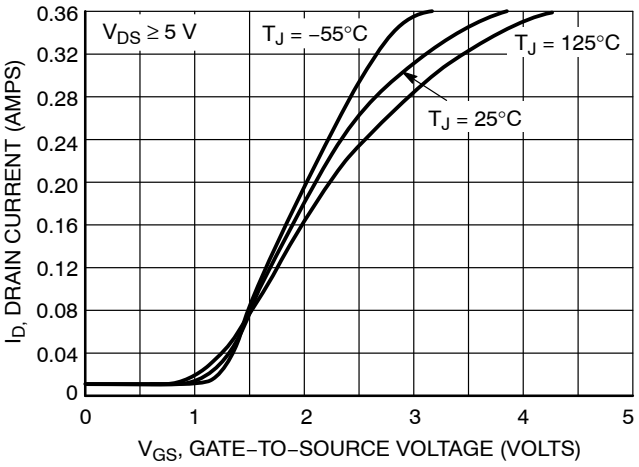


Figure 11. Transfer Characteristics

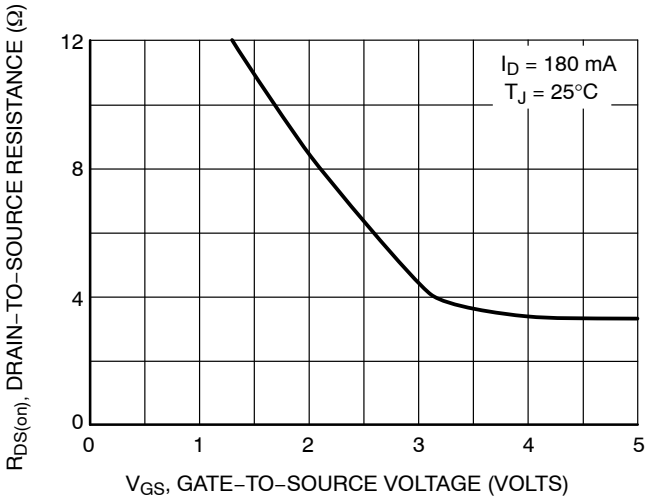


Figure 12. On–Resistance vs. Gate Voltage

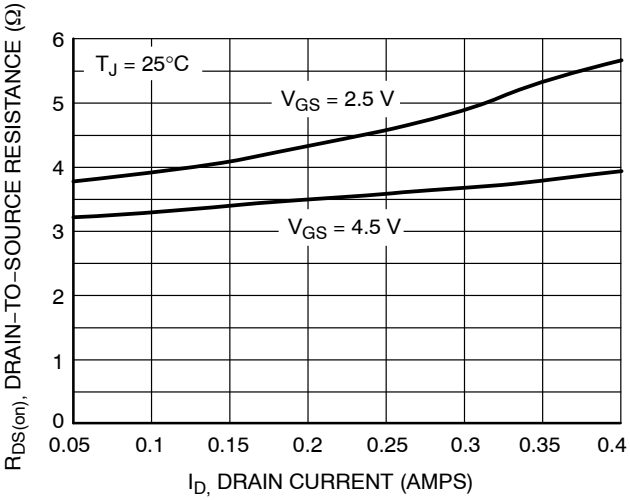


Figure 13. On–Resistance vs. Drain Current and Gate Voltage

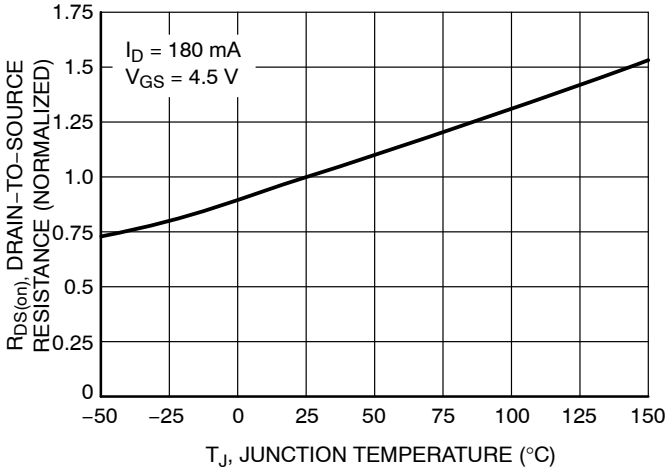


Figure 14. On–Resistance Variation with Temperature

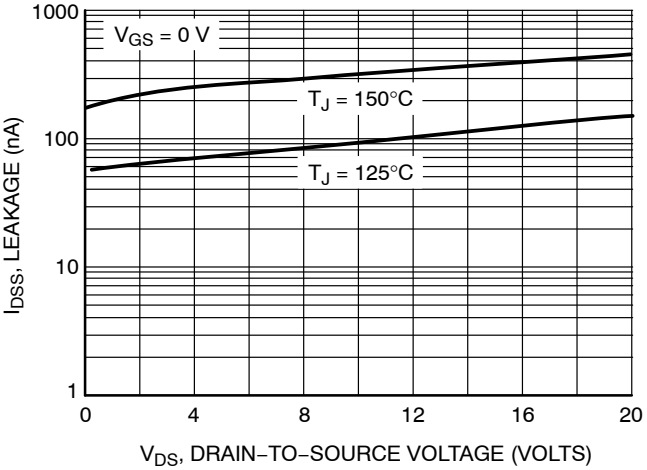


Figure 15. Drain–to–Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES – P–CHANNEL

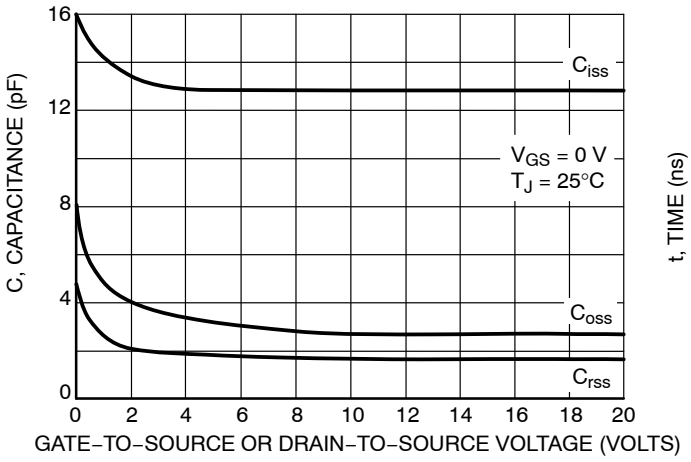


Figure 16. Capacitance Variation

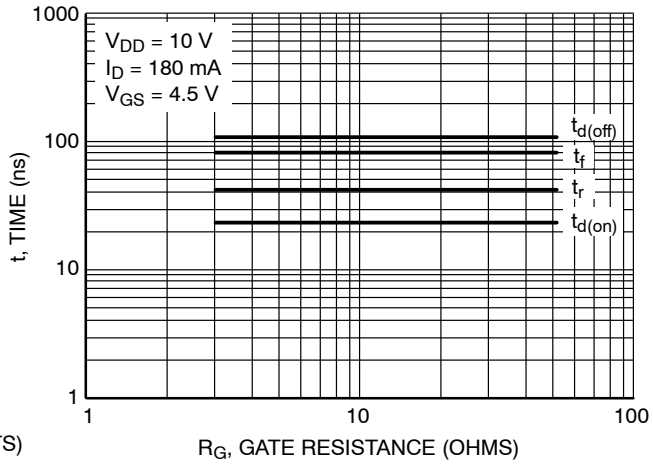


Figure 17. Resistive Switching Time Variation vs. Gate Resistance

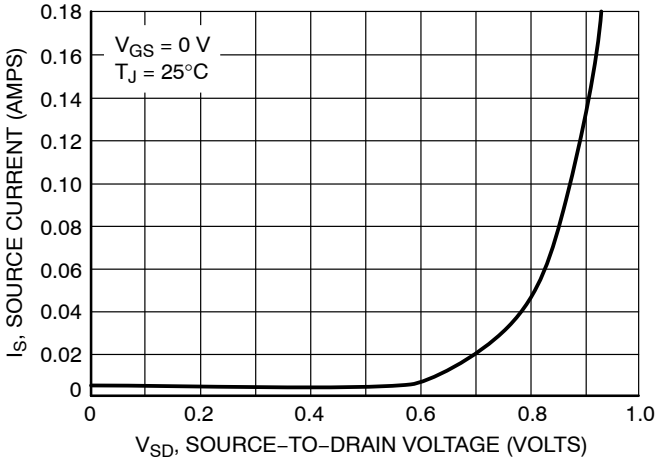
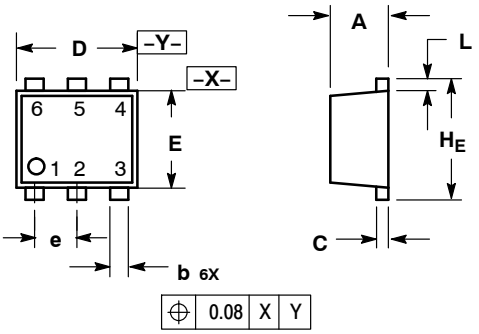


Figure 18. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

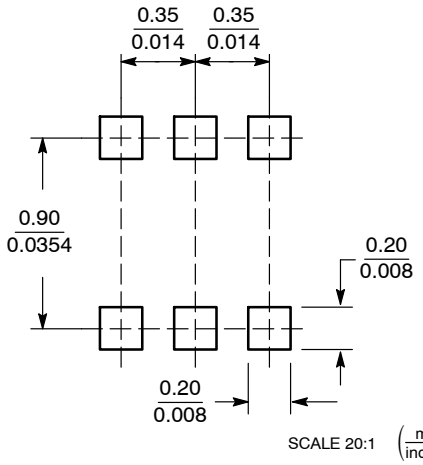
SOT−963
CASE 527AA−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.40	0.45	0.50	0.016	0.018	0.020
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.05	0.10	0.15	0.002	0.004	0.006
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
H_E	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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