

LPC802

Errata sheet LPC802

Rev. 1.5 — 25 September 2019

Errata sheet

Document information

Info	Content
Keywords	LPC802M001JDH16;LPC802M001JDH20;LPC802M011JDH20;LPC802M001JHI33; LPC802UK; LPC802 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.



Revision history

Rev	Date	Description
1.5	20190925	Added device revision (1D) and updated VDD.1 errata.
1.4	20190910	Updated device revision and VDD.1 errata.
1.3	20190604	Added VDD.1 errata
1.2	20180427	Added LPC802UK part.
1.1	20180313	- Updated Table 1 "Device revision table". - Updated work-around of Section 3.1 "DPD.1: Port pin PIO0_4 cannot be used to wake up the device from deep power-down mode.".
1.0	20171129	Initial version.

Contact information

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1. Product identification

The LPC802 HVQFN33 packages have the following top-side marking:

- First line: LPC802M0
- Second line: xxxx
- Third line: yywwx[R]
 - yyww: Date code with yy = year and ww = week.
 - xR = Boot code version and device revision.

The LPC802 TSSOP20 packages typically have the following top-side marking:

- First line: LPC802
- Second line: M0y1
 - y: 0 or 1
- Third line: xxxx
- Fourth line: xxywwx[R]
 - yyww: Date code with y = year and ww = week.
 - xR = Boot code version and device revision.

The LPC802 TSSOP16 packages have the following top-side marking:

- First line: LPC802
- Second line: M001J
- Third line: xxxx
- Fourth line: ywwx[R]
 - yyww: Date code with y = year and ww = week.
 - xR = Boot code version and device revision.

The LPC802 WLCSP16 packages have the following top-side marking:

- First line: LPC802
- Second line: xxxxx
- Third line: xyywwx[R]
 - yyww: Date code with ww = week and yy = year.
 - xR = Boot code version and device revision.
- Fourth line: xxx - yyy

Table 1. Device revision table

Revision identifier (R)	Revision description
0A	Initial device revision with Boot ROM version 13.0
1A	Second device revision with Boot ROM version 13.1
1B	Third device revision with Boot ROM version 13.1
1C	Fourth device revision with Boot ROM version 13.1
1D	Fifth device revision with Boot ROM version 13.1

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
DPD.1	Port pin PIO0_4 cannot be used to wake up the device from deep power-down mode.	0A, 1A	Section 3.1

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
VDD.1	The minimum rise time of the power supply ramp must be 1 ms or less.	0A, 1A, 1B, 1C	Section 4.1

Table 4. Errata notes

Note	Short description	Detailed description
n/a	n/a	n/a

3. Functional problems detail

3.1 DPD.1: Port pin PIO0_4 cannot be used to wake up the device from deep power-down mode.

Introduction:

On the LPC802, the following pins can be used as WAKEUP pins to wake up from deep power-down mode: PIO0_4, PIO0_8, PIO0_9, PIO0_10, PIO0_11, PIO0_13, PIO0_15, and PIO0_17.

Problem:

The PIO0_4 pin does not function properly and cannot be used to wake up the device from deep power-down mode. Other pins listed above are functional.

Work-around:

No work-around on device revisions 0A and 1A. This issue is fixed in device revision 1B.

4. AC/DC Deviation

4.1 VDD.1: The rise time of the power supply ramp must be 1 ms or below.

Problem:

The LPC802 device might not always start-up if the rise time of the power supply ramp on the VDD pin is 1 ms or above.

Work-around:

For device revisions 0A, 1A, 1B, and 1C, the rise time of power supply ramp must be 1 ms or below. This issue is fixed in device revision 1D.

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