
KSZ8863 Daughter Board Information Sheet

Abstract

The KSZ8863 Daughter Board (AC320004-7) enables Ethernet communication with a variety of Microchip starter kits. This information sheet provides an overview and a detailed schematic of the KSZ8863 Daughter Board.

This daughter board is designed specifically to be used with the PIC32 Ethernet Starter Kit II (DM320004-2) or the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Starter Kit (DM320007); however, it can also be used with other Microchip development hardware.

For additional information about the KSZ8863 Daughter Board, visit Microchip web site: <http://www.microchip.com>.

1 Features

The KSZ8863 Daughter Board features a 22-pin header for connecting the board into compatible PIC32 starter kits. The board has a KSZ8863 Ethernet Physical Layer Chip, configured to use RMII. The KSZ8863 Daughter Board is suitable for use with the PIC32 Ethernet Starter Kit II and PIC32MZ EF Starter Kit.

The following are features of the KSZ8863 Daughter Board:

- RMII interface with MDC/MDIO management interface for register configuration
- Fast start-up and link
- Loopback modes for diagnostics
- Integrated 3-Port 10/100 Managed Switch with PHYs
- IEEE 802.1q VLAN Support
- Optional SPI interface
- Compliant with IEEE 802.3u standard

2 Applications

- VoIP Phone
- Set-Top/Game Box
- Automotive
- Industrial Control
- IPTV POF
- SOHO Residential Gateway
- Broadband Gateway/Firewall/VPN
- Integrated DSL/Cable Modem

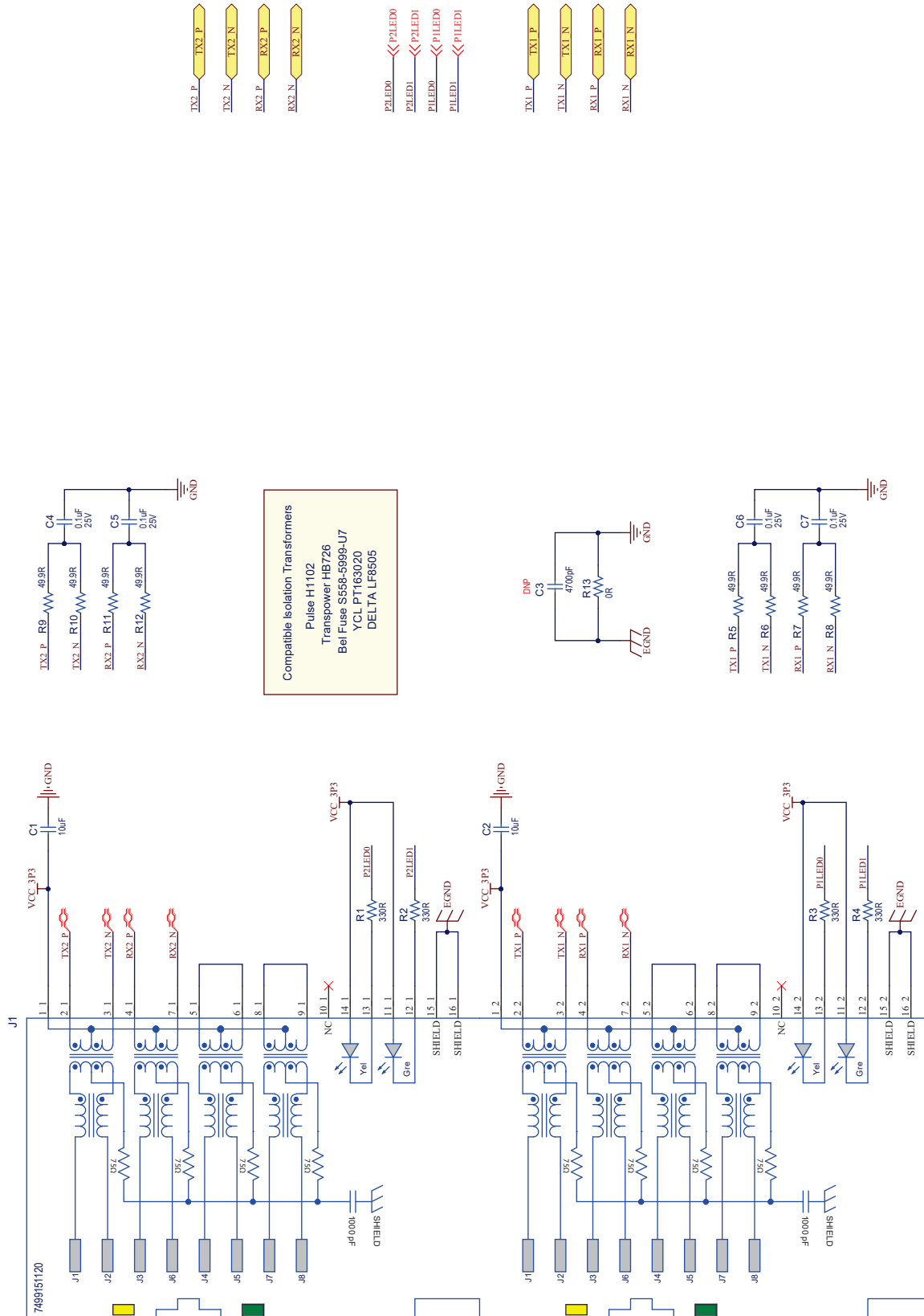
- Wireless LAN Access Point + Gateway
- Standalone 10/100 Switch

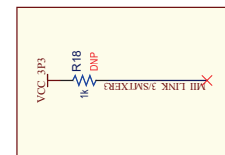
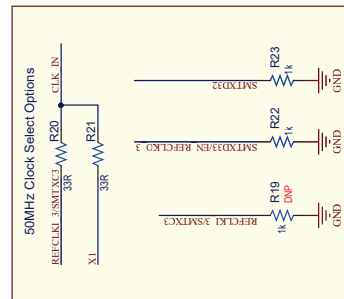
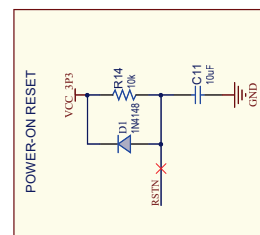
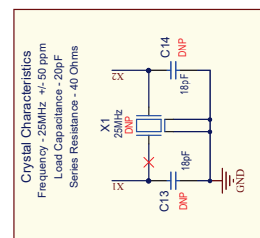
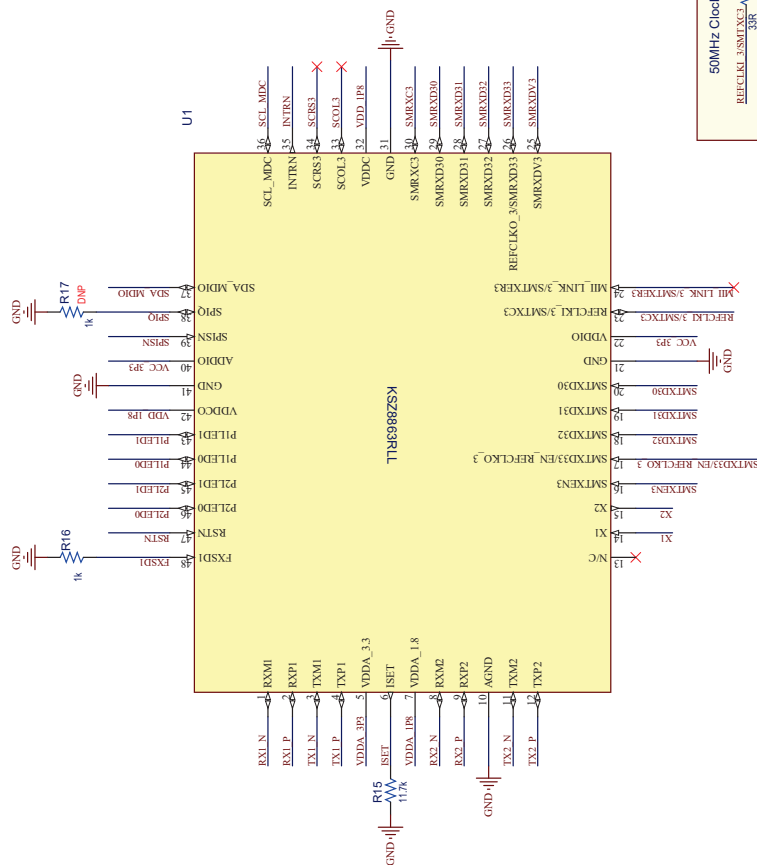
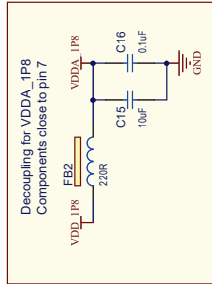
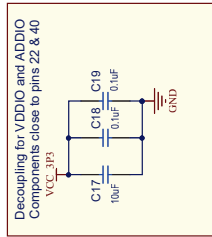
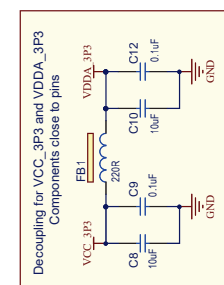
3 Additional Information

For additional information on drivers and examples, follow these links:

- <https://www.microchip.com/wwwproducts/en/KSZ8863>
- <http://www.microchip.com/mplab/mplab-harmony>

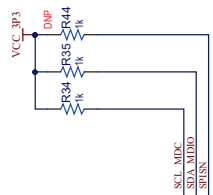
1. Schematics





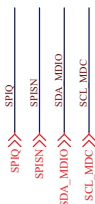
SPI Communication Option	
SPI SN	R44 = Placed
SPI Q	R24 = Placed

I2C Communication	
R34 & R35	Replace with 4.7k



Port Configuration Options

PORT 1 - OPTIONS		PORT 2 - OPTIONS	
SPIQ	Force Flow Control Placed = DISABLE	SMRXD30	Force Flow Control Placed = DISABLE
SMRXDV3	Force Full/Half Duplex DNP = FULL DUPLEX Placed = HALF DUPLEX	SMRXD31	Force Full/Half Duplex DNP = FULL DUPLEX Placed = HALF DUPLEX
P1LED1	Force Speed DNP = 100baseTX Placed = 10baseT	SMRXD32	Force Speed DNP = 100baseTX Placed = 10baseT
P1LED0	Auto-Negotiation DNP = ENABLE Placed = DISABLE	SMRXD33	Auto-Negotiation DNP = ENABLE Placed = DISABLE



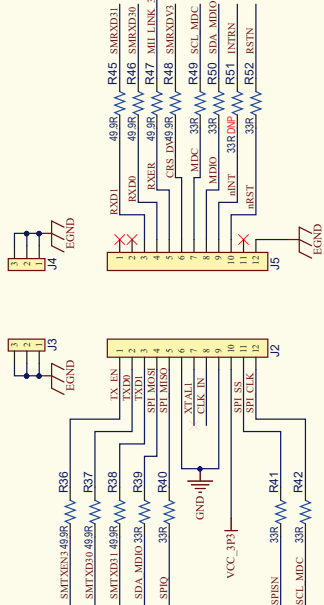
Bus Communication Configuration

Serial Bus Configuration	
[P2LED1, P2LED0]	I2C (master mode) EEPROM
[Placed Placed]	I2C Slave Mode
[Placed DNP]	SPI Slave Mode
[DNP, Placed]	SPI Mode
[DNP, DNP]	SPI Mode

Clock Source Configuration			
Reg[19:16] [3]	Pin 17 SMTXD33 (EN REFCLK0_3 Internal Pull-Up)	Pin 18 SMTXD32 (EN REFCLK0_3 Internal Pull-Up)	Note
0	0 (use 1k Pull-Down)	0 (use 1k Pull-Down)	External 50MHz OSC input to SMTXD33/REFCLK0_3 and XT pin directly to Disable REFCLK0_3 for better EMI
0	1 (use 1k Pull-Down)	0 (use 1k Pull-Down)	50MHz on XT pin is clock source. REFCLK0_3 is disabled. Output is connected to REFCLK0_3 externally to Enable REFCLK0_3
0	1	1	25MHz on XT pin is clock source. Output is connected to REFCLK0_3 externally to Enable REFCLK0_3
1	0	0 or 1	25MHz on XT pin is clock source. Output is connected to REFCLK0_3 internally to Enable REFCLK0_3 for better EMI

NOTE !!

Signals INTRN and RSTN, Pins 35 and 47 have
internal pull-up resistors integrated into the pad structure



2. Revision History

Revision B - March 2019

The following changes were implemented for this release:

- Updated the schematics:
 - Added the property and notation DNP to the resistor R51
- Updated document format

Revision A - June 2018

Initial release of this document.

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