User's Guide
SLUUBH5–November 2016

Using the Stacking TPS546C23 Two Phase Evaluation Module

The TPS546C23EVM2-746 evaluation module (EVM) is a two phase buck converter with two TPS546C23 devices. The TPS546C23 device is a stackable synchronous buck with PMBus interface that can operate from a nominal 4.5-V to 18-V supply. The device allows programming and monitoring via the PMBus interface.

Two TPS546C23 devices are configured as two phase buck converter in factory default, output current is evenly distributed in the two devices; both the negative and positive output terminals are connected together.

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Trademarks

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1 Description

The TPS546C23EVM2-746 is a two phase buck converter with two stacked TPS546C23 devices. It uses a nominal 12-V bus to produce a regulated 1.2-V output at up to 70 A of load current. The TPS546C23EVM2-746 is designed to demonstrate stacking operation of the TPS546C23 in a two phase low output voltage application while providing a number of test points to evaluate the performance of the devices. The TPS546C23EVM2-746 can be modified to two separated single phase buck converters by changing the components assembled. Refer to the TPS546C23 (SLUSCC7) datasheet for more information on single-phase configuration.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS546C23EVM2-746. Observe all safety precautions.

Warning The TPS546C23EVM2-746 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

Caution Do not leave the EVM powered when unattended.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the Battery- potential of the EVM.

1.2 Typical Applications

- High-density power solutions
- Wireless infrastructure
- Switcher
- Router Network
- Server
- Storage
- Smart power systems

1.3 Features

- Regulated 1.2-V output up to 70-A DC steady-state output current
- The output voltage is marginable and trimmable via the PMBus interface
  - Programmable UVLO, soft-start, and enable via the PMBus interface
  - Programmable overcurrent warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable overvoltage and undervoltage warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable turn-on and turn-off delays
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 1 lists the electrical performance specifications under room temperature 25°C.

Table 1. TPS546C23EVM2-746 Electrical Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input Characteristics					
Voltage range	V_{IN}	5	12	18	V
Maximum input current	V_{IN} = 12 V, I_O = 70 A		8.5		A
No load input current	V_{IN} = 12 V, I_O = 0 A		120		mA
Output Characteristics					
Output voltage, V_{OUT}			1.2		V
Output load current, I_{OUT} (1)		0		70	A
Output voltage regulation	Line Regulation: Input voltage = 5 V to 18 V		1%		
	Load Regulation: Output current = 0 A to 70 A		1%		
Output voltage ripple, V_{OUT}	V_{IN} = 12 V, I_{OUT} = 70 A		10		mVpp
Output Over-current Protection Threshold	Load current I_{OUT1}, default setting of U1		42		A
	Load current I_{OUT2}, default setting of U2		42		A
Systems Characteristics					
Switching frequency	V_{IN} = 12 V		500		kHz
Full load efficiency, V_{OUT} (2)	V_{IN} = 12 V, I_{OUT} = 70 A,		86%		
Operating temperature	$T_{ambient}$		25		°C
PMBUS Interface and Pin-Strapping					
U1 PMBUS Address	Programmed by R_{33} and R_{35}		27		Decimal
U2 PMBus Address	Programmed by R_{37} and R_{36}		36		
U1 Voltage reference	Default setting of VOUT_COMMAND		600		mV
U2 Voltage reference	Default setting of VOUT_COMMAND		600		
U1 Soft-start time (TON_RISE)	Default setting of TON_RISE		3		ms
U2 Soft-start time (TON_RISE)	Default setting of TON_RISE		3		

(1) The output current I_{OUT} can be up to 80 A, if the output overcurrent limit (IOUT_OC_FAULT_LIMIT) is set to 45 A.
(2) The efficiency is measured based on Figure 2 and test setups, which includes power loss caused by on board copper traces.

3 Schematic

Figure 1 illustrates the TPS546C23EVM2-746 EVM schematic.

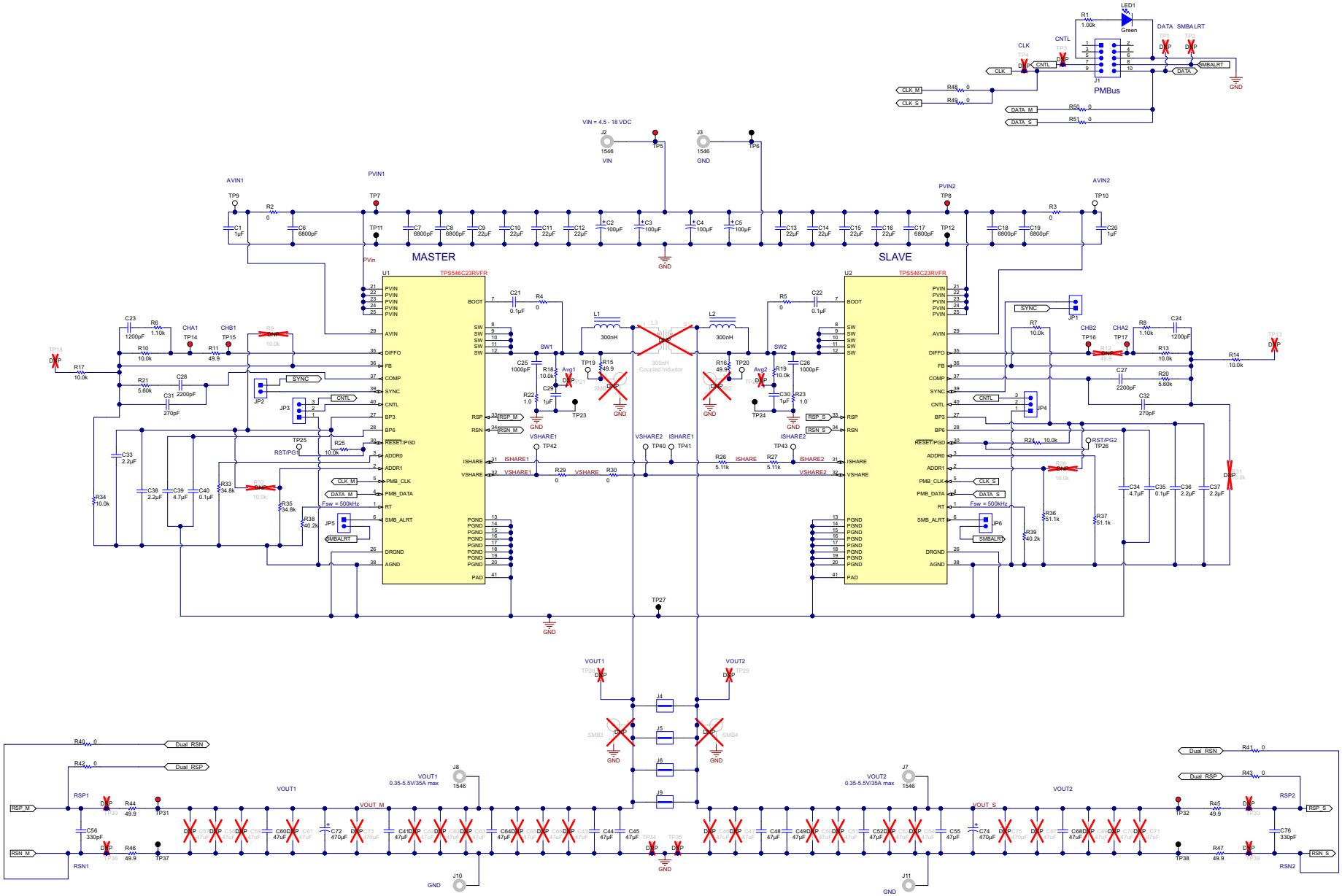


Figure 1. TPS546C23EVM2-746 Schematic

4 Test Setup

4.1 Test and Configuration Software

In order to change any of the default configuration parameters on the EVM, it is necessary to obtain the TI Fusion Digital Power Designer software.

4.1.1 Description

The Fusion Digital Power Designer is the graphical user interface (GUI) used to configure and monitor the Texas Instruments TPS546C23 power converter installed on this evaluation module. The application uses the PMBus protocol to communicate with the controller over serial bus by way of a TI USB adapter. This adapter can be purchased at http://www.ti.com/tool/usb-to-gpio. (see).

4.1.2 Features

Some of the tasks you can perform with the GUI include:

- Turn on or off the power supply output, either through the hardware control line or the PMBus operation command.
- Monitor real-time data. Items such as output voltage, output current, die temperature, warnings and faults which are continuously monitored and displayed by the GUI.
- Configure common operating characteristics such as V_{OUT} trim and margin, UVLO, soft-start time, warning and fault thresholds, fault response, and ON/OFF modes.

This software is available for download at this location:
http://www.ti.com/tool/fusion_digital_power_designer

4.2 Test Equipment

4.2.1 Voltage Source

The input voltage source V_{IN} should be a 0-V to 20-V variable DC source capable of supplying 25 ADC. Connect input VIN and GND to J2 and J3 as shown in Figure 2 and .

4.2.2 Multimeters

It is recommended to use two separate multi-meters as shown in Figure 2 and . One meter to measure V_{IN}, the other to measure V_{OUT}.

4.2.3 Output Load:

A variable electronic load is recommended for the test setup as shown in Figure 2 or . The load should be capable of 80 A.

4.2.4 Oscilloscope

An oscilloscope is recommended for measuring output noise and ripple. Output ripple should be measured using a *Tip-and-Barrel* method or better as shown in Figure 3.

4.2.5 Fan:

During prolonged operation at high loads, it may be necessary to provide forced air cooling with a small fan aimed at the EVM. The surface temperature of the devices on the EVM should be maintained below 105°C.

4.2.6 USB-to-GPIO Interface Adapter:

A communications adapter is required between the EVM and the host computer. This EVM was designed to use the Texas Instruments USB-to-GPIO Adapter, see . This adapter can be purchased here:
http://www.ti.com/tool/usb-to-gpio.

4.2.7 Recommended Wire Gauge

- Input VIN and GND to J2 and J3 (GND) (12-V input) – The recommended wire size is AWG #12, with the total length of wire less than 2 feet (1 feet input, 1 feet return).
- Output J8/J7 and GND J10/J11 (0.9-V output) – The minimum recommended wire size is AWG #10, with the total length of wire less than 2 feet (1 feet OUTPUT, 1 feet return).

4.3 Recommended Test Setup

Figure 2 and shows the recommended test setup.

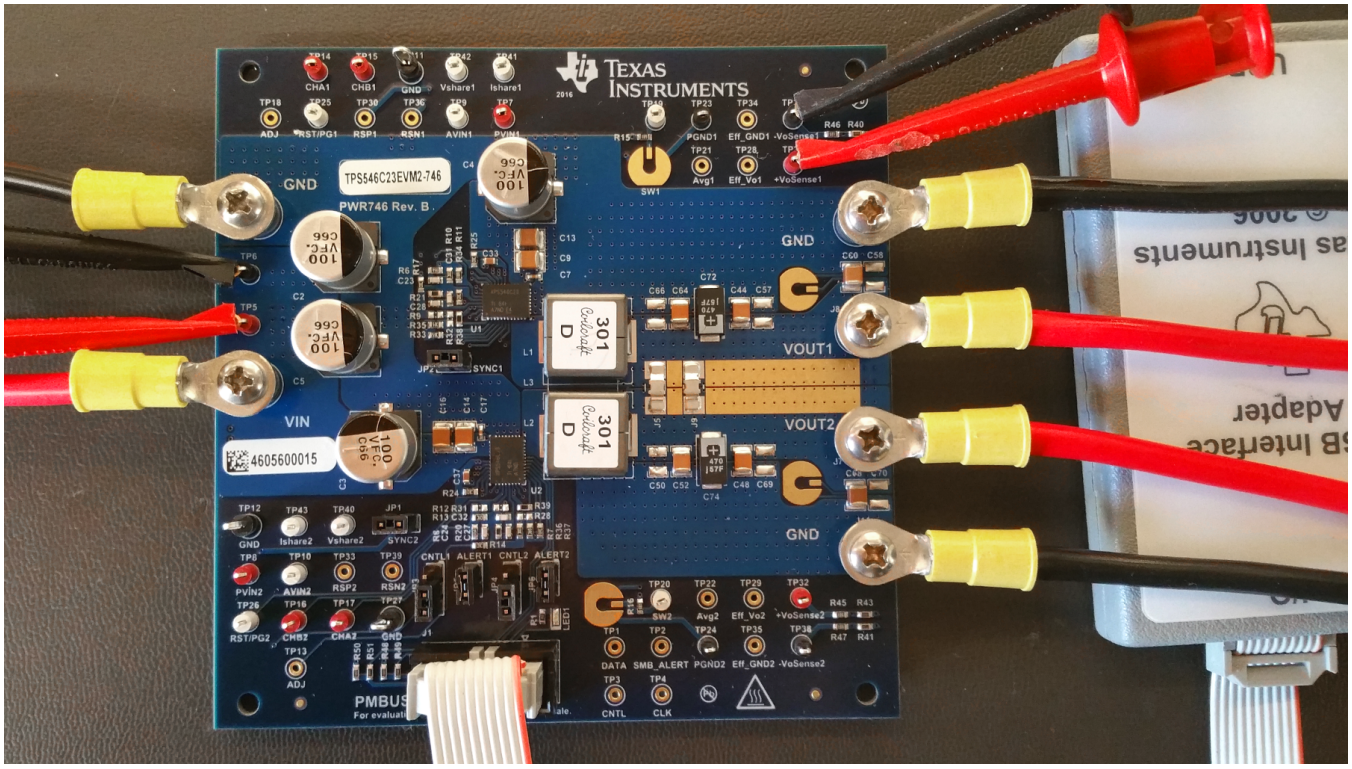
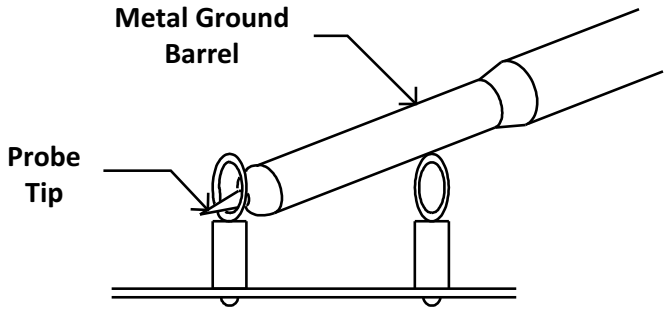


Figure 2. TPS546C23EVM2-746 EVM Recommended Test Set Up

Figure 3 illustrates the tip and barrel measurement for switching node waveform on TP19 with TP23 or TP20 with TP24.



Tip and Barrel V_{OUT} Ripple Measurement

Figure 3. Tip and Barrel Measurement

4.4 List of Test Points, Jumpers and Connectors

Table 2 lists the test point functions.

Table 2. Test Point Functions

Test Point	Type	Name	Description
TP1	Not Assembled	DATA	DATA signal on J1 socket
TP2	Not Assembled	SMB_ALERT	SMBALERT signal on J1 socket
TP3	Not Assembled	CNTL	CNTL signal on J1 socket
TP4	Not Assembled	CLK	CLK signal on J1 socket
TP5	T-H Loop	VIN	V_{IN}+ measurement point
TP6	T-H Loop	GND	V_{IN}- measurement point
TP7	T-H Loop	PVIN1	PVIN pin voltage of U1 device measurement point
TP8	T-H Loop	PVIN2	PVIN pin voltage of U2 device measurement point
TP9	T-H Loop	AVIN1	AVIN pin voltage of U1 device measurement point
TP10	T-H Loop	AVIN2	AVIN pin voltage of U2 device measurement point
TP11	T-H Loop	GND	GND reference
TP12	T-H Loop	GND	GND reference
TP13	Not Assembled	ADJ	Analog input to adjust rail 2 output voltage
TP14	T-H Loop	CHA1	Input for small signal loop gain measurements for output rail 1 (B/A setup)
TP15	T-H Loop	CHB1	OUTPUT for small signal loop gain measurements for output rail 1 (B/A setup)
TP16	T-H Loop	CHB2	OUTPUT for small signal loop gain measurements for output rail 2 (B/A setup)
TP17	T-H Loop	CHA2	Input for small signal loop gain measurements for output rail 2 (B/A setup)
TP18	Not Assembled	ADJ	Analog input to adjust rail 1 output voltage
TP19	T-H Loop	SW1	Switching node of output rail 1 measurement point, reference to TP23
TP20	T-H Loop	SW2	Switching node of output rail 2 measurement point, reference to TP24
TP21	Not Assembled	AVG1	Rail 1 switching node average voltage measurement point, reference to TP23
TP22	Not Assembled	AVG2	Rail 2 switching node average voltage measurement point, reference to TP24
TP23	T-H Loop	PGND1	GND reference for switching node measurement
TP24	T-H Loop	PGND2	GND reference for switching node measurement
TP25	T-H Loop	RST/RG1	PGOOD signal of output 1
TP26	T-H Loop	RST/PG2	PGOOD signal of output 2
TP27	T-H Loop	GND	GND reference
TP28	Not Assembled	EFF_VO1	U1 output voltage measurement point for efficiency, reference to TP34
TP29	Not Assembled	EFF_VO2	U2 output voltage measurement point for efficiency, reference to TP35
TP30	Not Assembled	RSP1	Output 1 remote sense + voltage point
TP31	T-H Loop	+VOSENSE1	V_{OUT1}+ measurement point
TP32	T-H Loop	+VOSENSE2	V_{OUT2}+ measurement point
TP33	Not Assembled	RSP2	Output 2 remote sense + voltage point
TP34	Not Assembled	EFF_GND1	Rail 1 output voltage referencing GND for efficiency measurement
TP35	Not Assembled	EFF_GND2	Rail 1 output voltage referencing GND for efficiency measurement
TP36	Not Assembled	RSN1	Output 1 remote sense - voltage point
TP37	T-H Loop	–VOSENSE1	V_{OUT1}– measurement point
TP38	T-H Loop	–VOSENSE2	V_{OUT2}– measurement point
TP39	Not Assembled	RSN2	Output 2 remote sense - voltage point
TP40	T-H Loop	Vshare2	VSHARE of U2 measurement point.Sensitive signal.
TP41	T-H Loop	Ishare1	ISHARE of U1 measurement point.Sensitive signal.
TP42	T-H Loop	Vshare1	VSHARE of U1 measurement point.Sensitive signal.
TP43	T-H Loop	Ishare2	ISHARE of U2 measurement point. Sensitive signal.

Table 3 lists the EVM jumpers.

Table 3. Jumpers

Jumper	Type	Name	Description
JP1	Header, 100 mil, 2x1	SYNC2	Synchronization connection between U1 and U2. Jumper is plugged as default.
JP2	Header, 100 mil, 2x1	SYNC1	Synchronization connection between U1 and U2. Jumper is plugged as default.
JP3	Header, 100 mil, 3x1	CNTL1	PMBUS CNTL connection options for U1 to socket J1 or GND. Jumper connecting U1 to J1 is plugged as default.
JP4	Header, 100 mil, 3x1	CNTL2	PMBUS CNTL connection options for U2 to socket J1 or GND. Jumper connecting U2 to J1 is plugged as default.
JP5	Header, 100 mil, 2x1	ALERT1	PMBUS SMBALERT connection between U1 and socket J1. Jumper connecting U1 to J1 is plugged as default.
JP6	Header, 100 mil, 2x1	ALERT2	PMBUS SMBALERT connection between U2 and socket J1. Jumper connecting U2 to J1 is plugged as default.

Table 4 lists the EVM connector functions.

Table 4. Connector Functions

Connector	Type	Name	Description
J1	Header, 100mil, 5x2	PMBUS	PMBUS socket for TI FUSION adaptor
J2	Keystone 1546	VIN	VIN+ connector
J3	Keystone 1546	GND	VIN- (GND) connector
J8	Keystone 1546	VOUT1	VOUT1+ connector
J10	Keystone 1546	GND	VOUT1- connector
J7	Keystone 1546	VOUT2	VOUT2+ connector
J11	Keystone 1546	GND	VOUT2- connector

5 EVM Configuration Using the Fusion GUI

The TPS546C23 on this EVM leave the factory pre-configured. See Table 5 for a short list of key factory configuration parameters as obtained from the configuration file.

Table 5. Key Factory Configuration Parameters

ADDRESS HEX	ADDRESS DEC	PART ID	DESIGNATOR	
0x33	27	TPS546C23	U1	
0x44	36	TPS546C23	U2	
GENERAL				
CMD Code	CMD CODE HEX	ENCODED HEX	DECODED	COMMENTS
VIN_OFF	0x36	0xF010	4.0 V	Turn OFF voltage
VIN_ON	0x35	0xF012	4.5 V	Turn ON voltage
IOUT_CAL_OFFSET	0x39	0xE000	0.0000 A	Current offset for PMBUS readout
IOUT_OC_FAULT_LIMIT	0x46	0xF854	42 A	OC fault level
IOUT_OC_FAULT_RESPONSE	0x47	0xFF	Restart	Response to OC fault
IOUT_OC_WARN_LIMIT	0x4A	0xF84A	37 A	OC warning level
VOUT_COMMAND	0x21	0x0133	0.6 V	Reference voltage
VOUT_MIN	0x2B	00B3h	0.35V	minimum reference voltage
VOUT_MAX	0x24	0x034D	1.65 V	maximum reference voltage
VOUT_TRANSITION_RATE	0x27	0xD03C	1 mV/us	Vout transition rate
VOUT_SCALE_LOOP	0x29	0xF004	1	Output sense scaling ratio for main control loop
PCT_OV_UV_WRN_FLT_LIMITS	0xD6	0x00	UV FAULT 83% UV WARN 88% OV WARN 112% OV FAULT 117%	Output OV/UV Settings, reference to nominal reference voltage.
VOUT_OV_FAULT_RESPONSE	0x41	0xBF	Restart	Output overvoltage fault response
VOUT_UV_FAULT_RESPONSE	0x45	0xBF	Restart	Output undervoltage fault response
ON_OFF_CONFIG	0x02	0x16	CNTL only, Active High.	Control signal and operation command
OPERATION	0x01	0x00	Operation is not used to enable regulation	Can be used to control device On/Off
OT_FAULT_LIMIT	0x4F	0x0091	145°C	OT fault level
OT_WARN_LIMIT	0x51	0x0078	120°C	OT warn level
OT_FAULT_RESPONSE	0x50	0x3F	Ignore	Response to over temperature faults
TON_DELAY	0x60	0x0000	0 ms	Turn-on delay
TON_RISE	0x61	0x0003	3 ms	Soft-start time
TON_MAX_FAULT_LIMIT	0x62	0x0000	Disabled	Upper limit for Vout reaching regulation
TOFF_DELAY	0x64	0x0000	0 ms	Turn-off delay
TOFF_FALL	0x65	0x0000	0 ms	Soft-stop fall time

If it is desired to configure the EVM to settings other than the factory settings shown above, the TI Fusion Digital Power Designer software can be used for reconfiguration. It is necessary to have input voltage applied to the EVM prior to launching the software so that the TPS546C23 may respond to the GUI and the GUI can recognize the device. The default configuration for the EVM is to start converting at an input voltage of 4.5V, therefore to avoid any converter activity during configuration, an input voltage less than 4.5 V should be applied. An input voltage of 4 V is recommended.

5.1 Configuration Procedure

1. Adjust the input supply to provide 4 VDC, current limited to 1 A.
2. Apply the input voltage to the EVM. Refer to Figure 2 for connections and test setup.
3. Launch the Fusion GUI software. Refer to the screenshots in Section 10 for more information.
4. Configure the EVM operating parameters as desired.

By default, U1 is configured as loop master, U2 is configured as loop slave, PMBUS address for U1 is 27 decimal and for U2 is 36 decimal.

Both device can be configured or monitored through PMBUS interface at different address.

6 Test Procedure

6.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as described in Figure 2.
2. Ensure the electronic loads is set to draw 0 Adc.
3. Increase V_{IN} from 0 V to 12 V using voltage meter to measure input voltage.
4. Use the other voltage meter to measure output voltage V_{OUT}.
5. Vary the load from 0 to 70 Adc. V_{OUT} should remain in regulation as defined in Table 1.
6. Vary V_{IN} from 5 V to 18 V. V_{OUT} should remain in regulation as defined in Table 1.
7. Decrease the load to 0 A.
8. Decrease V_{IN} to 0 V.

6.2 Control Loop Gain and Phase Measurement Procedure

The TPS546C23EVM2-746 EVM includes a 49.9-Ω series resistor in the feedback loop for V_{OUT} . The resistor is accessible at the test points TP14 / TP15 for loop response analysis. These test points should be used during loop response measurements as the perturbation injecting points for the loop . See the description in Table 6.

Table 6. List of Test Points for Loop Response Measurements

Test Point	Node Name	Description	Comment
TP14	CHA1	Input to feedback divider of V_{OUT}	The amplitude of the perturbation at this node should be limited to less than 30 mV
TP15	CHB1	Resulting output of V_{OUT}	Bode can be measured by a network analyzer with a CH-B/CH-A configuration

Measure only one output at a time, with the following procedure:

1. Set up the EVM as described in Figure 2.
2. For V_{OUT}, connect the network analyzer's isolation transformer from TP14 to TP15,
3. Connect the input signal measurement probe to TP14. Connect the output signal measurement probe to TP15.
4. Connect the ground leads of both probe channels to TP11.
5. On the network analyzer, measure the Bode as TP15/TP14 (Out/In).

6.3 Efficiency Measurement

In order to evaluate the efficiency of the power train (device and inductor), it is important to measure the voltages at the correct location. This is necessary because otherwise the measurements will include losses that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, which should not be included in efficiency measurements.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

Table 7 shows the measurement points for input voltage and output voltage. VIN and VOUT are measured to calculate the efficiency. Using these measurement points will result in efficiency measurements that excluded losses due to the connectors and PCB traces.

Table 7. Test Points for Better Efficiency Measurements

Test Point	Node Name	Description	Comment
VOUT			
TP7	PVIN1	Input voltage measurement point for VIN1+	The pair of test points are connected to the PVIN/GND pins of U1. The voltage drop between input terminal to the device pins is excluded for efficiency measurement.
TP23	PGND1	Input voltage measurement point for VIN1- (GND)	
TP28	Eff_Vo1	Output voltage measurement point for VOUT1+	The pair of test points are connected to the closest points of Vout /GND to the inductor. The voltage drop from the output point of inductor to the output terminals is excluded for efficiency measurement.
TP34	Eff_GND1	Output voltage measurement point for VOUT1- (GND)	

7 Performance Data and Typical Characteristic Curves

Figure 4 through Figure 17 present typical performance curves for the TPS546C23EVM2-746 .

7.1 Efficiency

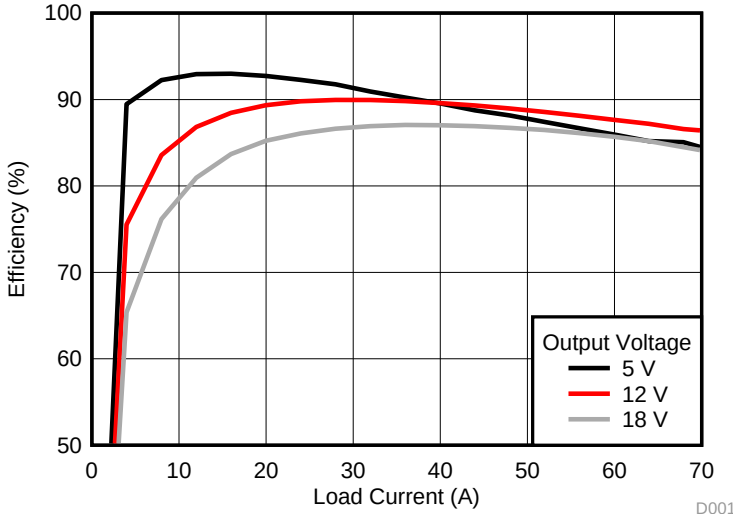


Figure 4. Efficiency of 1.2-V Output vs Line and Load

7.2 Load Regulation

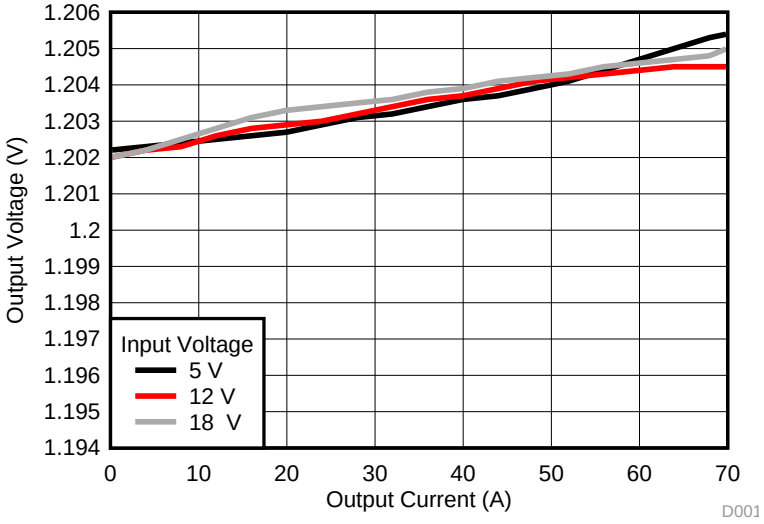


Figure 5. Load Regulation of 1.2-V Output

7.3 Line Regulation

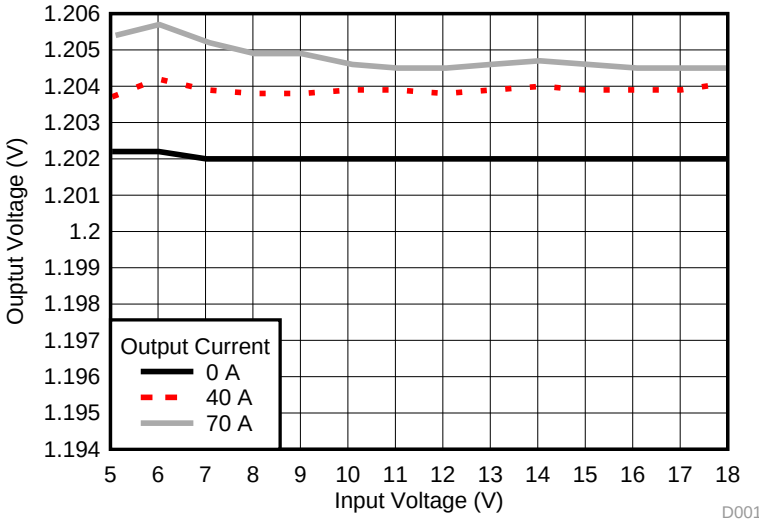
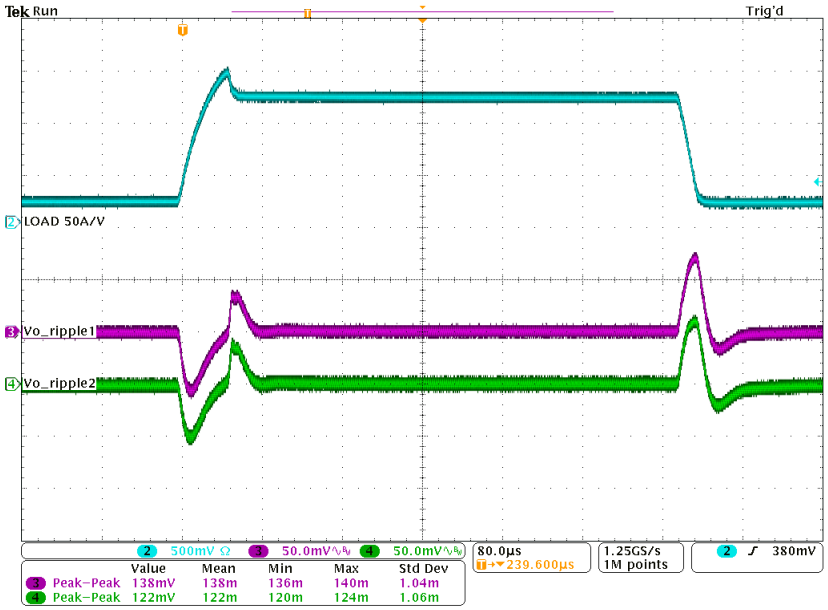


Figure 6. Line Regulation of 1.2-V Output (Different Board)

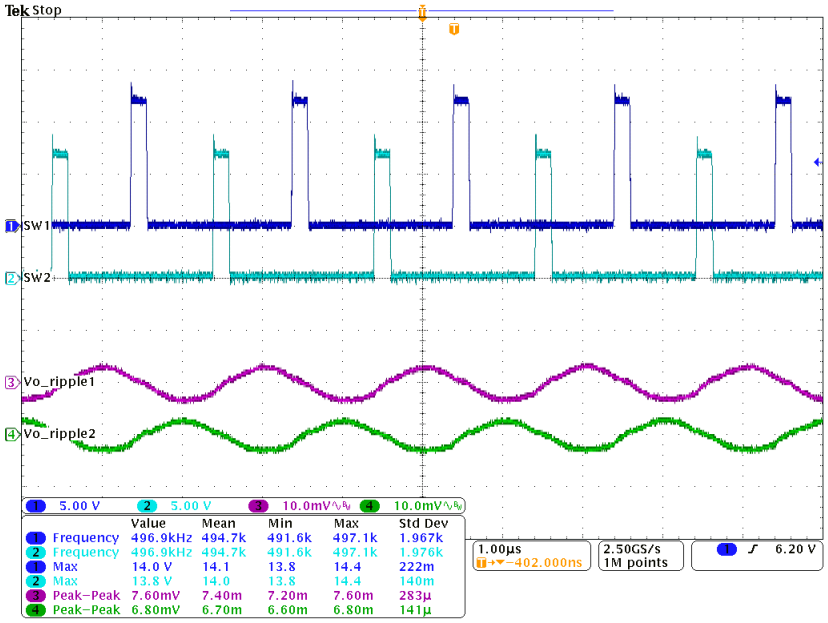
7.4 Transient Response



Ch1 = I_{OUT} at 25 A/division, Ch3 = V_{OUT} (AC coupled, measured at U1 side) at 50 mV/division, Ch4 = V_{OUT} (AC coupled, measured at U2 side) at 50 mV/division

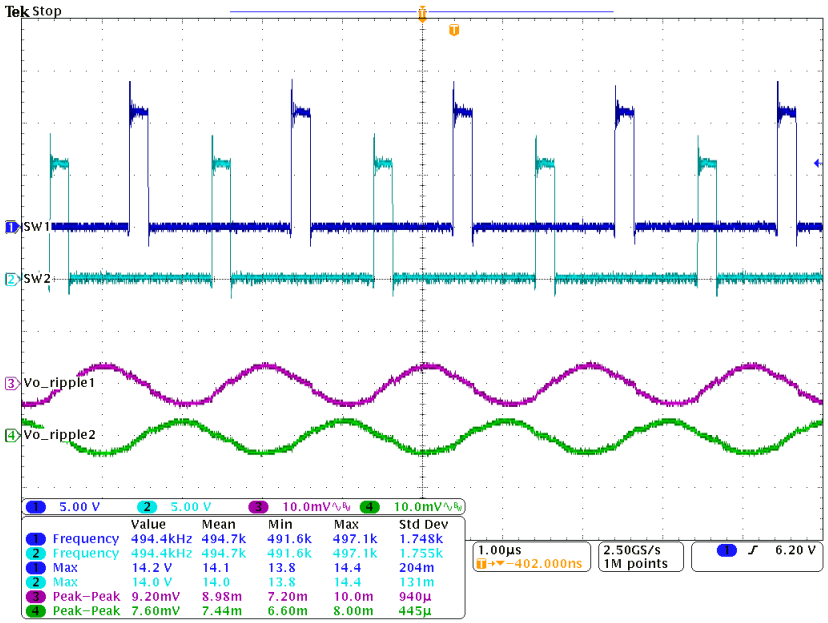
Figure 7. Transient Response of 1.2-V Output at 12 V_{IN}, Transient is 10 A to 60 A, 0.2 A/µs

7.5 Output Ripple



Ch1 = V_{SW1} at 5 V/division, Ch2 = V_{SW2} at 5 V/division, Ch3 = V_{OUT} (AC coupled, measured at U1 side) ripple at 10 mV/division, Ch4 = V_{OUT} (AC coupled, measured at U2 side) ripple at 10 mV/division

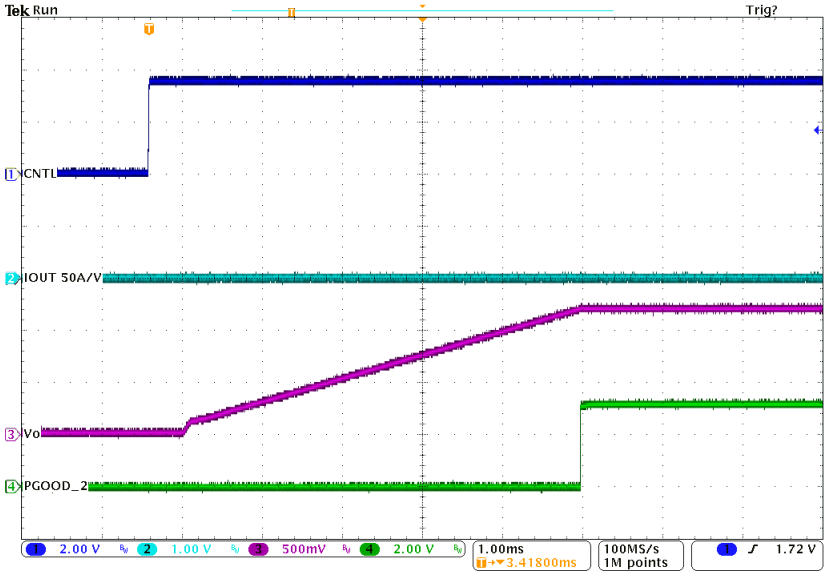
Figure 8. Output Ripple and SW Node of 1.2-V Output at 12 V_{IN}, 0-A Output



Ch1 = V_{SW1} at 5 V/division, Ch2 = V_{SW2} at 5 V/division, Ch3 = V_{OUT} (AC coupled, measured at U1 side) ripple at 10 mV/division, Ch4 = V_{OUT} (AC coupled, measured at U2 side) ripple at 10 mV/division

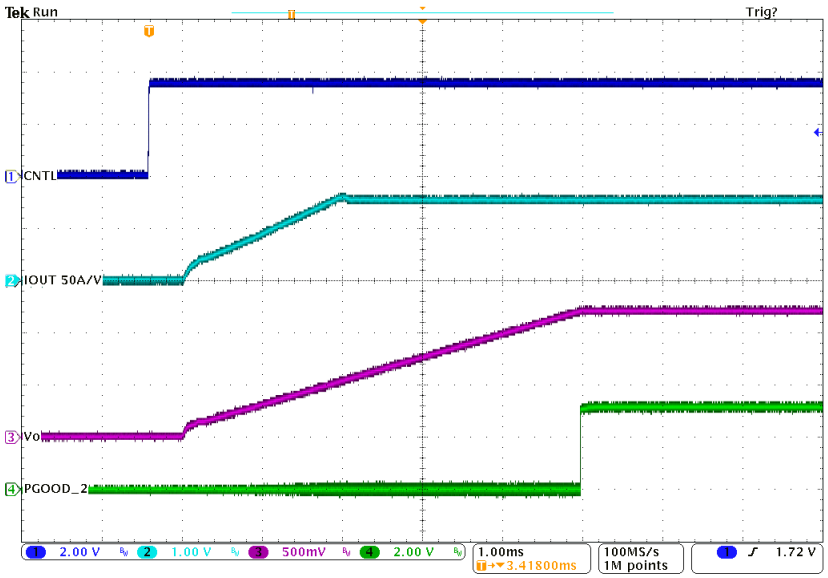
Figure 9. Output Ripple and SW Node of 1.2-V Output at 12 V_{IN}, 70-A Output

7.6 Control On



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

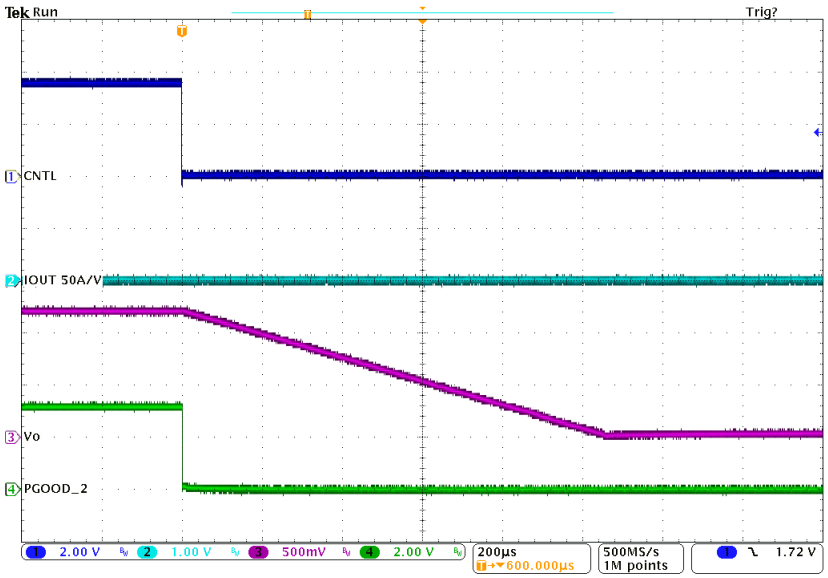
Figure 10. Start up from Control, 1.2-V Output at 12 V_{IN}, 0-A Output (TON_RISE is modified to 5ms)



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

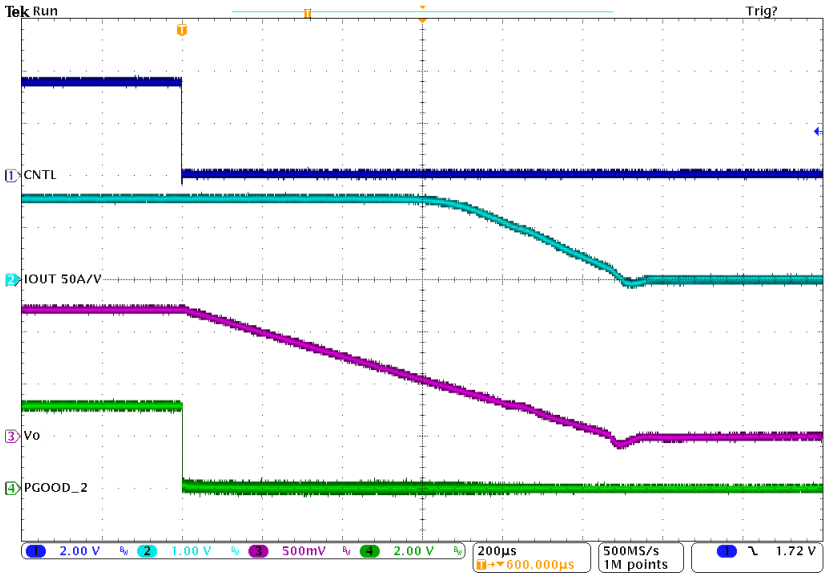
Figure 11. Start up from Control, 1.2-V Output at 12 V_{IN}, 70-A Output (TON_RISE is modified to 5ms)

7.7 Control Off



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

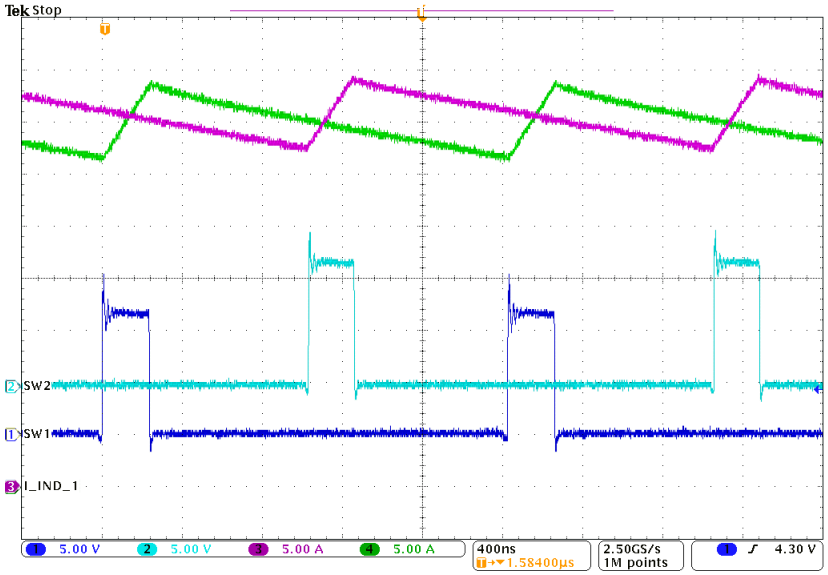
Figure 12. Soft Stop from Control, 1.2-V Output at 12 V_{IN}, 0-A Output (TON_RISE is modified to 5ms)



Ch1 = CNTL at 2 V/division, Ch2 = I_{OUT} at 50 A/division, Ch3 = V_{OUT} at 500 mV/division, Ch4 = PGOOD at 2 V/division

Figure 13. Soft Stop from Control, 1.2-V Output at 12 V_{IN}, 70-A Output (TON_RISE is modified to 5ms)

7.8 Current Sharing between two phases



Ch1 = V_{SW1} at 5 V/division, Ch2 = V_{SW2} at 5 V/division, Ch3 = I_{L2} at 5 A/division, Ch4 = I_{L1} at 5 A/division

Figure 14. Inductor Current and Switch Node Waveform, 1.2-V Output at 12 V_{IN}, 70-A Output

7.9 Control Loop Bode Plot

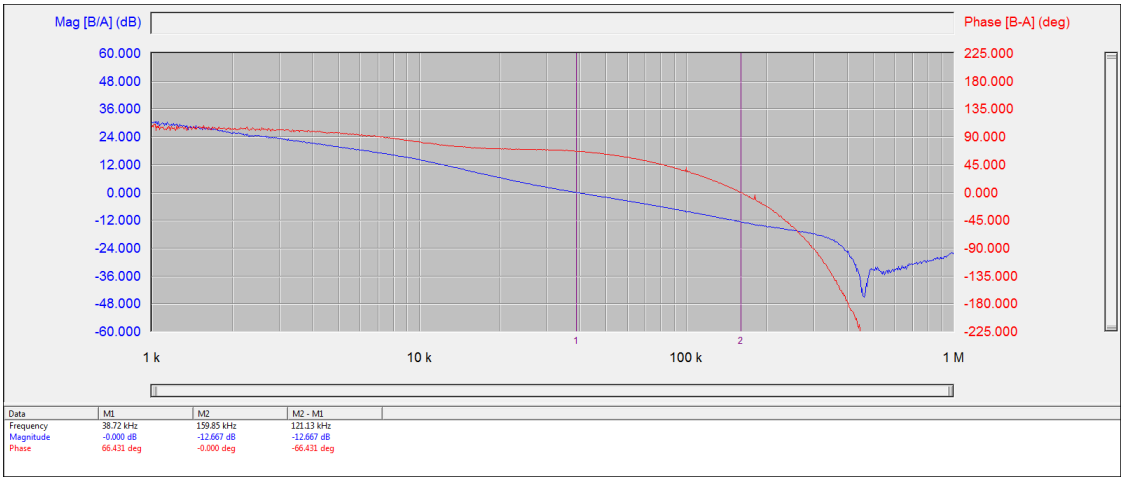


Figure 15. Bode Plot at 1.2-V Output at 12 V_{IN}, 0-A Output

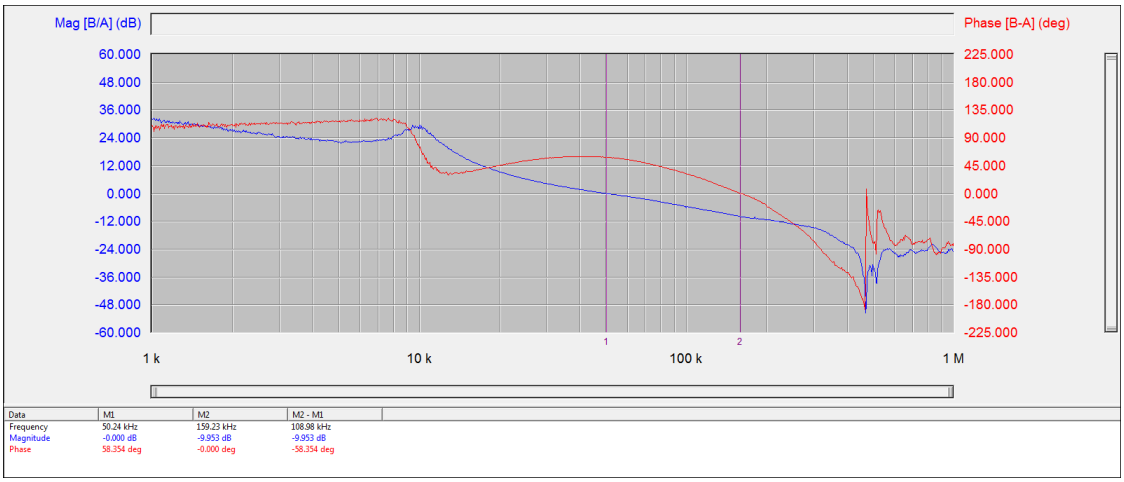
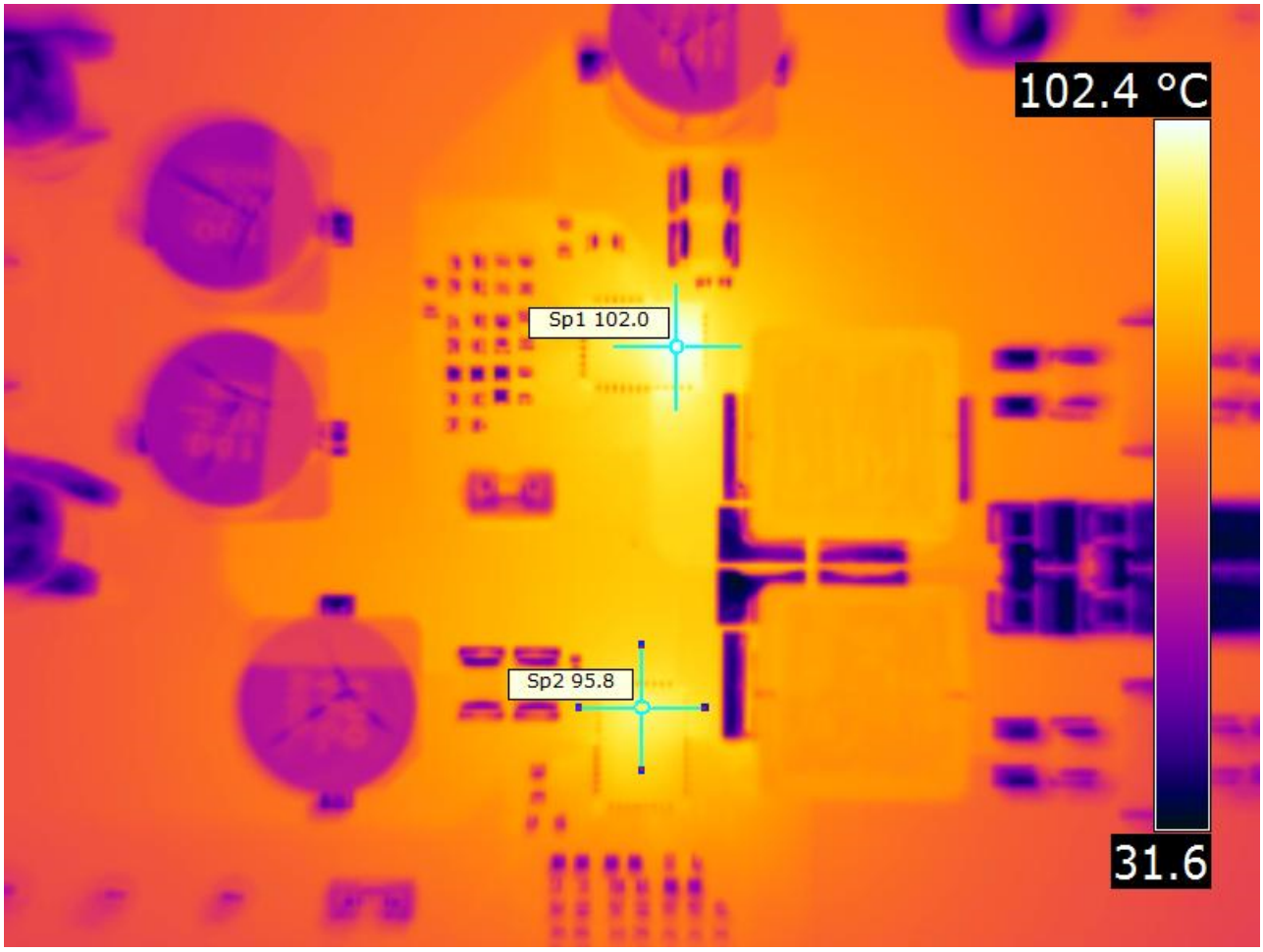


Figure 16. Bode Plot at 1.2-V Output at 12 V_{IN}, 70-A Output

7.10 Thermal Image



V_{IN} = 12 V, I_{OUT} = 70 A, V_{OUT} = 1.2V, F_{sw} = 500 kHz

Figure 17. Thermal Image

8 EVM Assembly Drawing and PCB Layout

Figure 18 through Figure 26 show the design of the TPS546C23EVM2-746 EVM printed circuit board.

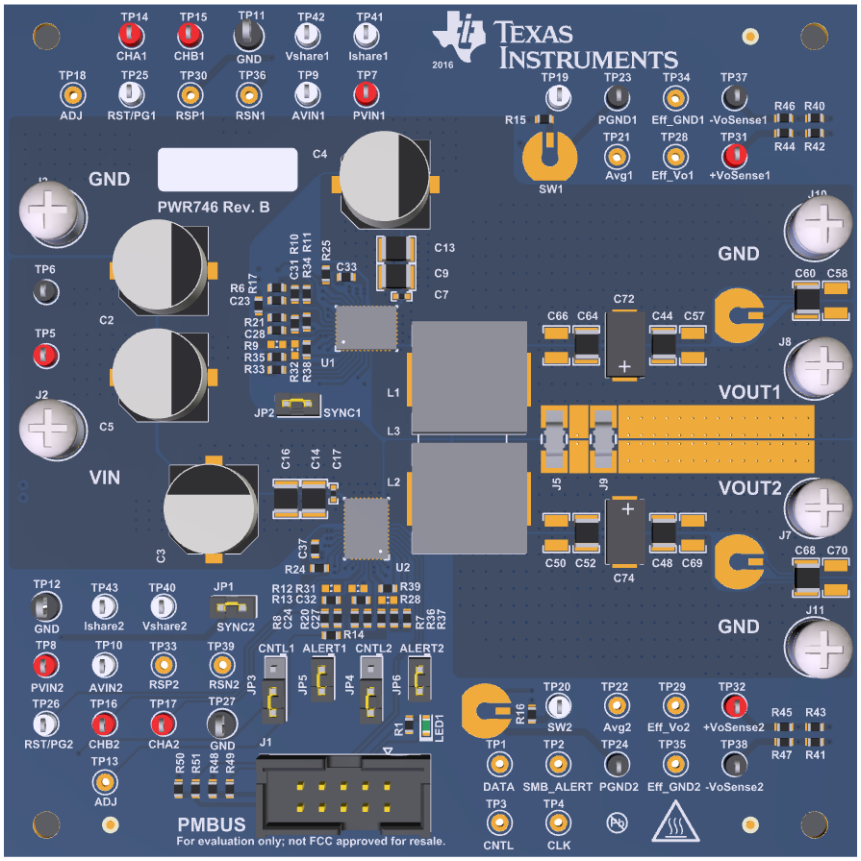


Figure 18. TPS546C23EVM2-746 EVM 3D Top View

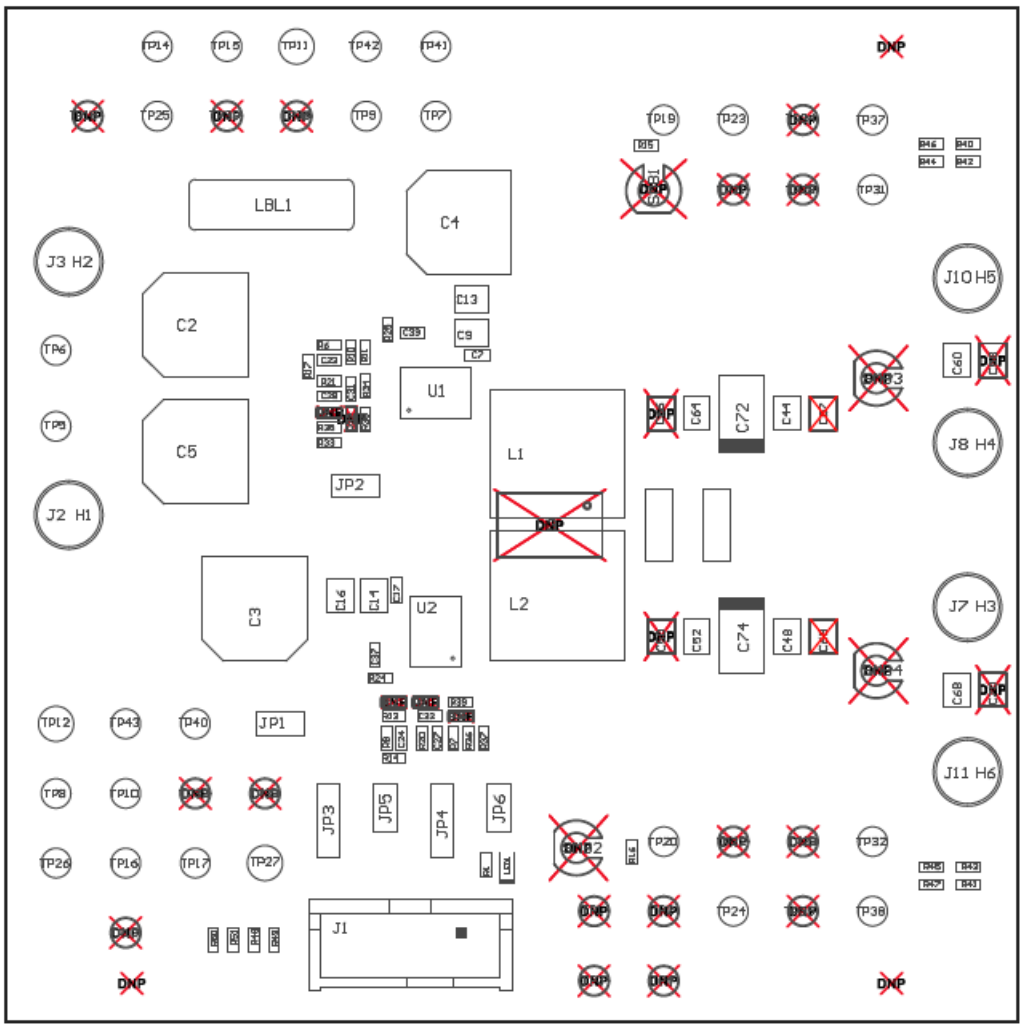


Figure 19. TPS546C23EVM2-746 EVM Top Layer Assembly Drawing (Top View)

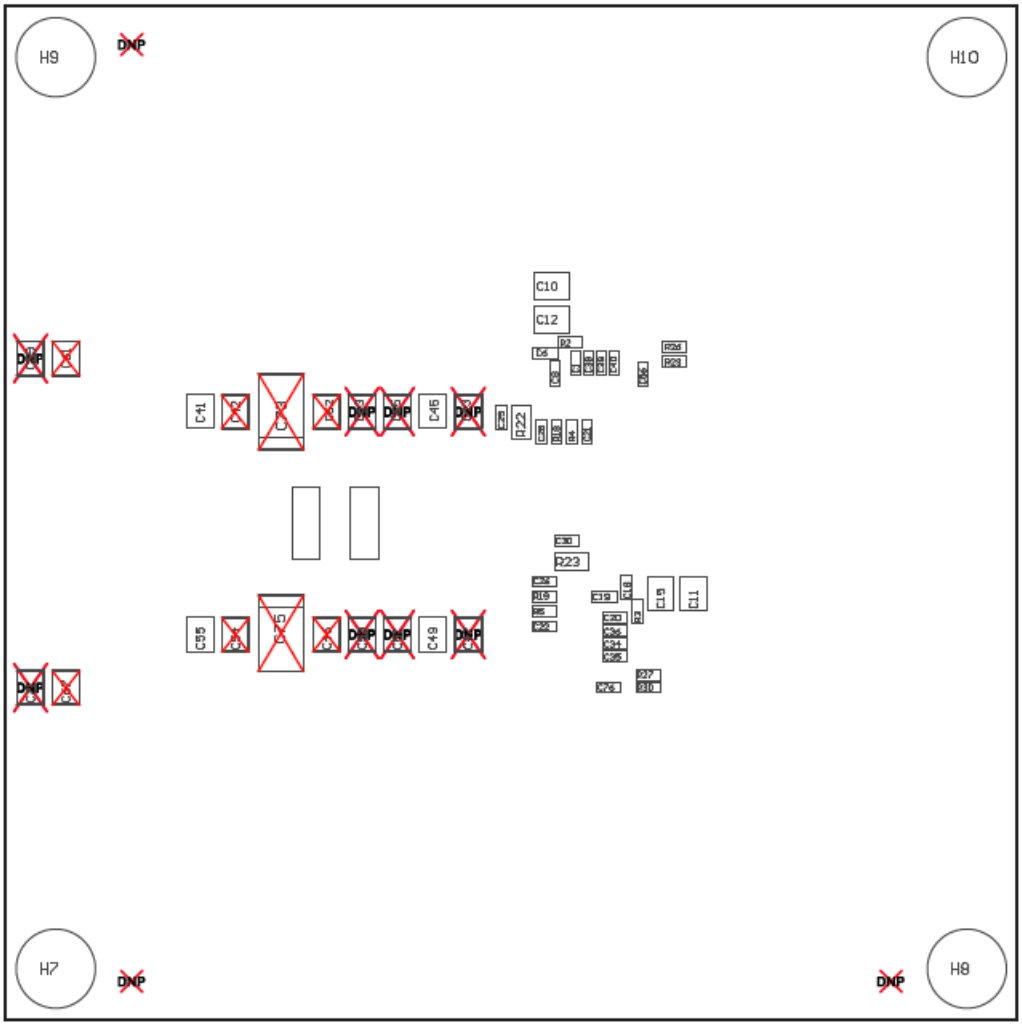


Figure 20. TPS546C23EVM2-746 EVM Bottom Assembly Drawing (Bottom View)

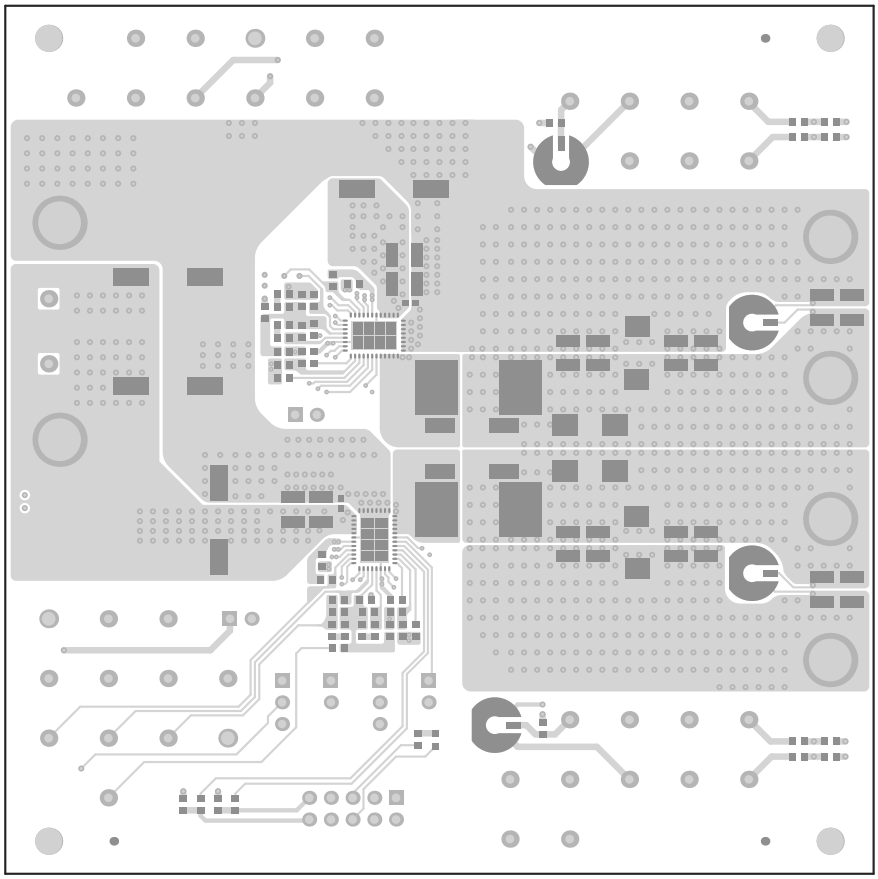


Figure 21. TPS546C23EVM2-746 EVM Top Copper (Top View)

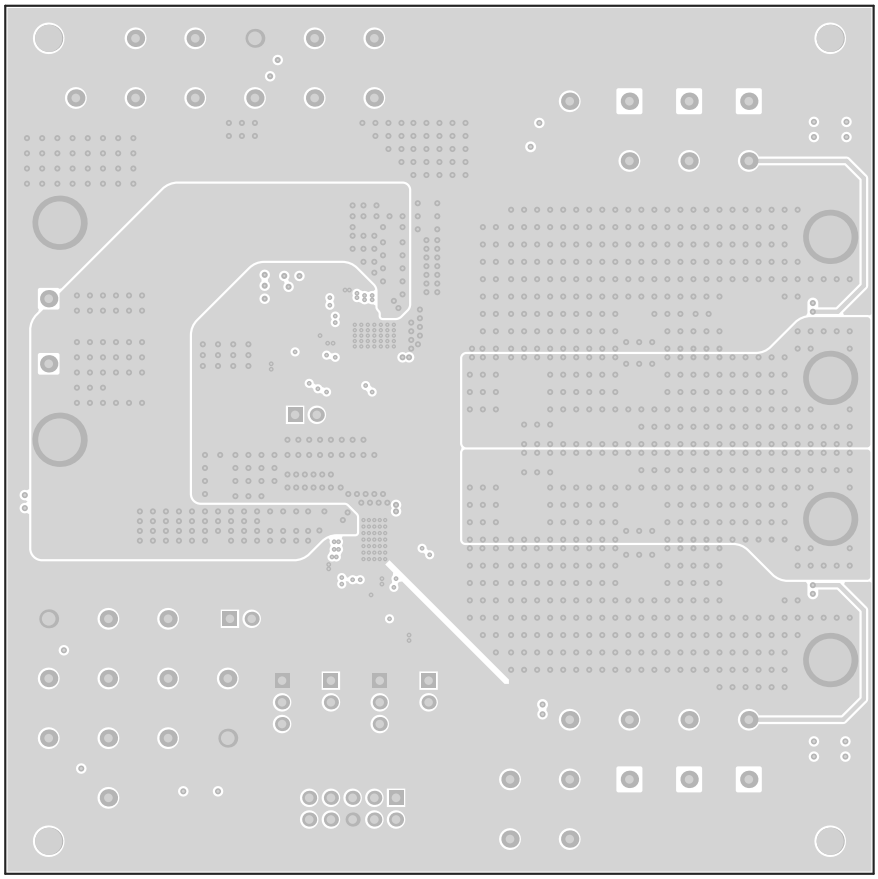


Figure 22. TPS546C23EVM2-746 EVM Internal Layer 1 (Top View)

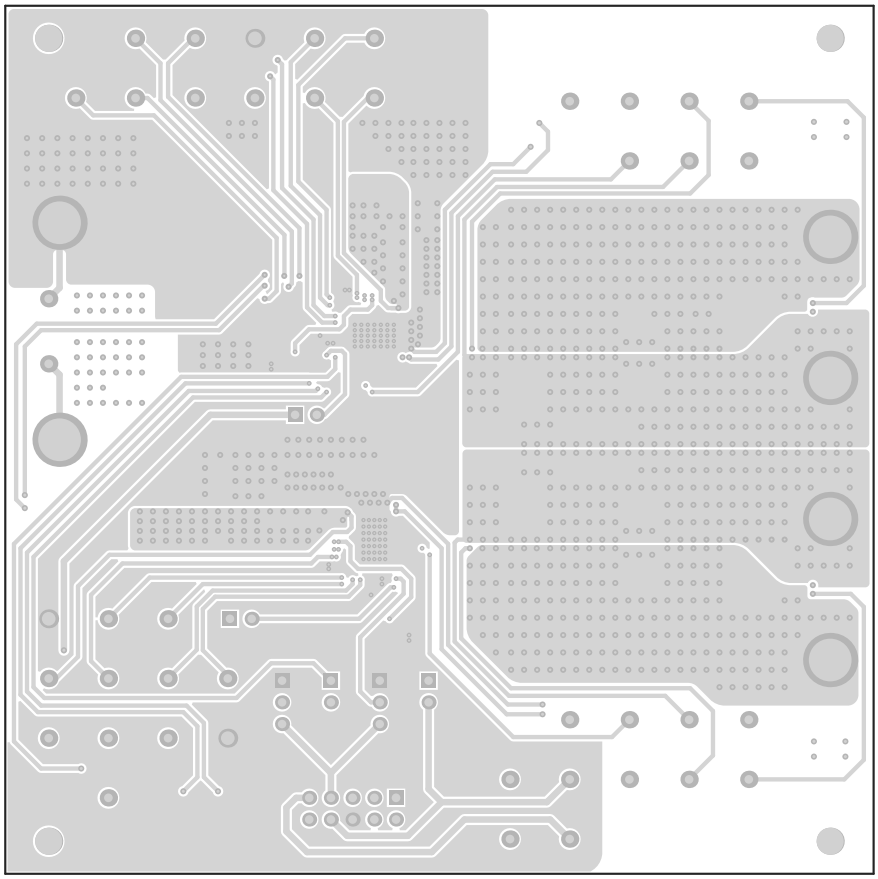


Figure 23. TPS546C23EVM2-746 EVM Internal Layer 2 (Top View)

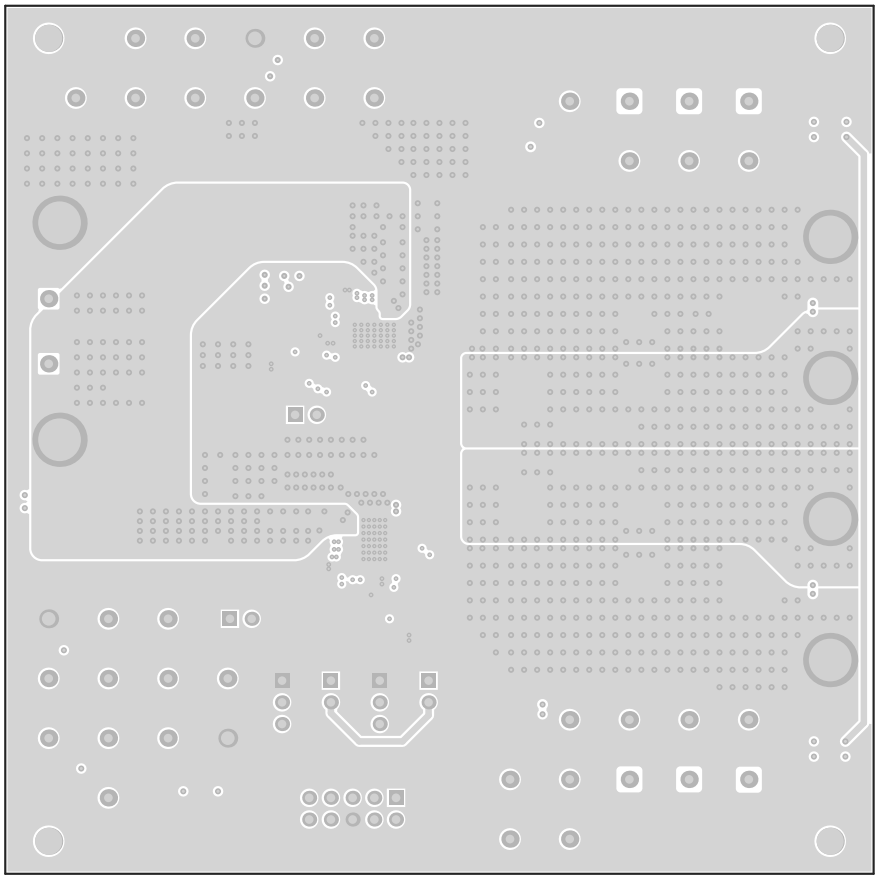


Figure 24. TPS546C23EVM2-746 EVM Internal Layer 3 (Top View)

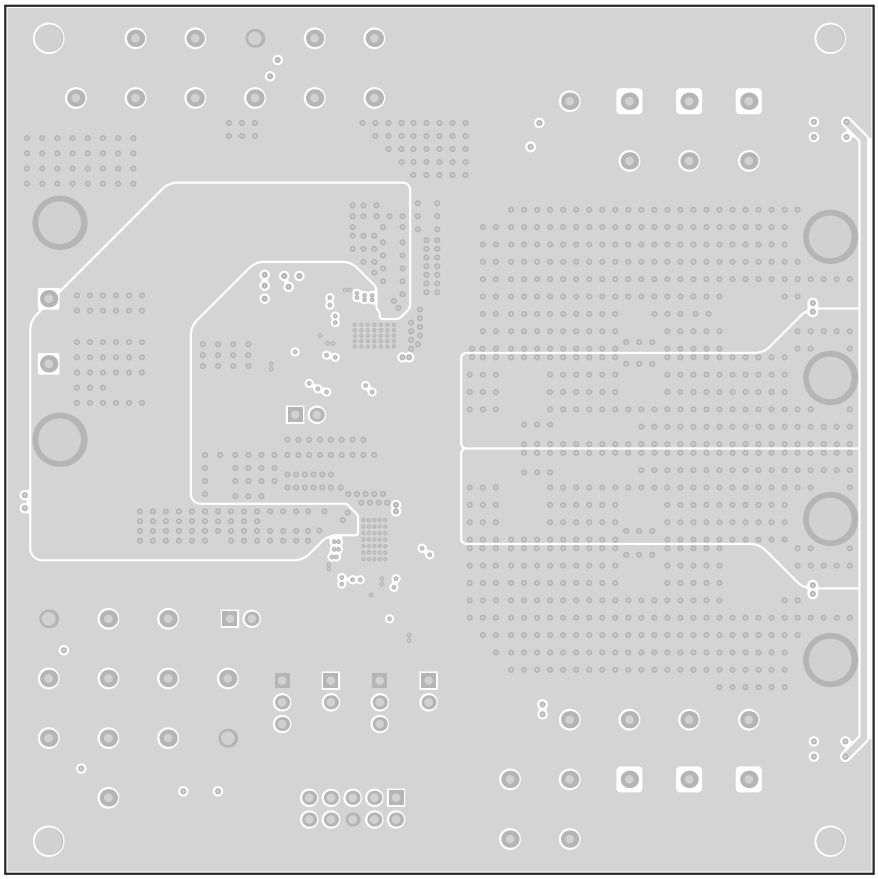


Figure 25. TPS546C23EVM2-746 EVM Internal Layer 4 (Top View)

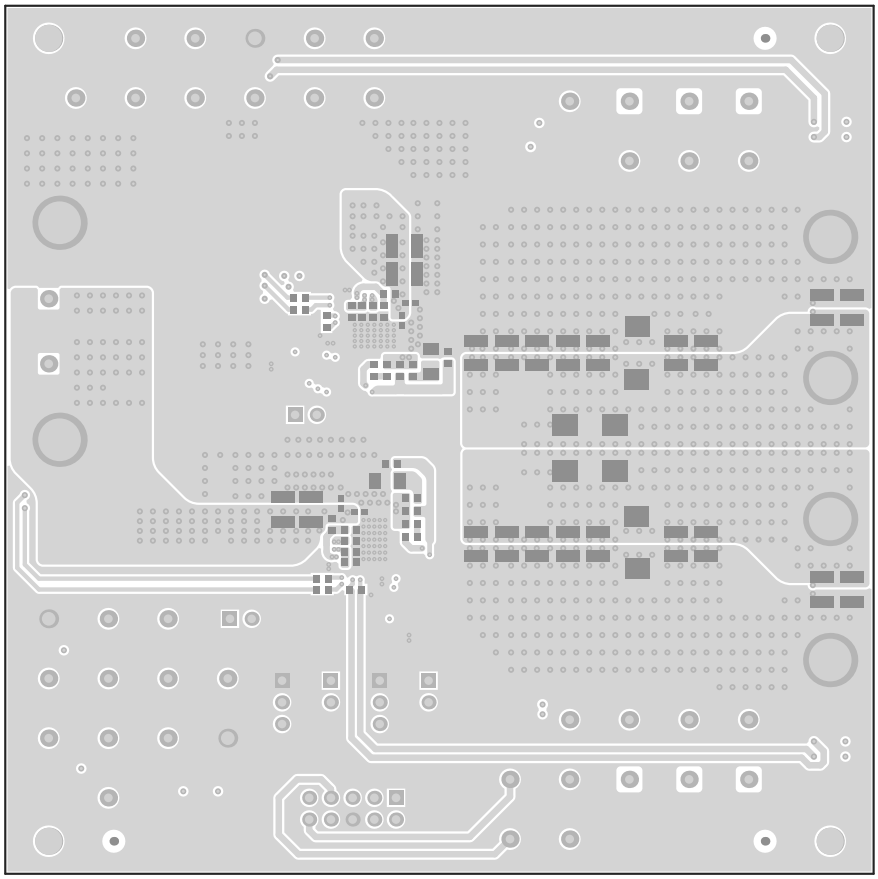


Figure 26. TPS546C23EVM2-746 EVM Bottom Copper (Top View)

9 Bill of Materials

Table 8 lists the BOM for the TPS546C23EVM2-746 (TPS546C23 EVM).

Table 8. TPS546C23EVM2-746 Components List

Qty	Designator	Description	Part Number	Manufacturer
4	C1, C20, C29, C31	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	GRM188R71E105KA12D	MuRata
4	C2, C3, C4, C5	CAP, AL, 100 µF, 35 V, +/- 20%, 0.15 ohm, SMD	EEE-FC1V101P	Panasonic
6	C6, C7, C8, C17, C18, C19	CAP, CERM, 6800 pF, 50 V, +/- 10%, X7R, 0402	GRM155R71H682KA88D	MuRata
8	C9, C10, C11, C12, C13, C14, C15, C16	CAP, CERM, 22 µF, 25 V, +/- 10%, X6S, 1210	GRM32EC81E226KE15L	MuRata
2	C21, C22	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	C0603C104K5RACTU	Kemet
2	C23, C24	CAP, CERM, 1200 pF, 100 V, +/- 5%, C0G/NP0, 0603	GRM1885C2A122JA01D	MuRata
2	C25, C26	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	06031C102JAT2A	AVX
2	C27, C28	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	GRM1885C1H222JA01D	MuRata
2	C31, C32	CAP, CERM, 270 pF, 50 V, +/- 5%, C0G/NP0, 0603	GRM1885C1H271JA01D	MuRata
4	C33, C36, C37, C38	CAP, CERM, 2.2 µF, 16 V, +/- 10%, X7R, 0603	GRM188Z71C225KE43	MuRata
2	C34, C39	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0603	C0603C475K8PACTU	Kemet
2	C35, C40	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	C0603C104K4RACTU	Kemet
10	C41, C44, C45, C48, C49, C52, C55, C60, C64, C68	CAP, CERM, 47 µF, 10 V, +/- 10%, X7R, 1210	GRM32ER71A476KE15L	MuRata
2	C56, C76	CAP, CERM, 330 pF, 50 V, +/- 1%, C0G/NP0, 0603	C1608C0G1H331F080AA	TDK
2	C72, C74	CAP, Tantalum Polymer, 470 µF, 6.3 V, +/- 20%, 0.01 ohm, 7343-40 SMD	6TPF470MAH	Panasonic
6	H1, H2, H3, H4, H5, H6	MACHINE SCREW PAN PHILLIPS 6-32	PMSSS 632 0038 PH	B&F Fastener Supply
4	H7, H8, H9, H10	Bumpon, Cylindrical, 0.312 X 0.200, Black	SJ61A1	3M
1	J1	Header (shrouded), 100mil, 5x2, Gold, TH	5103308-1	TE Connectivity
6	J2, J3, J7, J8, J10, J11	Swage Threaded Standoff, Brass,Swage Mount, TH	1546	Keystone
4	J4, J5, J6, J9	JUMPER TIN SMD	S1911-46R	Harwin
8	JP1, JP2, JP5, JP6	Header, 100mil, 2x1, Tin, TH	5-146278-2	TE Connectivity
2	JP3, JP4	Header, 100mil, 3x1, Tin, TH	5-146278-3	TE Connectivity
2	L1, L2	Inductor, Shielded, Ferrite, 300 nH, 52 A, 0.00015 ohm, SMD	SLC1480-301MLB	Coilcraft
1	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
1	LED1	LED, Green, SMD	150060GS75000	Wurth Elektronik
1	R1	RES, 1.00 k, 1%, 0.1 W, 0603	CRCW06031K00FKEA	Vishay-Dale
14	R2, R3, R4, R5, R29, R30, R40, R41, R42, R43, R48, R49, R50, R51	RES, 0, 5%, 0.1 W, 0603	ERJ-3GEY0R00V	Panasonic
2	R6, R8	RES, 1.10 k, 1%, 0.1 W, 0603	RC0603FR-071K1L	Yageo America
9	R7, R10, R13, R14, R17, R18, R19, R24, R25	RES, 10.0 k, 0.1%, 0.1 W, 0603	RT0603BRD0710KL	Yageo America
7	R11, R15, R16, R44, R45, R46, R47	RES, 49.9, 1%, 0.1 W, 0603	CRCW060349R9FKEA	Vishay-Dale
8	R14, R17, R18, R19, R20, R21, R24, R25	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo America
2	R20, R21	RES, 5.60 k, 1%, 0.1 W, 0603	RC0603FR-075K6L	Yageo America
2	R22, R23	RES, 1.0, 5%, 0.25 W, 1206	CRCW12061R00JNEA	Vishay-Dale
2	R26, R27	RES, 5.11 k, 1%, 0.1 W, 0603	CRCW06035K11FKEA	Vishay-Dale
1	R34	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo America
2	R33, R35	RES, 34.8 k, 1%, 0.1 W, 0603	RC0603FR-0734K8L	Yageo America
2	R36, R37	RES, 51.1 k, 1%, 0.1 W, 0603	RC0603FR-0751K1L	Yageo America
2	R38, R39	RES, 40.2 k, 1%, 0.1 W, 0603	CRCW060340K2FKEA	Vishay-Dale
6	SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6	Shunt, 100mil, Gold plated, Black	969102-0000-DA	3M

Table 8. TPS546C23EVM2-746 Components List (continued)

Qty	Designator	Description	Part Number	Manufacturer
7	TP5, TP14, TP15, TP16, TP17, TP31, TP32	Test Point, Miniature, Red, TH	5000	Keystone
3	TP6, TP23, TP24	Test Point, Miniature, Black, TH	5001	Keystone
2	TP7, TP8	Test Point, Miniature, Red, TH	5000	Keystone
10	TP9, TP10, TP25, TP26, TP43, TP19, TP20, TP40, TP41, TP42	Test Point, Miniature, White, TH	5002	Keystone
3	TP11, TP12, TP27	Test Point, Multipurpose, Black, TH	5011	Keystone
2	TP37, TP38	Test Point, Miniature, Black, TH	5001	Keystone
2	U1, U2	4.5V-18V, 35A PMBUS STACKABLE SYNCHRONOUS BUCK CONVERTER, RVF0040A	TPS546C23	Texas Instruments

10 Screenshots

10.1 Fusion GUI Screenshots

When launching the Fusion GUI, select **IC_DEVICE_ID** in Figure 27 as scanning mode to find TPS546C23.

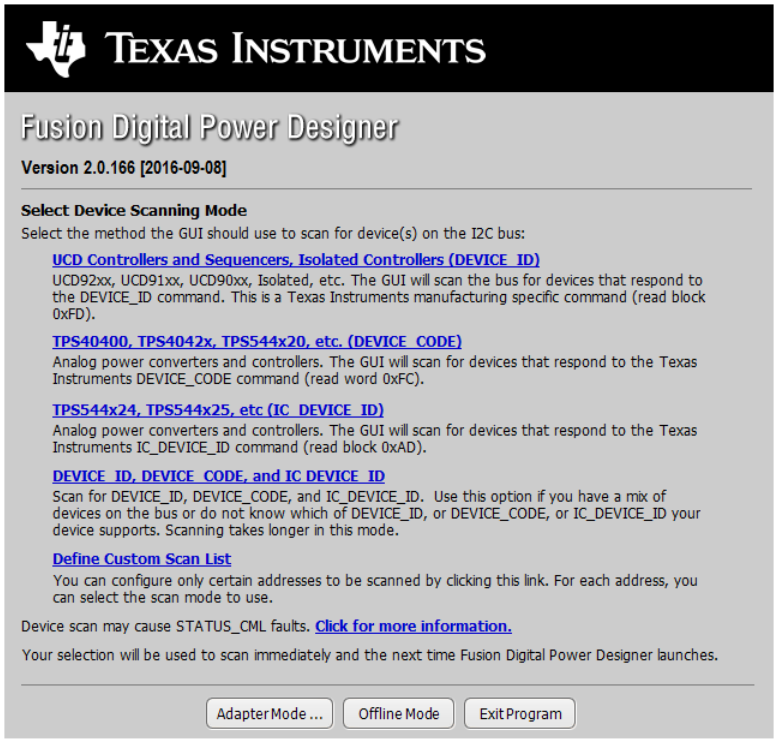


Figure 27. Select Device Scanning Mode

- Use the **Limits & On/Off** tab Figure 28 to configure the following:
  - V_{ref} (Vout_Command)
  - OC Fault and OC Warn
  - OT Fault and OT Warn (Die Temperature)
  - Power Good Limits
  - Fault response
  - UVLO
  - On/Off Config
  - Soft Start time (Turn On Rise)
  - Margin voltage

After making changes to one or more configurable parameters, the changes can be committed to nonvolatile memory by clicking ***Store DefaultAll***. This action prompts a **confirm selection** pop-up, and if confirmed, the changes are committed to nonvolatile memory to store all the modifications in non-volatile memory.

Both the loop master device and the loop slave device are tied to same bus interface, a scroll-down menu in the upper right corner can be used to switch view screens from one to the other. In two phase stacking system, most configurable parameters are disabled in GUI if the device is detected as loop slave. Figure 33.

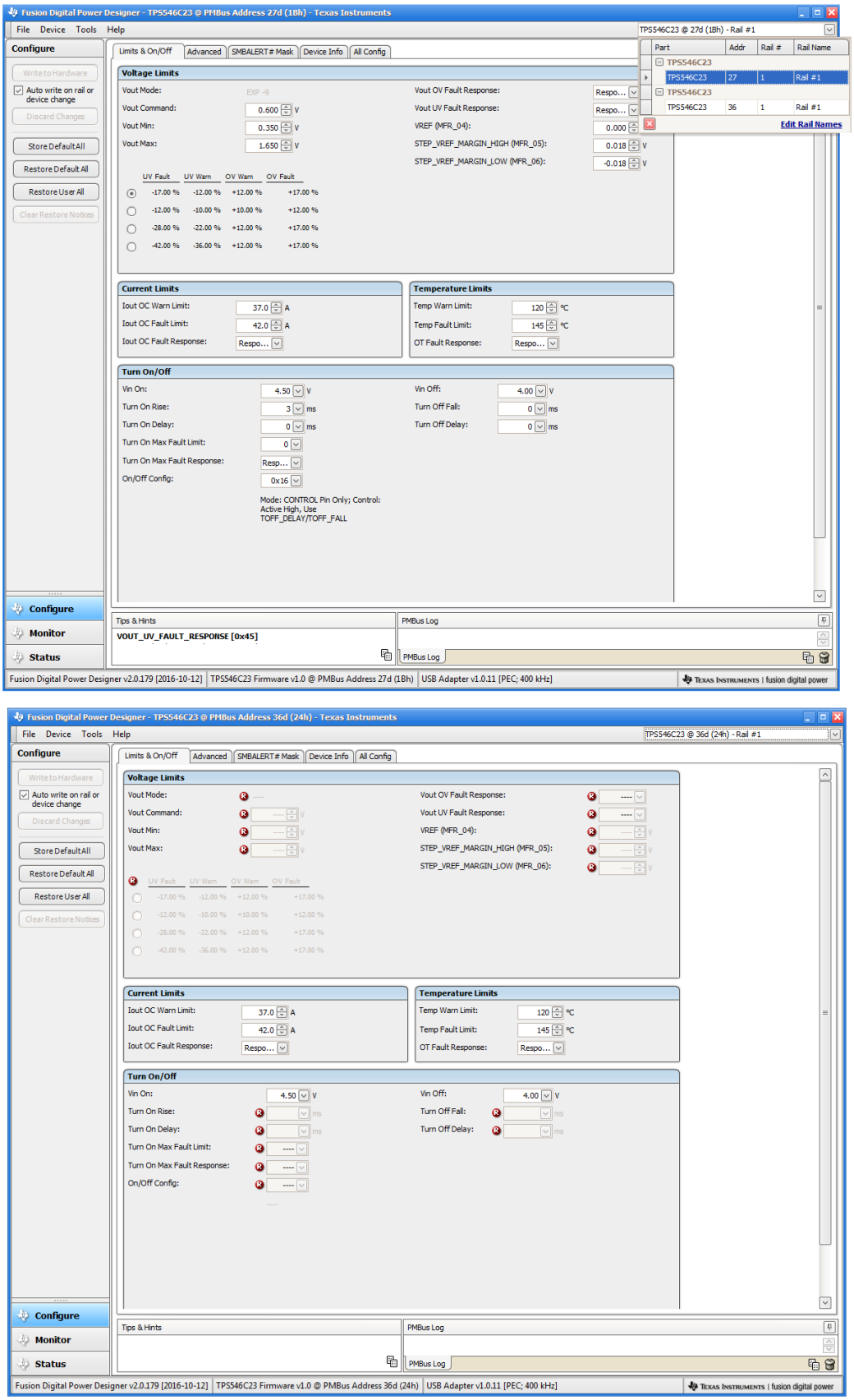


Figure 28. Configure- Limits and On/Off

Changing the on/off configuration prompts a pop-up window with details of the options Figure 29.

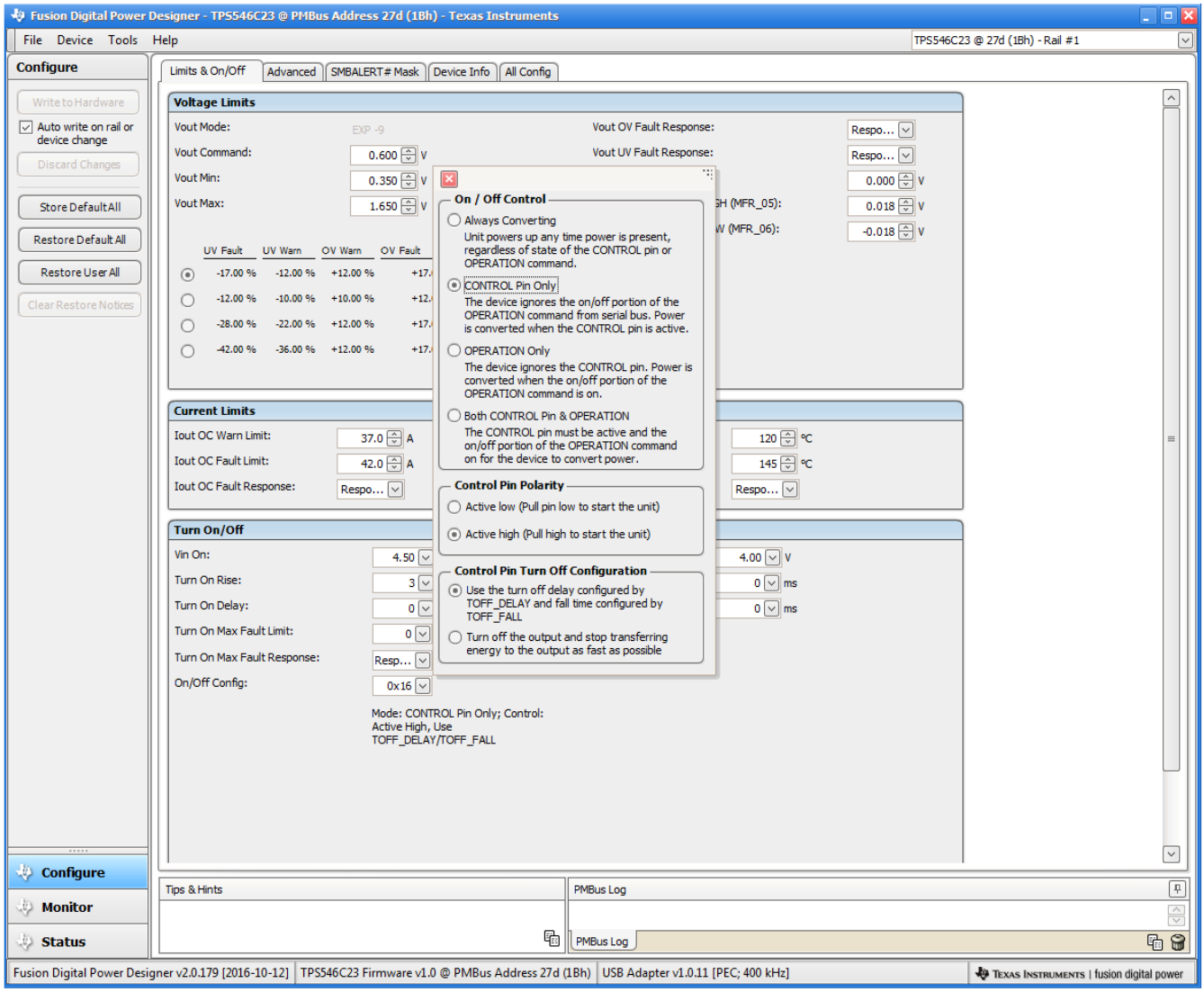


Figure 29. ON/OFF Control Pop-up

- Use the **Advanced** tab Figure 30 to configure:
  - OPTIONS: MFR_SPECIFIC_21 register
  - API_OPTIONS: MFR_SPECIFIC_32 register

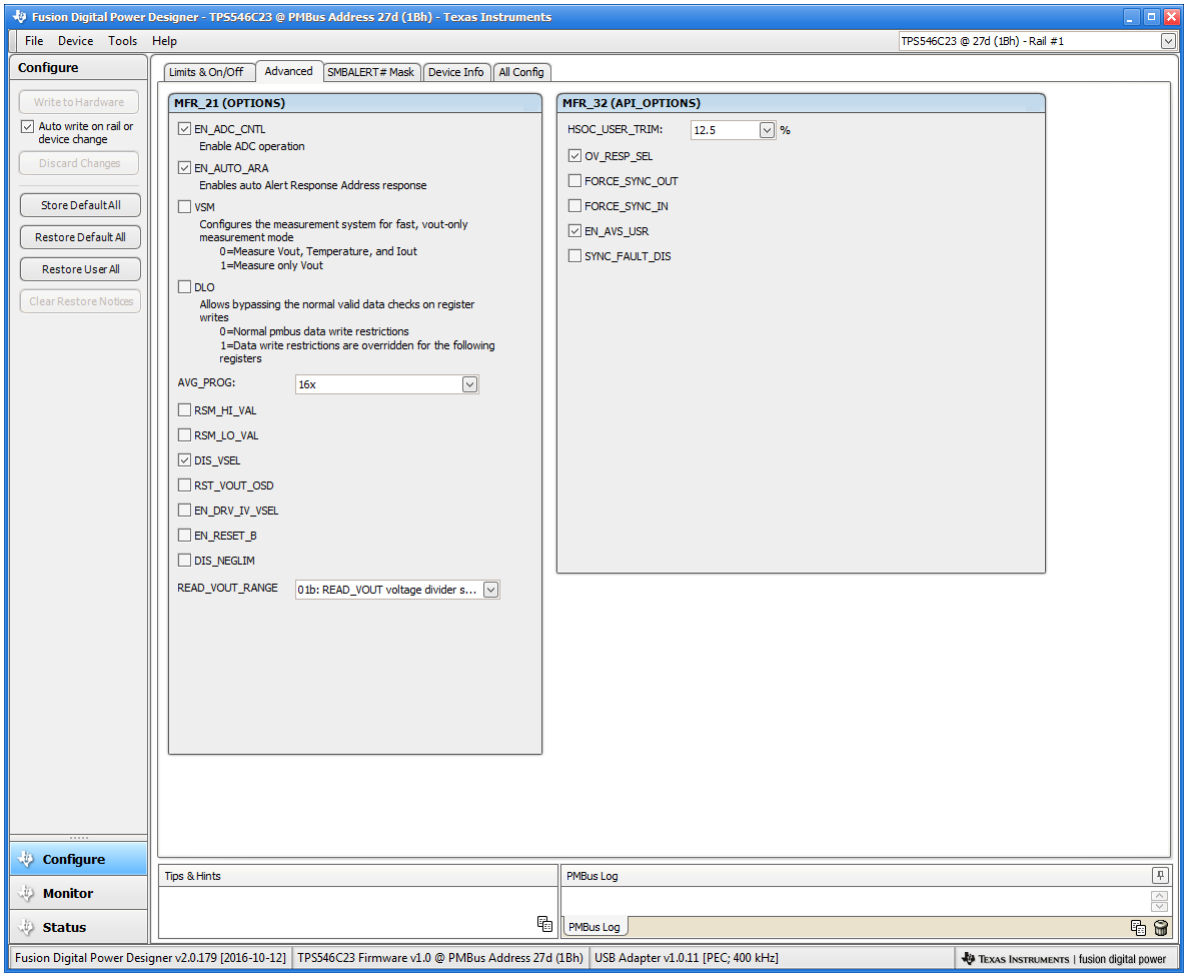


Figure 30. Configure - Advanced

The sources of SMBALERT which can be masked can be found and configured on the ***SMBALERT # Mask*** tab Figure 31

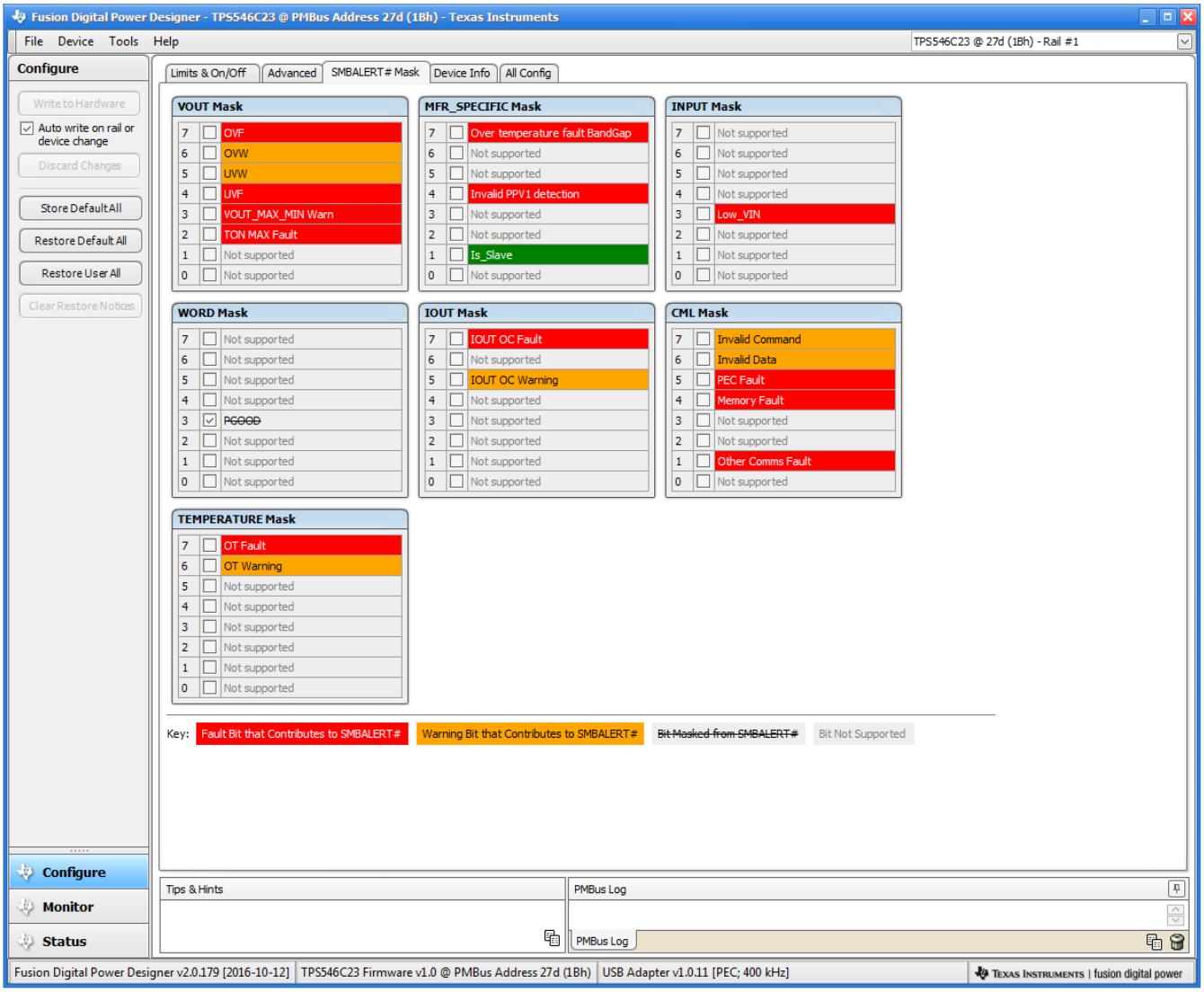


Figure 31. Configure - SMBALERT # Mask

The device information, User Scratch Pad, Write Protection options, the configuration of ***Vout Scale Loop***, ***Vout Transition Rate*** and ***Iout Cal Offset*** can be found on **Device Info** tab Figure 32.

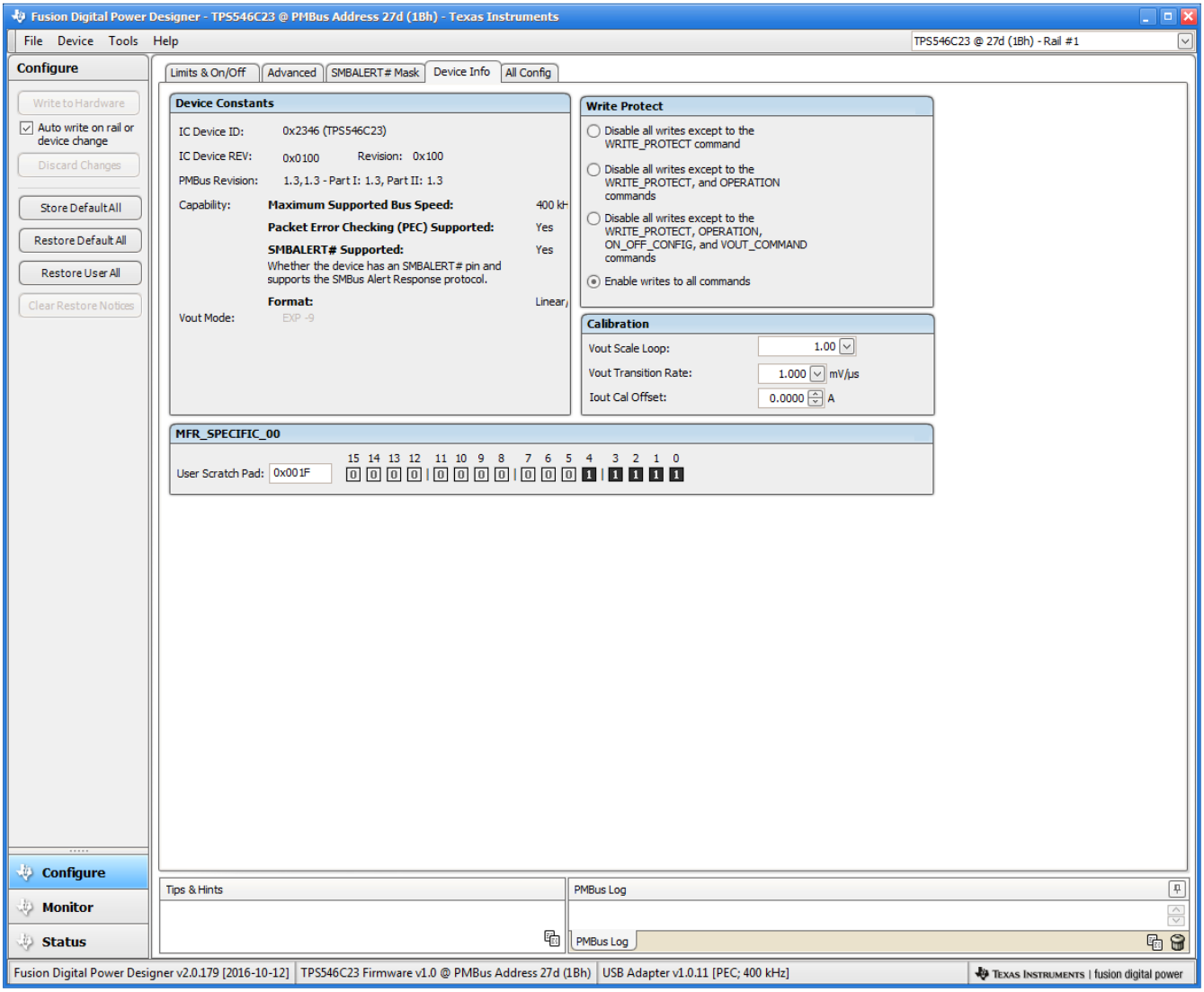


Figure 32. Configure - Device Info

Use the **All Config** tab Figure 33 to configure all of the configurable parameters, which also shows other details like Hex encoding.

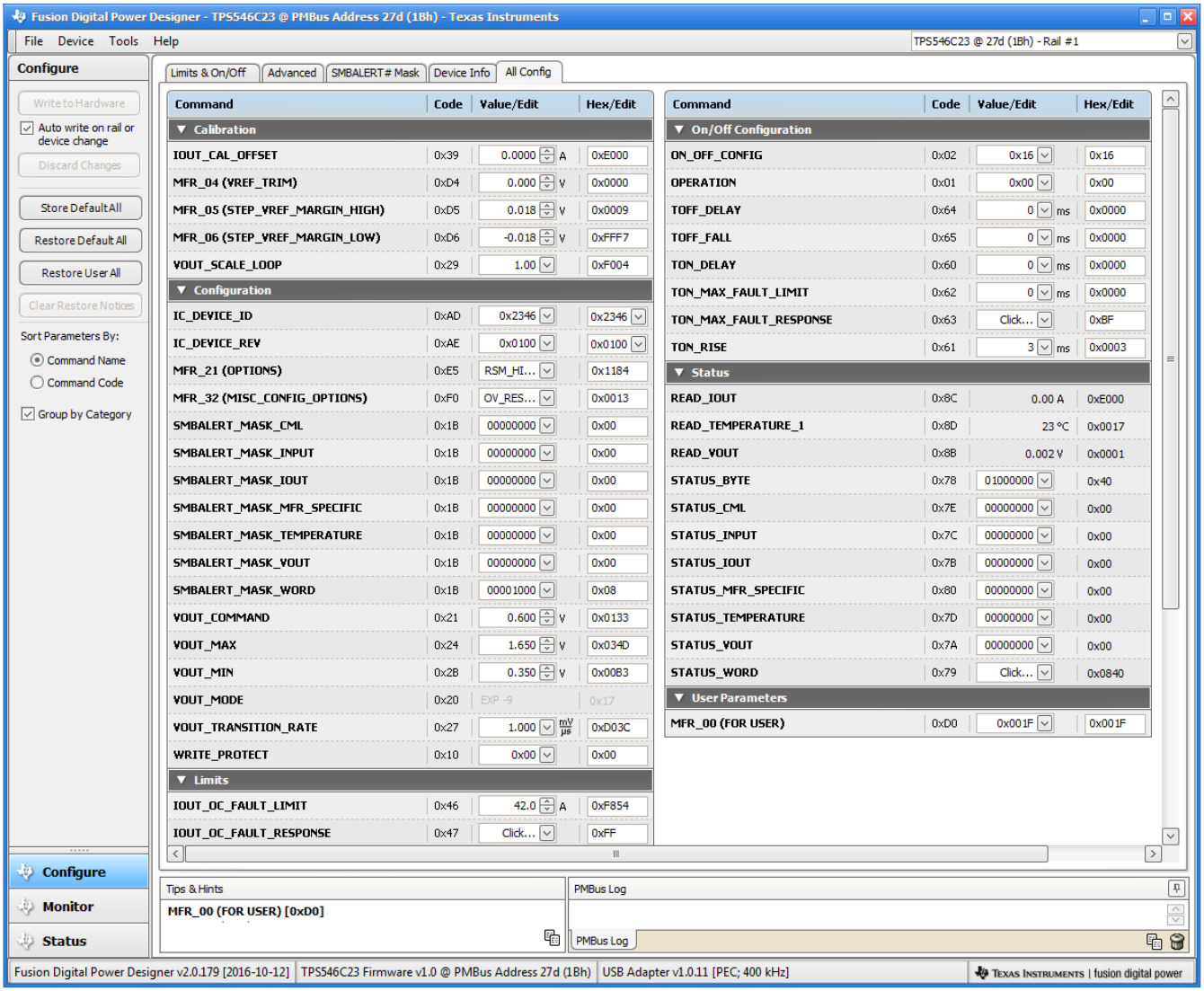
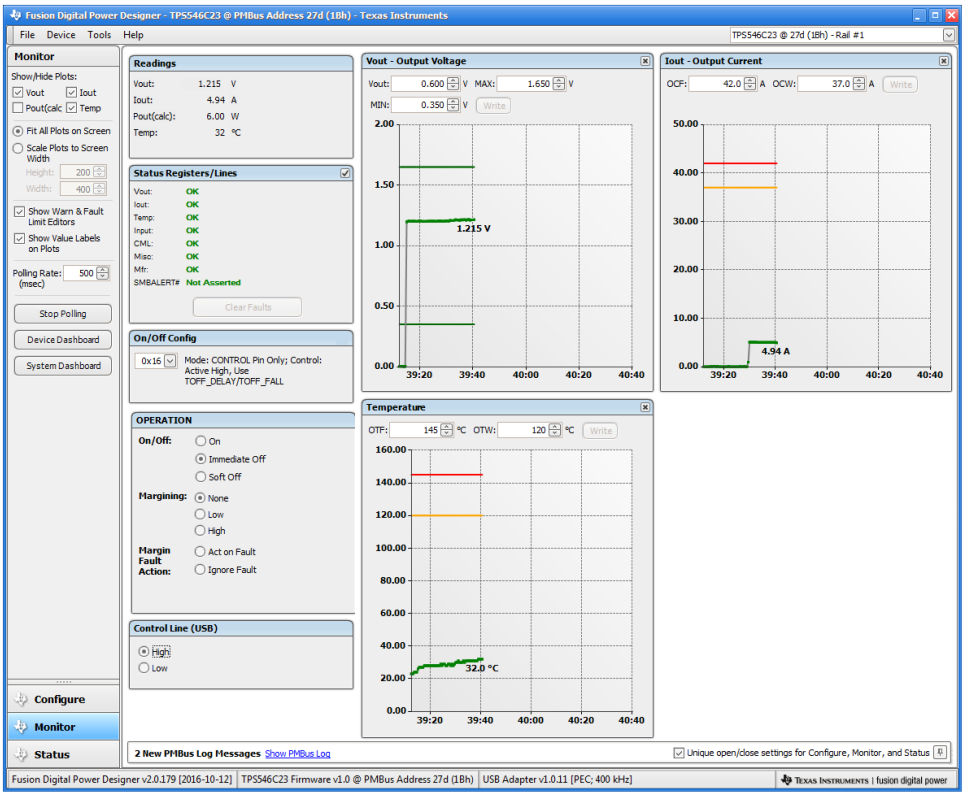


Figure 33. Configure - All Config

When the *Monitor* screen Figure 34 is selected, the screen changes to display real-time data of the parameters that are measured by the device. This screen provides access to:

- Graphs of V_{OUT}, *Iout*, *Temperature*, and *Pout*.
- *Start/Stop Polling* which turns ON or OFF the real-time display of data.
- Quick access to On/Off config
- Control pin activation, and OPERATION command.
- Margin control.
- Clear Fault. Selecting ***Clear Faults*** clears any prior fault flags.

With two devices stacked together, the **IOUT** reading from either the loop master or the loop slave device is the load current supported by the device itself, thus the **Iout** reading is half of the total load.



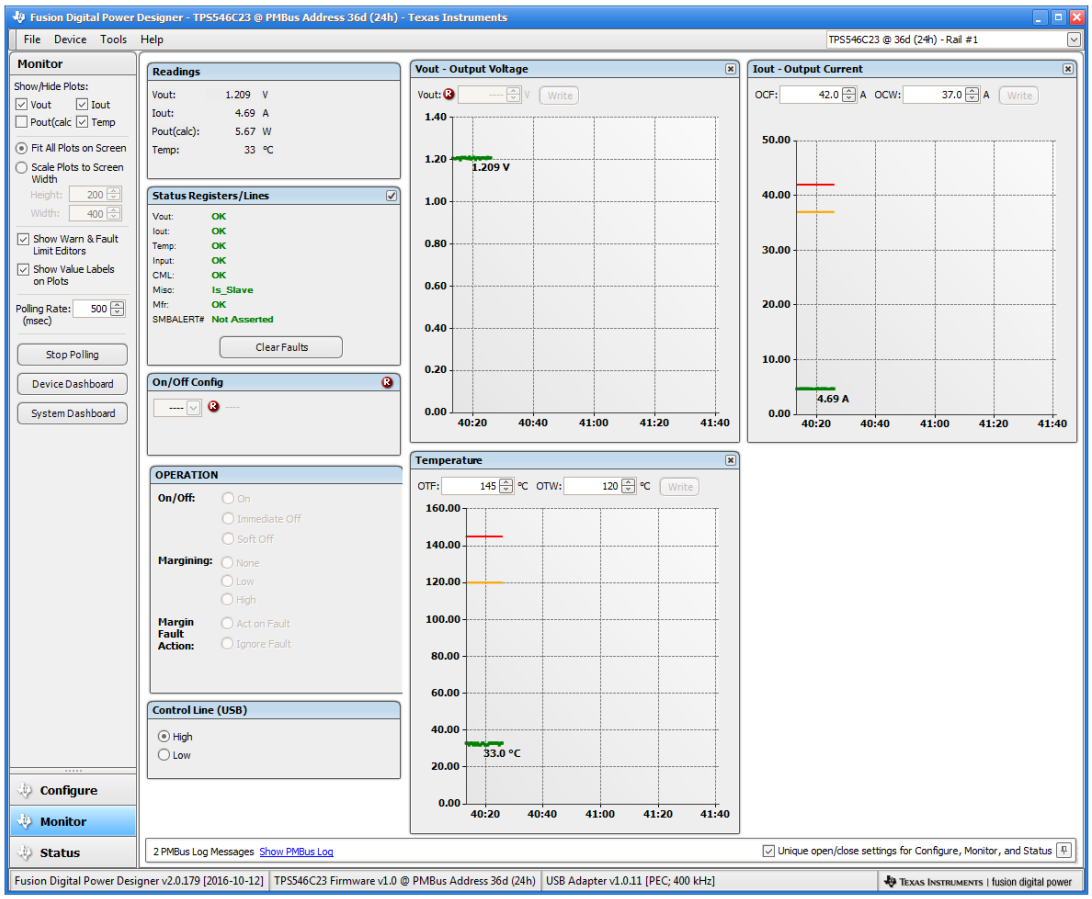
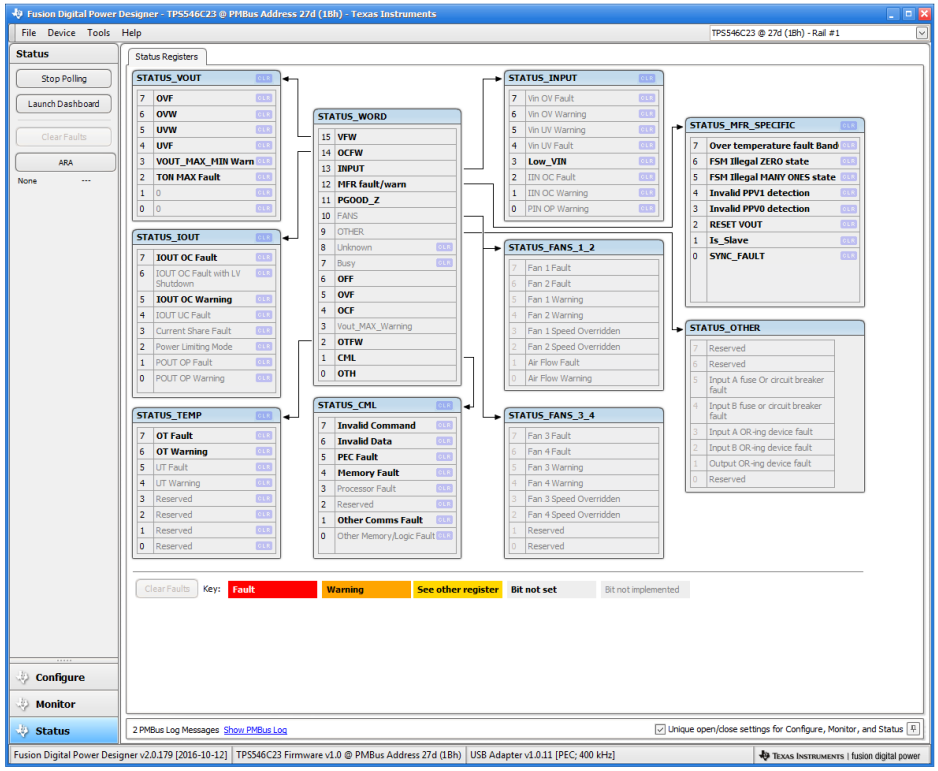


Figure 34. Monitor Screen with 10A total load

Selecting *Status* screen Figure 35 from lower left corner shows the status of the device .



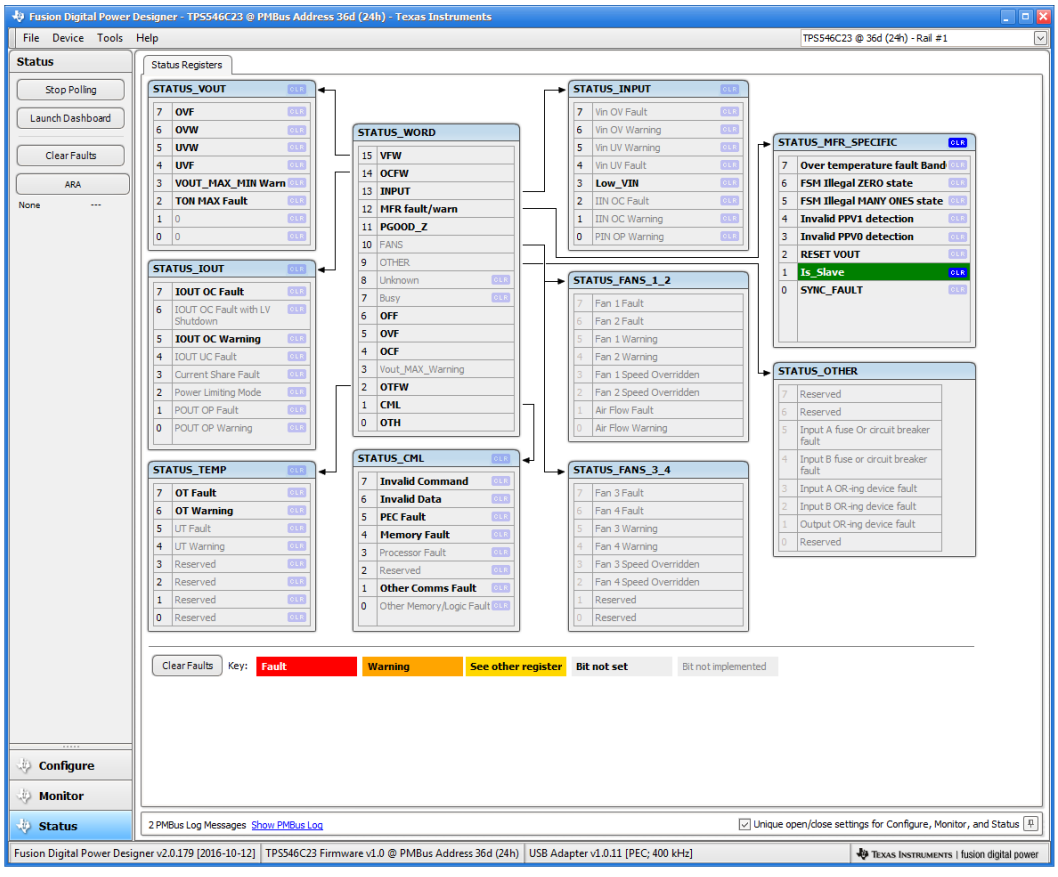


Figure 35. Status Screen

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