TPS54120EVM, Low Noise 1A Power Supply Evaluation Module

This User's Guide describes operational use of the TPS54120 Evaluation Module (PWR103) as a reference design for engineering demonstration and evaluation of the TPS54120, low noise 1A power supply. Included in this user's guide are setup and operation instructions, a schematic diagram, layout description, a bill of materials, and test results.

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1 Background

The Texas Instruments TPS54120 EVM (PWR103) helps design engineers evaluate the operation and performance of the TPS54120 (Switcher + LDO) for possible use in their own circuit application. This particular EVM configuration contains all of the external components required for a low noise 1A solution with internal thermal and current limit shutdowns, and enable circuitry in a 3.5mm x 5.5mm, QFN, thermally enhanced PowerPad™ package.

The power input of the IC (PVIN) is rated for 1.6V to 17V while the control input (VIN) is rated for 4.5 to 17V. The TPS54120 provides both inputs but this EVM is designed and tested using the PVIN connected to VIN with a minimum input voltage of 7V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54120 device. The switching frequency is externally set at a nominal 480 KHz.

The integrated switcher (SW) and LDO are optimized to allow the TPS54120 to achieve high efficiencies and a low output noise. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable LDO output voltage from 0.8V to 6V. Additionally, the TPS54120 provides adjustable slow start, tracking and enable inputs. The TPS54120, including other external components that is capable of delivering up to 1A low noise supply to the load.

Table 1. EVM Specifications

EVM	Input Voltage	SW Output Voltage	LDO Output Voltage	Output Current
TPS54120	7-17V	4.1V	3.3V	0-1A

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup and use the TPS54120EVM.

2.1 Input and Output Connections and Jumper Descriptions

- **J1-LDO OUT** & **J2-GND:** The output of the LDO and the ground connector. Default setting is 3.3V. This is the low noise output from the TPS54120.
- **J3-VIN** & **J4-GND:** Input power supply voltage and the ground connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added across J3 & J4 if the supply leads are greater than six inches. For example, an additional 47µF electrolytic capacitor across J3 & J4 can improve the transient response of the TPS54120 while eliminating unwanted ringing on the input due to long wire connections.
- **J5:** SMA connector for the output voltage of the LDO. The connector for J5 is not populated on the TPS54120EVM (PWR103). This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements.
- **J7-SW OUT** & **J6-GND:** The output of the SW and the ground connector. This is the output voltage from the switcher converter and the input voltage to the LDO. Default setting is 4.1V
- **J8:** SMA connector for the output voltage of the SW. The connector for J8 is not populated on the TPS54120EVM (PWR103). This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements.
- **JP1-LDOEN:** LDO enable. To enable the output of the LDO, connect this jumper from the center pin to the “on” pin. This will connect the enable pin to the LDO input supply. To disable connect this jumper from the center pin to the “off” pin. This will short the LDO enable pin to ground.
- **JP2:** The jumper connection between the output of the switcher converter to the LDO input. A shorting jumper is required for normal operation. If you want to disconnect the LDO from the SW, remove the shorting jumper wire.

- **JP3-SW EN:** Switcher converter enable jumper. To enable the SWITCHER output, leave this jumper unconnected (there is an internal pull up on this pin). To disable, install a shorting jumper. This will short the enable pin to ground.
- **TP1-PWRGD:** Power Good connector test point. It is power good open collector flag for the switcher converter. Tie this pin through a 10k resistor to a regulated supply <5.5V to monitor the status of the switcher converter output.
- **TP2-SENSE:** The SW sense (feedback) pin test point.
- **TP3-SW OUT:** This is the positive switcher output test point. In addition to J7, this test point can also be used to measure the output voltage of the switcher.
- **TP4-LDO IN:** The LDO input voltage test point.
- **TP5-LDO OUT:** The LDO output test point. In addition to J1, this test point can also be used to measure the output voltage of the LDO.

2.2 Modifications

These evaluation modules are designed to provide access to the features of the TPS54120. However, some modifications can be made to this module.

2.2.1 SW Output Voltage Set Point

The output voltage of the switcher is set by the resistor divider network of R5 and R6. R6 is fixed at 10kohm. To change the switcher output voltage of the EVM, it is necessary to change the value of resistor R5. The value of R5 for a specific output voltage can be calculated using Equation 1. Note that the SW output should be 0.8V above the LDO output for best PSR and noise performance.

$$R5 = 10\ k\Omega\ (SW\ Vout – 0.8V)/\ (0.8V) \quad (1)$$

Table 2 lists the R5 values for some common output voltages. The values given in Table 2 are standard values, not the exact value calculated using Equation 1.

Table 2. Sample 1% Resistor Values for Common SW Output Voltages

SW Output Voltage (V)	R5 Value (kΩ)
1.8	12.4
2.5	21.5
3.3	31.6
4.1	41.2
5	52.3
6	64.9

2.2.2 LDO Output Voltage Set Point

The output voltage of the LDO also can be set by an external resistor divider network (R1 and R2). R2 is fixed at 10kohm. To change the LDO output voltage of the EVM, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage from 0.8 V to 6V. The value of R1 for a specific output voltage can be calculated using Equation 2. Note that the LDO output should be 0.8V below the SW output for best PSR and noise performance.

$$R1 = 10\ k\Omega\ (LDO\ Vout – 0.8V)/\ (0.8V) \quad (2)$$

Table 3 lists the R1 values for some common output voltages. Note that the minimum VIN equals VOUT + VDO or 2.2V, whichever is greater. The values given in Table 3 are standard values, not the exact value calculated using Equation 2.

Table 3. Sample 1% Resistor Values for Common LDO Output Voltages

LDO Output Voltage (V)	R1 Value (kΩ)
0.8	0 (Short)
1	2.49

Table 3. Sample 1% Resistor Values for Common LDO Output Voltages (continued)

LDO Output Voltage (V)	R1 Value (kΩ)
1.2	4.99
1.5	8.87
1.8	12.5
2.5	21
3.3	30.9
5	52.3

2.2.3 Switcher Slow Start Time

The slow start time can be adjusted by changing the value of C7. Use Equation 3 to calculate the required value of C7 for a desired slow start time (Tss)

$$C7(nF) = Tss(ms)\ Iss(\mu A)/Vref(V) \quad (3)$$

Basically the device has an internal pull-up current source of 2.3 µA=Iss that charges the external slow start capacitor C7. The voltage reference Vref(V) for this part is 0.8V.

2.2.4 LDO Start Up

The start up time of the LDO can be adjusted by changing the value of C13. In addition to start up time, the capacitor on the NR pin is used for noise reduction as well. However, the noise reduction effect is nearly saturated at 0.01µF.

2.3 Equipment Interconnect

- Turn off the input power supply after verifying that its output voltage is set to the desired supply voltage (less than 17V) and the current limit is set to approximately 500mA. Connect the positive voltage lead from the input power supply to J3 (Vin) and the ground lead to J4 (GND).
- Connect a 0-1A load (I_{Load}) between LDO OUT and GND using J1 and J2
- Disable the output of the LDO by connecting a shorting jumper at JP1 from the “off” pin to the center pin (LDO EN).

3 Operation

- Turn on the input power supply. Verify that the switcher output voltage is near 4.1V and the LDO output is near 0V.
- Enable the LDO output by connecting the jumper on JP1 from the “on” pin to the center pin (LDO EN).
- Verify that the LDO output voltage is 3.3V.
- Vary the load current and VIN voltage as necessary for test purposes.

4 Test Results

This section provides typical performance waveforms for the TPS54120EVM (PWR103) characteristic of this EVM design.

4.1 Output Voltage Ripple

Figure 1 shows the output voltage ripple of the LDO and SWITCHER converter for the TPS54120EVM with Vin = 12V, SW OUT = 4.1V, LDO OUT = 3.3V, Iout = 400mA, Fswitching = 480kHz.

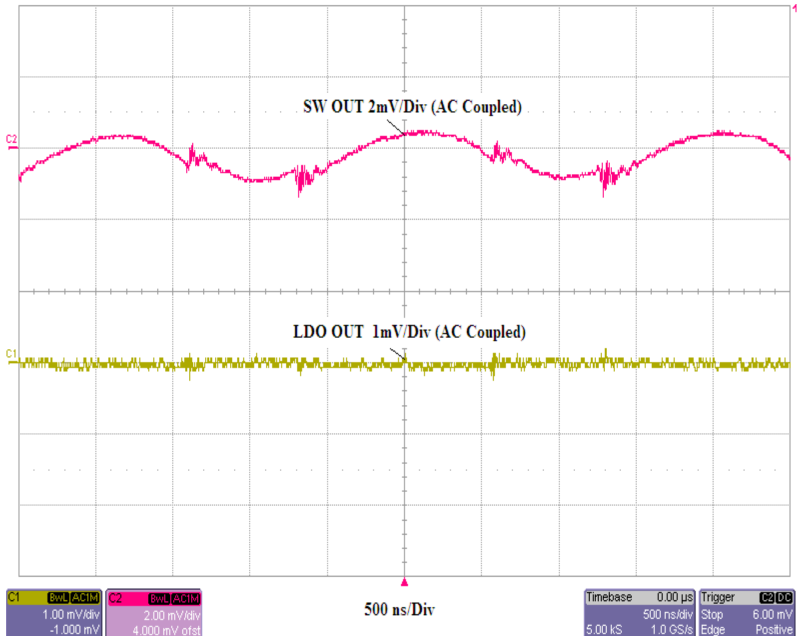

Figure 1. Output Voltage of Both the SW and LDO with 400mA Load

4.2 Output Noise

Figure 2 shows the output voltage noise spectrum for the TPS54120EVM with Vin = 12V, LDO OUT = 3.3V, SW OUT = 4.1V, Iout = 400mA, Fswitching = 480kHz.

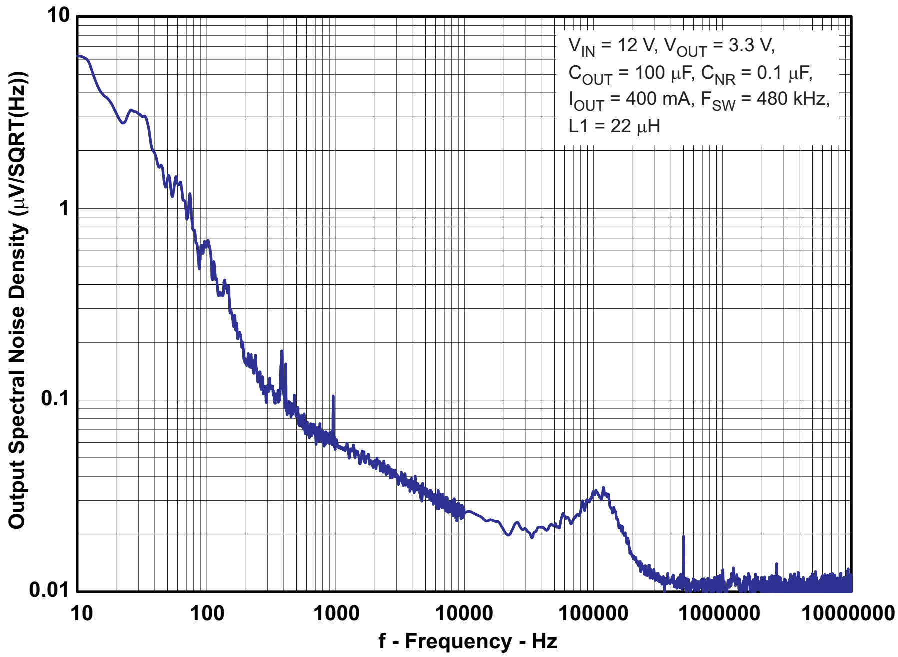

Figure 2. Output Spectrum Noise Density vs. Frequency

4.3 Output Turn On

Figure 3 shows the SW output voltage turn-on from SW enable for the TPS54120EVM with Vin = 12V, SW OUT = 4.1V, LDO OUT = 3.3V, and Iout = 400mA, Fswitching = 480kHz.

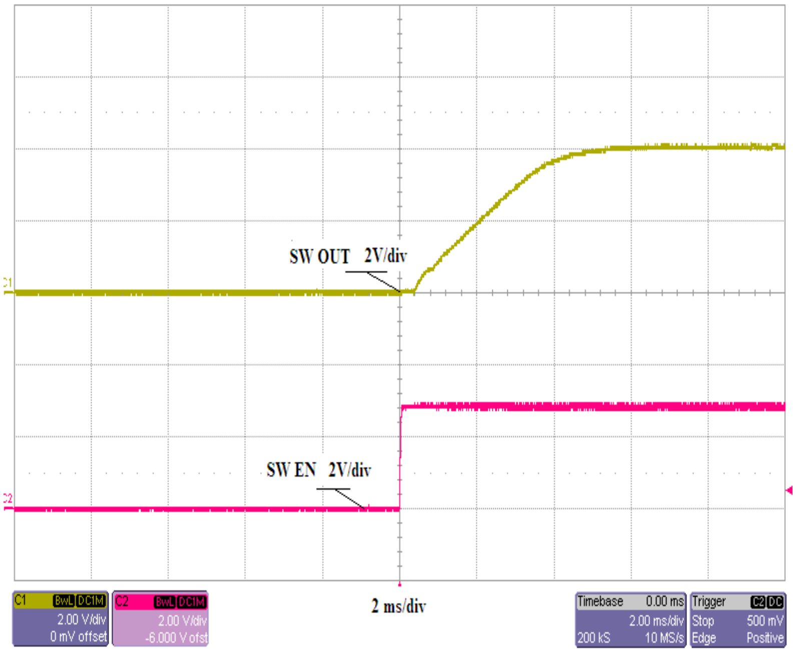

Figure 3. Switcher Converter Output Voltage Turn-on, SW Enable

Figure 4 shows the LDO output voltage turn-on from LDO enable for the TPS54120EVM with Vin = 12V, SW OUT = 4.1V, LDO OUT = 3.3V, and Iout = 400mA, Fswitching = 480kHz.

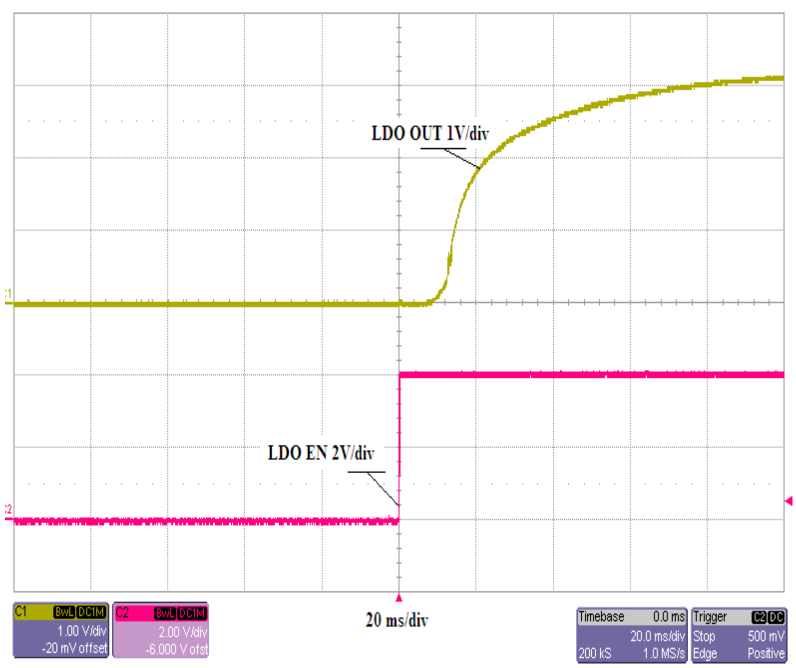

Figure 4. LDO Output Voltage Turn-on, LDO Enable

Figure 5 shows the LDO output voltage turn-on of TPS54120 from SW enable for the TPS54120EVM with Vin = 12V, SW OUT = 4.1V, LDO OUT = 3.3V, and Iout = 400mA, Fswitching = 480kHz.

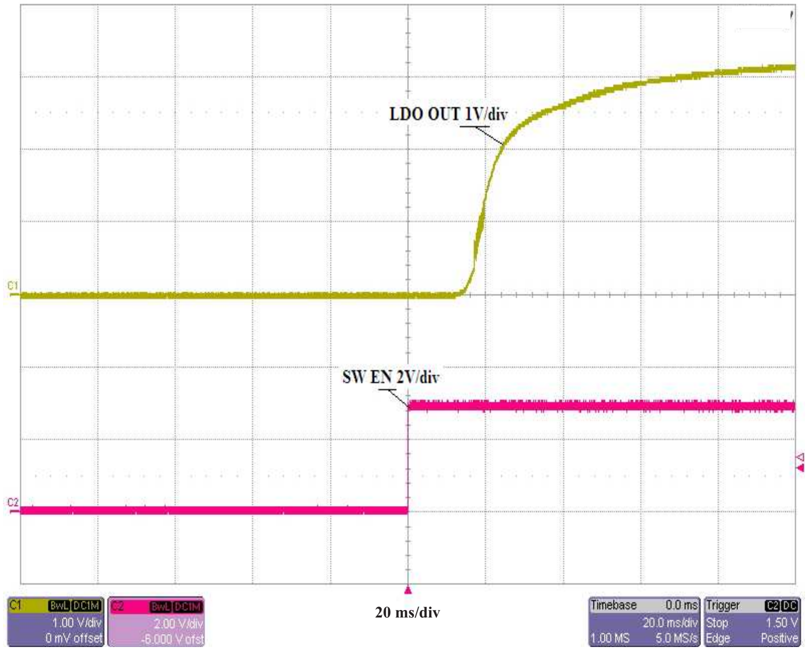

Figure 5. LDO Output Voltage Turn-on, SW Enable

4.4 Load Transient

Figure 6 shows the TPS54120 response to load transients. The current step is from 30% to 75% of the maximum rated load at 12 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output of both the switcher and the LDO.

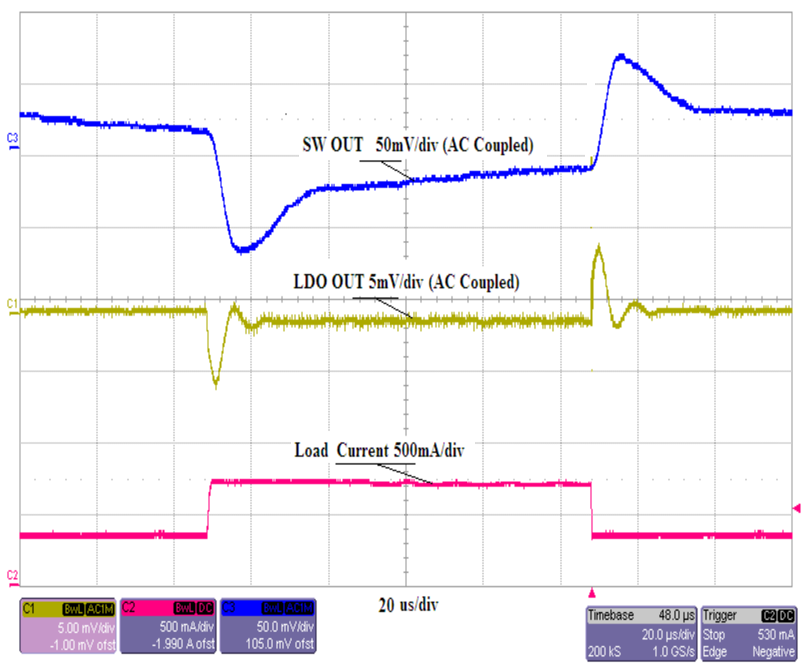

Figure 6. TPS54120 Transient Response

4.5 Efficiency

Figure 7 shows the efficiency for the TPS54120 at an ambient temperature of 25°C for Vin= 8V, 10V, 12V, and 15V. The switcher output voltage is set to 4.1V and the LDO is set to 3.3V.

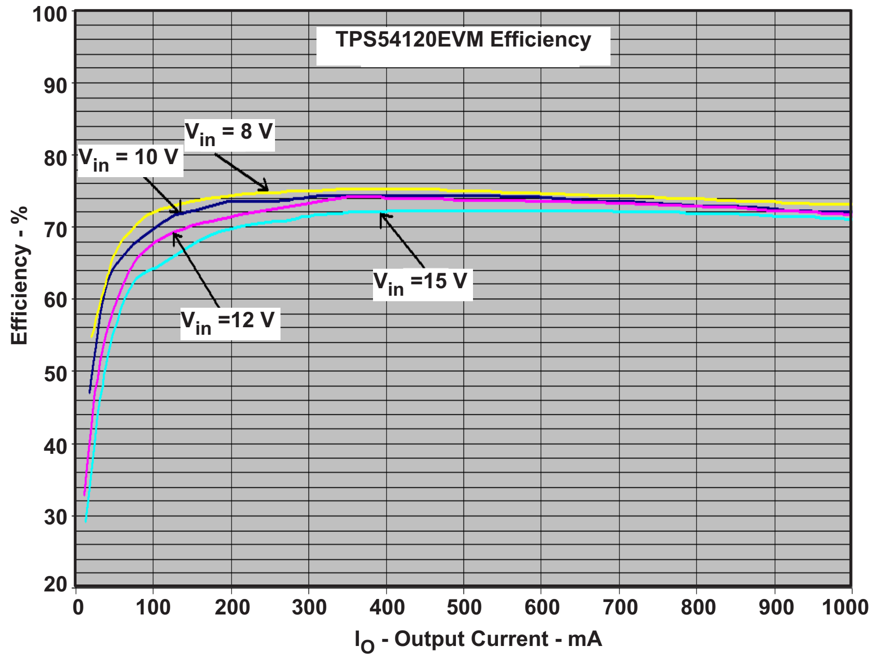

Figure 7. TPS54120 Efficiency

4.6 Thermal Characteristic

This section shows a thermal image of the TPS54120 running at 12 V input and 1A load, 3.3V LDO OUT, and 4.1V Switcher out. There is no air flow and the ambient temperature is 25°C. The peak temperature of the IC (56.4°C) is well below the maximum recommended operating condition listed in the data sheet of 150°C.

Figure 8. TPS54120 Thermal Image

5 Board Layout

This section provides a description of the TPS54120, board layout, and layer illustrations.

5.1 Layout Description

The board layout for the TPS54120 evaluation board is shown in Figure 9 through Figure 12. The board consists of 4 layers. It is laid out in such a way the analog ground of the LDO is shielded as much as possible from the noise of the switcher. Also, critical analog circuits such as the voltage set point divider, frequency set resistor, slow start capacitor and compensation components are terminated to ground using a via separate from the power ground pour. The topside layer of the EVM is laid out in a manner typical of a user application.

The top layer contains the analog ground of the LDO and a portion of the output power ground of the SW side. The first internal layer is connected to the power pad and the analog ground of the IC; mostly this layer is used for power dissipation. Only a few traces are implemented on this layer such as the LDO enable, and the PWRGD test point trace.

The second internal layer is mostly used for analog ground as well. For shielding the LDO ground from the switch node noise, a small isolated power ground plane is made in the center of this layer to reduce capacitive coupling with analog ground. This layer also contains the input voltage trace of the switcher connecting the input cap and the connector J3.

About one quarter of the bottom layer contains the main input power ground trace. In the center of the layer, the inductor (L1) and the output caps (C9, C10) of the switcher are located. The remaining surface area is connected to the analog ground of the top and the internal layers through vias. Some of these vias are directly under the TPS54120 device to provide a thermal path from the top-side ground plane to the internal and bottom-side ground plane.

The input decoupling capacitor of the SW (C5) is located as close as possible to the IC. PVIN and VIN are connected together in this EVM, and then through vias they are connected to the input voltage trace in the second internal layer. Whereas, the decoupling capacitor ground is connected through vias to the bottom layer. The compensation and the soft start capacitors (C6, C7 and C8), the CLK/RT resistor (R3), and the SW feedback resistor (R6) are grounded to a power ground trace in the center of the top layer. This helps shield them from noises of the high current ground plane.

The inductor (L1), the boot cap (C12), and the output caps of the SW (C9, C10) are placed on the bottom layer of the board to shield the switching noise into the LDO side. However, the boot cap (C12) and the inductor (L1) are connected through vias directly into the PH pin of the IC. This connects them as close as possible to the PH pin and reduces parasitic inductance of long traces. Also, the noise reduction capacitor (C13) is placed as close as possible to the IC.

The input of the LDO is connected to the output of the switcher using a shorting jumper and a long trace parallel with the trace that connects the ground on the LDO with the ground of the switcher. Critical analog ground of the LDO circuits such as the voltage set point divider, the LDO input, and output caps are terminated to ground using a wide ground trace separate from the power ground pour. In addition, the input and the output LDO capacitors are kept close to the IC. The voltage divider network of the LDO ties to the LDO output voltage at the copper of the LDO output trace.

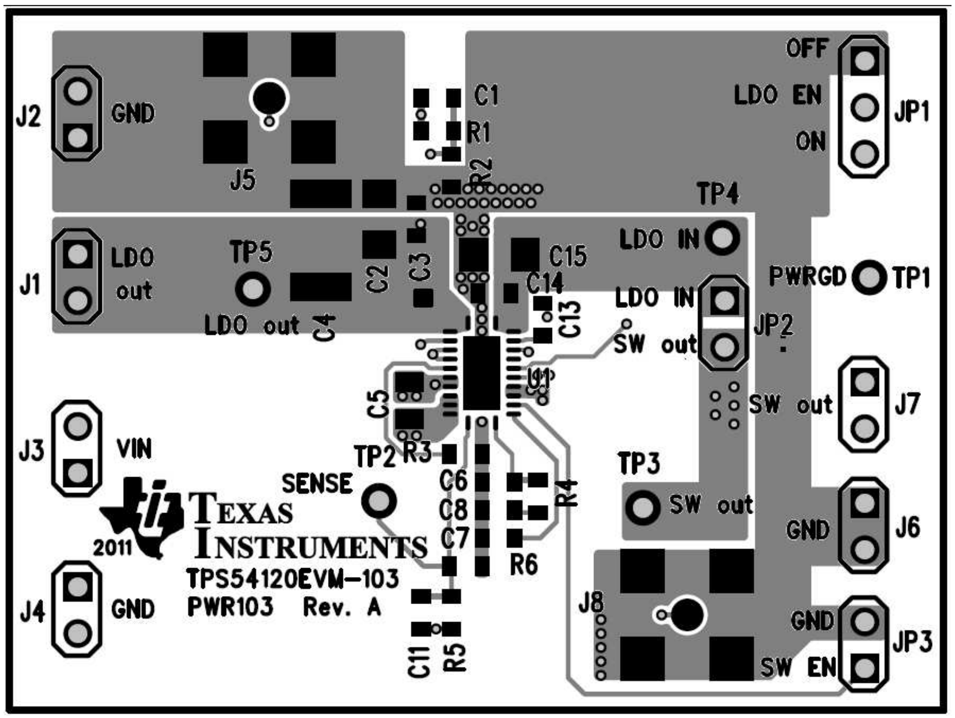

Figure 9. Top Side Silkscreen and Routing

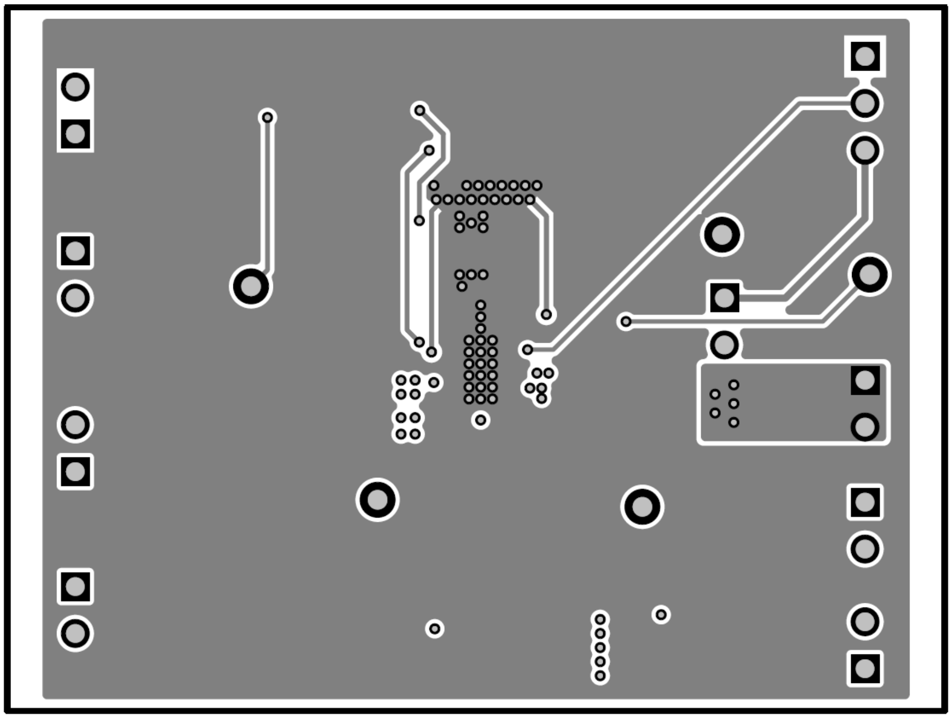

Figure 10. Second Layer (Internal) Routing

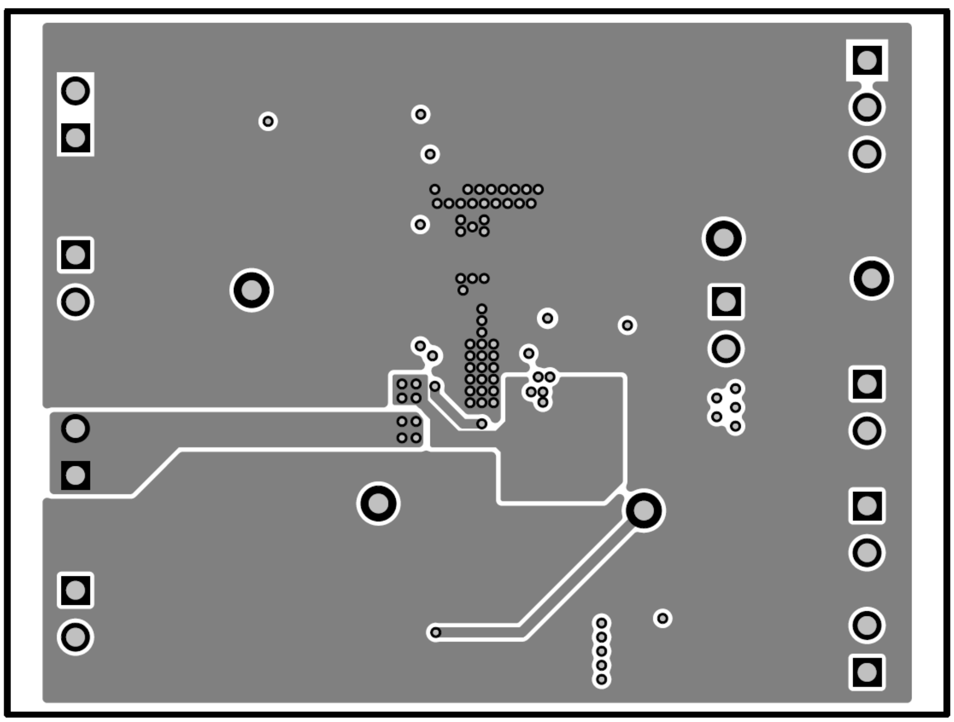

Figure 11. Third Layer (Internal) Routing

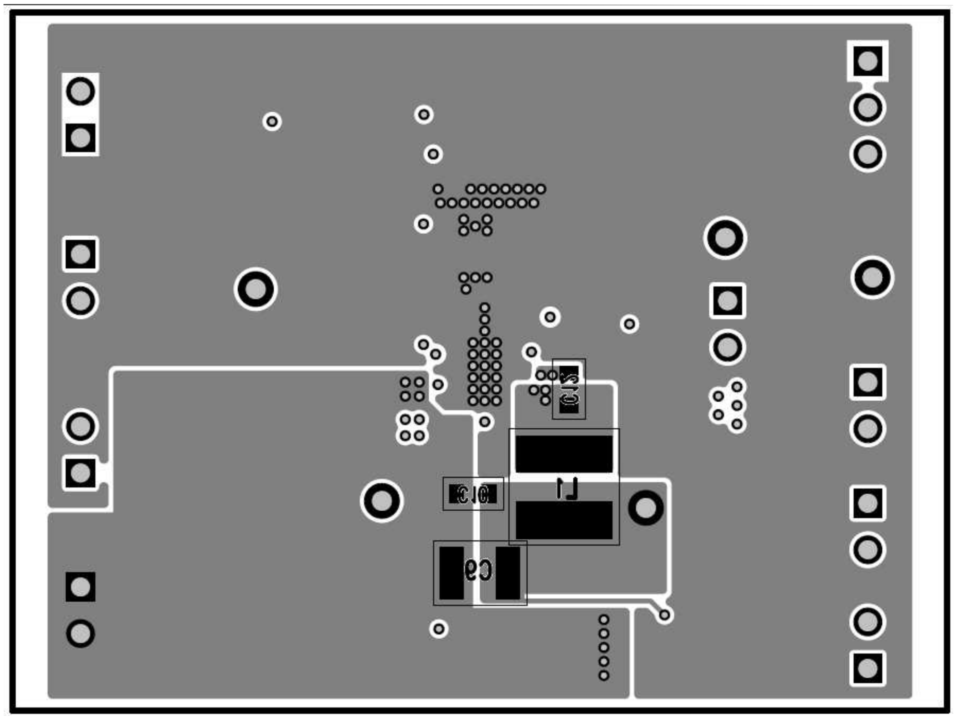

Figure 12. Bottom Layer Silkscreen and Routing

6 Schematic

Figure 13 is the schematic for the TPS54120 evaluation board.

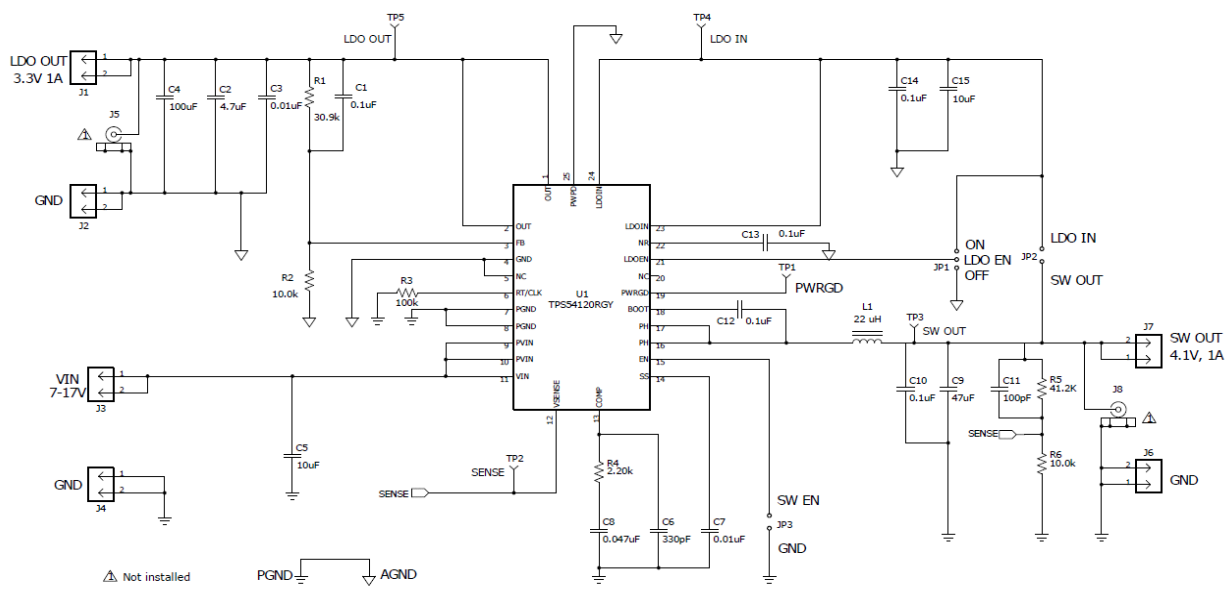

Figure 13. Schematic

7 Bill of Materials

Table 4 presents the bill of materials for the TPS54120 evaluation board.

Table 4. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
5	C1, C10 C12–C14	0.1uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	STD	STD
1	C11	100pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	STD	STD
1	C15	10uF	Capacitor, Ceramic, 6.3V, X7R, 10%	1206	STD	STD
1	C2	4.7uF	Capacitor, Ceramic, 10V, X7R, 10%	1206	STD	STD
2	C3, C7	0.01uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	STD	STD
1	C4	100uF	Capacitor, Ceramic, 6.3V, 20%, X5R	1812	STD	STD
1	C5	10uF	Capacitor, Ceramic, 25V, X5R, 10%	0805	STD	STD
1	C6	330pF	Capacitor, Ceramic, 25V, X7R, 10%	0603	STD	STD
1	C8	0.047uF	Capacitor, Ceramic, 25V, X7R, 10%	0603	STD	STD
1	C9	47uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	STD	STD
6	J1-4 J6-7	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
0	J5 J8	Open	Connector, SMT Straight, Jack Receptacle	0.250 SQ	142-0711-201	Johnson
1	JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
2	JP2-3	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	22 uH	Inductor, SMT, Power Choke 1.1A, ±20%	4838	74408943220	WE
1	R1	30.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R6	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	2.20k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	41.2K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
5	TP1-5	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch		Keystone
1	U1	TPS54120RGY	IC, Integrated SWITCHER and LDO Low Noise 1A Power Supply	QFN-24	TPS54120RGY	TI
3	—		Shunt, 100-mil, Black	0.100	929950-00	3M
1			PCB, 2.0" x 1.5" x 0.031"		PWR103	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 7 V to 17 V and the output voltage range of 0.8 V to 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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【ご使用にあたっての注】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

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2. 実験局の免許を取得後ご使用いただく。
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なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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