

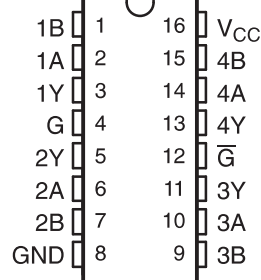
FEATURES

- Controlled Baseline
 - One Assembly
 - One Test Site
 - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree ⁽¹⁾
- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Low Power, $I_{CC} = 10\text{ mA Typ}$
- $\pm 7\text{ V Common-Mode Range With } \pm 200\text{ mV Sensitivity}$
- Input Hysteresis . . . 60 mV Typ
- $t_{pd} = 17\text{ ns Typ}$
- Operates From a Single 5 V Supply
- 3-State Outputs
- Input Fail-Safe Circuitry
- Improved Replacements for AM26LS32

AM26C32... D PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The AM26C32 is a quadruple differential line receiver for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design specifies that if the inputs are open, the outputs always are high.

The AM26C32 devices are manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32, while maintaining ac and dc performance.

The AM26C32 is characterized for operation over the extended temperature range of -55°C to 125°C .

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOIC – D	Reel of 2500	AM26C32MDREP	26C32EP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AM26C32-EP

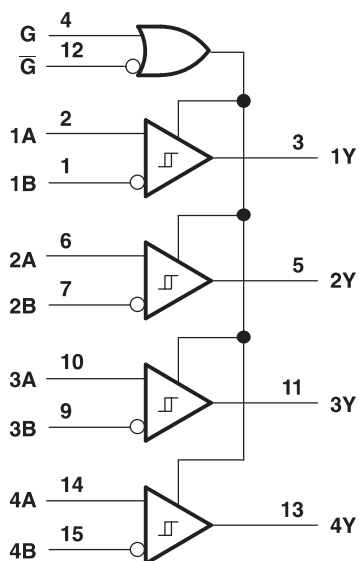
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS870–NOVEMBER 2007

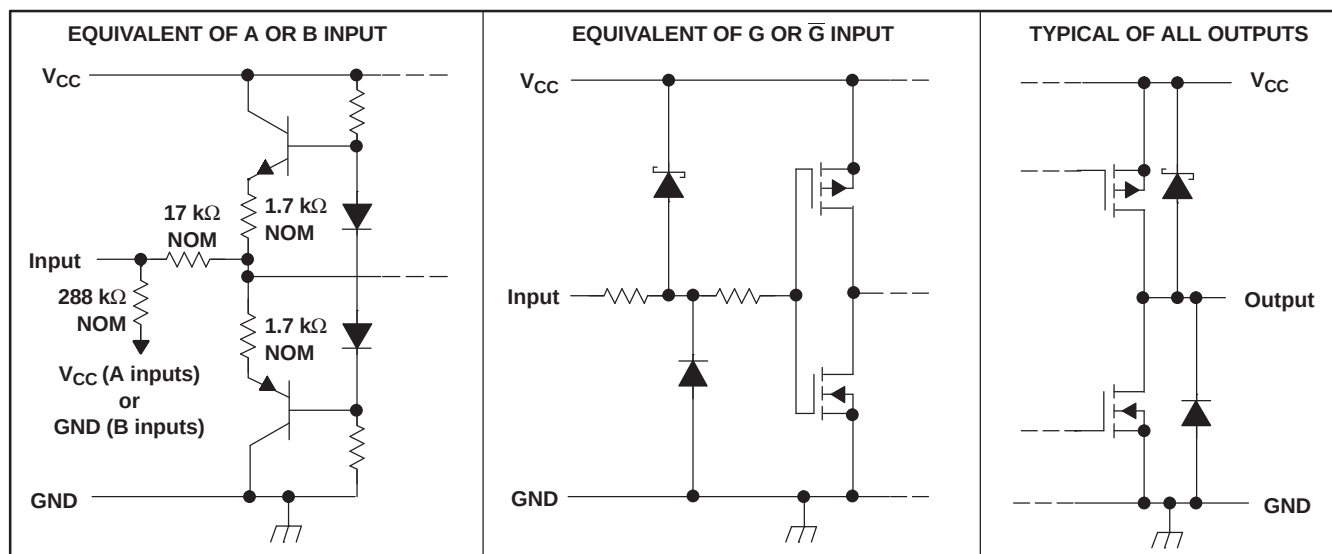
FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS



AM26C32-EP

QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS870–NOVEMBER 2007

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾		7	V
V_I	Input voltage range	A or B inputs		–11 14 V
		G or $\overline{G}$ inputs		–0.5 $V_{CC} + 0.5$ V
V_{ID}	Differential input voltage range	–14	14	V
V_O	Output voltage range	–0.5	$V_{CC} + 0.5$	V
I_O	Output current		±25	mA
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package		73 °C/W
		PW package		108
T_J	Operating virtual junction temperature		150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential output voltage, V_{OD} , are with respect to network GND. Currents into the device are positive and currents out of the device are negative.
- (3) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{IC}	Common-mode input voltage			±7	V
I_{OH}	High-level output current			–6	mA
I_{OL}	Low-level output current			6	mA
T_A	Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of V_{CC} , V_{IC} , and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+} Differential input high-threshold voltage	$V_O = V_{OH} \text{ (min),}$	$V_{IC} = -7 \text{ V to } 7 \text{ V}$			0.2	V
	$I_{OH} = -440 \text{ }\mu\text{A}$	$V_{IC} = 0 \text{ to } 5.5 \text{ V}$			0.1	
V_{IT-} Differential input low-threshold voltage	$V_O = 0.45 \text{ V,}$	$V_{IC} = -7 \text{ V to } 7 \text{ V}$			-0.2 ⁽²⁾	V
	$I_{OL} = 8 \text{ mA}$	$V_{IC} = 0 \text{ to } 5.5 \text{ V}$			-0.1 ⁽²⁾	
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK} Enable input clamp voltage	$V_{CC} = 4.5 \text{ V,}$	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 200 \text{ mV,}$	$I_{OH} = -6 \text{ mA}$	3.8			V
V_{OL} Low-level output voltage	$V_{ID} = -200 \text{ mV,}$	$I_{OL} = 6 \text{ mA}$		0.2	0.3	V
I_{OZ} Off-state (high-impedance state) output current	$V_O = V_{CC} \text{ or GND}$			± 0.5	± 5	μA
I_I Line input current	$V_I = 10 \text{ V,}$	Other input at 0 V			1.5	mA
	$V_I = -10 \text{ V,}$	Other input at 0 V			-2.5	
I_{IH} High-level enable current	$V_I = 2.7 \text{ V}$				20	μA
I_{IL} Low-level enable current	$V_I = 0.4 \text{ V}$				-100	μA
r_I Input resistance	One input to ground		12	17		k Ω
I_{CC} Supply current	$V_{CC} = 5.5 \text{ V}$			10	15	mA

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $V_{IC} = 0$, and $T_A = 25^\circ\text{C}$.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

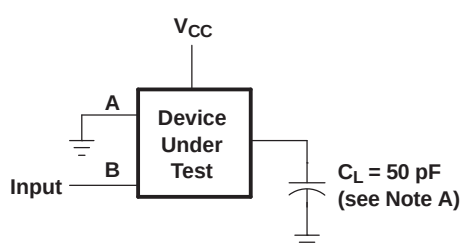
SWITCHING CHARACTERISTICS

over recommended ranges of operation conditions, $C_L = 50 \text{ pF}$ (unless otherwise noted)

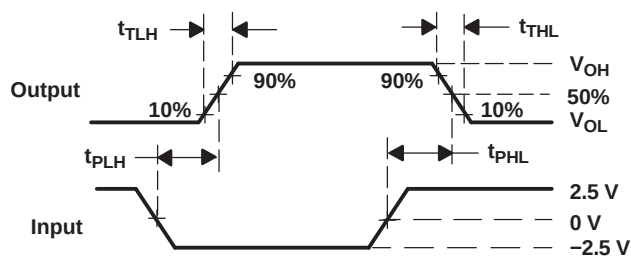
PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	See Figure 1	9	17	27	ns
t_{PHL} Propagation delay time, high- to low-level output		9	17	27	ns
t_{TLH} Output transition time, low- to high-level output	See Figure 1		4	10	ns
t_{THL} Output transition time, high- to low-level output			4	9	ns
t_{PZH} Output enable time to high level	See Figure 2		13	22	ns
t_{PZL} Output enable time to low level			13	22	ns
t_{PHZ} Output disable time from high level	See Figure 2		13	26	ns
t_{PLZ} Output disable time from low level			13	25	ns

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



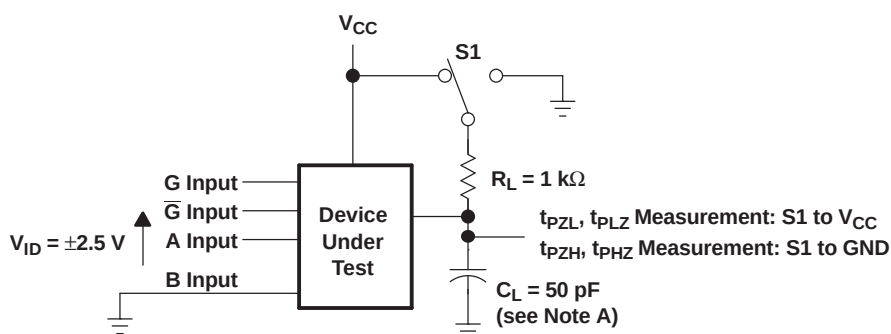
TEST CIRCUIT



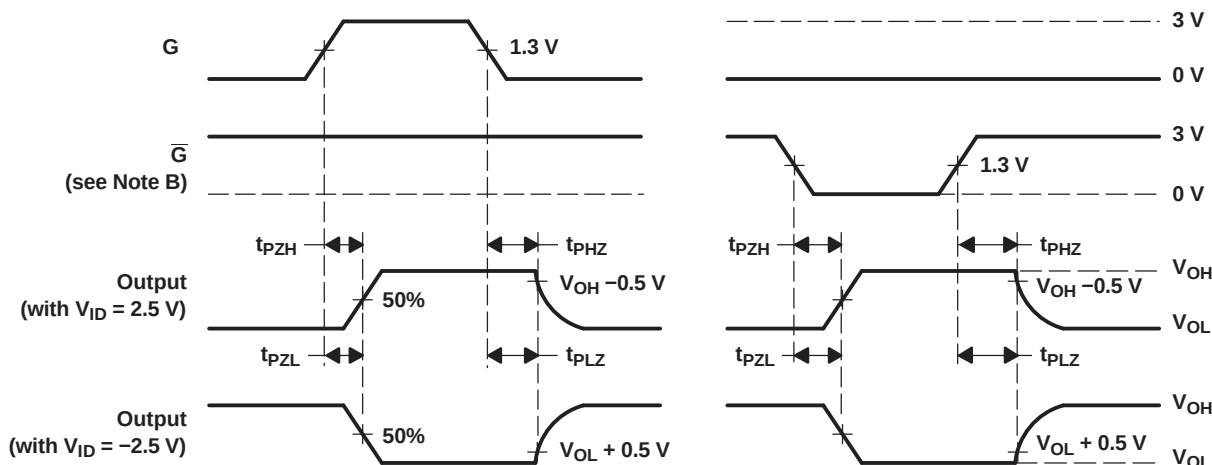
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

Figure 1. Switching Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle $\leq$ 50%, $t_r = t_f = 6$ ns.

Figure 2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C32MDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	Call TI NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C32EP	Samples
V62/07648-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C32EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

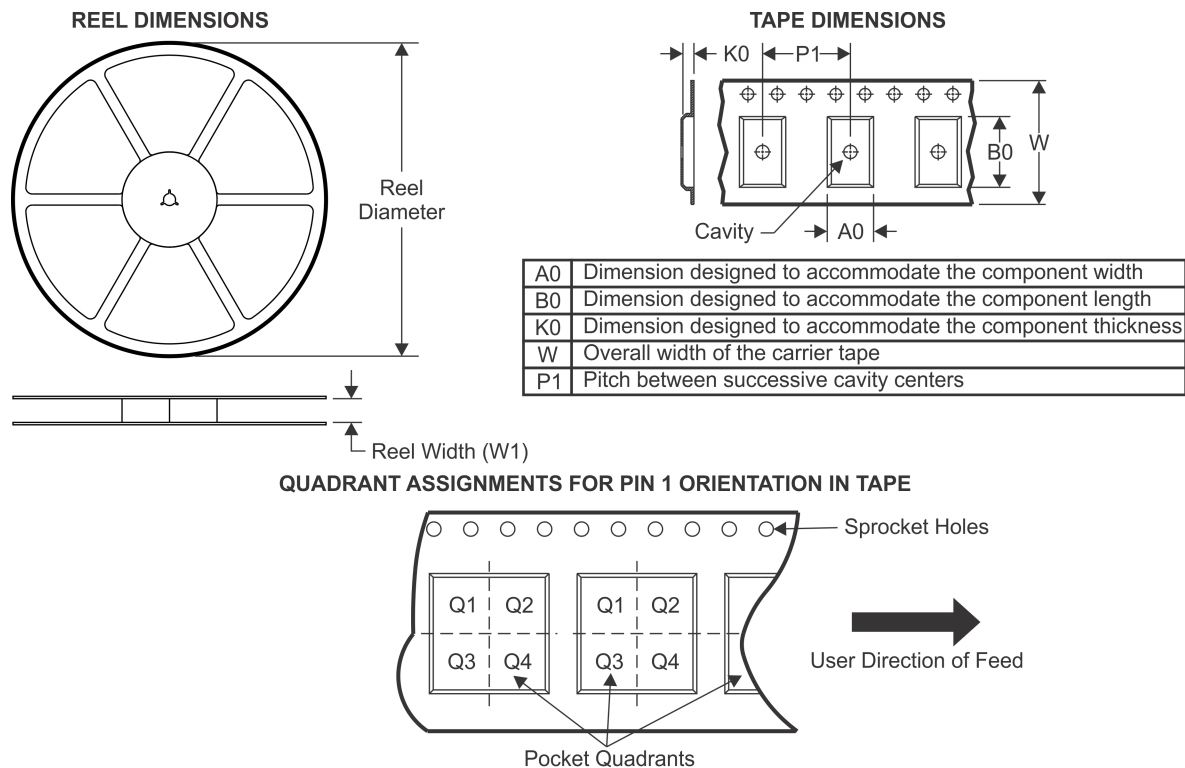
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM26C32-EP :

- Catalog: [AM26C32](#)
- Military: [AM26C32M](#)

NOTE: Qualified Version Definitions:

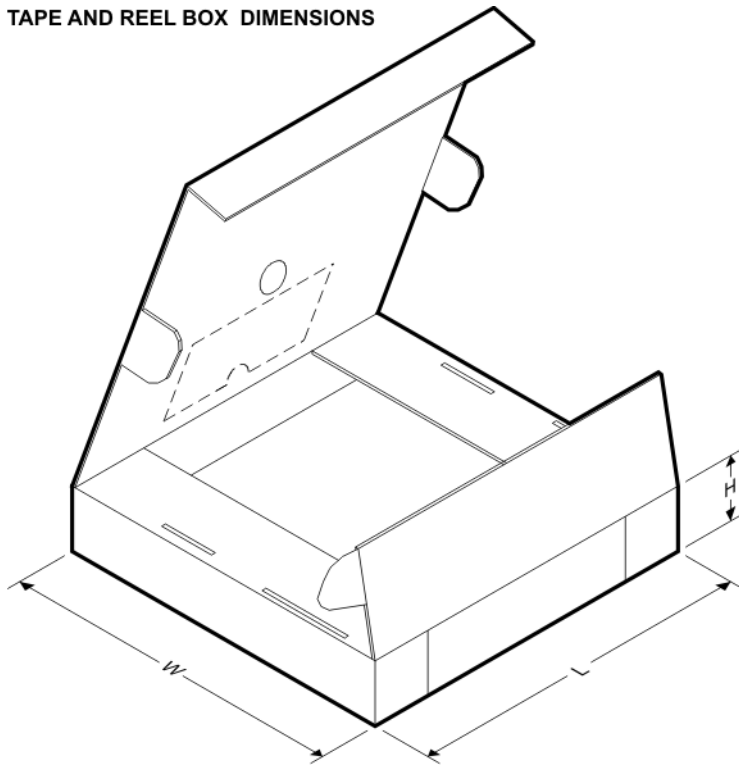
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C32MDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

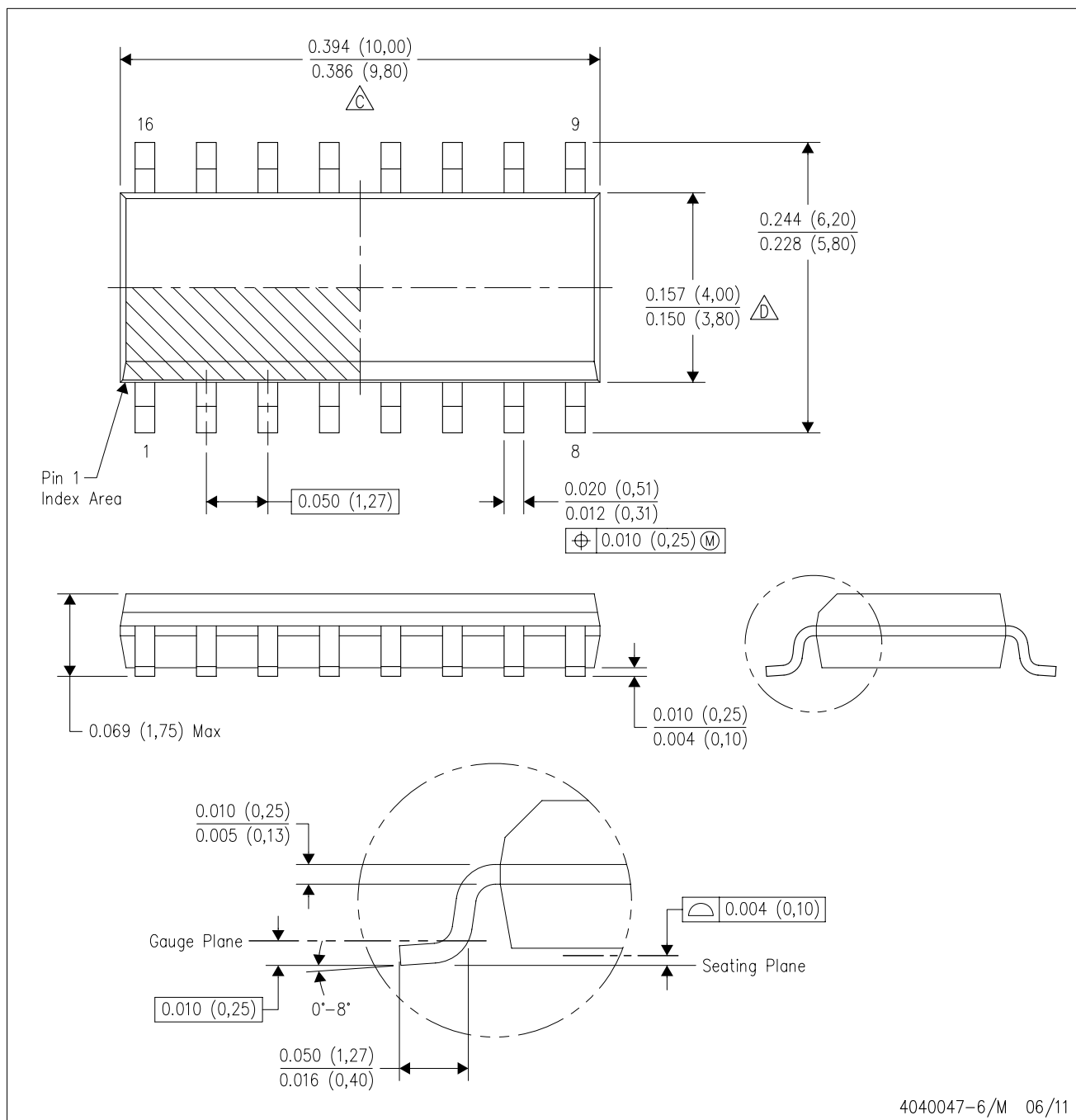


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C32MDREP	SOIC	D	16	2500	346.0	346.0	33.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated