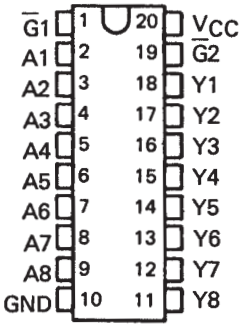
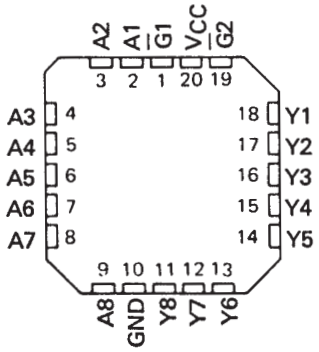
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

SN54LS540, SN54LS541 . . . J OR W PACKAGE
SN74LS540, SN74LS541 . . . DW OR N PACKAGE
(TOP VIEW)




SN54LS540, SN54LS541 . . . FK PACKAGE
(TOP VIEW)




## description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

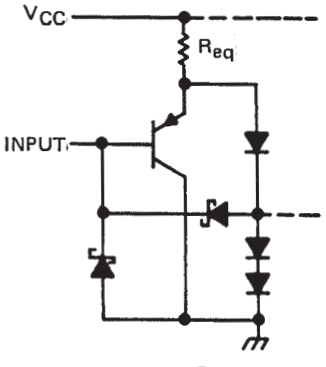
The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LS540 and SN74LS541 are characterized for operation from 0°C to 70°C.

| TYPE | RATED $I_{OL}$ (SINK CURRENT) | RATED $I_{OH}$ (SOURCE CURRENT) | TYPICAL POWER DISSIPATION (ENABLED) 'LS540 | 'LS541 |
|---|---|---|---|---|
| SN54LS' | 12 mA | – 12 mA | 92.5 mW | 120 mW |
| SN74LS' | 24 mA | – 15 mA | 92.5 mW | 120 mW |

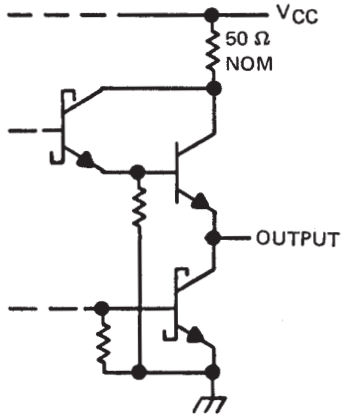
## schematics of inputs and outputs

EQUIVALENT OF EACH INPUT




Enable Inputs: $R_{eq}$ = 9 kΩ NOM
All Other Inputs: $R_{eq}$ = 10 kΩ NOM

TYPICAL OF ALL OUTPUTS

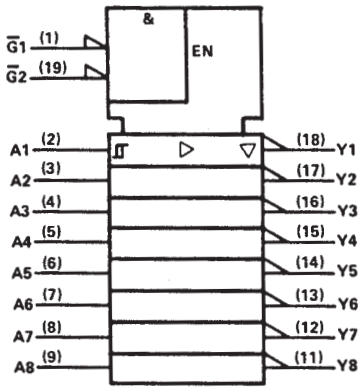



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

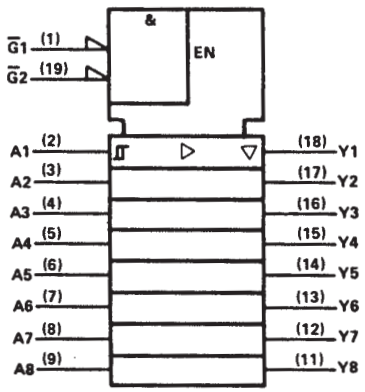
Copyright © 1988, Texas Instruments Incorporated

## logic symbols†

'LS540



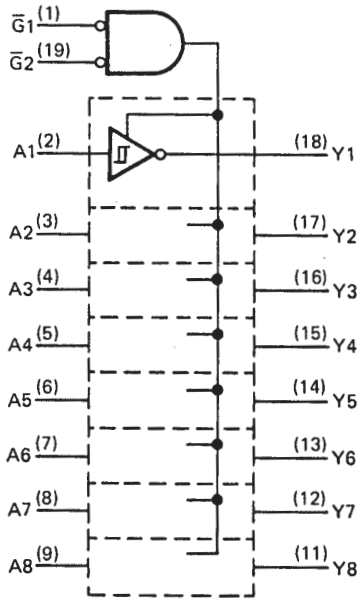

'LS541



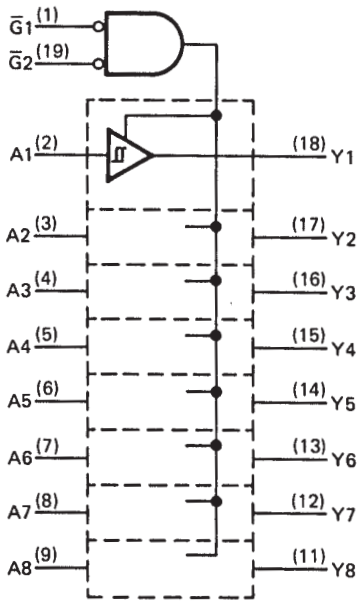

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

'LS540




'LS541




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS540, SN54LS541 . . . . . −55°C to 125°C
SN74LS540, SN74LS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

## recommended operating conditions

| PARAMETER | SN54LS' | | | SN74LS' | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ (see Note 1) | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −12 | | | −15 | mA |
| Low-level output current, $I_{OL}$ | | | 12 | | | 24 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

NOTE 1: Voltage values are with respect to network ground terminal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS' | | | SN74LS' | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.6 | | | 0.6 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| | Hysteresis ($V_{T+} - V_{T-}$) | $V_{CC}$ = MIN | | 0.2 | 0.4 | | 0.2 | 0.4 | | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = −3 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | $V_{CC}$ = MIN, $V_{IL}$ = 0.5 V, | $V_{IH}$ = 2V, $I_{OH}$ = MAX | 2 | | | 2 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | Off-state output current, high-level voltage applied | $V_{CC}$ = MAX, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $V_O$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{OZL}$ | Off-state output current, low-level voltage applied | | $V_O$ = 0.4 V | | | −20 | | | −20 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current, any input | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −0.2 | | | −0.2 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | −40 | | −225 | −40 | | −225 | mA |
| $I_{CC}$ | Supply current | Outputs high | 'LS540 | $V_{CC}$ = MAX, Outputs open | | 13 | 25 | | 13 | 25 | mA |
| | | | 'LS541 | | | 18 | 32 | | 18 | 32 | |
| | | Outputs low | 'LS540 | | | 24 | 45 | | 24 | 45 | |
| | | | 'LS541 | | | 30 | 52 | | 30 | 52 | |
| | | All outputs disabled | 'LS540 | | | 30 | 52 | | 30 | 52 | |
| | | | 'LS541 | | | 32 | 55 | | 32 | 55 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | 'LS540 | | | 'LS541 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 45 pF, $R_L$ = 667 Ω, See Note 2 | | 9 | 15 | | 9 | 15 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 9 | 15 | | 10 | 18 | ns |
| $t_{PZL}$ | Output enable time to low level | | | 25 | 38 | | 25 | 38 | ns |
| $t_{PZH}$ | Output enable time to high level | | | 15 | 25 | | 20 | 32 | ns |
| $t_{PLZ}$ | Output disable time from low level | $C_L$ = 5 pF, $R_L$ = 667 Ω, See Note 2 | | 10 | 18 | | 10 | 18 | ns |
| $t_{PHZ}$ | Output disable time from high level | | | 15 | 25 | | 18 | 29 | ns |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 84155012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84155012A SNJ54LS 540FK | Samples |
| 8415501RA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415501RA SNJ54LS540J | Samples |
| 8415501RA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415501RA SNJ54LS540J | Samples |
| 8415601SA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415601SA SNJ54LS541W | Samples |
| 8415601SA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415601SA SNJ54LS541W | Samples |
| JM38510/32404B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32404B2A | Samples |
| JM38510/32404B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32404B2A | Samples |
| JM38510/32404BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32404BRA | Samples |
| JM38510/32404BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32404BRA | Samples |
| JM38510/32405BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32405BRA | Samples |
| JM38510/32405BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32405BRA | Samples |
| M38510/32404B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32404B2A | Samples |
| M38510/32404B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32404B2A | Samples |
| M38510/32404BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32404BRA | Samples |
| M38510/32404BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32404BRA | Samples |
| M38510/32405BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32405BRA | Samples |
| M38510/32405BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 32405BRA | |
| SN54LS540J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS540J | Samples |
| SN54LS540J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS540J | Samples |
| SN54LS541J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS541J | Samples |
| SN54LS541J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS541J | Samples |
| SN74LS540DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS540 | Samples |
| SN74LS540DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS540 | Samples |
| SN74LS540DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS540 | Samples |
| SN74LS540DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS540 | Samples |
| SN74LS540DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS540 | Samples |
| SN74LS540DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS540 | Samples |
| SN74LS540N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS540N | Samples |
| SN74LS540N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS540N | Samples |
| SN74LS540NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS540 | Samples |
| SN74LS540NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS540 | Samples |
| SN74LS541DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS541 | Samples |
| SN74LS541DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS541 | Samples |
| SN74LS541DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS541 | Samples |
| SN74LS541DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS541 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS541DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS541 | Samples |
| SN74LS541DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS541 | Samples |
| SN74LS541N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS541N | Samples |
| SN74LS541N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS541N | Samples |
| SN74LS541NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS541N | Samples |
| SN74LS541NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS541N | Samples |
| SN74LS541NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS541 | Samples |
| SN74LS541NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS541 | Samples |
| SN74LS541NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS541 | Samples |
| SN74LS541NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS541 | Samples |
| SNJ54LS540FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84155012A SNJ54LS 540FK | Samples |
| SNJ54LS540FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84155012A SNJ54LS 540FK | Samples |
| SNJ54LS540J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415501RA SNJ54LS540J | Samples |
| SNJ54LS540J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415501RA SNJ54LS540J | Samples |
| SNJ54LS541J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54LS541J | Samples |
| SNJ54LS541J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54LS541J | Samples |
| SNJ54LS541W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415601SA SNJ54LS541W | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54LS541W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8415601SA SNJ54LS541W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LS540, SN54LS541, SN74LS540, SN74LS541 :**

- Catalog: SN74LS540, SN74LS541

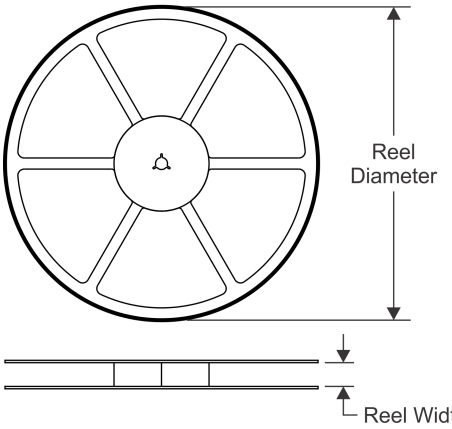
- Military: SN54LS540, SN54LS541

NOTE: Qualified Version Definitions:

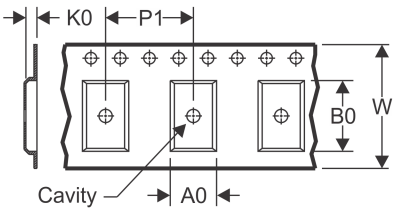
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

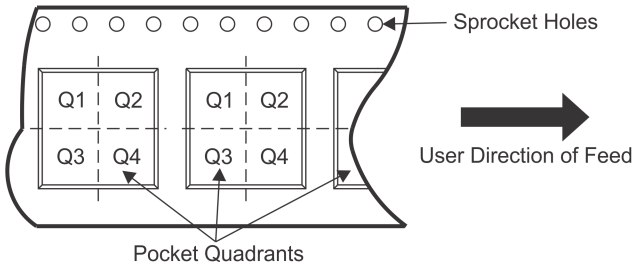



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

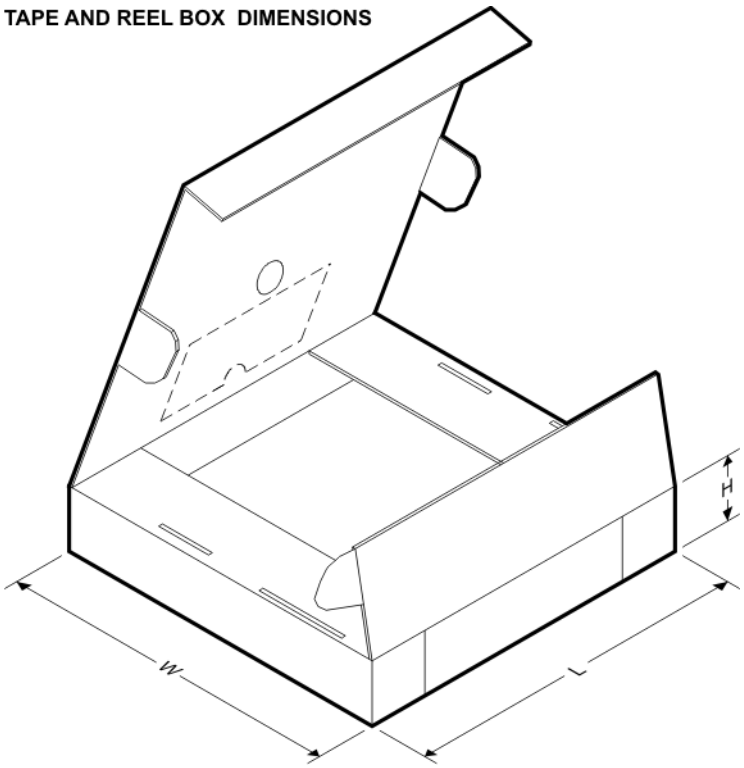
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS540DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS540DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS540NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS541DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS541NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

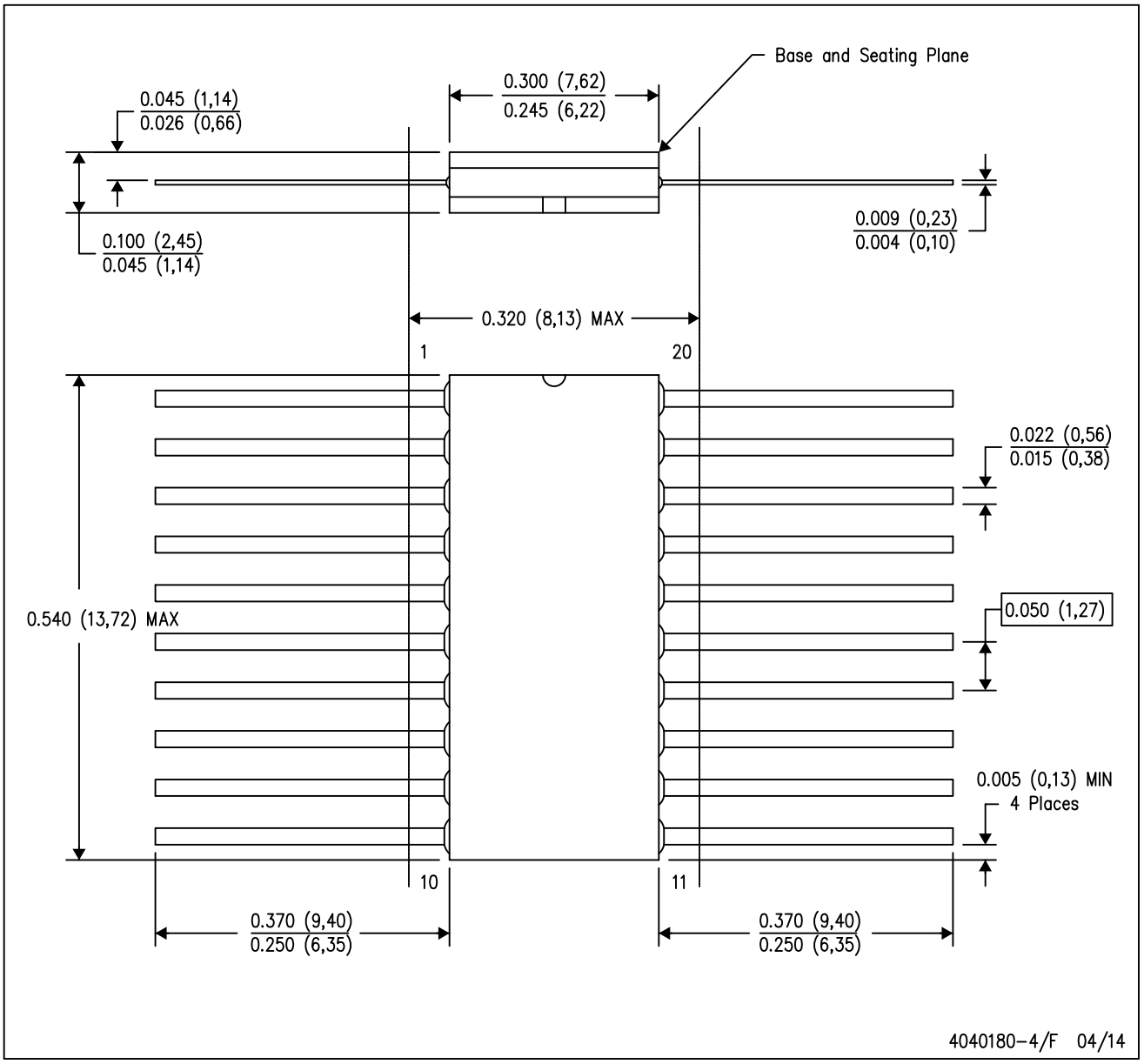
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS540DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LS540DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS540NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS541DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS541NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

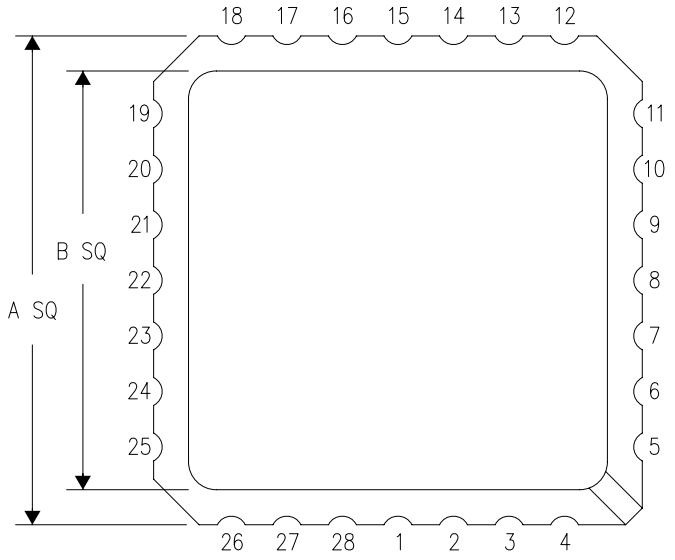
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



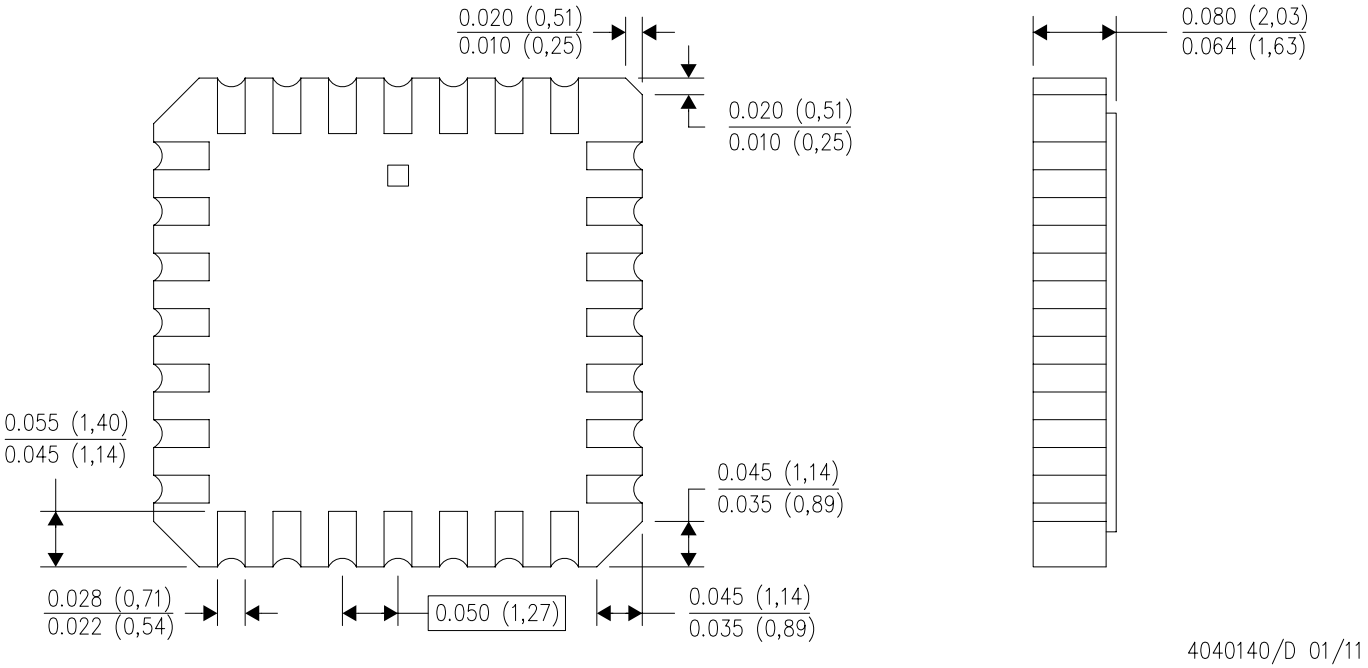

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

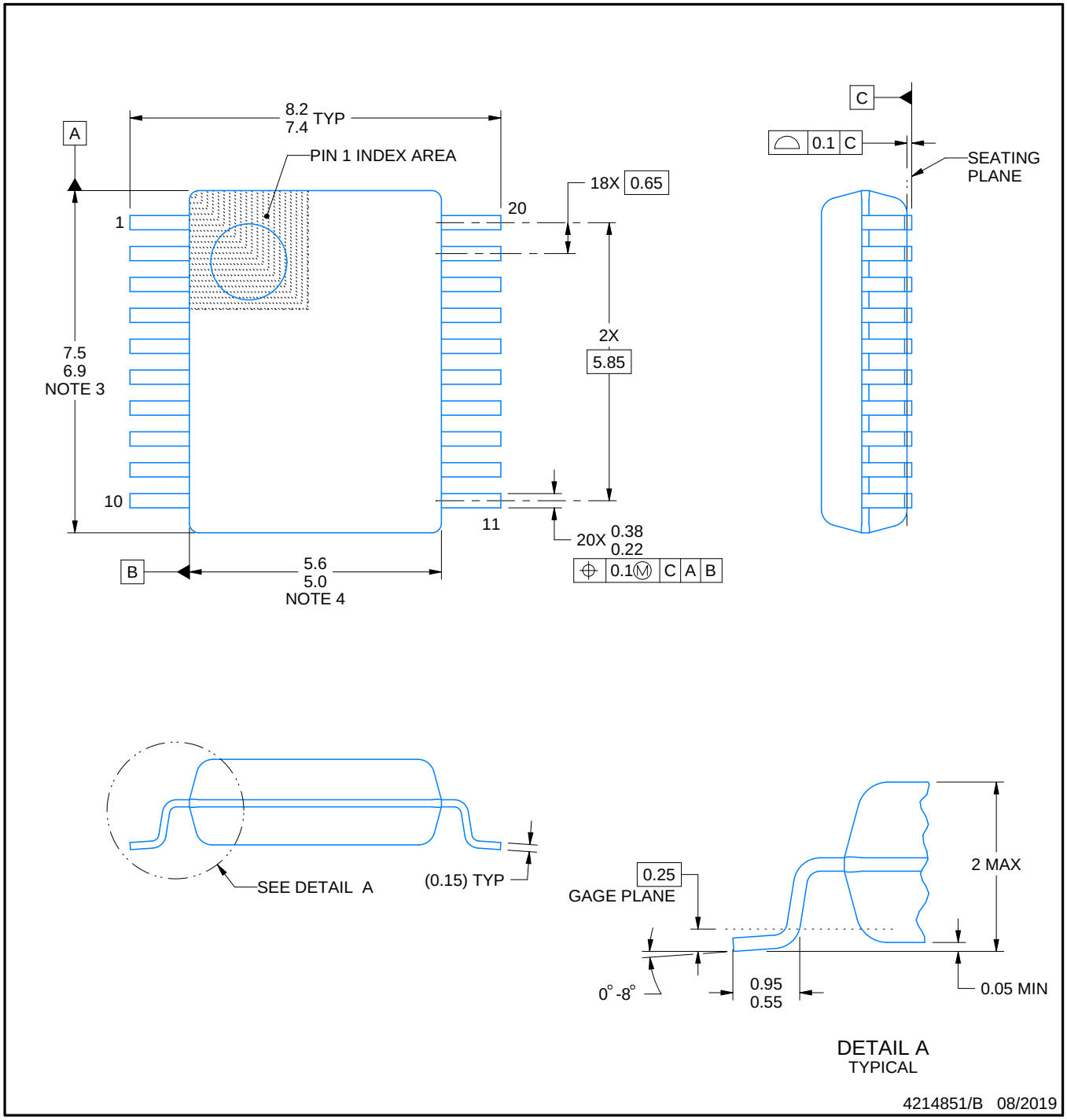
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

# PACKAGE OUTLINE

## DB0020A

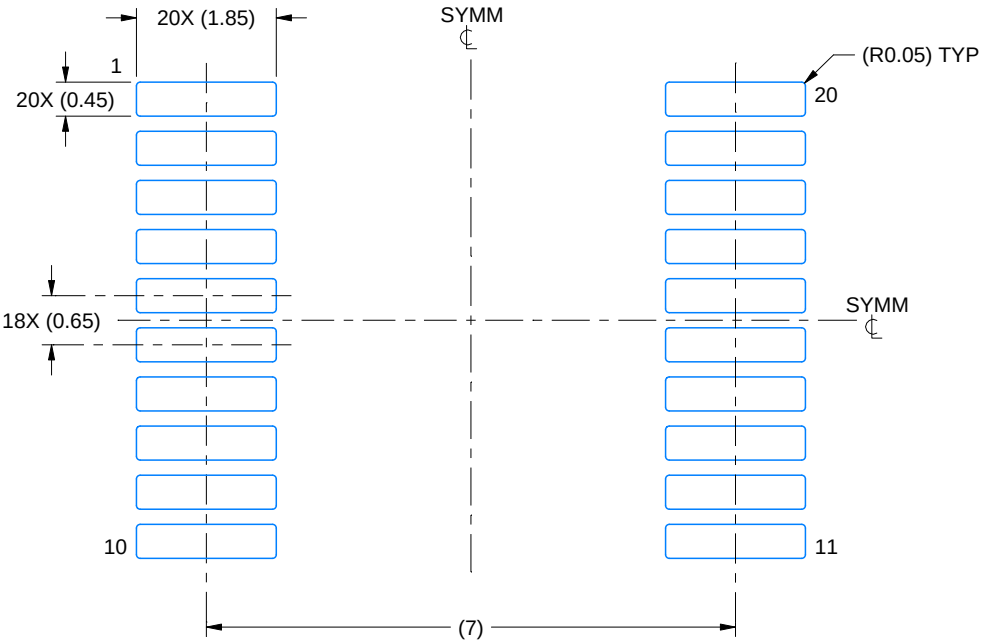
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

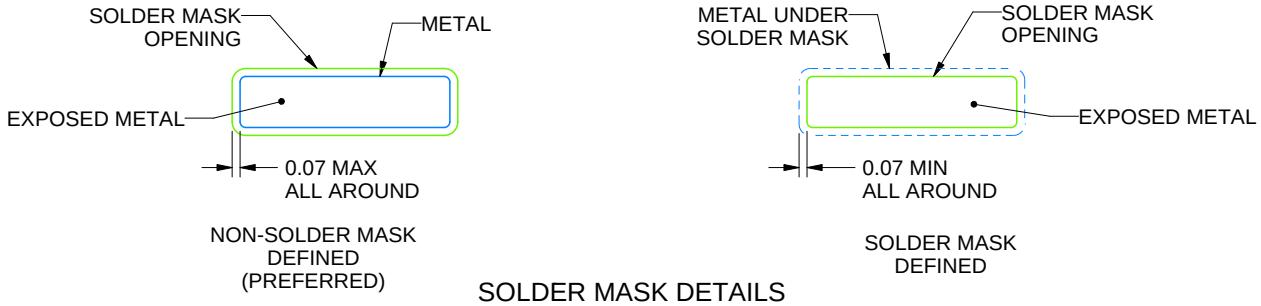



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

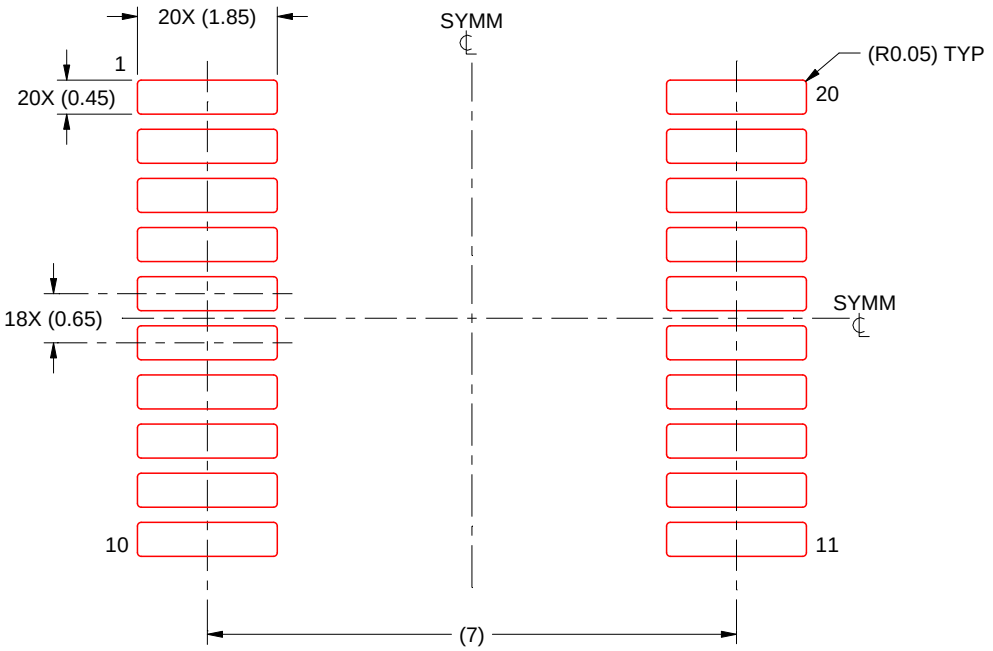
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

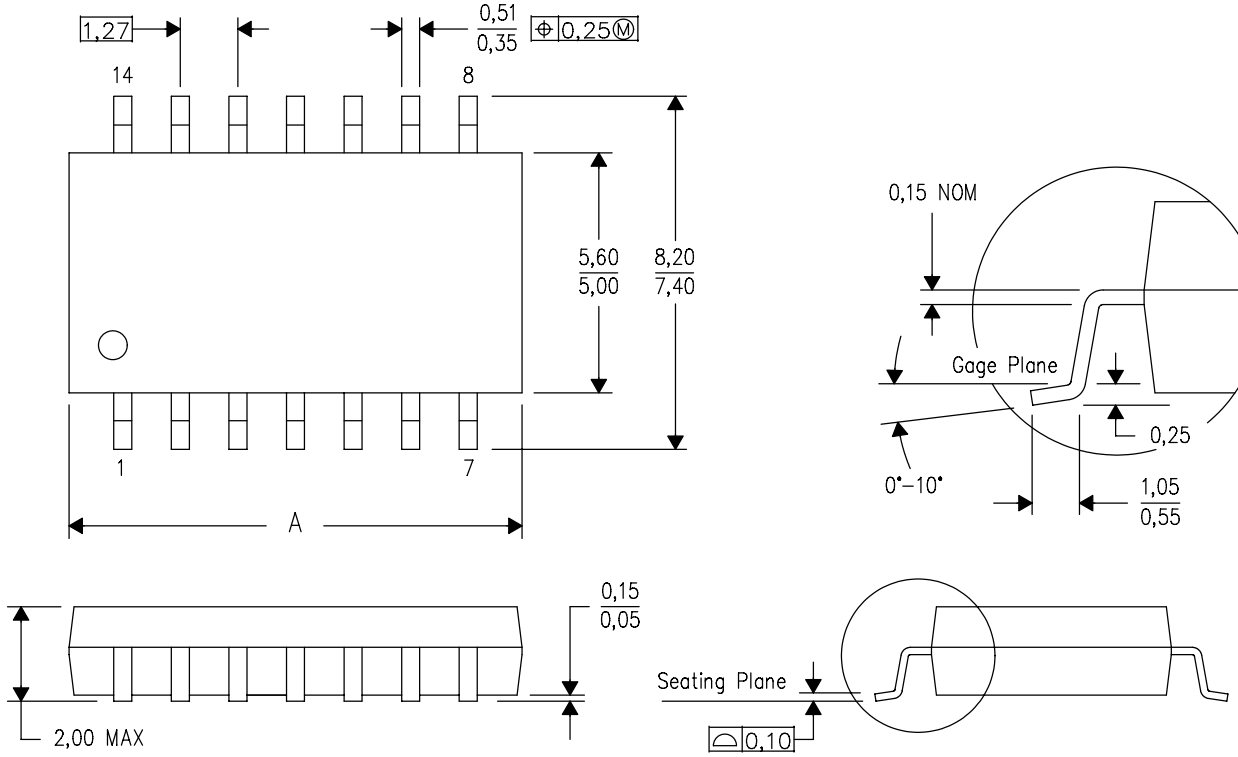
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

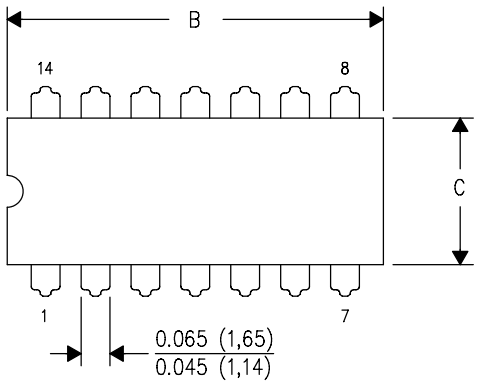
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

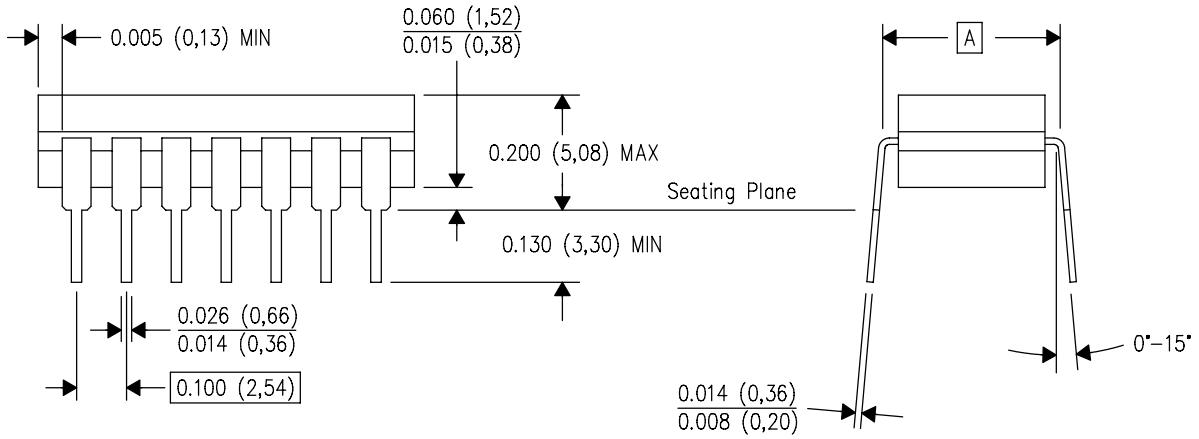
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



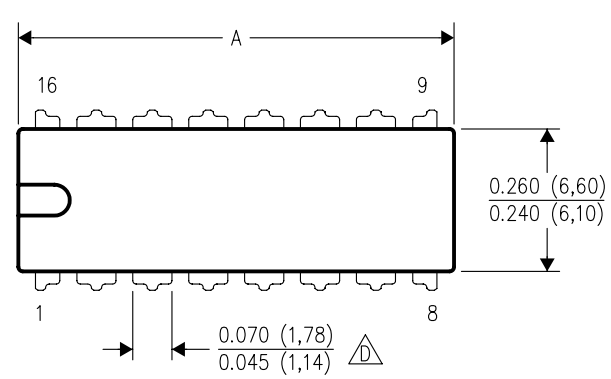

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

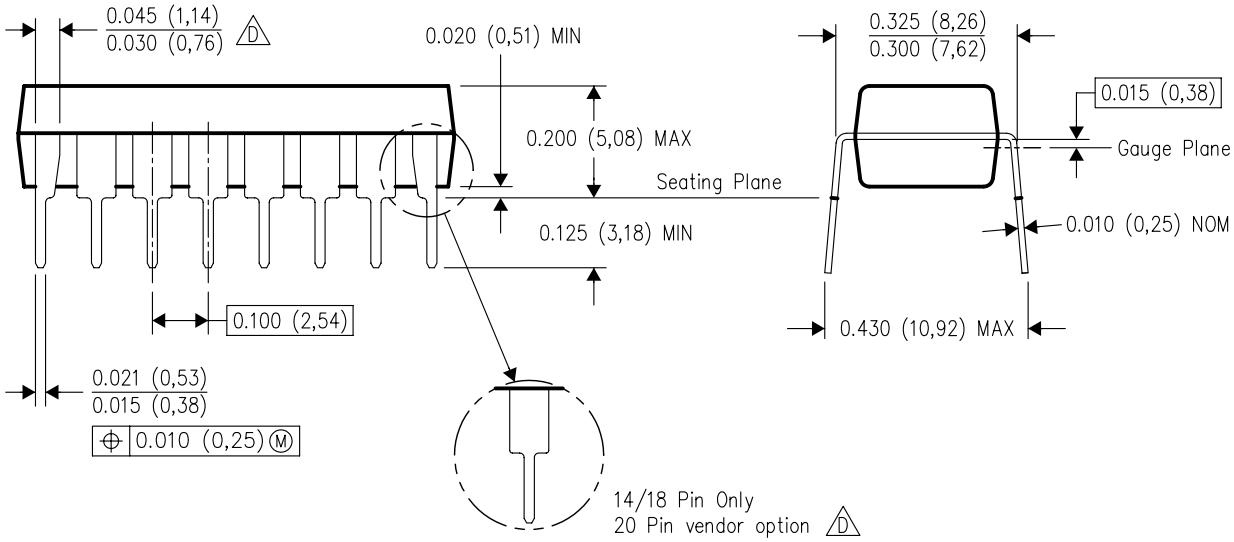
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

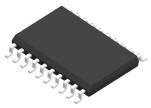



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

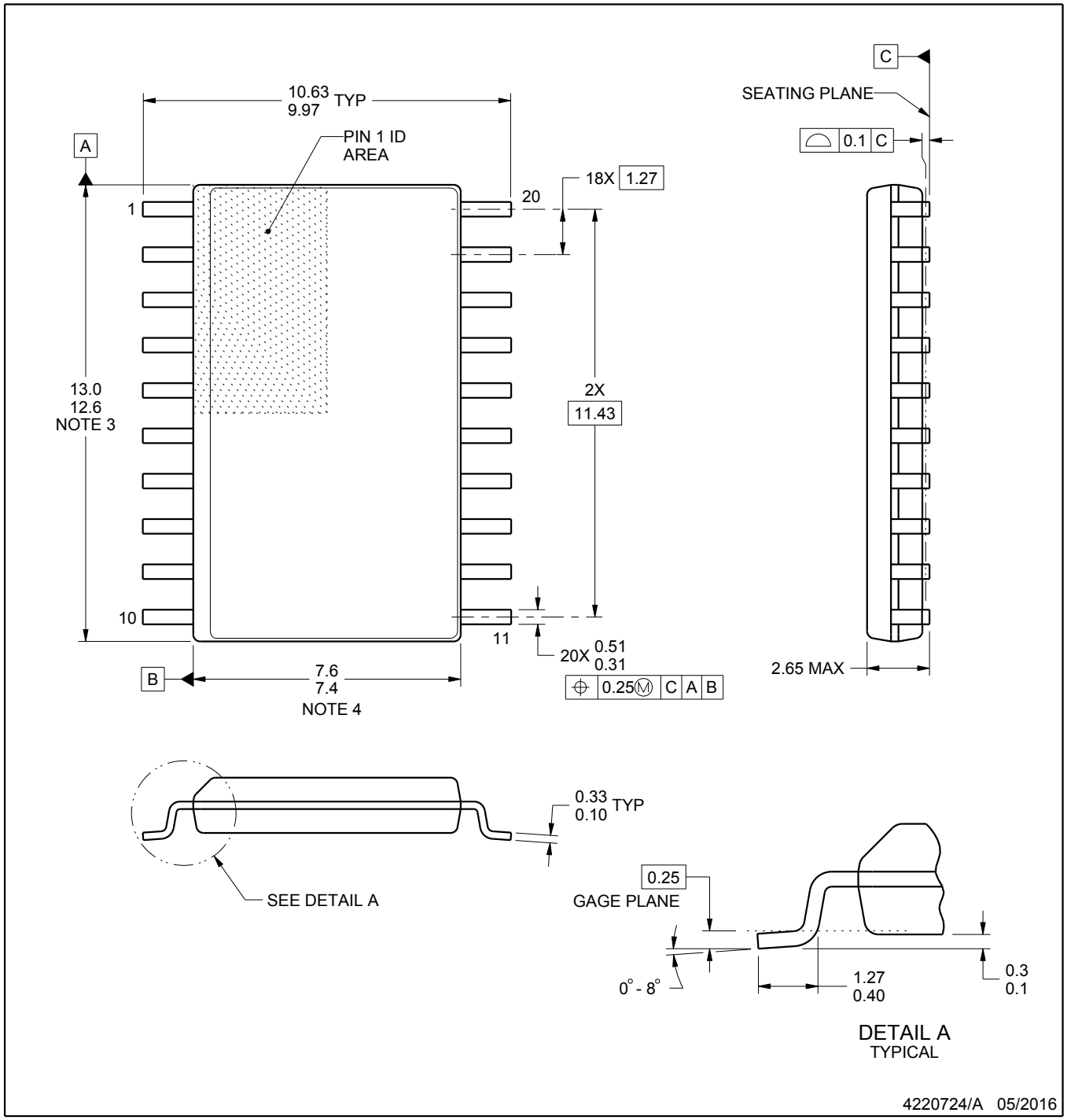


# PACKAGE OUTLINE

## DW0020A

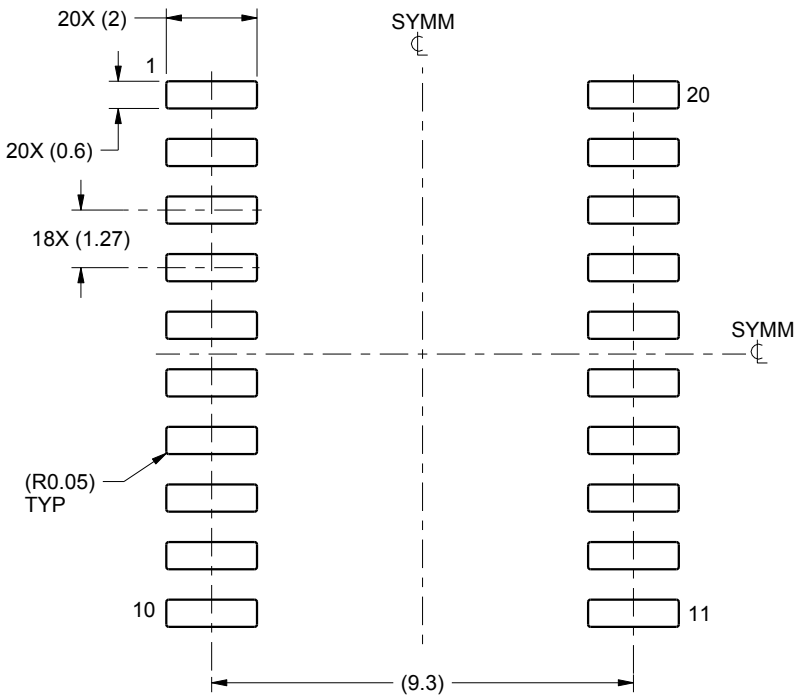
## SOIC - 2.65 mm max height

SOIC

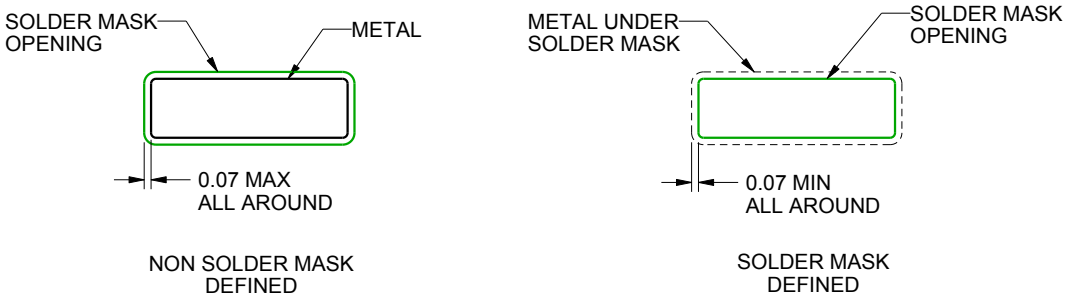



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

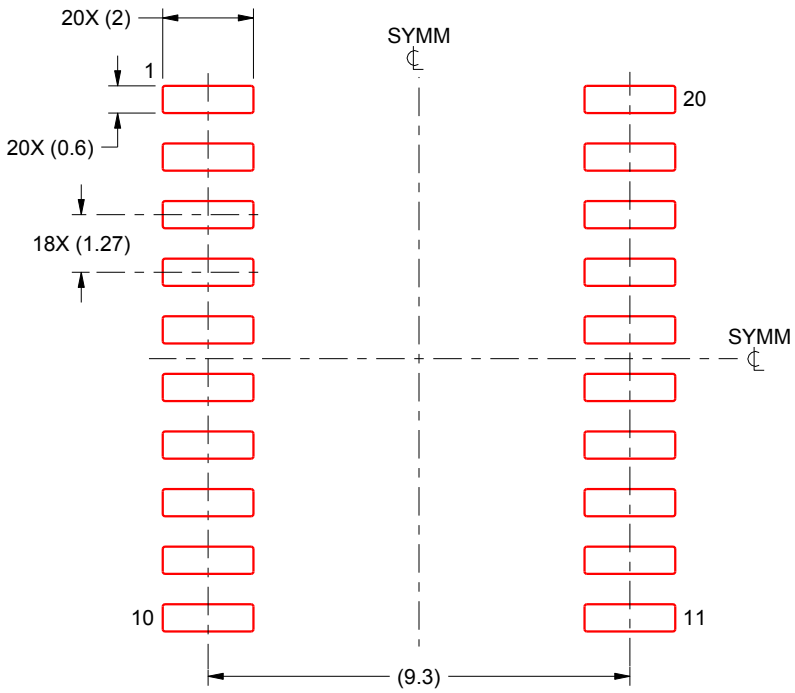



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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