Measurement methodology eSATA

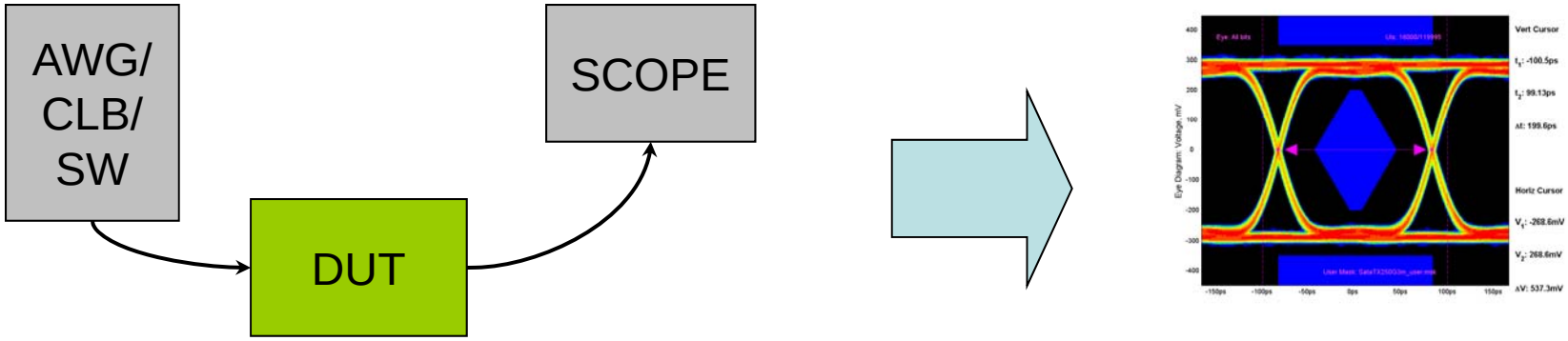
Rev 1.2

PHY testing methodology

- **DUT must be placed into a test mode, typically a BIST (built-in self-test) mode using outside stimulus or a hardware/software utility.**
  - **Special BIST sequences generated by AWGs, on-board software, or compliance load boards can place the DUT in a BIST mode.**

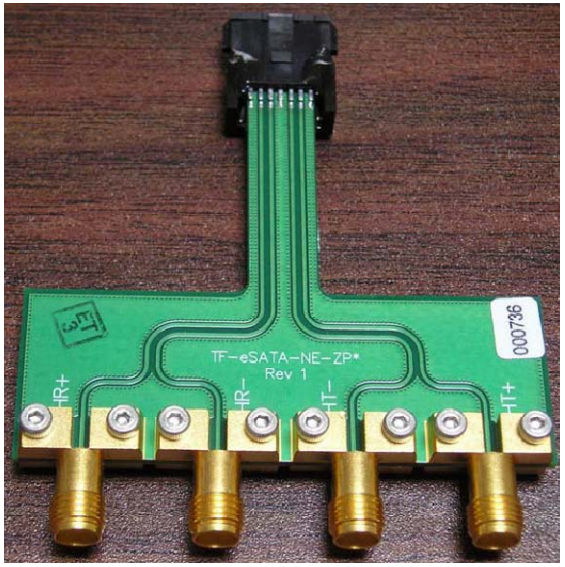
- **Compliance test patterns are loaded and measurements are taken.**
  - **Compliance test patterns and measurement procedures are available from the Standards Board, based on specific lab equipment used (Tektronix®, Agilent®, LeCroy® products, etc.).**

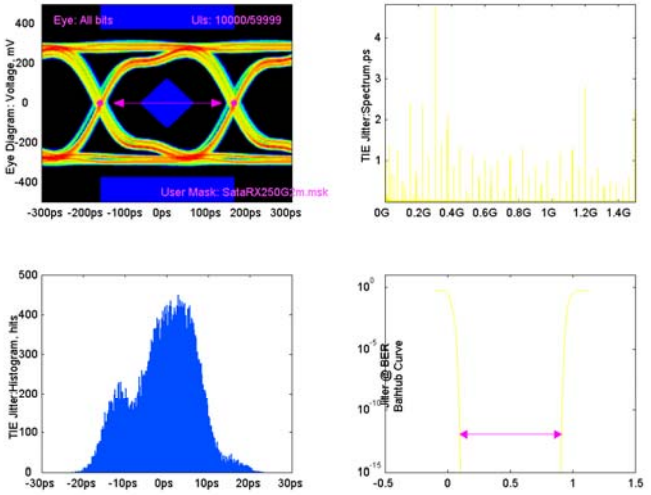
- **Analysis software is used to compare measured values to compliance limits.**



SATA and eSATA PHY testing

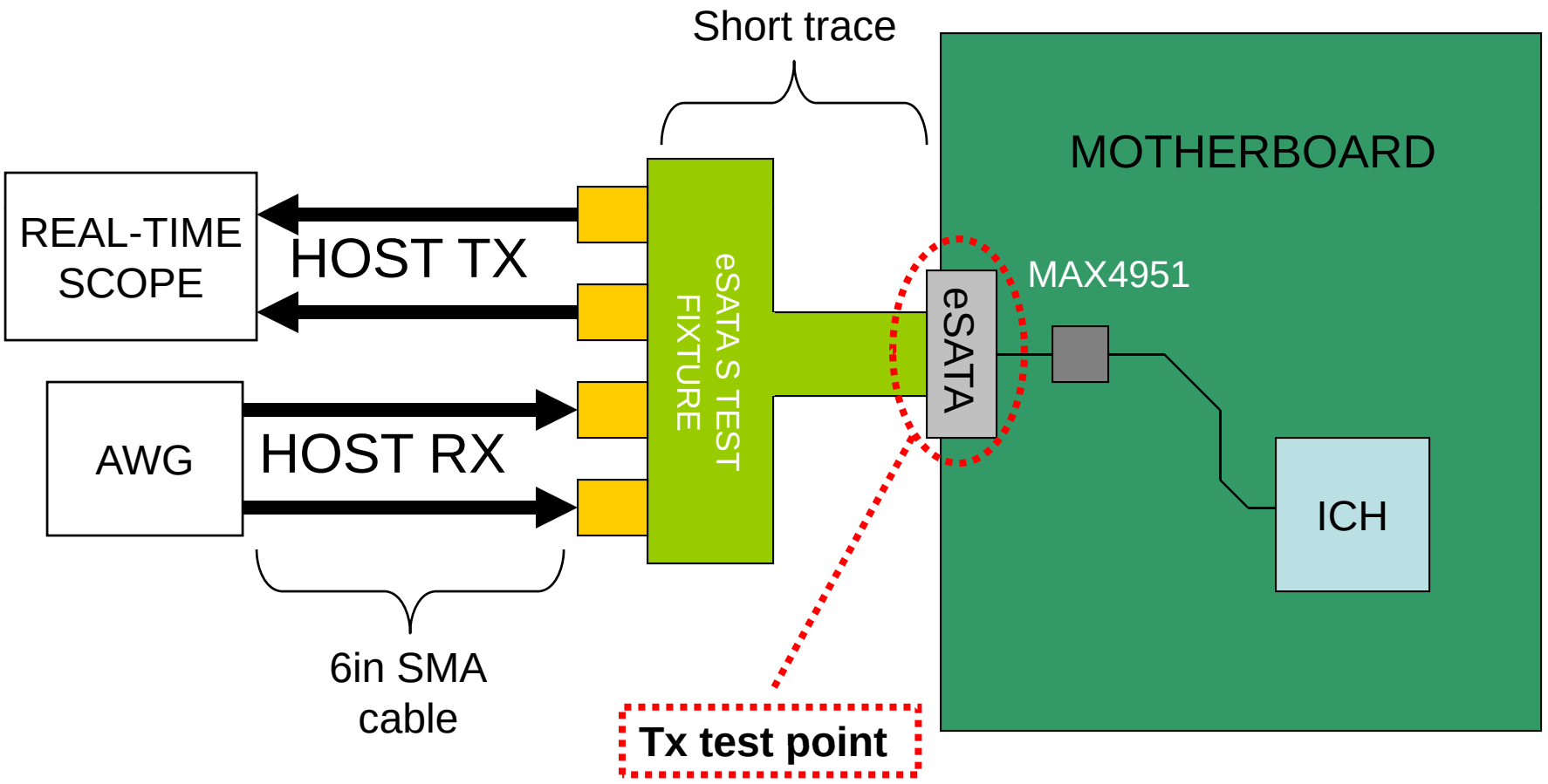
- **Eye diagrams and jitter measurements**
  - **RT-Eye and Jit3 or DPOJET analysis software packages are used with Tektronix test hardware (DSA70604 6GHz real-time oscilloscope or higher) and test fixtures from Crescent Heart (near-end eSATA-to-SMA test fixture).**
  - **The DUT is placed in a BIST mode and data is collected for 1.5Gbps and 3Gbps with an RT oscilloscope.**
  - **The analysis software processes the data to generate eye diagrams and a test report detailing eye height, eye width, rise time, fall time, unit interval length, jitter (DJ, RJ, and TJ).**





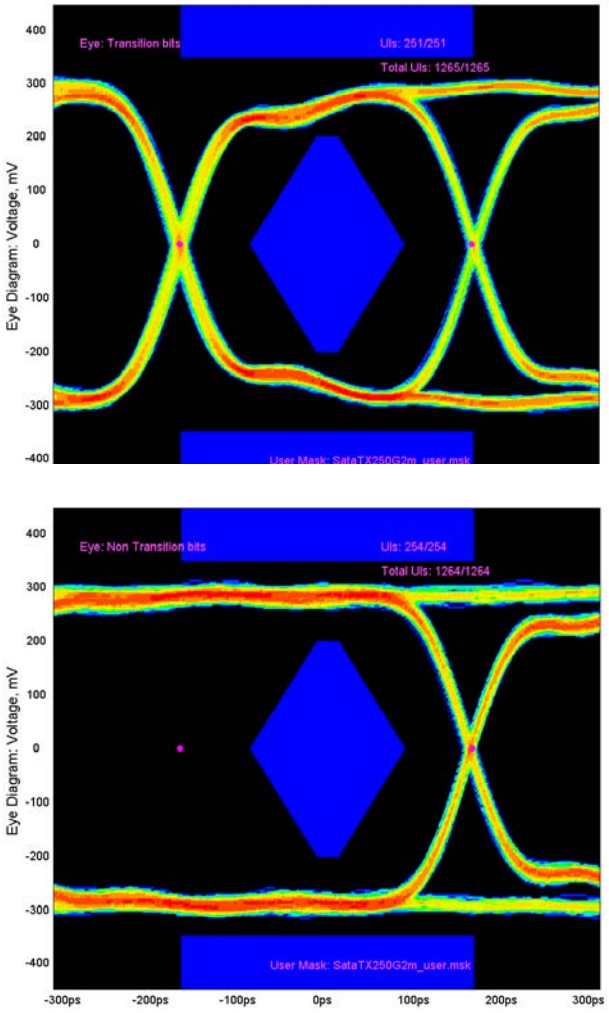
SATA and eSATA PHY testing

- **Our setup for SATA/eSATA testing**



SATA and eSATA PHY testing

- **Typical results for SATA/eSATA testing**



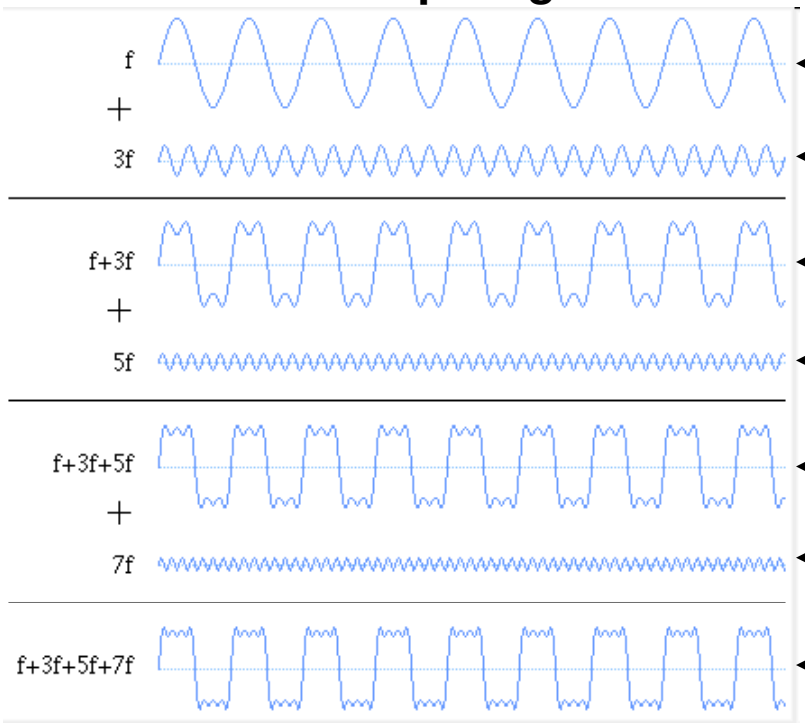
Measurement	Mean	Min	Max
Eye Width	316.11ps	313.92ps	318.78ps
Eye H: All Bits	493.23mV	489.12mV	497.97mV
Eye H: Non-Tr Bits	558.61mV	554.16mV	561.59mV
Eye H: Trans Bits	493.23mV	489.12mV	497.97mV
Rise Time	64.145ps	59.898ps	68.531ps
Fall Time	64.029ps	59.825ps	69.881ps
Unit Interval	334.39ps	334.03ps	334.74ps
Bit Rate	2.9905Gb/s	2.9874Gb/s	2.9937Gb/s
Differential Skew	4.8123ps	-4.9205ps	14.092ps
Diff Amplitude	529.24mV	492.97mV	565.63mV
High Amplitude	295.16mV	293.16mV	298.00mV
Low Amplitude	-288.10mV	-291.90mV	-285.46mV

Measurement	Mean	Limit
Random (RMS)	4.4046ps	---
Deterministic (Pk-Pk)	21.360ps	63.333ps ✓ (Pass)
Periodic	6.4339ps	---
Duty Cycle	1.3245ps	---
Data Dependent (ISI)	13.602ps	---
Total @ BER (Pk-Pk)	72.466ps	123.333ps ✓ (Pass)
Eye Opening @ BER	0.7830UI	---

Testing limitations and other considerations

Limitations and other considerations

- **As data rates increase, bandwidth limitations become more of an issue when taking compliance measurements.**
  - **A lower bandwidth test environment will have reduced rise- and fall-time measurements, as well as introduce "dips" in the eye diagram that can encroach on masks.**
- **RT o'scopes should have the bandwidth to capture at least the 5th harmonic of a 3Gbps signal.**



Fundamental frequency = 1.5GHz

3rd harmonic = 4.5GHz

Fundamental frequency + 3rd harmonic

5th harmonic = 7.5GHz

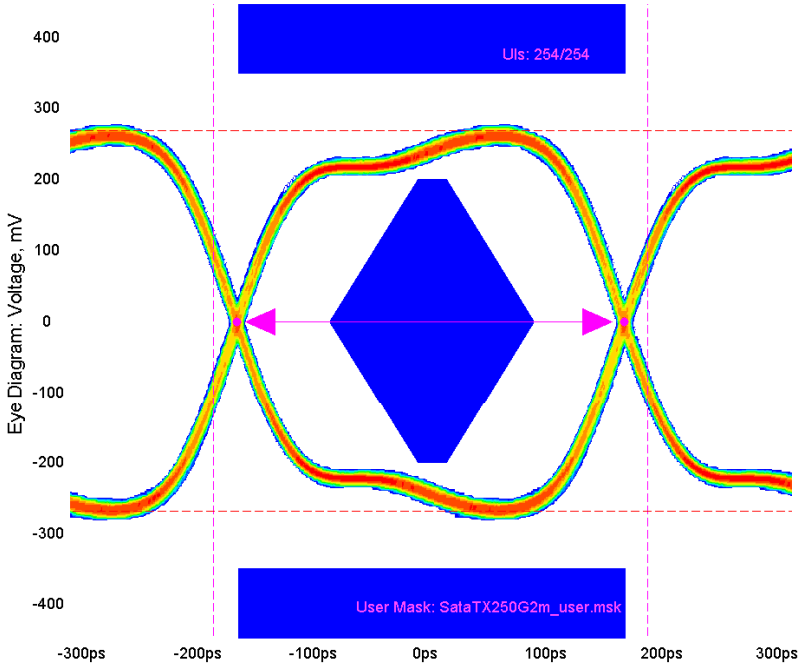
Fundamental frequency + 3rd and 5th harmonic

7th harmonic = 10.5GHz

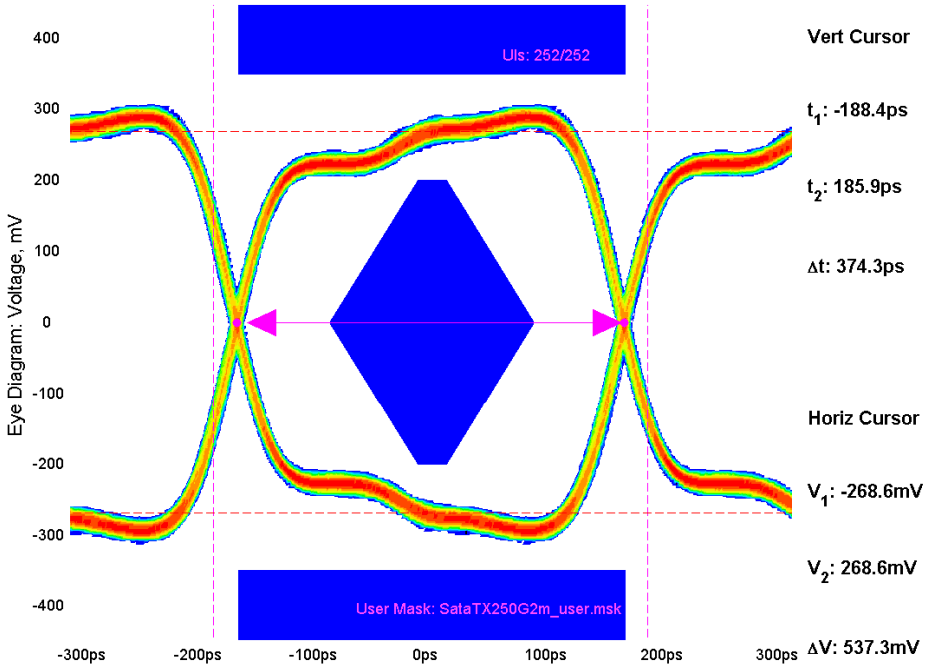
Fundamental frequency + 3rd, 5th and 7th harmonic

Limitations and other considerations

- **Bandwidth comparisons at 3Gbps**



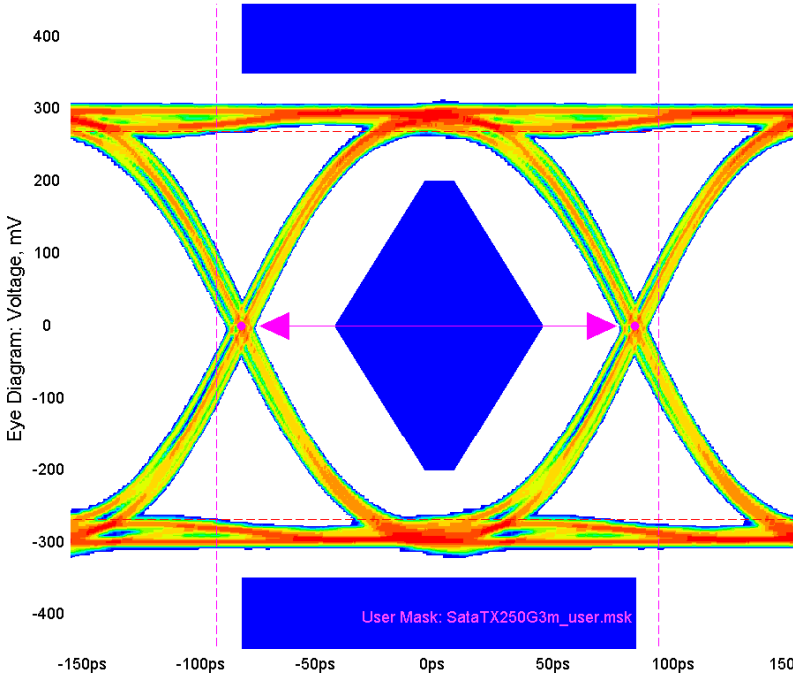
6GHz bandwidth limit



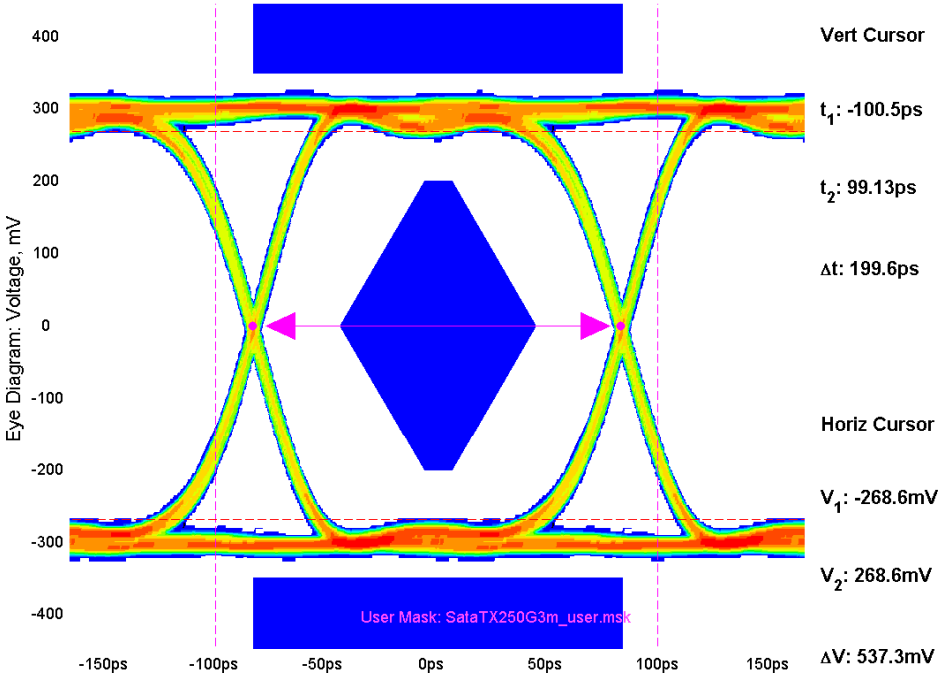
16GHz bandwidth limit

Limitations and other considerations

- **Bandwidth comparisons at 6Gbps**



6GHz bandwidth limit



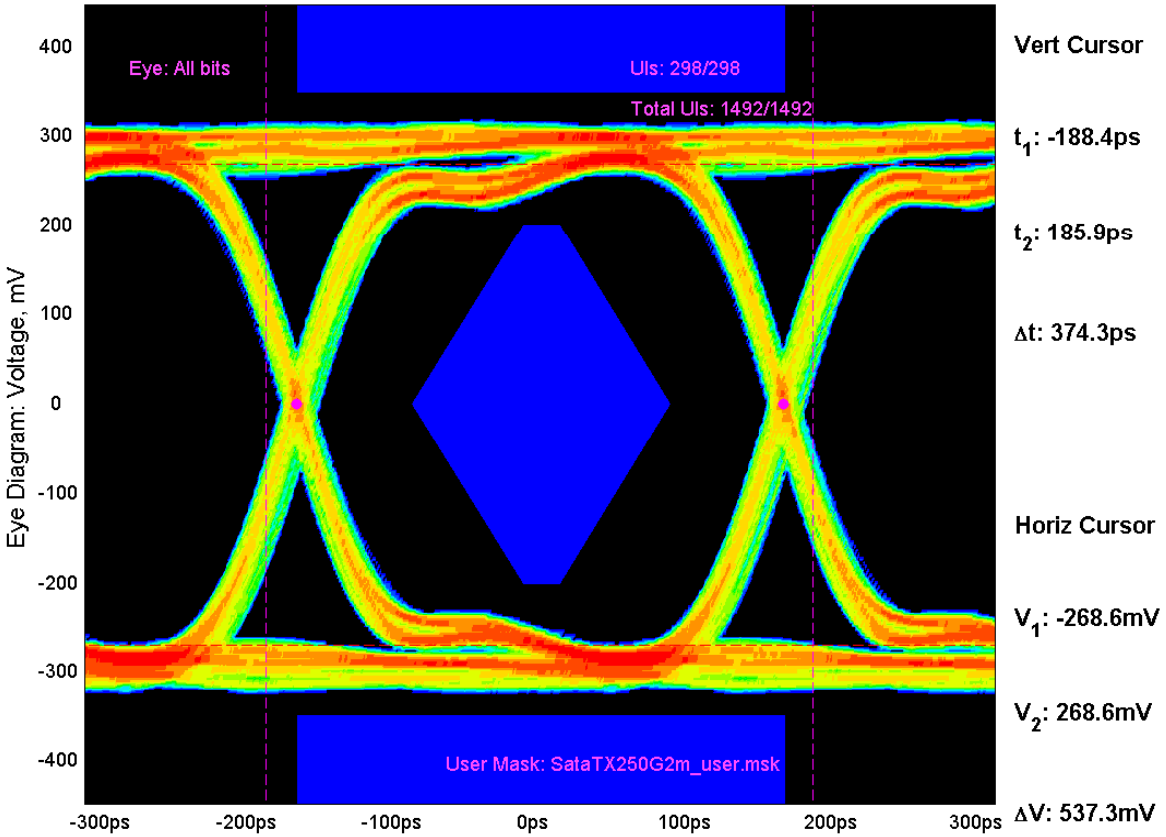
16GHz bandwidth limit

Best practices

- **We have learned a few things about optimal board layout in a system for the MAX4951.**
  - **Place the redriver close (1in to 2in) to an eSATA/SATA connector.**
  - **Keep layer transitions to a minimum.**
  - **Avoid any stubs or hanging traces from the main data path.**
  - **If the MAX4951 is used, keep boost OFF on the host Tx channel.**
  - **If the MAX4951A is used, boost can be ON or OFF on the host Tx channel, depending on the distance from the connector.**
  - **If the MAX4951B is used, boost can be ON or OFF on the host Tx channel, depending on the distance from the connector.**
  - **Reserve resistor pads on the control pins (at least during initial builds) to have an option to turn boost ON/OFF.**
  - **Avoid using custom-made internal cables between the redriver and the eSATA connector.**

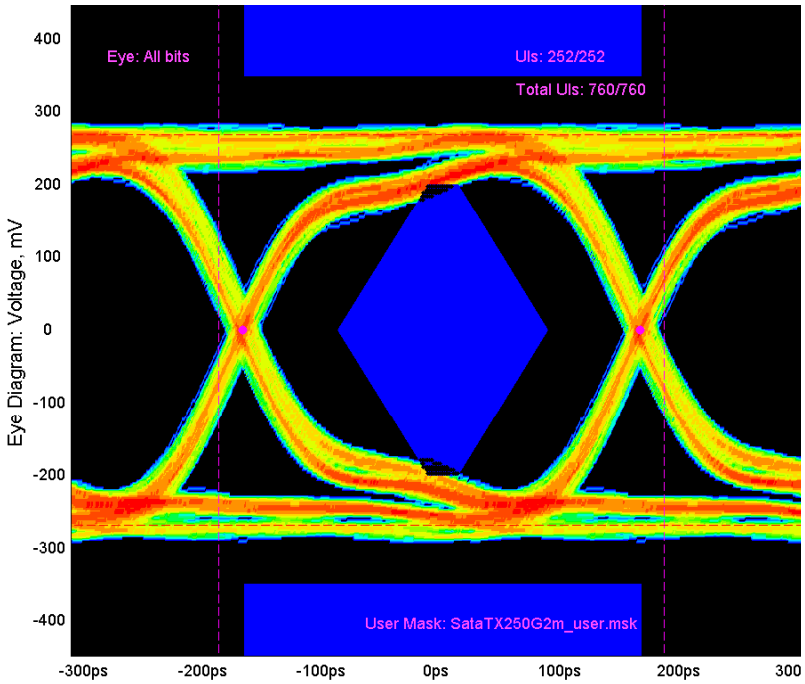
Best practices

- **Good eye diagram**

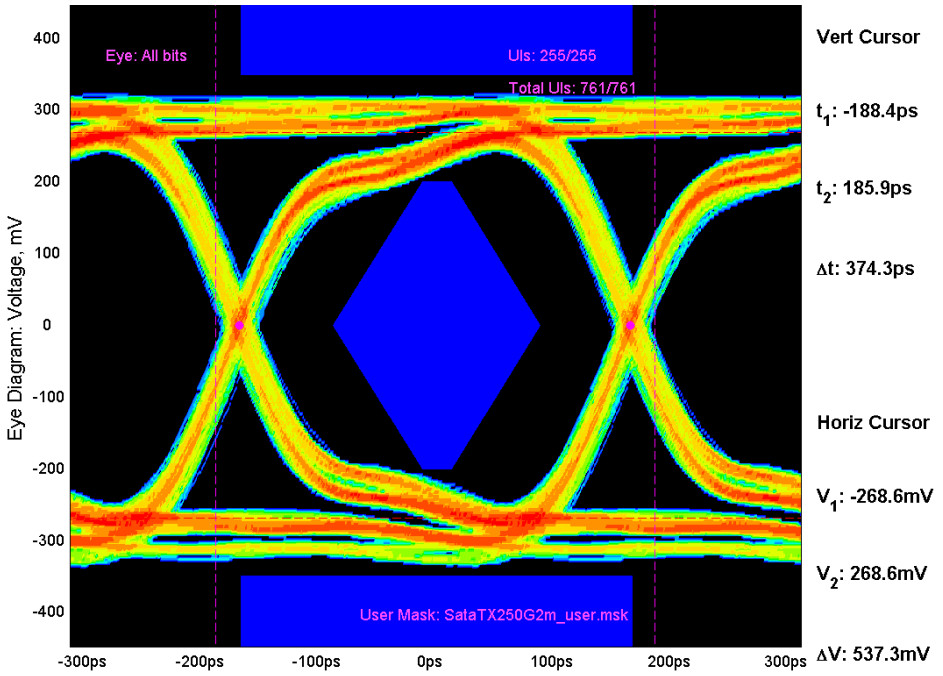


Best practices

- **MAX4951 vs. MAX4951AE in a “lossy” application**



MAX4951



MAX4951AE