

SLVS373 – AUGUST 2001

3.3-V LDO AND DUAL SWITCH FOR USB PERIPHERAL POWER MANAGEMENT

FEATURES

- **Complete Power Management Solution for USB Bus-Powered Peripherals**
- **3.3-V 200 mA Low-Dropout Voltage Regulator With Enable**
- **3.3-V 340-mΩ (Typ) High-Side MOSFET**
- **5-V 340-mΩ (Typ) High-Side MOSFET**
- **Independent Thermal- and Short-Circuit Protection for LDO and Each Switch**
- **2.9-V to 5.5-V Operating Range**
- **CMOS- and TTL-Compatible Enable Inputs**
- **75-μA (Typ) Supply Current**
- **Available in 8-Pin MSOP (PowerPAD™)**
- **−40°C to 85°C Ambient Temperature Range**

APPLICATIONS

- **USB Peripherals**
  - **Digital Cameras**
  - **Zip Drives**
  - **Speakers and Headsets**

DESCRIPTION

The TPS2148 incorporates two power distribution switches and an LDO in one small package, providing a USB peripheral power management solution that saves up to 60% in board space over typical implementations.

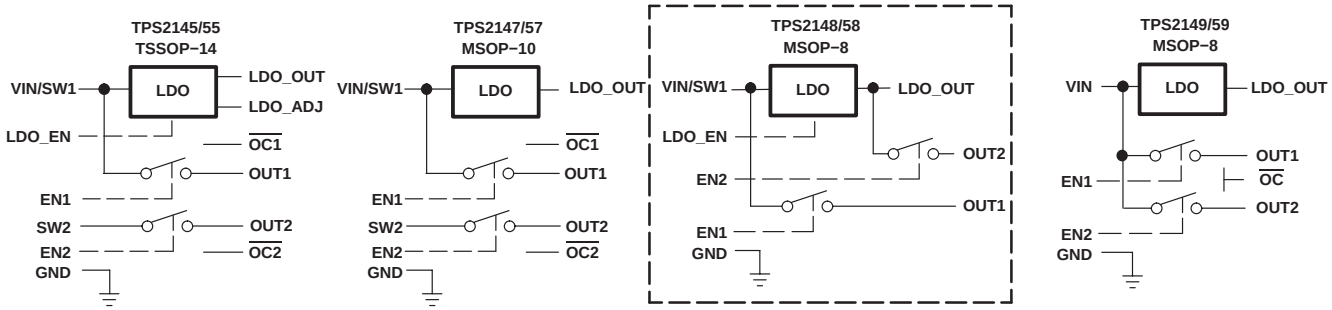
The TPS2148 meets USB 2.0 bus-powered peripheral requirements. An integrated LDO regulates the 5-V bus power down to 3.3 V for the USB controller, and a MOSFET switch that is internally connected to the output of the LDO simplifies meeting the suspend and enumeration current requirements imposed by the USB specification.

A second switch is available to support a downstream port, stage power to a second voltage regulator, or disable power to selected circuitry in power-save modes.

Each power-distribution switch is capable of supplying 200 mA of continuous current, and the independent logic enables are compatible with 5-V logic and 3-V logic. The switches and the LDO are designed with controlled rise times and fall times to minimize current surges.

The TPS2148 has active-low enables while the TPS2158 has active-high enables.

LDO and dual switch family selection guide and schematics



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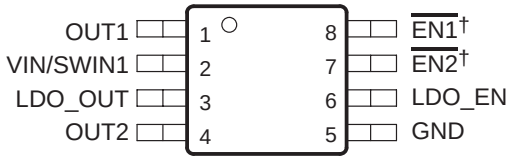
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AVAILABLE OPTIONS

T_A	DESCRIPTION	PACKAGE AND PIN COUNT	PACKAGED DEVICES	
			ACTIVE LOW (SWITCH)	ACTIVE HIGH (SWITCH)
−40°C to 85°C	Adjustable LDO with LDO enable	TSSOP-14	TPS2145IPWP	TPS2155IPWP
	3.3-V fixed LDO	MSOP-10	TPS2147IDGQ	TPS2157IDGQ
	3.3-V Fixed LDO with LDO enable and LDO output switch	MSOP-8	TPS2148IDGN	TPS2158IDGN
	3.3-V Fixed LDO, shared input with switches	MSOP-8	TPS2149IDGN	TPS2159IDGN

NOTE: All options available taped and reeled. Add an R suffix (e.g. TPS2145IPWPR)

TPS2148, TPS2158
MSOP (DGN) PACKAGE
(TOP VIEW)



† Pins 7 and 8 are active high for TPS2158.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range: $V_{I(VIN/SWIN1)}$, $V_{I(ENx)}$, $V_{I(LDO_EN)}$ . . . . . −0.3 V to 6 V
Output voltage range: $V_{O(OUTx)}$, $V_{O(LDO_OUT)}$, $V_{O(OCx)}$ . . . . . −0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$, $I_{O(LDO_OUT)}$ . . . . . Internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual-junction temperature range, T_J . . . . . −40°C to 110°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Electrostatic discharge (ESD) protection: Human body model . . . . . 2 kV
Charged device model (CDM) . . . . . 1 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
MSOP8	1455.5 mW	17.1 mW/°C	684.9 mW	428.08 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(VIN/SWIN1)}$	2.9	5.5	V
	$V_{I(\overline{ENx})}$	0	5.5	
	$V_{I(LDO_EN)}$	0	5.5	
Continuous output current, I_O	LDO_OUT		200	mA
	OUT1, OUT2		150	
Output current limit, $I_{O(LMT)}$	LDO_OUT	275	550	mA
	OUT1, OUT2	200	400	
Operating virtual-junction temperature range, T_J		−40	100	°C

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $T_J = -40°C$ to 100°C (unless otherwise noted)

general

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Off-state supply current	$V_{I(VIN/SWIN1)} = 5\ V$	$V_{I(\overline{ENx})} = 5$ V (inactive), $V_{I(LDO_EN)} = 0$ V (inactive), $V_{O(LDO_OUT)}$ = no load, $V_{O(OUTx)}$ = no load			20	µA
	Forward leakage current		$V_{I(\overline{ENx})} = 5$ V (inactive), $V_{I(LDO_EN)} = 0$ V (inactive), $V_{O(LDO_OUT)} = 0$ V, $V_{O(OUTx)} = 0$ V (measured from outputs to ground)			1	µA
I_I	Total input current at VIN/SWIN1 and SWIN2	$V_{I(VIN/SWIN1)} = 5$ V, No load on OUTx, No load on LDO_OUT	$V_{I(LDO_EN)} = 5$ V (active), $V_{I(ENx)}$ = on (active)			150	µA
			$V_{I(LDO_EN)} = 0$ V (inactive), $V_{I(ENx)}$ = on (active)			100	µA
			$V_{I(LDO_EN)} = 5$ V (active), $V_{I(ENx)}$ = off (inactive)			100	µA

power switches

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance, VIN/SWIN1 or SWIN2 to OUTx	$I_{O(LDO_OUT)} = 50$ mA, IOUT1 and IOUT2 = 150 mA, $T_J = -40°C$ to 100°C				680	mΩ
		$I_{O(LDO_OUT)} = 50$ mA, IOUT1 and IOUT2 = 150 mA, $T_J = 25°C$			340		
$I_{lkg(R)}$	Reverse leakage current at OUTx	$V_{O(OUTx)} = 5$ V, LDO_EN = don't care	$V_{I(\overline{ENx})} = 5$ V, $V_{I(ENx)} = 0$ V, $V_{I(VIN/SWIN1)} = 5$ V			10	µA
			$V_{I(\overline{ENx})} = 5$ V, $V_{I(ENx)} = 0$ V, $V_{I(VIN/SWIN1)} = 2.9$ V			10	
			$V_{I(\overline{ENx})} = 5$ V, $V_{I(ENx)} = 0$ V, $V_{I(VIN/SWIN1)} = 0$ V			10	
I_{OS}	Short circuit output current	OUTx connected to GND, device enabled into short circuit		0.2		0.4	A

NOTE 1: Specified by design, not tested in production.

electrical characteristics over recommended operating junction-temperature range, 2.9 V ≤ $V_{I(VIN/SWIN1)}$ ≤ 5.5 V, T_J = −40°C to 100°C (unless otherwise noted)

timing parameters, power switches

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{on}	Turnon time, OUTx switch, (see Note 1)	C_L = 100 µF	R_L = 33 Ω	0.5		6	ms
		C_L = 1 µF		0.1		3	
t_{off}	Turnoff time, OUTx switch (see Note 1)	C_L = 100 µF	R_L = 33 Ω	5.5		10	
		C_L = 1 µF		0.05		2	
t_r	Rise time, OUTx switch (see Note 1)	C_L = 100 µF	R_L = 33 Ω	0.5		5	
		C_L = 1 µF		0.1		2	
t_f	Fall time, OUTx switch (see Note 1)	C_L = 100 µF	R_L = 33 Ω	5.5		9	
		C_L = 1 µF		0.05		1.2	

NOTE 1. Specified by design, not tested in production.

undervoltage lockout at VIN/SWIN1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO Threshold		2.2		2.85	V
Hysteresis (see Note 1)			260		mV
Deglitch (see Note 1)		50			µs

NOTE 1. Specified by design, not tested in production.

undervoltage lockout at switch 2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO Threshold		2.2		2.85	V
Hysteresis (see Note 1)			260		mV
Deglitch (see Note 1)		50			µs

NOTE 1. Specified by design, not tested in production.

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $V_{I(\overline{ENx})} = 0\ V$, $V_{I(LDO_EN)} = 5\ V$, $C_{L(LDO_OUT)} = 10\ \mu F$, $T_J = -40°C$ to $100°C$ (unless otherwise noted)

3.3 V LDO

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_O	Output voltage, dc	$V_{I(VIN/SWIN1)}$ = 4.25 V to 5.25 V, $I_{O(LDO_OUT)}$ = 0.5 mA to 200 mA	3.20	3.3	3.40	V
	Dropout voltage	$V_{I(VIN/SWIN1)}$ = 3.2 V, I_O = 200 mA, $I_{O(OUT)}$ = 150 mA			0.35	V
	Line regulation voltage (see Note 1)	$V_{I(VIN/SWIN1)}$ = 4.25 V to 5.25 V, $I_{O(LDO_OUT)}$ = 5 mA			0.1	%/V
	Load regulation voltage (see Note 1)	$V_{I(VIN/SWIN1)}$ = 4.25 V, $I_{O(LDO_OUT)}$ = 5 mA to 200 mA		0.4	1%	
I_{OS}	Short-circuit current limit	$V_{I(VIN/SWIN1)}$ = 4.25 V, LDO_OUT connected to GND	0.275	0.33	0.55	A
$I_{lkg(R)}$	Reverse leakage current into LDO_OUT	$V_{O(LDO_OUT)}$ = 3.3 V, $V_{I(VIN/SWIN1)}$ = 0 V, $V_{I(LDO_EN)}$ = 0 V		10		µA
		$V_{O(LDO_OUT)}$ = 5.5 V, $V_{I(VIN/SWIN1)}$ = 2.7 V, $V_{I(LDO_EN)}$ = 0 V		10		µA
	Power supply rejection	f = 1 kHz, $C_{L(LDO_OUT)}$ = 4.7 µF, ESR = 0.25 Ω, I_O = 5 mA, $V_{I(VIN/SWIN1)p-p}$ = 100 mV		50		dB
t_{on}	Turnoff time, LDO_EN transitioning low (see Note 1)	R_L = 16 Ω, $C_{L(LDO_OUT)}$ = 10 µF	0.25		1	ms
t_{off}	Turnon time, LDO_EN transitioning high (see Note 1)	R_L = 16 Ω, $C_{L(LDO_OUT)}$ = 10 µF	0.1		1	ms
	Ramp-up time, LDO_OUT (0% to 90%)	$V_{I(LDO_EN)}$ = 5 V, VIN ramping up from 10% to 90% in 0.1 ms, R_L = 16 Ω, $C_{L(LDO_OUT)}$ = 10 µF	0.1		1	ms

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

NOTE 1. Specified by design, not tested in production.

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $2.9\ V \le V_{I(SWIN2)} \le 5.5\ V$, $V_{I(\overline{ENx})} = 0\ V$, $V_{I(LDO_EN)} = 5\ V$, $T_J = -40°C$ to $100°C$ (unless otherwise noted)

enable input, $\overline{ENx}$ (active low)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_I	Input current, pullup (source)	$V_{I(ENx)} = 0\ V$			5	µA

enable input, ENx (active high)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_I	Input current, pulldown (sink)	$V_{I(ENx)} = 5\ V$			5	µA

enable input, LDO_EN (active high)

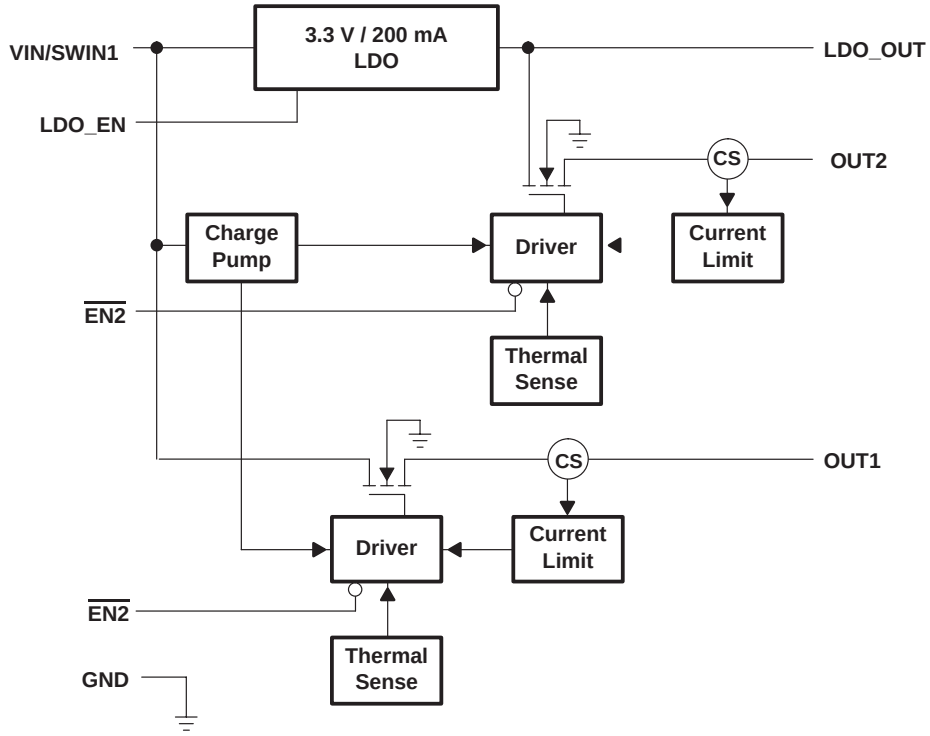
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_I	Input current, pulldown	$V_{I(LDO_EN)} = 5\ V$			5	µA
	Falling-edge deglitch (see Note 1)		50			µs

NOTE 1. Specified by design, not tested in production.

thermal shutdown characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
First thermal shutdown (shuts down switch or regulator in overcurrent)	Occurs at or above specified temperature when overcurrent is present.	120			°C
Recovery from thermal shutdown		110			
Second thermal shutdown (shuts down all switches and regulator)	Occurs on rising temperature, irrespective of overcurrent.	155			
Second thermal shutdown hysteresis			10		

TPS2148 functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2148	TPS2158		
EN1		8	I	Logic level enable to transfer power to OUT1
$\overline{EN1}$	8			
EN2		7	I	Logic level enable to transfer power to OUT2
$\overline{EN2}$	7			
GND	5	5		Ground
LDO_EN	6	6	I	Logic level LDO enable. Active high.
LDO_OUT	3	3	O	LDO output
OUT1	1	1	O	Switch 1 output
OUT2	4	4		Switch 2 output
VIN/SWIN1	2	2	I	Input for LDO and switch 1; device supply voltage

detailed description

VIN/SWIN1

The VIN/SWIN1 serves as the input to the internal LDO and as the input to one N-channel MOSFET. The 3.3-V LDO has a dropout voltage of 0.35 V and is rated for 200 mA of continuous current. The power switch is an N-channel MOSFET with a maximum on-state resistance of 580 mΩ. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch is rated at 150 mA, continuous current. VIN/SWIN1 must be connected to a voltage source for device operation.

OUTx

OUT1 and OUT2 are the outputs from the internal power-distribution switches.

LDO_OUT

LDO_OUT is the output of the internal 200-mA LDO. It is also the input to a second power switch. This power switch in an N-channel MOSFET with a maximum on-state resistance of 580 mΩ. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch is rated at 150 mA, continuous current.

LDO_EN

The active high input, LDO_EN, is used to enable the internal LDO and is compatible with TTL and CMOS logic.

enable ($\overline{\text{ENx}}$, ENx)

The logic enable disables the power switch. Both switches have independent enables and are compatible with both TTL and CMOS logic.

current sense

A sense FET monitors the current supplied to the load. Current is measured more efficiently by the sense FET than by conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

thermal sense

A dual-threshold thermal trip is implemented to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 120°C, the internal thermal sense circuitry determines which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Because hysteresis is built into the thermal sense, the switch turns back on after the device has cooled approximately 10 degrees. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2.5 V, a control signal turns off the power switch.

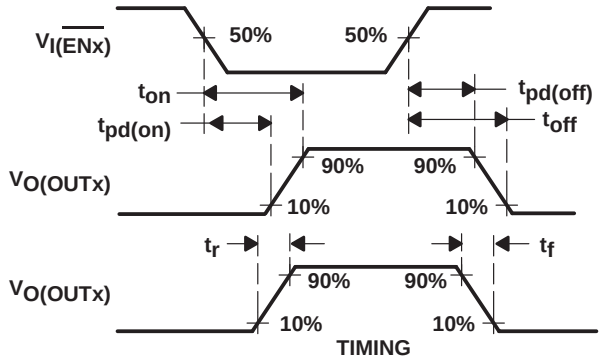


Figure 1. Timing and Internal Voltage Regulator Transition Waveforms

TYPICAL CHARACTERISTICS

SWITCH TURNON DELAY AND RISE TIME
WITH 1-μF LOAD

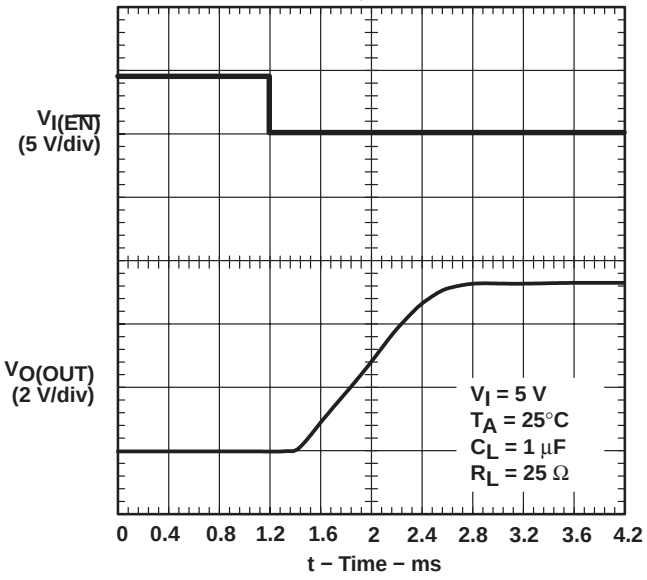


Figure 2

SWITCH TURNOFF DELAY AND FALL TIME
WITH 1-μF LOAD

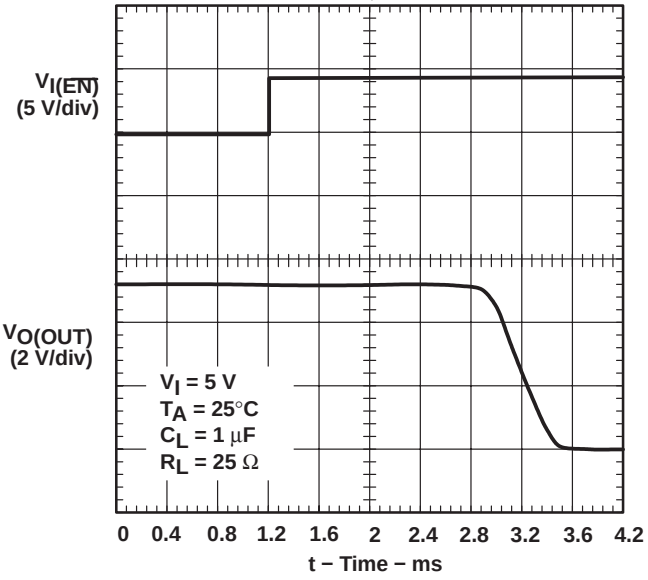


Figure 3

SWITCH TURNON DELAY AND RISE TIME
WITH 120-μF LOAD

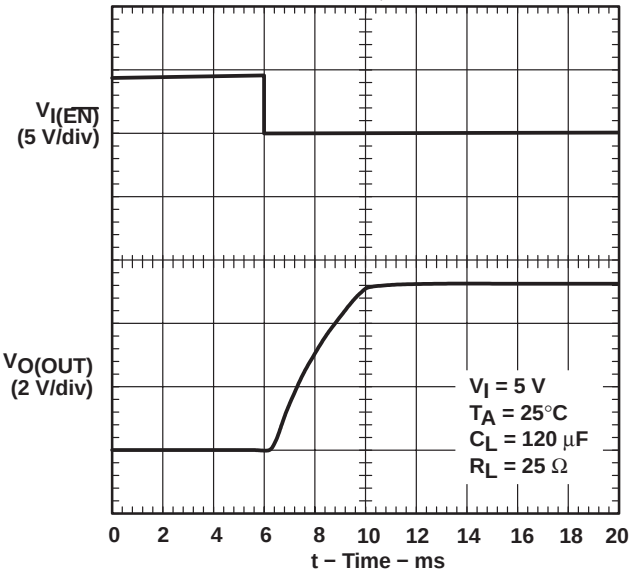


Figure 4

SWITCH TURNOFF DELAY AND FALL TIME
WITH 120-μF LOAD

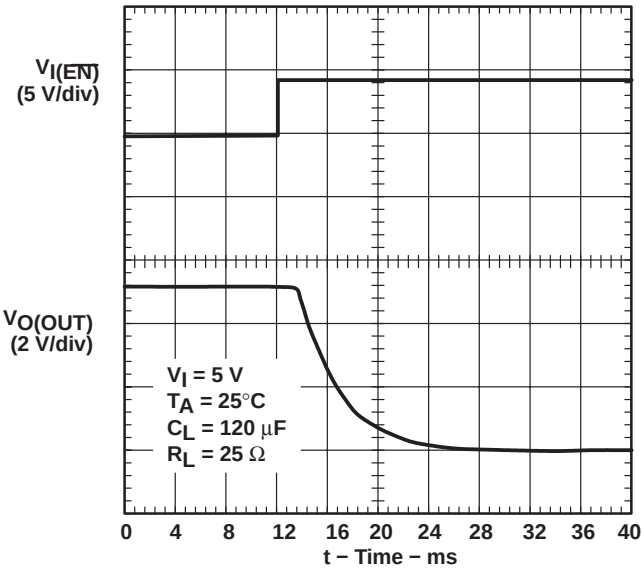


Figure 5

TYPICAL CHARACTERISTICS

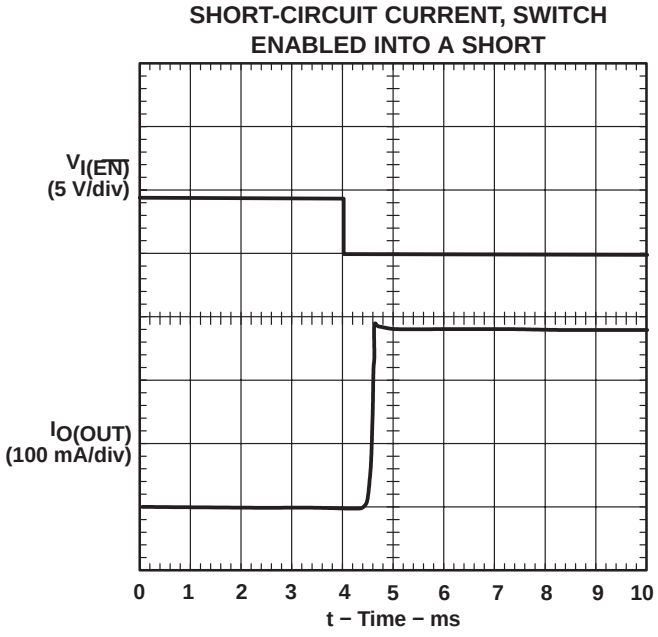


Figure 6

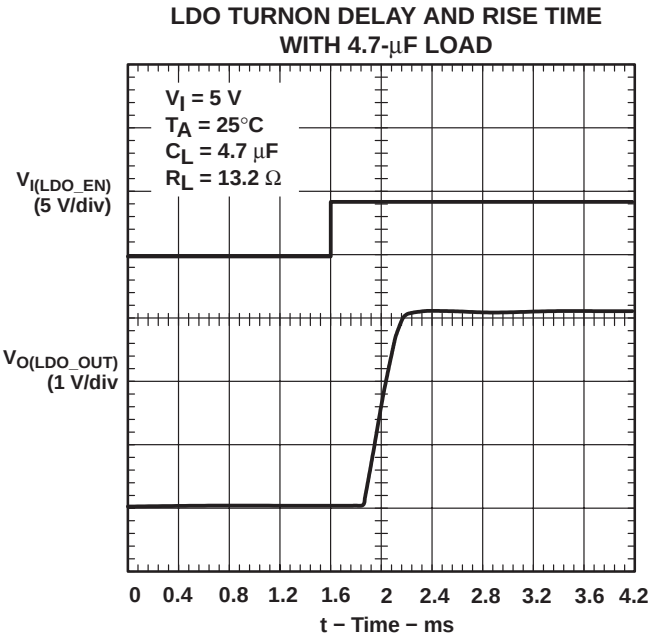


Figure 7

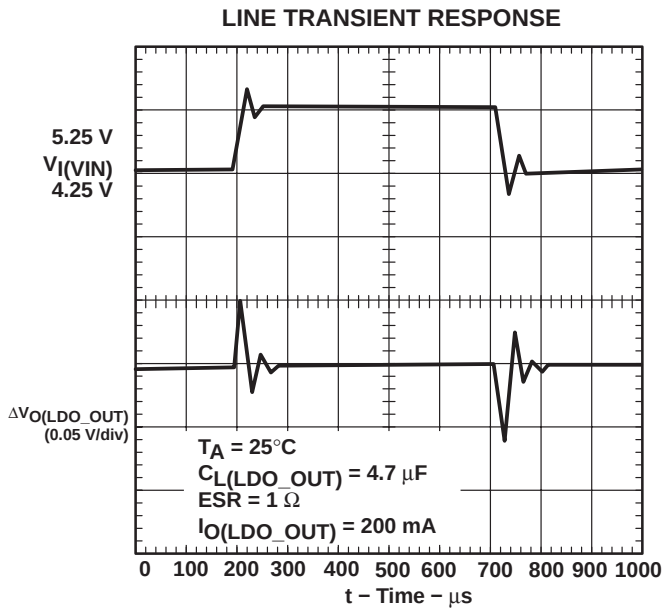


Figure 8

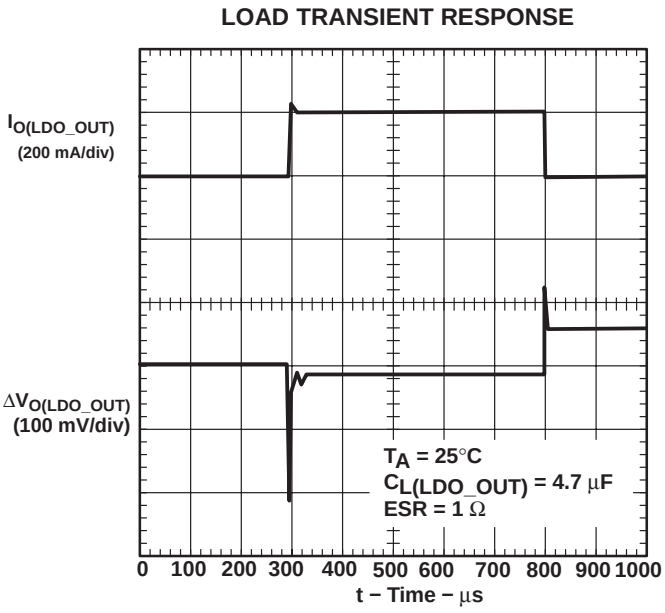


Figure 9

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
JUNCTION TEMPERATURE**

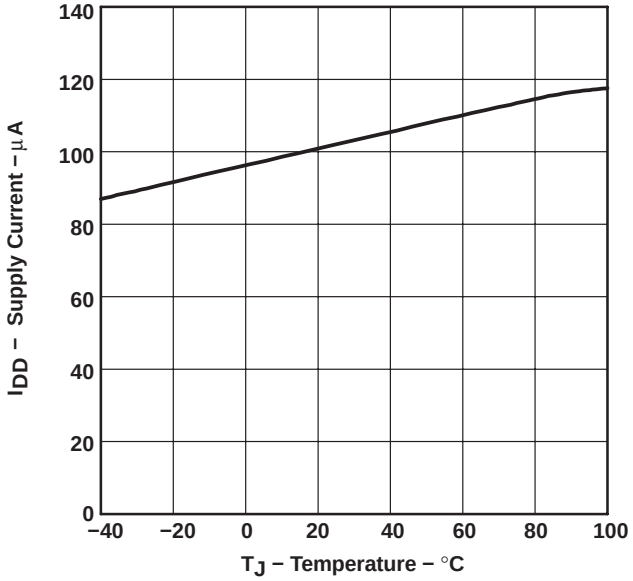


Figure 10

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

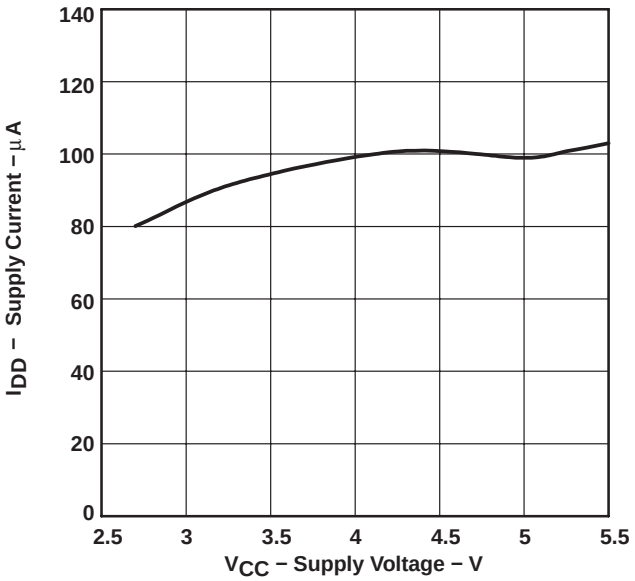


Figure 11

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE**

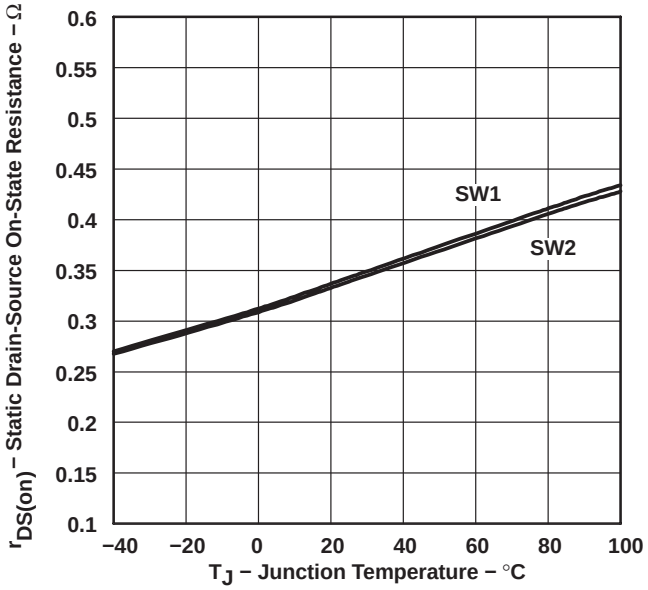


Figure 12

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
SUPPLY VOLTAGE**

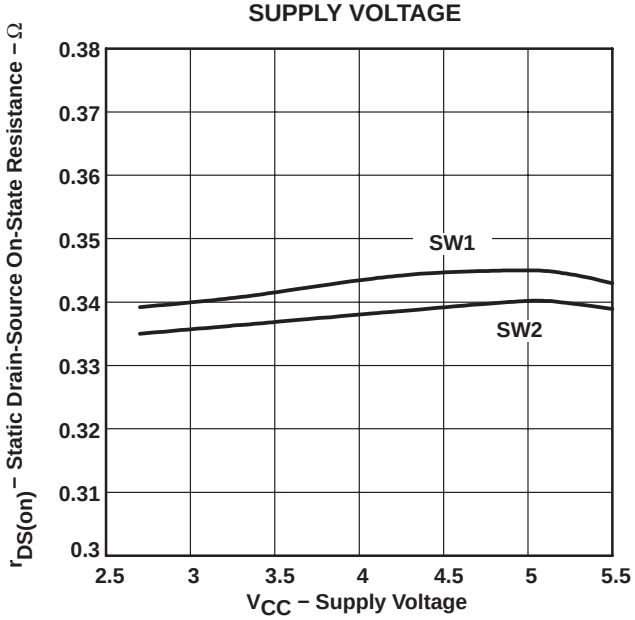


Figure 13

TYPICAL CHARACTERISTICS

SHORT CIRCUIT CURRENT vs JUNCTION TEMPERATURE

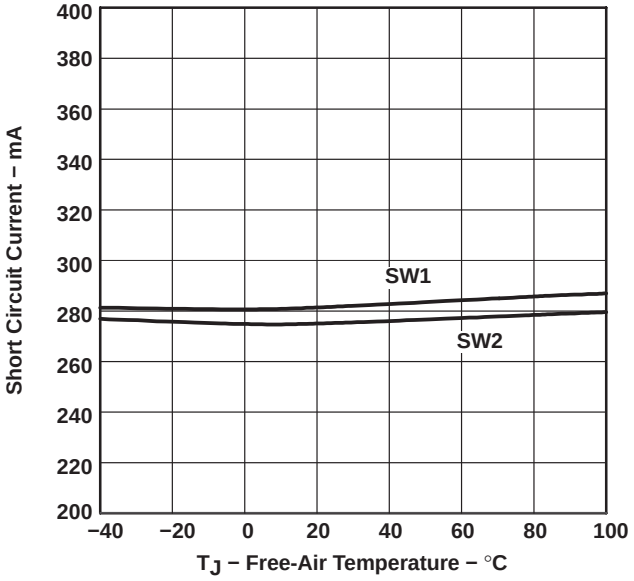


Figure 14

SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE

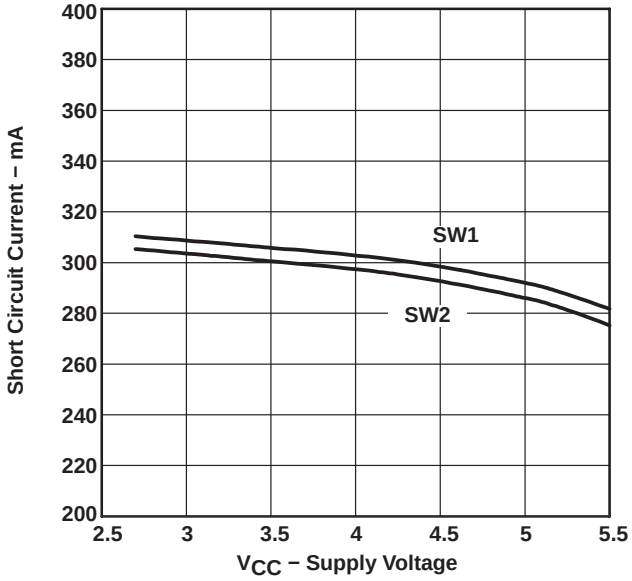


Figure 15

UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE

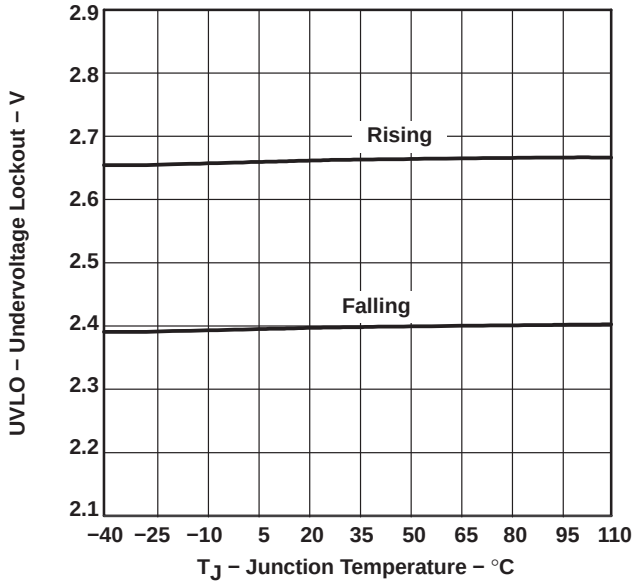


Figure 16

APPLICATION INFORMATION

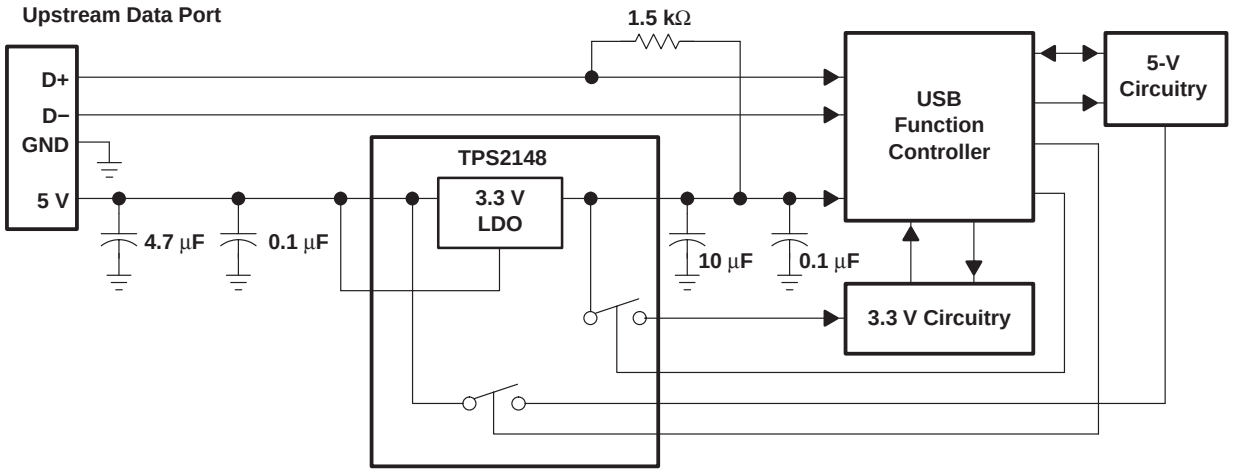


Figure 17. Example of a Peripheral Design With TPS2148

external capacitor requirements on power lines

A ceramic bypass capacitor (0.01-μF to 0.1-μF) between VIN/SWIN1 and GND, close to the device, is recommended to improve load transient response and noise rejection.

A bulk capacitor (4.7-μF) between VIN/SWIN1 and GND is also recommended, especially if load transients in the hundreds of milliamps with fast rise times are anticipated.

A 66-μF bulk capacitor is recommended from OUTx to ground, especially when the output load is heavy. This precaution helps reduce transients seen on the power rails. Additionally, bypassing the outputs with a 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

LDO output capacitor requirements

Stabilizing the internal control loop requires an output capacitor connected between LDO_OUT and GND. The minimum recommended capacitance is a 4.7 μF with an ESR value between 200 mΩ and 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the ESR requirements.

overcurrent

A sense FET is used to measure current through the device. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current. Complete shut down occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output is shorted before the device is enabled or before VIN has been applied. The TPS2148 and TPS2158 sense the short and immediately switches to a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a very short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2148 and TPS2158 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

APPLICATION INFORMATION

power dissipation and junction temperature

The main source of power dissipation for the TPS2148 and TPS2158 comes from the internal voltage regulator and the N-channel MOSFETs. Checking the power dissipation and junction temperature is always a good design practice and it starts with determining the $r_{DS(on)}$ of the N-channel MOSFET according to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the graphs shown in the Typical Characteristics section of this data sheet. Using this value, the power dissipation per switch can be calculated using:

$$P_D = r_{DS(on)} \times I^2 \quad (1)$$

Multiply this number by two to get the total power dissipation coming from the N-channel MOSFETs.

The power dissipation for the internal voltage regulator is calculated using:

$$P_D = \left(V_I – V_{O(min)}\right) \times I_O \quad (2)$$

The total power dissipation for the device becomes:

$$P_{D(total)} = P_{D(voltage\ regulator)} + \left(2 \times P_{D(switch)}\right) \quad (3)$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (4)$$

Where:

T_A = Ambient Temperature °C

$R_{\theta JA}$ = Thermal resistance °C/W, equal to inverting the derating factor found on the power dissipation table in this datasheet.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2148 and TPS2158 into constant-current mode at first, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels.

The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2148 and TPS2158 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 120°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 120°C and reach 155°C, the device will turn off.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the device (LDO and switches) is in the off state at power up. The UVLO will also keep the device from being turned on until the power supply has reached the start threshold (see undervoltage lockout table), even if the switches are enabled. The UVLO will also be activated whenever the input voltage falls below the stop threshold as defined in the undervoltage lockout table. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switches before input power is removed. Upon reinsertion, the power switches will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a multiplexed serial bus operating at either 12 Mb/s, or 1.5 Mb/s for USB 1.1, or 480 Mb/s for USB 2.0. The USB interface is designed to accommodate the bandwidth required by PC peripherals such as keyboards, printers, scanners, and mice. The four-wire USB interface was conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub or across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

The TPS2148 and TPS2158 are well suited for USB peripheral applications.

APPLICATION INFORMATION

USB power distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

USB applications

Figure 17 shows the TPS2148 being used in a USB bus-powered peripheral design. The internal 3.3-V LDO is used to provide power for the USB function controller as well as to the 1.5-kΩ pullup resistor.

Switch 1 provides power to the 5-V circuitry which is only enabled after enumeration is complete to ensure meeting the 100-mA USB power up requirement. Switch 2 provides power to the 3.3-V circuitry. Switch 2 is also enabled only after enumeration is complete to satisfy the 100 mA requirement.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2148IDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXB	Samples
TPS2158IDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

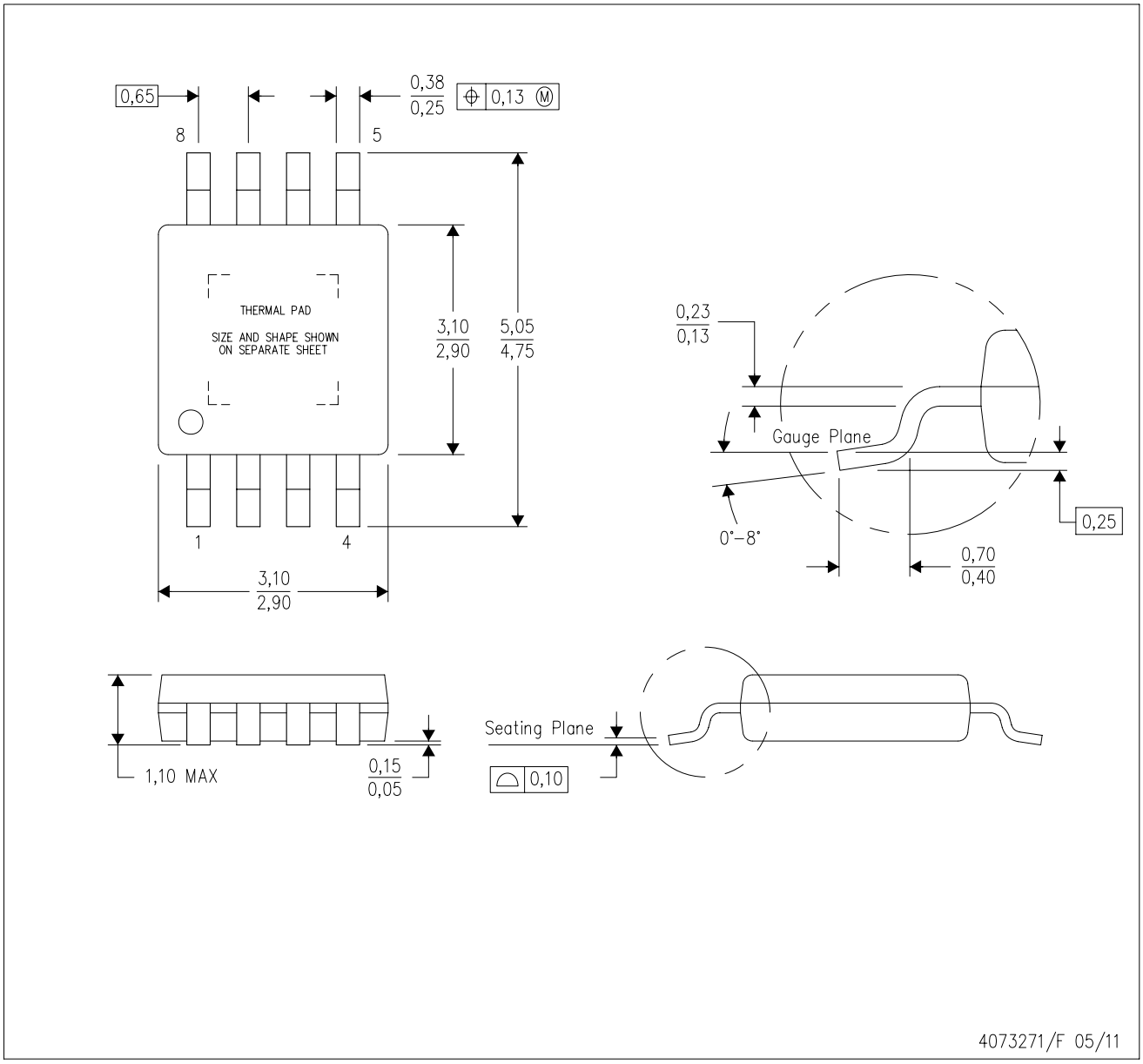
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

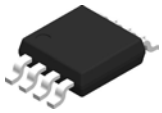


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

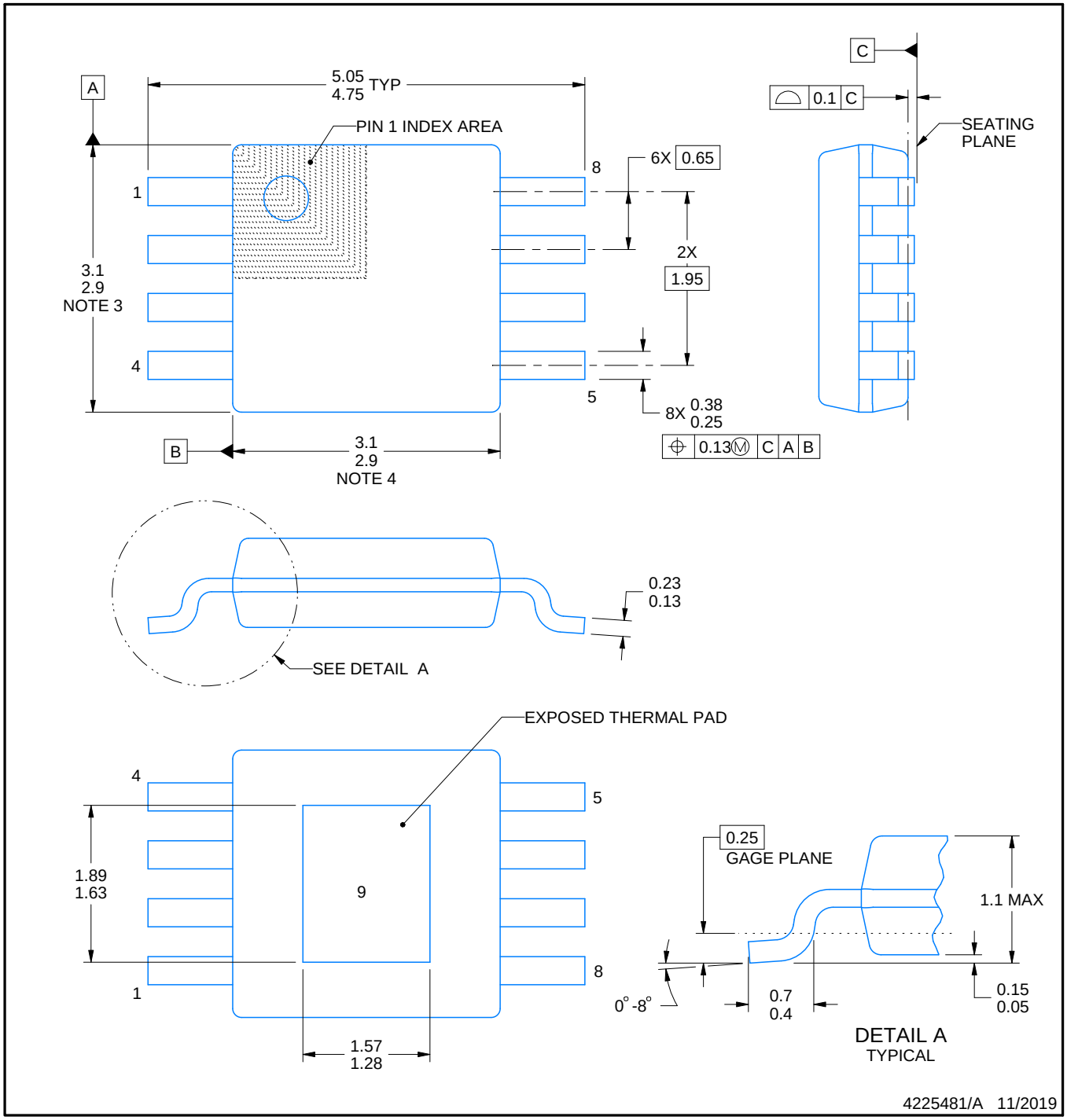
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

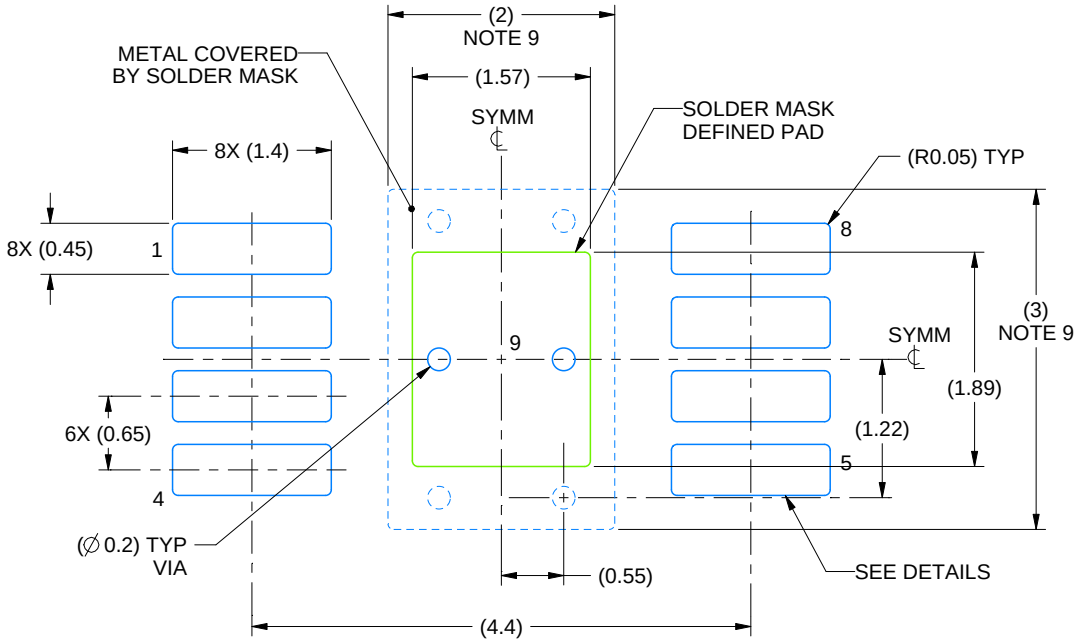
SMALL OUTLINE PACKAGE



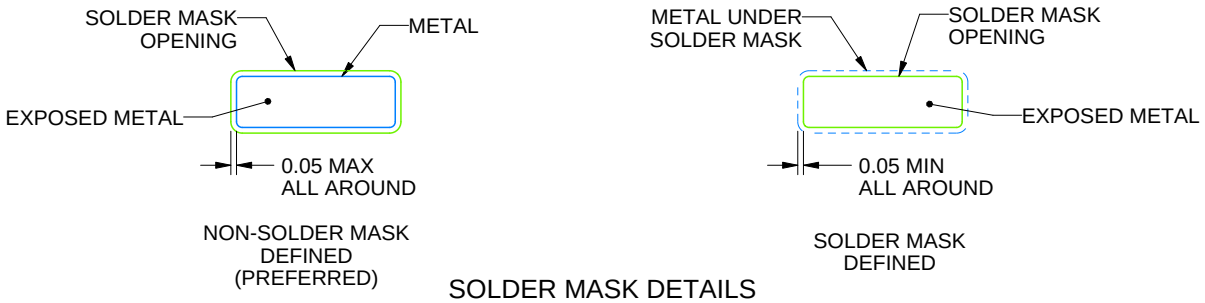
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

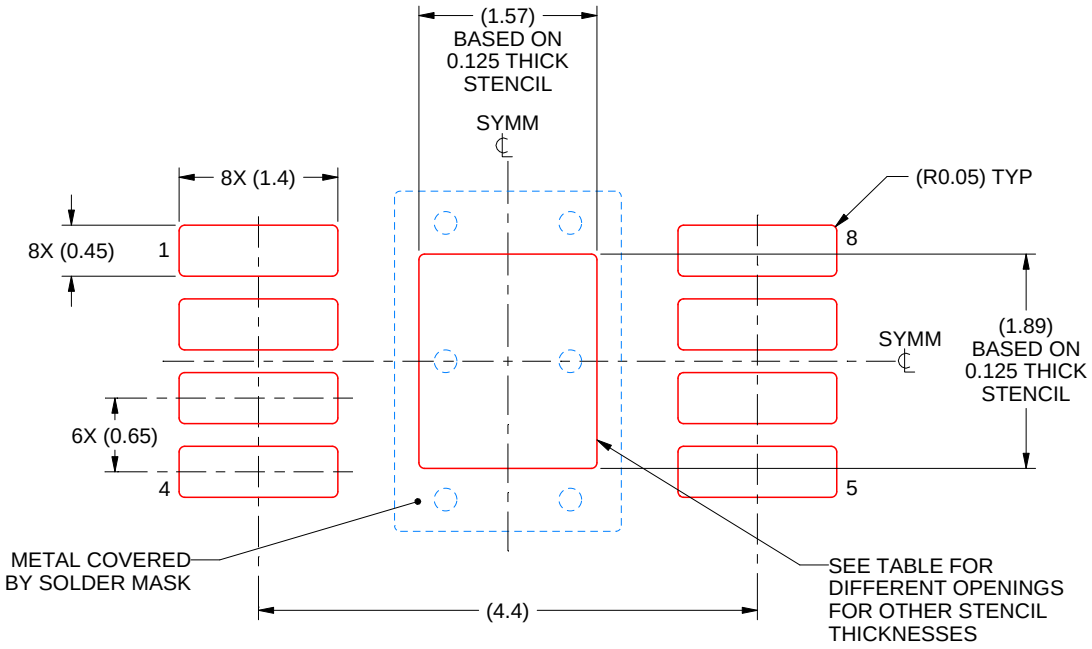


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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