

Automotive-grade N-channel 40 V, 3.0 mΩ typ., 55 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

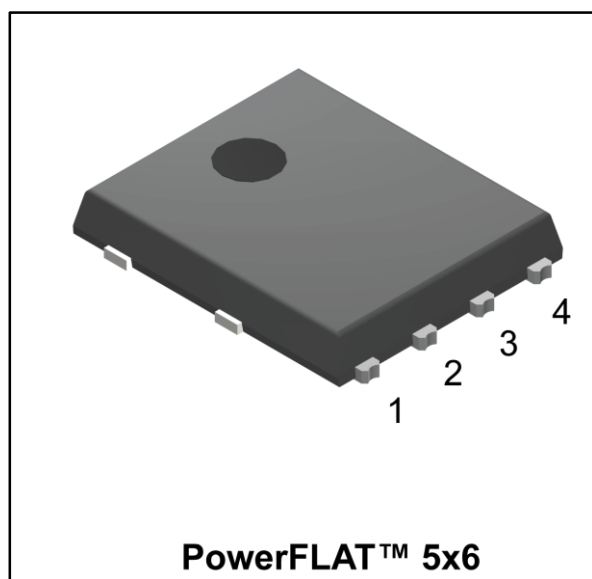
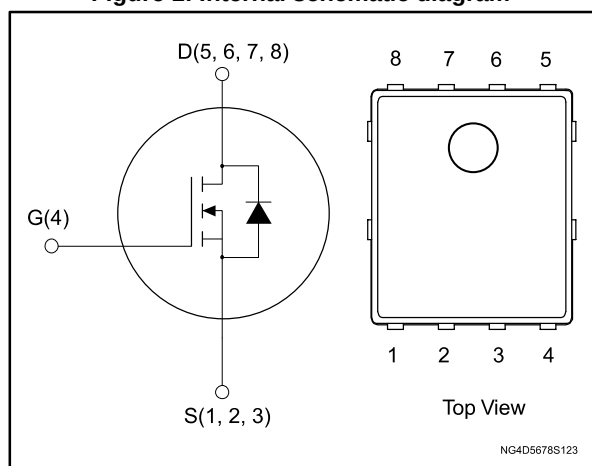


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL120N4LF6AG	40 V	3.6 mΩ	55 A	96 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL120N4LF6AG	120N4LF6	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package information	9
	4.1 PowerFLAT™ 5x6 WF type R package information	9
	4.2 PowerFLAT™ 5x6 WF packing information	12
5	Revision history	14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	40	V
V_{DS}	Drain-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	55	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	55	A
$I_{DM}^{(2)}$	Drain current (pulsed)	220	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	96	W
T_{stg}	Storage temperature range	- 55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature range		$^{\circ}\text{C}$

Notes:

⁽¹⁾ Drain current is limited by package, the current capability of the silicon is 120 A at 25 $^{\circ}\text{C}$

⁽²⁾ Pulse width is limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.56	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

Notes:

⁽¹⁾When mounted on 1 inch² 2 Oz. Cu board, $t \leq 10\text{ s}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	26	A
E_{AS}	Single pulse avalanche energy ($T_j = 25\text{ }^{\circ}\text{C}$, $I_C = I_{AV}$, $V_{DD} = 25\text{ V}$)	200	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
I _{DSS}	Zero gate voltage Drain current	V _{GS} = 0 V, V _{DS} = 40 V			1	μA
		V _{GS} = 0 V, V _{DS} = 40 V, T _J = 125 °C ⁽¹⁾			10	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 13 A		3.0	3.6	mΩ
		V _{GS} = 5 V, I _D = 13 A		3.2	4.5	

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	4260	-	pF
C _{oss}	Output capacitance		-	647	-	
C _{rss}	Reverse transfer capacitance		-	373	-	
Q _g	Total gate charge	V _{DD} = 20 V, I _D = 26 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	80	-	nC
Q _{gs}	Gate-source charge		-	15	-	
Q _{gd}	Gate-drain charge		-	15	-	
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	1.5	-	Ω

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 20 V, I _D = 13 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	20	-	ns
t _r	Rise time		-	70	-	
t _{d(off)}	Turn-off delay time		-	40	-	
t _f	Fall time		-	20	-	

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		26	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		104	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 13\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	40		ns
Q_{rr}	Reverse recovery charge		-	5.6		nC
I_{RRM}	Reverse recovery current		-	2.8		A

Notes:

⁽¹⁾This value is rated according to $R_{thj-pcb}$

⁽²⁾Pulse width is limited by safe operating area

⁽³⁾Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

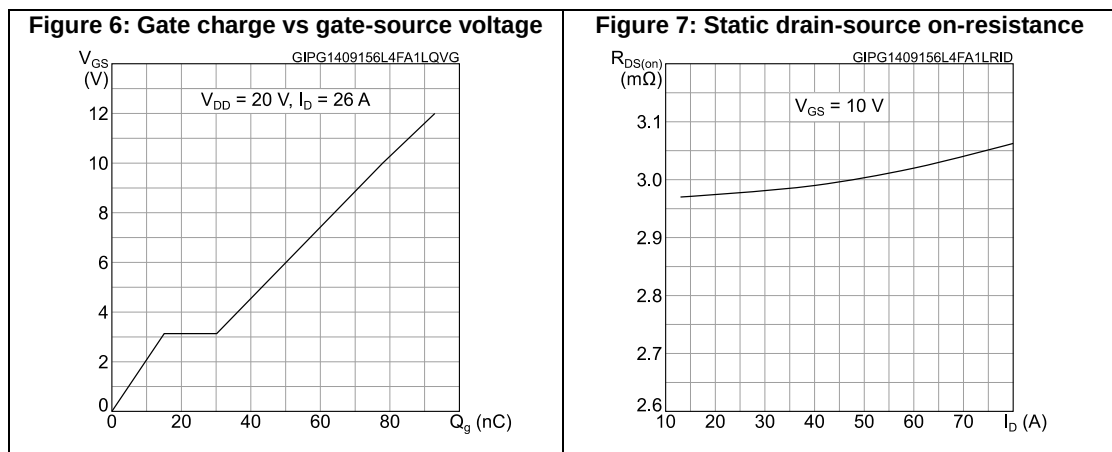
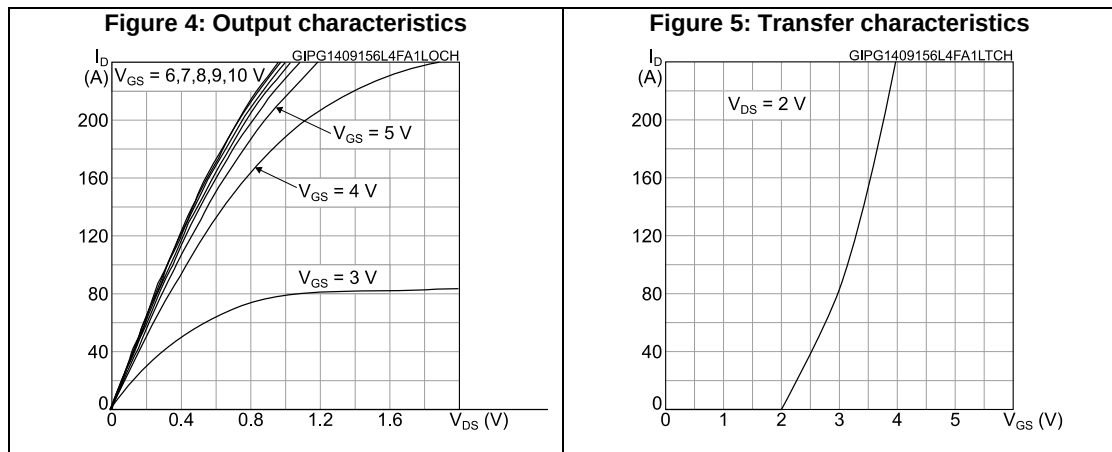
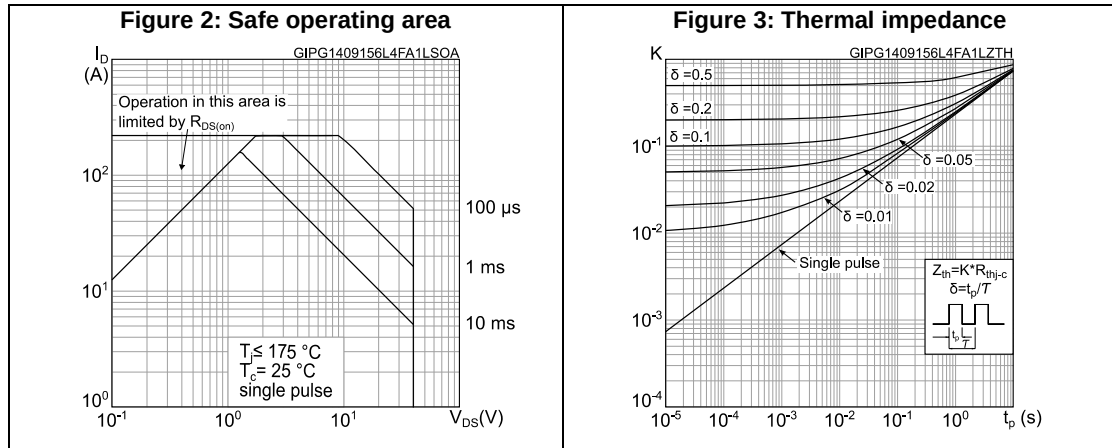


Figure 8: Capacitance variations

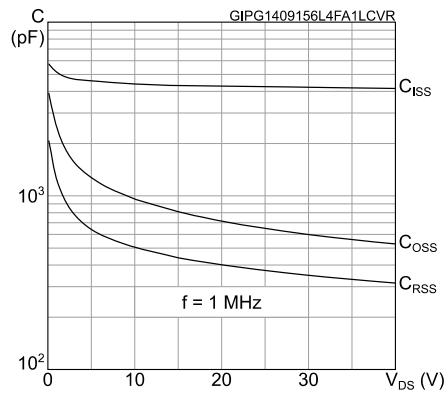


Figure 9: Normalized gate threshold voltage vs temperature

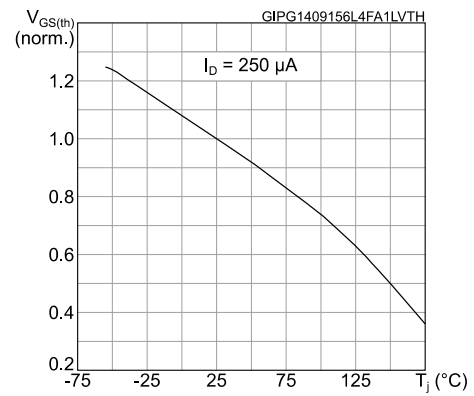


Figure 10: Normalized on-resistance vs temperature

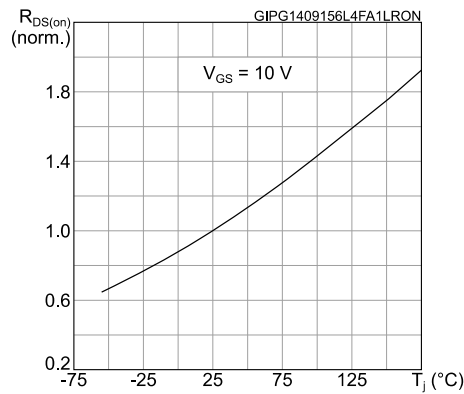


Figure 11: Normalized V(BR)DSS vs temperature

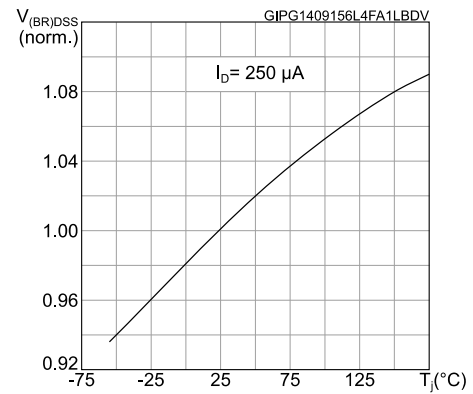
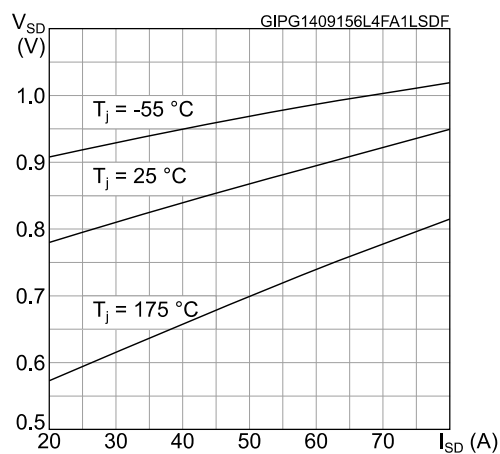
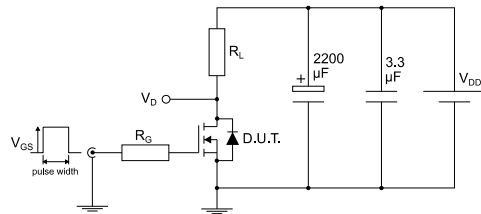


Figure 12: Source-drain diode forward characteristics



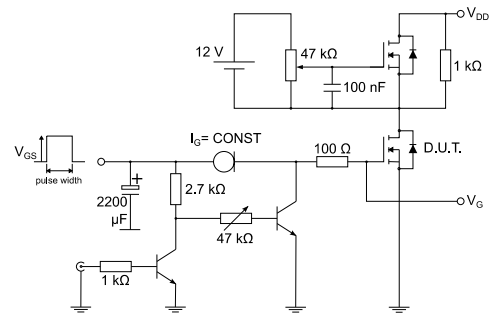
3 Test circuits

Figure 13: Test circuit for resistive load switching times



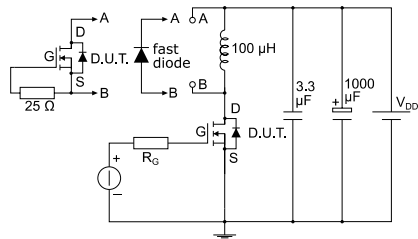
AM01468v1

Figure 14: Test circuit for gate charge behavior



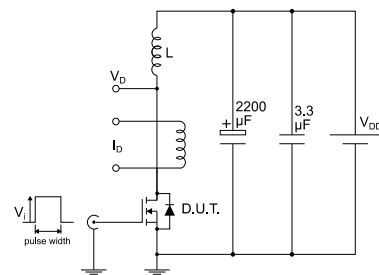
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



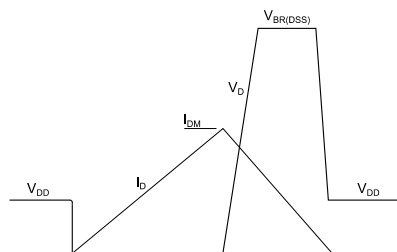
AM01470v1

Figure 16: Unclamped inductive load test circuit



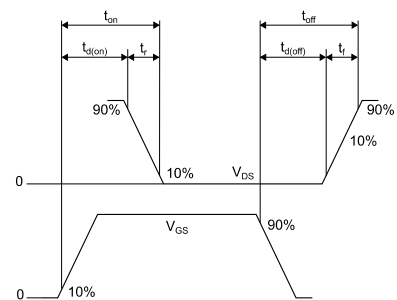
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 19: PowerFLAT™ 5x6 WF type R package outline

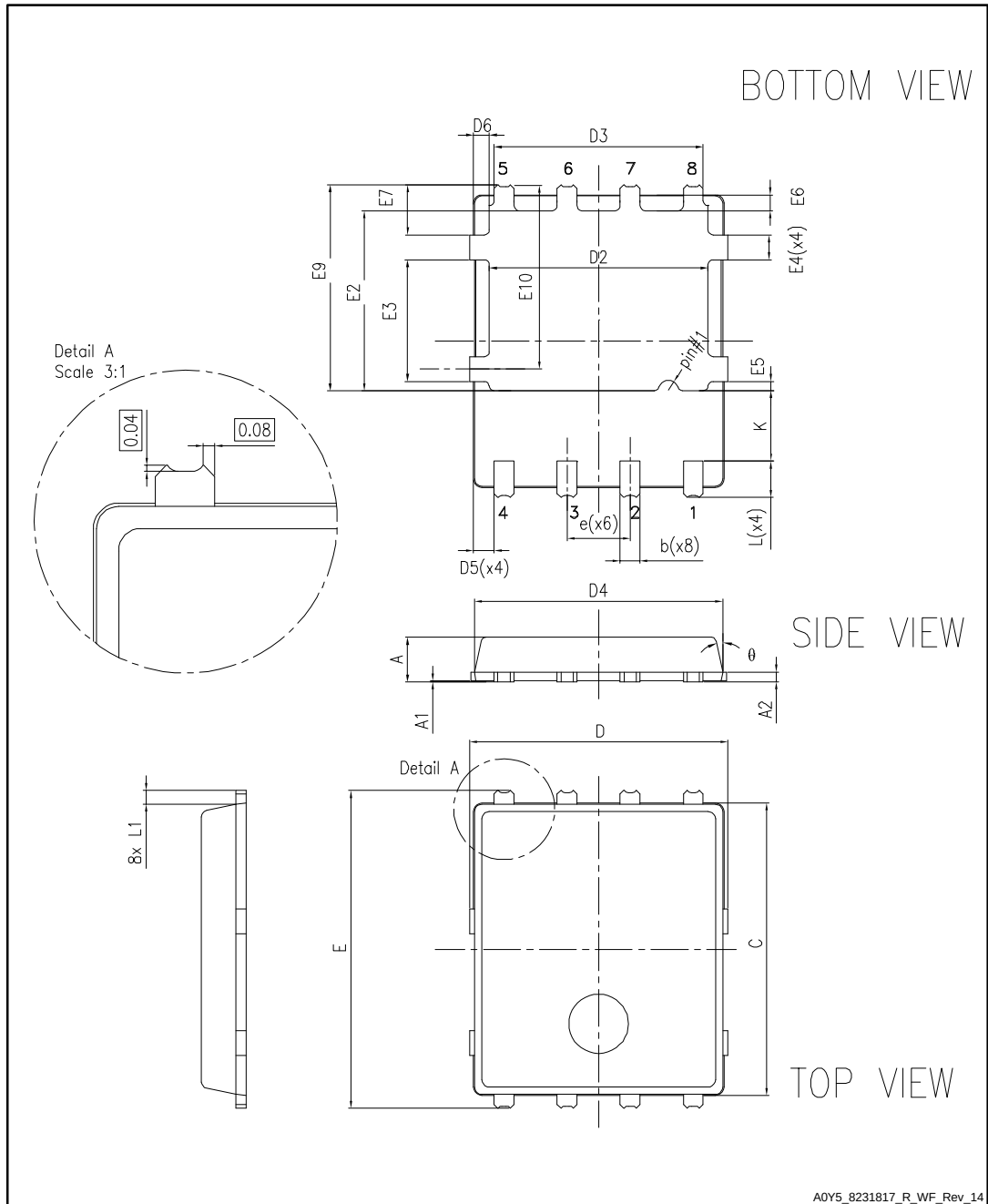
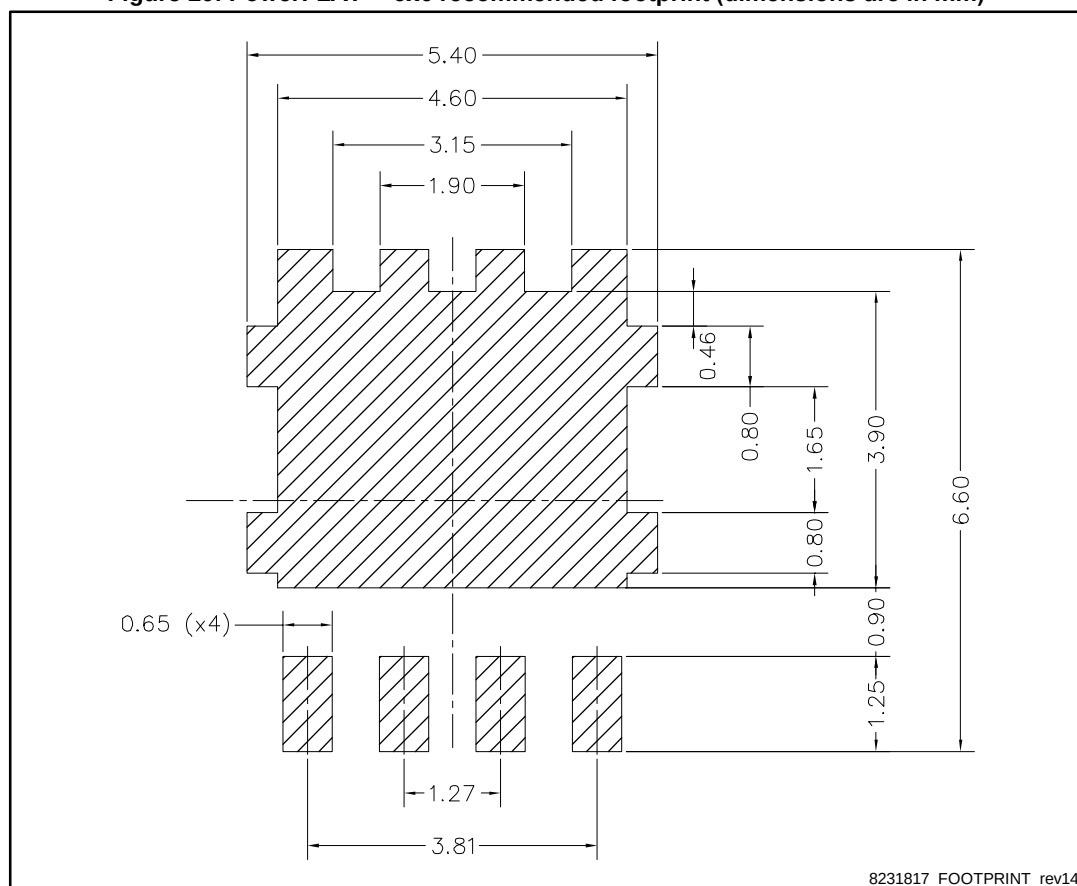


Table 9: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

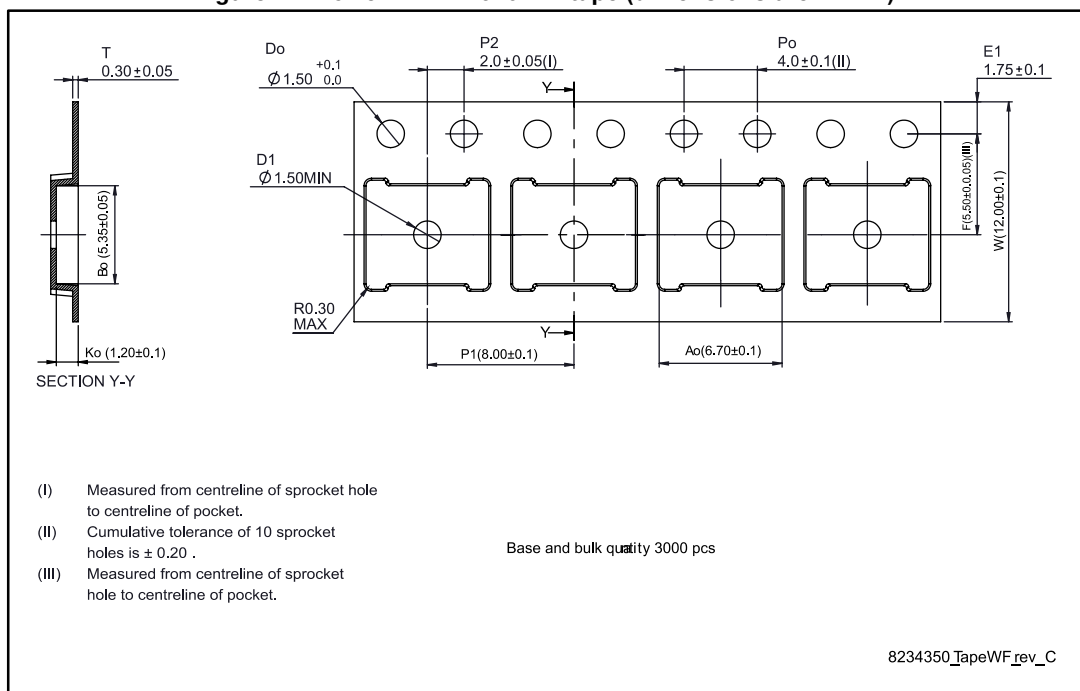


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

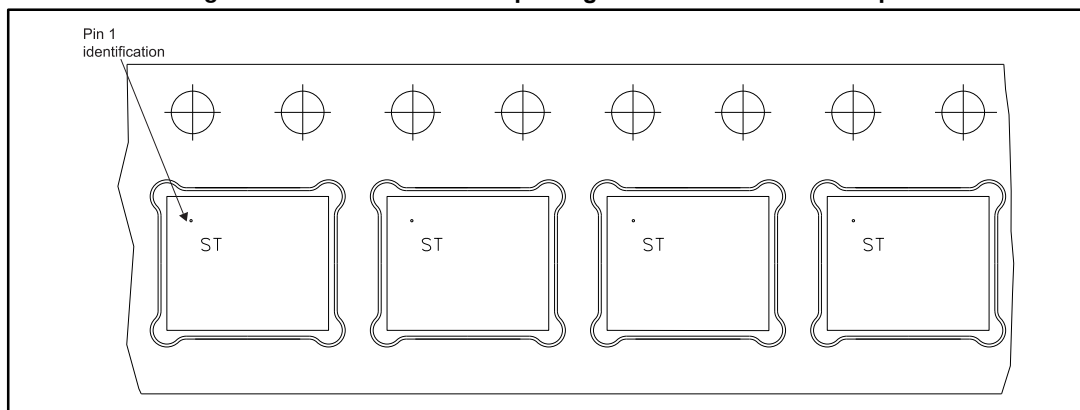
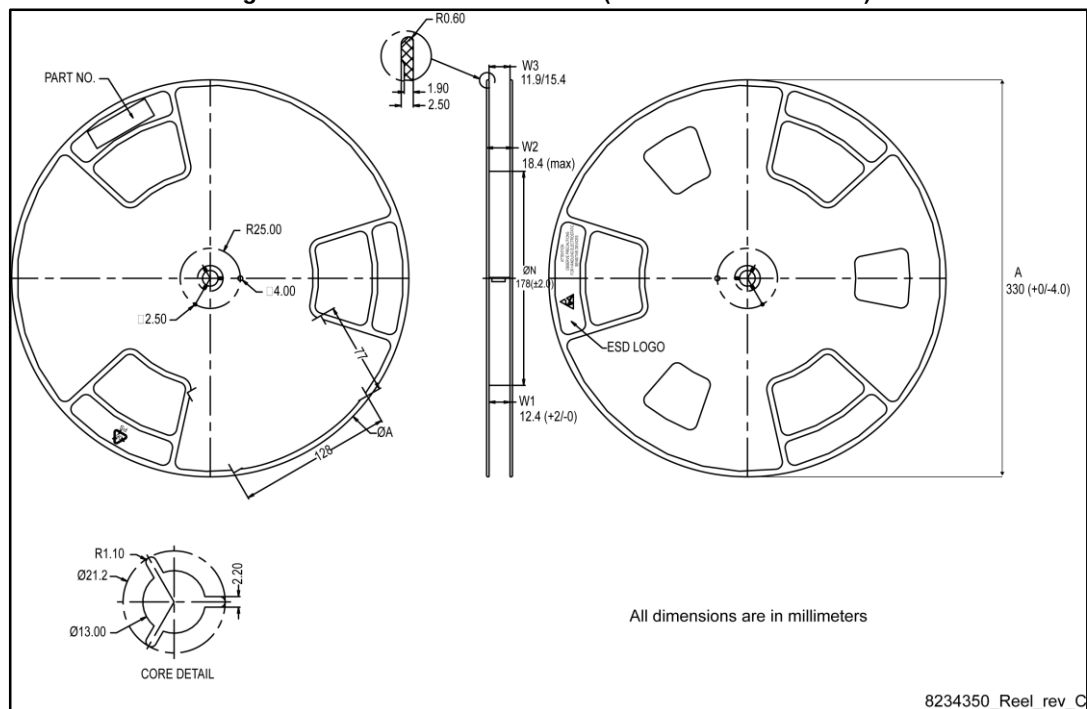


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
25-Sep-2015	1	First release.
15-Apr-2016	2	Updated title, description and features in cover page . Updated Table 2: "Absolute maximum ratings" and Table 5: "On/off states" . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved