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TUTORIAL 4676

Introduction to the DS8500 HART Modem

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Abstract: This application note describes how to use of DS8500 HART modem for a process-control application. The article explains how to interface the DS8500 to a microcontroller and 4–20mA current loop to ensure proper HART communication.

Introduction

This application note introduces the DS8500 single-chip modem for HART® communication. This document should be used in conjunction with the DS8500 data sheet. While the specific requirements for an application can vary, the reference design shown here is a basic example for implementing a process-control circuit.

HART Overview

Highway Addressable Remote Transducer (HART) communication is a commonly used mode of transmission for digital signals that are superimposed on the analog signal of a 4–20mA current loop. The HART protocol is based on the phase continuous frequency shift keying (FSK) technique. Bit 0 is modulated to a 2200Hz sinusoidal signal, and bit 1 is modulated to a 1200Hz sinusoidal signal with a baud rate of 1200bps. These two frequencies can easily be superimposed on the analog current-loop signal, which is in the range of DC to 10Hz, without affecting either signal. This unique nature of the HART protocol enables simultaneous analog and digital communication on the same wire.

DS8500 HART Modem

The DS8500 is a HART modem that provides phase-continuous FSK modulation and demodulation for process-control applications. This device is a feature-rich low-power modem that satisfies the physical layer specifications set by the HART Communication Foundation. The DS8500 has many features that allow the user to easily and effectively design a process-control system that requires a HART modem.

- Reliable signal detection
- Few external components
- Sinusoidal output signal
- Low power consumption
- Standard 3.6864MHz crystal

An internal, digital-signal-processing technique enables reliable FSK_IN signal detection; very few external components are required to separate a HART signal from the noise. FSK_OUT is a sinusoidal signal that provides the lowest harmonic distortion to the system.

Figure 1 shows a top-level block diagram of the DS8500 in an intelligent process transmitter. The design

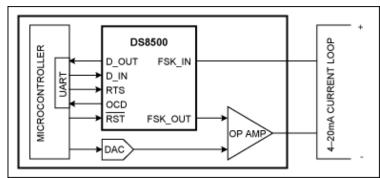highlights the interface between the HART modem and other external ICs.

Figure 1. An intelligent process transmitter features the DS8500 HART modem communicating with a system microcontroller.

Basic DS8500 Operation

Clock

The DS8500 requires a 3.6864MHz clock as an input source with ±1% accuracy to guarantee proper operation. **Figure 2** shows a typical circuit for clock source. When XCEN is set high, the user can drive an external clock directly onto the XTAL1 pin. If an external 3.6864MHz crystal is desired, XCEN should be set low and the crystal needs to be connected between XTAL1 and XTAL2.
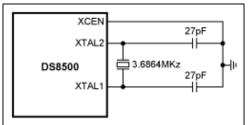

Figure 2. Crystal connection for the DS8500.

Microcontroller Interface

The HART protocol requires signals to be communicated in a specific 11-bit UART format: a start bit, 8 data bits, one parity bit, and a stop bit. The modulator and the demodulator blocks of the DS8500 need to interface with a microcontroller UART to satisfy the protocol requirement.

In demodulator mode, the DS8500 expects a valid UART start signal to synchronize the data communication. The interface between the HART modem and the microcontroller is also shown in Figure 1. Referring back to Figure 1, the microcontroller must contain the HART software stack required for communication. D_IN is the digital-signal data input to the DS8500 which will modulate it to an FSK_OUT signal. D_OUT is the digital-signal data output from the DS8500 that has been demodulated from an FSK_IN signal. RTS receives the microcontroller's request to initiate the demodulate (Rx) or modulate (Tx) mode of the modem.

Active-low RST provides a reset to the DS8500 and ensures that all the internal registers and filters start from a known default value. OCD is a carrier-detect signal that determines an FSK signal with a valid amplitude at the input of the demodulator. A logic high on OCD indicates that the FSK_IN signal amplitude is greater than 120mV; a logic low indicates that the FSK_IN signal amplitude is less than 80mV or that there is no carrier signal. Optionally, the microcontroller can provide a 3.6864MHz clock to the DS8500.

Modulator Waveform

Figure 3 shows the DS8500 in modulate mode where D_IN is the input to the modem and FSK_OUT is the modulated output. The data is provided in an 11-bit UART format.
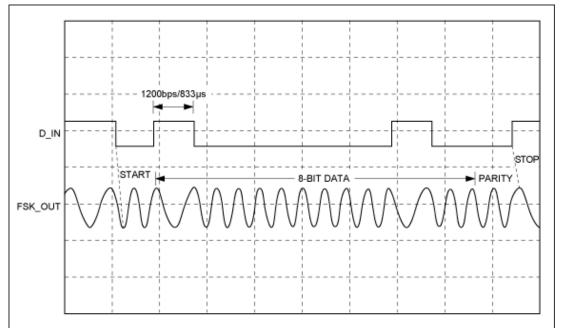

Figure 3. Modulator waveform.

Demodulator Waveform

Figure 4 shows the DS8500 in demodulate mode where FSK_IN is the input to the modem and D_OUT is the output to the UART.
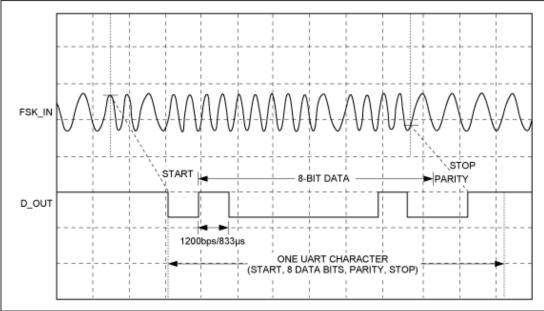

Figure 4. Demodulator waveform.

External Filters

Due to the digital nature of DS8500 and its built-in digital filters, the number of external passive components required for modem operation is greatly reduced.

Figure 5 shows the few external components needed on the receive and transmit sides. The demodulator in DS8500 requires just a simple lowpass filter with a cutoff frequency of 10kHz (R3, C3) and a highpass filter with a cutoff frequency of 480Hz (C2, R2) to separate the HART signal from the analog signal and interferences. The resistor-divider formed by R1 and R2 provides an input bias voltage of $V_{REF}/2$ to the DS8500's receive-side circuitry. The RC values shown below are just an example; a different set of RC values can be used, if the cutoff frequencies of lowpass and highpass filters are met.

Together these external components and the internal filters reject the low-frequency analog signals and prevent them from compromising digital reception. In addition, high-frequency components are also attenuated to prevent interference above the HART extended frequency band.
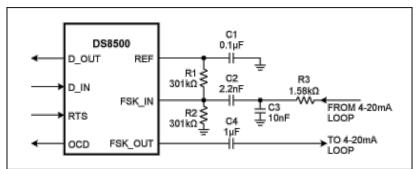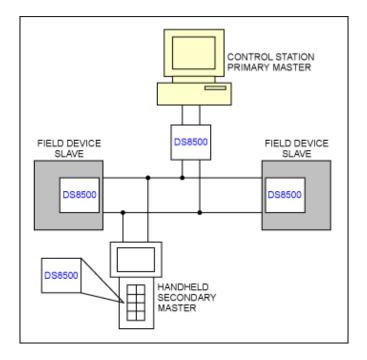

Figure 5. Receive/transmit side external components.

DS8500 as Slave or Master

The DS8500 modem can be used in either the slave side or the master side of HART communication. Typically, on the slave side the HART modem is part of the intelligent process transmitter unit; on the master side the modem is part of the HART master modem cable that connects the central control unit or the handheld unit to the current loop. **Figure 6** shows the interface between master, slave, and current loop.

Figure 6. HART devices connections.

Figure 7 shows a HART slave using DS8500 circuitry and the top-level blocks necessary for an intelligent process transmitter. A temperature process transmitter serves as an example for this circuit. The sensor on the process transmitter measures the system temperature in current or voltage and then passes the data to the ADC. The ADC, in turn, converts these analog signals to digital equivalents for the microcontroller to process. The microcontroller provides remote memory along with computation power. The microcontroller typically hosts the HART stack and is responsible for the protocol implementation; it also processes the digital data from the HART modem. Microcontroller capabilities can also be used for sensor calibration, linearization and signal conditioning. The DAC is primarily responsible for driving the current loop.
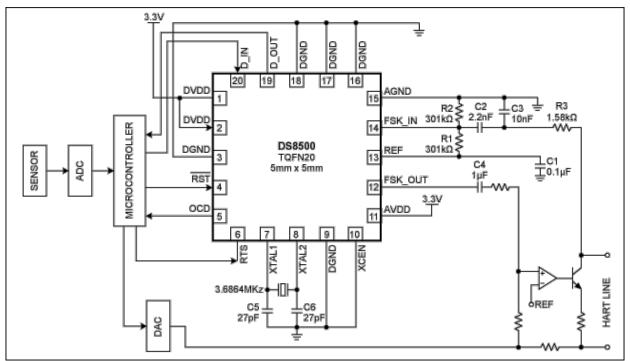

Figure 7. DS8500 on the slave side of HART communication. D_IN receives data from the microcontroller's UART. D_OUT transmits data to the UART. Active-low RST is the DS8500 reset. OCD is a carrier-detect signal that determines a FSK signal with a valid amplitude at the input of the demodulator.

On the master side, the DS8500 can be part of the master modem that resides either on the central control unit or the handheld HART communicator. **Figure 8** shows the master-side configuration. In this case, the DS8500 communicates to the PC through an RS-232 serial port. The HART protocol is usually supported by software that can be installed on the computer.
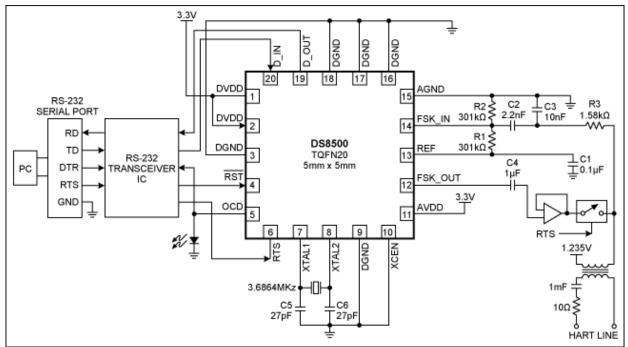
Figure 8. DS8500 on the master side of HART communication. D_IN receives data from the microcontroller's UART. D_OUT transmits data to the UART. Active-low RST is the DS8500 reset. OCD is a carrier-detect signal that determines a FSK signal with a valid amplitude at the input of the demodulator.

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