MCP3X6X Rev. B Silicon Errata and Data Sheet Clarification

The functionality of the MCP346x/356x Two/Four/Eight-Channel 16/24-Bit Delta-Sigma ADCs is described in the device Data Sheets (DS20006180**B** and DS20006181**B**, respectively), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the MCP346x/356x silicon.

Contact Microchip for the latest silicon fix.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Applies to the current silicon revision (Rev. B).

1. Module: DIDD Current

When $\overline{CS}$ is high (SPI inactive) the circuitry for SPI is still active and will consume approximately 26 µA/MHz additional current per pin if either the SDI or SCK pins are toggling. This can occur when other devices on the same SPI bus are being addressed.

Work around

No work around at this time. While the instantaneous current draw is an additional 26 µA/MHz of current, the overall system time-averaged current draw depends on the amount of time the SPI bus is active. If the SPI bus is only active 25% of the overall system operating time and operates at 5 MHz, the time-averaged current draw, as a result of this errata, becomes an additional 32.5 µA per pin.

2. Module: Data-Ready Events

A Data-Ready ($\overline{DR}$) Conversion complete event is indicated using three mechanisms:

1. The $\overline{DR\_STATUS}$ bit in the SPI STATUS byte
2. The $\overline{DR\_STATUS}$ bit in the IRQ Register
3. An $\overline{IRQ}$ pin falling edge

If a $\overline{DR}$ event occurs simultaneously within the transmission of a STATUS byte, between the second and eighth bits transmitted, the $\overline{DR}$ event will be missed and not reflected in the transmission of a subsequent STATUS byte.

Similarly, if a $\overline{DR}$ event occurs between the end of the Command Byte requesting a read of the IRQ Register and the transmission of the IRQ Register data-byte, the $\overline{DR}$ event will be missed and not reflected in subsequent IRQ Register reads.

The $\overline{IRQ}$ pin mechanism to indicate a $\overline{DR}$ event is not affected by this errata.

Work around

A software/firmware workaround can be put in place to check the state of the $\overline{DR\_STATUS}$ bits of the STATUS byte and of the IRQ Register within a single communication sequence. To do this, a read command of the IRQ Register must be executed.

During the transmission of the IRQ Register read command over SDI, a STATUS byte containing the state of the $\overline{DR\_STATUS}$ bit is simultaneously transmitted over SDO. Continued clocking of the SCK pin transmits the data-byte of the IRQ Register containing the state of the $\overline{DR\_STATUS}$ bit. Comparing the state of the $\overline{DR\_STATUS}$ bit of the STATUS byte with the $\overline{DR\_STATUS}$ bit of the IRQ Register determines if a new Data-Ready event has occurred.

If either mechanism indicates a $\overline{DR\_STATUS}$ bit state of '0', new data is available and can be read from the ADCDATA Register. If neither mechanism indicates a $\overline{DR\_STATUS}$ bit state of '0', no new data is available since the last check.

3. Module: Internal Oscillator

The Internal Oscillator PSRR and temperature coefficient can be significantly degraded when operating above 85°C.

Work around

It is recommended to write the code 0x900F00 at the register address 0xB before using the Internal Oscillator. If this workaround is not sufficient, an external clock is recommended.

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4. Module: POR Events During Full-Shutdown Mode

Device CHIPID Bits can become corrupted if power-loss occurs while in Full-Shutdown mode. The CHIPID Bits determine the feature set of the device and corruption of these bits can cause unintended operational behavior of the device.

Work around

As explained in **Section 5.9 Full-Shutdown Mode** of the MCP346x/356x Data Sheet, the AV_{DD}/DV_{DD} voltage levels during power-down (when in Full-Shutdown mode) must reach a level of 100 mV or less, before power can be reapplied. If the application cannot comply with these power cycling requirements, then Full-Shutdown mode is not recommended as a power-saving mode. Instead, Partial-Shutdown mode is recommended where the POR monitoring circuits remain active, allowing the device to properly resume operation in case of a POR event.

Data Sheet Clarifications:

In the MCP346x/356x Data Sheets (DS20006180**B** and DS20006181**B**, respectively), the following clarifications and corrections should be noted:

a) None to report at this time.

APPENDIX A: REVISION HISTORY

Rev. A Document (August 2019)

• Initial release of this document.

Rev B Document (February 2020)

• Updated Module 3: Internal Oscillator.
• Added Module 4: POR Events During Full-Shutdown Mode describing CHIPID corruption.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

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