

TLV320AIC26EVM

Audio Codec Evaluation Module

User's Guide

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Preface

Read This First

About This Manual

This users guide describes the function and operation of the TLV320AIC26, or simply AIC26, audio codec evaluation module. This manual will help you quickly set up the evaluation board and its accompanying software, so that you can rapidly test and evaluate the AIC26. A complete circuit description, as well as schematic diagram and bill of materials are included.

How to Use This Manual

This manual begins with an introductory chapter that describes the EVM and what it can do. If you are anxious to setup the EVM and start testing, we suggest you read at least the first two chapters. These two chapters introduce you to the board and how to set it up. Later chapters go into more detail on the board's design and how to access its many features.

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Data Sheets:

TLV320AIC26
TAS1020B
TPS767D318
SN74LVC125A

Literature Number:

SLAS412
SLES025A
SLVS209D
SCAS290M

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Introduction

The AIC26 is a low power high performance audio codec with mono input and stereo output. There are two digital interface buses on the AIC26 that communicate with a host processor: the SPI interface and the I²S interface. The SPI serial interface is for a host processor to control the AIC26, and the audio data is communicated to the AIC26 over the I²S bus. The AIC26 accesses both of these buses through the use of a USB microcontroller, which provides a way to generate data for both buses from a PC running Windows® 98, Windows 2000, or Windows XP.

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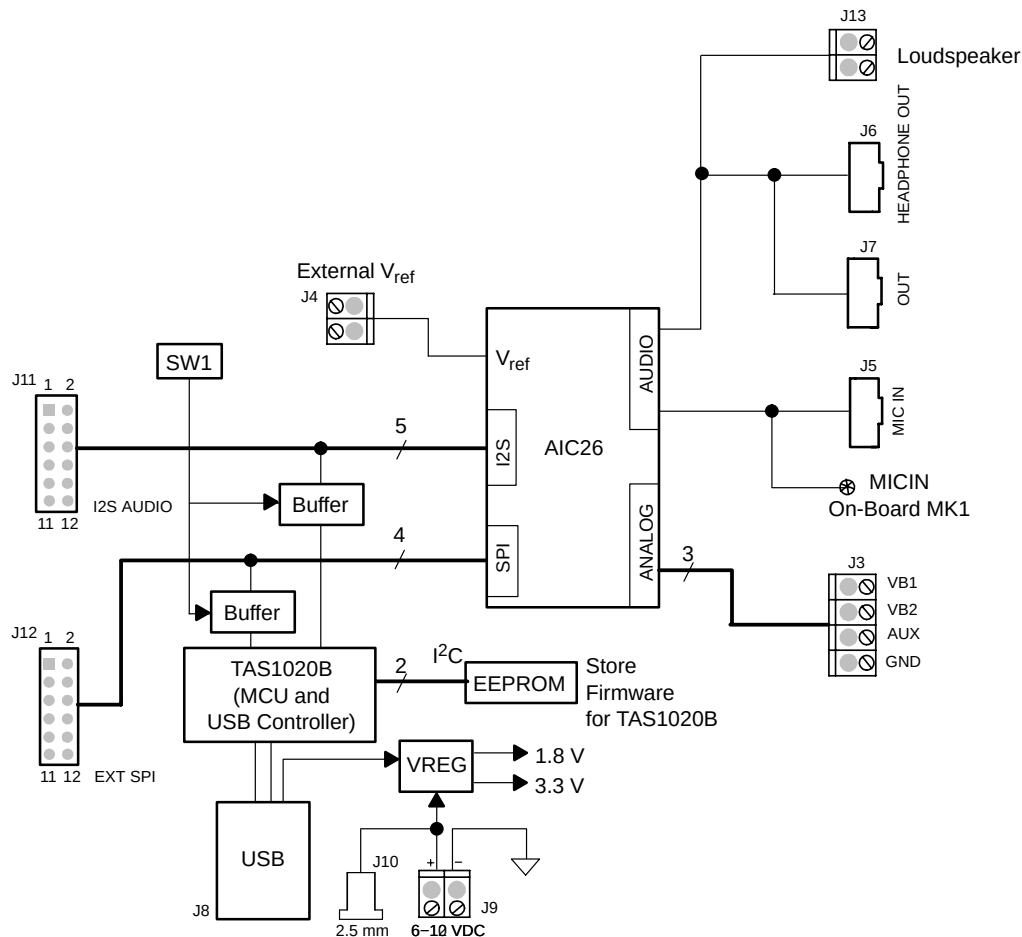
1.1 Device Characteristics

The AIC26 is an audio codec with headphone/speaker amplifier and a 12-bit battery/temperature/auxiliary measurement ADC. The AIC26 has audio playback and record capabilities. Access to the audio DAC and ADC sections of the AIC26 is through an I²S interface. The AIC26 interfaces to the host controller through a standard SPI serial interface. The AIC26 offers two battery measurement inputs capable of reading battery voltages up to 6 V, while operating with only a 2.7-V supply. It also has an on-chip temperature sensor capable of reading 1°C resolution.

1.2 EVM Block Diagram

A block diagram of the AIC26 evaluation kit is shown in Figure 1–1.

Figure 1–1. AIC26 Evaluation Kit Block Diagram



The digital control interface is through either the USB bus or an external SPI bus. The onboard microprocessor can be disabled, allowing the external SPI bus to control the AIC26.

Power supplies are derived from the USB bus, or may be provided to the kit through external connectors from an external user-supplied laboratory power supply.

1.3 Analog Inputs/Outputs

The audio signal comes from either the on-board microphone MK1 or an external microphone, connected to J5. The audio output is accessed through connectors J6, J7, and/or terminal block J13. The other analog inputs are brought onto the board through the J3 terminal block. The AUX input must be between 0 V and 3.3 V, while the battery inputs, VBAT1 and VBAT2 can range from 0 V to 6 V.

1.4 External Voltage Reference

If the external voltage reference is used, the reference can be input to the AIC26 device through the J4 terminal block. The reference (internal or external) is needed for the AUX, BAT1, or BAT2 ADC measurement.

1.5 Power Requirements

The AIC26EVM can be powered from either the USB port or an external 6-VDC to 10-VDC power supply.

1.6 Computer Requirements

The AIC26EVM software is designed to run on a PC running Windows™ platforms that support USB (Windows™ 98SE, 2000, XP, etc).

Minimum requirements include:

- ☐ IBM-compatible Pentium PC or higher
- ☐ Windows™ 98SE/2000/XP
- ☐ 64-MByte RAM minimum
- ☐ 20-MByte Available hard disk space
- ☐ CD-ROM drive
- ☐ USB Port

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Getting Started

This chapter guides you through unpacking your EVM and setting it up so you can begin working with it immediately.

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2.1 Unpacking the EVM

When unpacking the AIC26EVM, check to make sure that you received all of the material that should be in the box. The EVM kit should include the following:

- ☐ AIC26EVM board, PWB 6444324
- ☐ CD-ROM, 6460667

If any of these components is missing, contact Texas Instruments for a replacement.

2.2 Default Configuration

The AIC26EVM features a few simple means of configuring its operation. The default settings for these items are shown in Table 2–1. When you unpack your AIC26EVM, make sure that your board is initially configured as listed in the table.

Table 2–1. Default Configuration Settings

Board Identifier	Description		Default Setting
JMP1	Differential MIC input		Not installed
JMP2	MIC BIAS select		2 to 3
JMP3	A1 select for EEPROM		Installed
JMP4	PWR select		1 to 2
JMP9	IOVDD selected as 3.3 V		1 to 2
SW1	On board TAS1020B enable	On board I2S	SW1_1 ON
		On board MCLK	SW1_2 ON
		On board SPI	SW1_3 ON
		USB Reset	SW1_4 ON

NOTE: JMP5 through JMP8 are installed by default. These jumpers can be removed and replaced by current meters for evaluating or testing the corresponding power consumption.

2.3 Quick Start

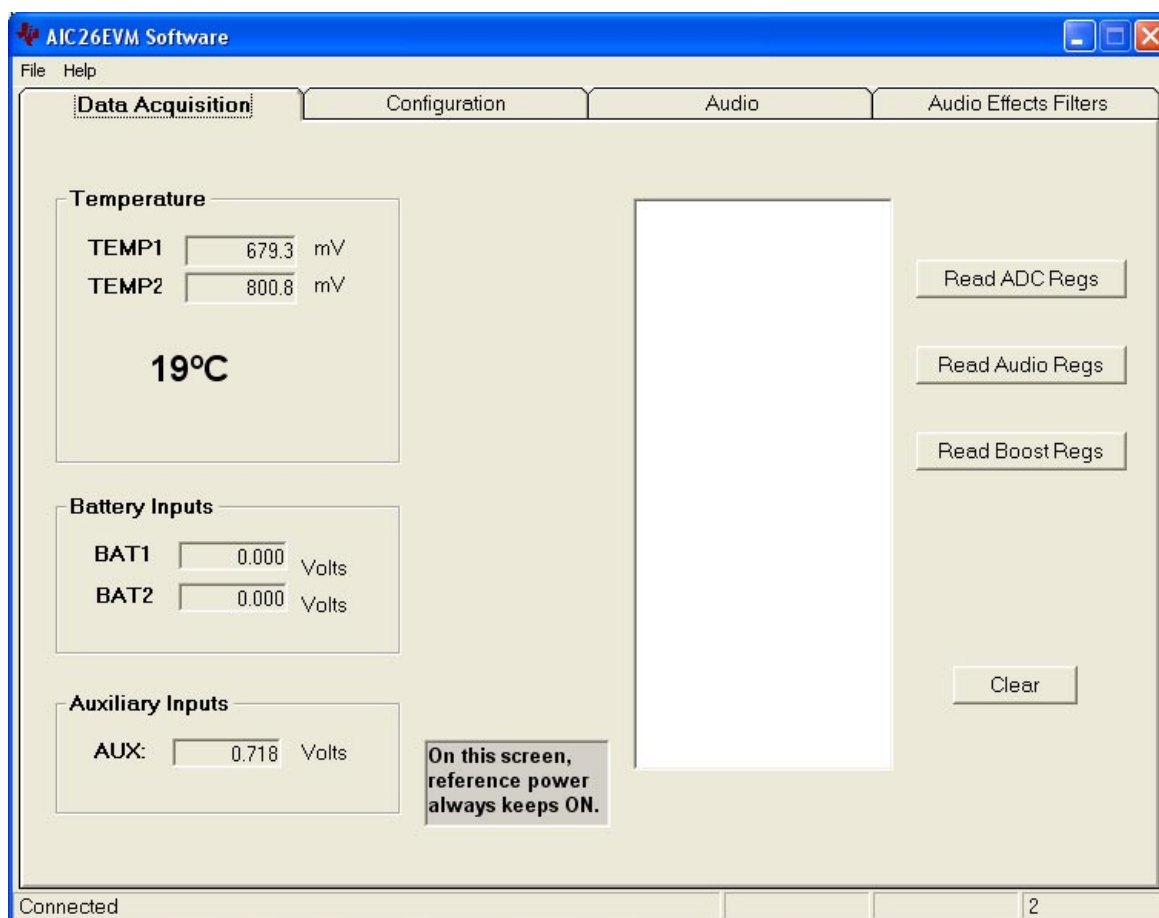
Once the AIC26EVM has been unpacked and you have verified that the board is configured as shown in Table 2–1, install the software.

Place the CD-ROM into your PC's CD-ROM drive. Locate the Setup program on the disk and run it. The Setup program installs the AIC26EVM software on your PC. Note that if you are running Windows™ 2000 or XP, you need administrator privileges to install the software. Follow the instructions that the installer gives you.

When the installation is complete, connect a USB cable from your PC to the AIC26EVM. You may see a message that a Human Interface /Audio Device has been connected. Once this connection has been made, launch the AIC26EVM software on your PC.

The software should automatically find the AIC26EVM. If the board is found, the screen shown in Figure 2–1 appears.

Figure 2–1. Default Software Screen



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Operation

This chapter describes each function of the AIC26 evaluation kit and how to use the accompanying software to control and use the AIC26.

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3.1 Jumpers

Table 3–1 shows the function of each jumper on the EVM.

Table 3–1. Jumper/Function Reference

Reference Designator	Setting	Function	Factory Default	Subsection
JMP1	1 to 2	Differential (MICIN and AUX) microphone input	Not installed	3.1.1
JMP2	1 to 2	MIC BIAS from fixed resistor	2 to 3	3.1.2
	2 to 3	MIC BIAS from AIC26		
JMP3	1 to 2	A1 select for EEPROM	Installed	3.1.3
JMP4	1 to 2	PWR select: USB powered	1 to 2	3.1.4
	2 to 3	PWR select: External power supply		
JMP5 – JMP8	Removed	Power is not provided to AIC26	Installed	3.1.5
	Installed	Power is provided to AIC26		
JMP9	1 to 2	AIC26 uses 3.3-V IOVDD	1 to 2	3.1.6
	2 to 3	AIC26 uses 1.8-V IOVDD		

3.1.1 Differential Microphone Input

The microphone signal can be input to the AIC26 through the MICIN or AUX, if the signal is single ended. In single-ended mode, JMP1 should be removed. The microphone signal, if differential, can be connected to the AIC26 through J5 and to the AIC26 MICIN and AUX pins. In differential mode, JMP1 should be installed.

3.1.2 MIC BIAS Selection

JMP2 selects the microphone bias to come from the AIC26 itself or from an external resistor, R11, which is not installed on the AIC26EVM board. If an external bias is needed, the appropriate size resistor can be soldered into the R11 location on the board and JMP2 set to connect between positions 1 and 2. If MIC BIAS is not required, do not install the jumper top for JMP2 in any position.

3.1.3 EEPROM A1 Select

The AIC26EVM loads its firmware from an onboard EEPROM. In order to use the firmware in this EEPROM, its address A2, A1, A0 should be 000b. JMP3 is used to pull the A1 line low so that the EEPROM is selected. When A1 is not low, the EEPROM is not able to interface to the on-board TAS1020B processor.

This jumper can be removed when firmware updates are to be made.

3.1.4 Power Supply Selection

The AIC26EVM can be powered from the USB port directly, or an external power supply can be provided through J9 or J10. JMP4 selects between the USB and external power sources.

3.1.5 Power Supply Current Measurement

Four jumpers are on the front of the four power supply pins of the AIC26. The jumpers can be replaced by current meters that measure and monitor the currents in the corresponding power supply pins. Refer to Table 2–1 note.

3.1.6 IOVDD Voltage Selection

One of the features of the AIC26 is that the digital IO power supply is flexible with a range from 1.1 V to 3.6 V. To evaluate the feature, the EVM has the JMP9 jumper for IOVDD selection. If JMP9 is at 1 to 2 position, IOVDD is 3.3 V; if JMP9 is at 2 to 3, IOVDD is 1.8 V; and without JMP9, an extra power supply (1.1 V to 3.6 V) can be connected to IOVDD.

3.2 Switches

The SW1 switch on the board gives users the option to select SPI and I²S as well as MCLK signal resources.

Table 3–2 shows the function of the switch.

Table 3–2. Switch Function Reference

Reference Designator		Setting	Function	Factory Default	Subsection
SW1	SW1-1	ON	On-board I ² S selected	ON	3.2.2
		OFF	External I ² S selected		
	SW1-2	ON	On-board MCLK selected	ON	3.2.3
		OFF	External MCLK selected		
	SW1-3	ON	On-board SPI selected	ON	3.2.1
		OFF	External SPI selected		
	SW1-4	ON	USB Reset connected to AIC26	ON	3.2.4
		OFF	USB Reset not connected to AIC26		

3.2.1 SPI Selection

The SPI bus on the AIC26 provides the main interface between a host-processor and the AIC26 device. The on-board TAS1020B plays the role of the host processor, if SW1-3 is set ON. If an external processor or SPI device is used, set the SW1-3 to the OFF position so as to disable the on-board SPI interface to the TAS1020B and open the AIC26 SPI port to the external SPI bus.

3.2.2 I²S Selection

The I²S bus on the AIC26 can interface with the onboard host processor, the TAS1020B USB controller, or with other offboard external I²S processor or devices. When SW1-1 is set ON, the manufacture default, the AIC26 I²S is connected to the TAS1020B's I²S. Otherwise, if SW1-1 is shifted to OFF, the buffer between the on board I²S port is disabled so that an external I²S can communicate with the AIC26 I²S port.

3.2.3 MCLK Selection

The AIC26 requires a proper MCLK for basic audio ADC/DAC functions. The TAS1020B onboard processor generates an 11.2896-MHz frequency to provide the MCLK. If an external MCLK is preferred, SW1-2 should be turned off.

3.2.4 USB Reset

A reset signal output from the onboard TAS1020B processor can be used to reset the the AIC26 whenever the TAS1020B is resetting. SW1-4 is used to enable/disable the connection. By default, the connection is enabled. If the processing is not active, the connection to the AIC26 should be disabled by turning off SW1-4.

3.3 I/O Connector and Signals

The various connectors on the AIC26EVM are described in this section.

3.3.1 Audio Connectors

The AIC26 audio inputs and outputs are routed through these stereo (TIP/RING/SLEEVE) 3.5-mm jacks. Note the polarity of the channel assignments for these connectors.

Table 3–3. Audio Connectors

Reference Designator	Name	Description
J5	Mic In	Microphone input ☐ tip = mic bias voltage (and MIC input–, if different) ☐ ring = mic input+ ☐ sleeve = ground
J6	Headphone Out	Stereo headphone audio outputs ☐ tip = left channel ☐ ring = right channel ☐ sleeve = virtual ground
J7	Line Out	Stereo headphone output with ac coupling ☐ tip = left channel ☐ ring = right channel ☐ sleeve = ground
J13	Loudspeaker	When the AIC26 output drive is in high power mode, an 8- Ω loudspeaker can be connected to J13.

3.3.2 USB Interface Connector

Connection to a USB cable from a PC is made through J8, a standard USB type B receptacle.

Table 3–4. USB Interface Connector

Reference Designator	Description	Pin Number	Signal Name	Function
J8	USB slave connection to PC	1	VCC	+ 5-V supply from USB
		2	D–	– Differential USB signal
		3	D+	+ Differential USB signal
		4	GND	Ground

3.3.3 External Power Connectors

While it is most convenient to power the AIC26EVM from the USB bus, external power supplies can be used. The two connectors detailed in Table 3–5 are provided for the external power.

Table 3–5. External Power Connectors

Reference Designator	Description	Pin Number	Signal Name
J9	External power terminal block	1	6 VDC to 10 VDC input
		2	Ground
J10	External power jack	–	6 VDC to 10 VDC input, positive center terminal

3.3.4 External Audio Data (I²S) Connector

The I²S bus, which carries audio data to and from the AIC26, is brought out to header J11 and can be connected to external I²S devices if the I²S interface to the on-board TAS1020B is disabled.

Table 3–6. Audio Data Connector

Reference Designator	Description	Pin Number	Signal Name
J11	Audio data (I ² S) connector	1	MCLK
		3	BCLK
		5	LRCLK
		7	I2SDIN
		9	I2SDOUT
		11	PWD/AWDS
		2,4,6,8,10,12	Ground

3.3.5 External SPI Connector

The AIC26 SPI port is brought out to the J12 header. It can be driven by an external source if the onboard microprocessor is disabled.

Table 3–7. External SPI Connector

Reference Designator	Description	Pin Number	Signal Name	Function
J12	External SPI Bus	1	RESET	Reset line
		3	$\overline{SS}$	Slave select for SPI bus.
		5	SCLK	Serial clock for SPI bus.
		7	MOSI	Master out, slave in data line for SPI bus. Data travels to the AIC26 over this line.
		9	MISO	Master in, slave out data line for SPI bus. Data travels from the AIC26 over this line.
		11	$\overline{PENIRQ}$	AUX, BAT1, BAT2 data available ($\overline{DAV}$) interrupt.
		2, 4, 6, 8, 10, 12	GND	Ground

3.3.6 Analog Input Connector

The auxiliary and battery inputs to the touch screen controller are brought onto the EVM board through terminal block J3. The pinout is shown in Table 3–8.

Table 3–8. Analog Input Connector

Reference Designator	Description	Pin Number	Signal Name	Function
J3	Battery and auxiliary inputs to the touch screen control	1	VBAT1	Battery input 1, 0 V to 6 V
		2	VBAT2	Battery input 2, 0 V to 6 V
		3	AUX	Auxiliary input, 0 V to VREF
		4	GND	Ground

3.4 Circuit Description

The AIC26 evaluation kit circuitry consists of a USB microprocessor, power supply circuitry, analog input interfaces, and audio interface circuitry (both analog and digital). These circuits are described in the following sections.

3.4.1 USB Microprocessor

The AIC26EVM has a USB interface for connecting to a PC. This connection is made through a TAS1020B streaming audio processor, U5.

The SPI interface to the AIC26 can be controlled from two sources: the external SPI header, J12, or through the onboard microprocessor (U5) via USB. The U5 outputs are enabled only when the supplied firmware is loaded and the TAS SPI switch SW1-3 is turned on. The firmware resides in the serial EEPROM chip (U2). U5 only loads firmware from U2 when U2's A1 address line is pulled low. To disable firmware loading, A1 must be high, by having JM3 removed.

When the firmware is loaded and active, D2 (a yellow LED) is lit.

If no firmware is loaded, U3's outputs are in 3-state, allowing the external SPI bus to drive the AIC26 and turn off SW1-3 to ensure the isolation of the TAS1020B from the SPI bus. When the firmware is loaded, the PC software enables the microprocessor to control the SPI bus.

Do not drive the external SPI bus when the firmware is loaded and the onboard microprocessor is active. Disable the microprocessor by removing JMP3, turn off SW1-3, and cycle power to the AIC26EVM in order to use the external SPI bus.

Each signal from the SPI inputs is connected directly to the AIC26. As such, signals on these pins must not exceed the power supply voltage of the AIC26, which is 3.3 V on this EVM.

Likewise, the I²S signals for the digital audio can be driven either externally by J11 or by the USB audio controller (U5).

Do not drive the external I²S bus when the firmware is loaded and the onboard microprocessor is active. Disable the microprocessor by removing JMP3, turn off SW1-1 and SW1-2, and cycle power to the AIC26EVM in order to use the external I²S bus.

3.4.2 Power Supply

Power to the AIC26EVM can be derived directly from the USB interface or externally supplied through the J9 terminal block or the J10 barrel jack connector. Supply voltages of 6 VDC to 10 VDC must be supplied from an external supply. Since it is regulated on the AIC26EVM, this input voltage does not need to be regulated, as long as it falls within this range. D1 prevents damage to the board in the event a power supply is connected in reverse polarity.

U6 regulates the input supply voltage to provide 1.8 V for the AIC26's digital core, or the digital IO power supply if the IOVDD is selected as 1.8 V by JMP9. Also, J3 provides the 3.3 V for the remaining hardware. The regulated supply voltages have LEDs attached that alert the user that the supply is working. D4 (red) is the indicator for the 1.8-V power supply and D3 (green) is the indicator for the 3.3-V power supply.

3.4.3 Analog Inputs

Terminal block J3 provides input connection points for the battery and auxiliary inputs. Battery inputs can range from 0 V to 6 V, and the auxiliary input can range from 0 V to V_{reg} .

Each of these three inputs to the AIC26 internal ADC circuitry has a provision for an RC filter to be placed in line with the signal. As shipped, all of the resistors are 0 Ω and the capacitor is not installed. If noisy conditions prevent obtaining good readings from the AIC26, 0.01- μ F to 0.1- μ F capacitors can be installed in positions C5 through C7. If more filtering is required, the 0- Ω resistors should be unsoldered from the board and replaced with small resistors.

3.4.4 Voltage Reference

The AIC26 has an internal voltage reference, selectable at 1.25 V or 2.5 V. If an external reference is preferred, the external voltage can be input from J4.

3.4.5 Audio Interface Circuitry

A mono electret microphone can be connected to J5. This jack provides both audio and bias connections. Bias for the microphone can be supplied either from the AIC26's mic bias circuitry or from an external resistor (R11). R11 is not installed on the AIC26EVM, but can be installed by the user. Internal or external bias is selected by JMP2.

There is also a small on-board microphone on the EVM, parallel to J5. Without an external electrical microphone, voice can be input to the AIC26 through this microphone.

The AIC26 has a built-in headphone amplifier. J6 is the jack for connection to the amplifier and for driving a 16- Ω load at over 25 mW. Also, under audio

output high power mode (refer to the data sheet) an 8- Ω loudspeaker can be connected to the terminal block J13.

Another audio output jack (J7) is parallel to J6 and provides a secondary connection to the AIC26 built-in headphone amplifier (with ac coupling).

3.5 Program Description

After installing the software for the AIC26EVM as described in Section 2.3, you may begin using it to evaluate and develop with the AIC26.

3.5.1 Data Acquisition Screen

The program's interface is a simple, four-tab interface. Clicking on a tab takes you to the functions associated with that tab. The program begins on the Data Acquisition screen (the default) as shown in Figure 2–1.

The status bar is at the bottom of the screen is divided into four sections and shows the status of communication between the PC and the EVM. Starting from the left, the first section shows the status of the connection; if an error in communication occurs, an error message appears here, otherwise it looks as shown in Figure 2–1. The final section, on the right side of the status bar, shows the number of readings per second.

When on this screen, the AIC26 is commanded to perform the battery and auxiliary input voltage readings, and then it is commanded to perform a TEMP1 and TEMP2 measurement. These measurements are all repeated twice every second, and the results are displayed on this screen.

On the right hand side of this screen there is a window that shows the AIC26 internal control register values. The three buttons next to the window selects which group of control registers is required to be read and shown. The clear button clears the window contents.

This window is useful for debugging purposes.

Figure 3–1, Figure 3–2, and Figure 3–3 show the AIC26 ADC control registers, the AIC26 audio control registers, and the AIC26 audio base boost filter coefficients, respectively.

Figure 3–1. Data Acquisition Screen With ADC Registers Reading

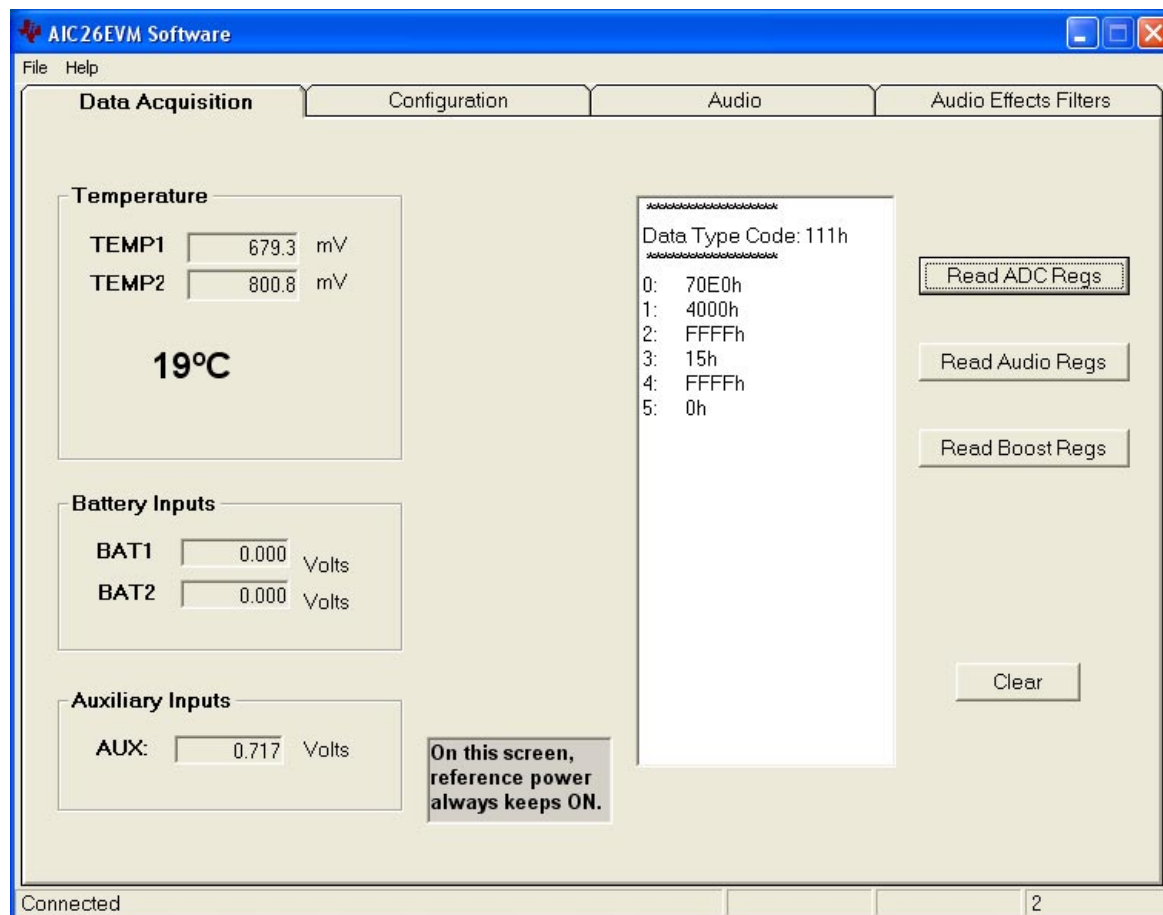


Figure 3–2. Data Acquisition Screen with Audio Registers Reading

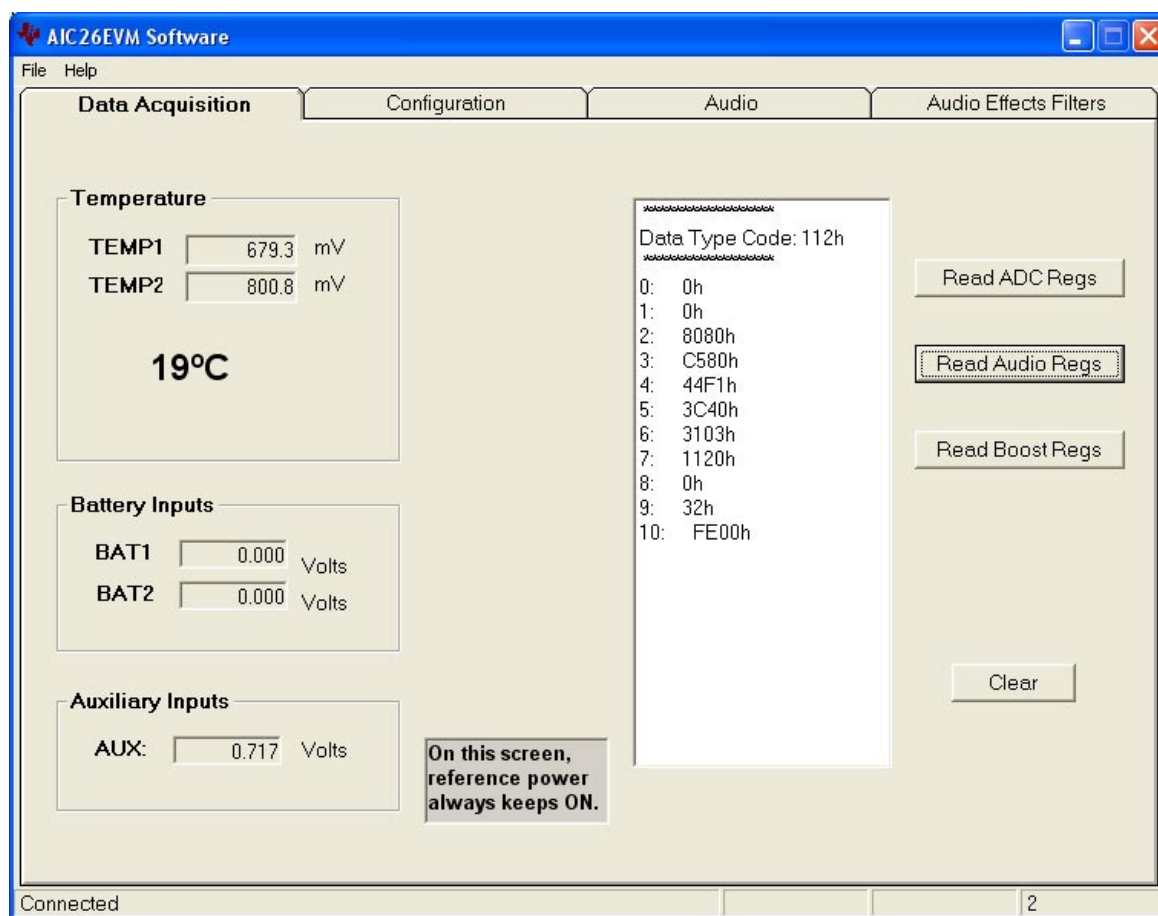
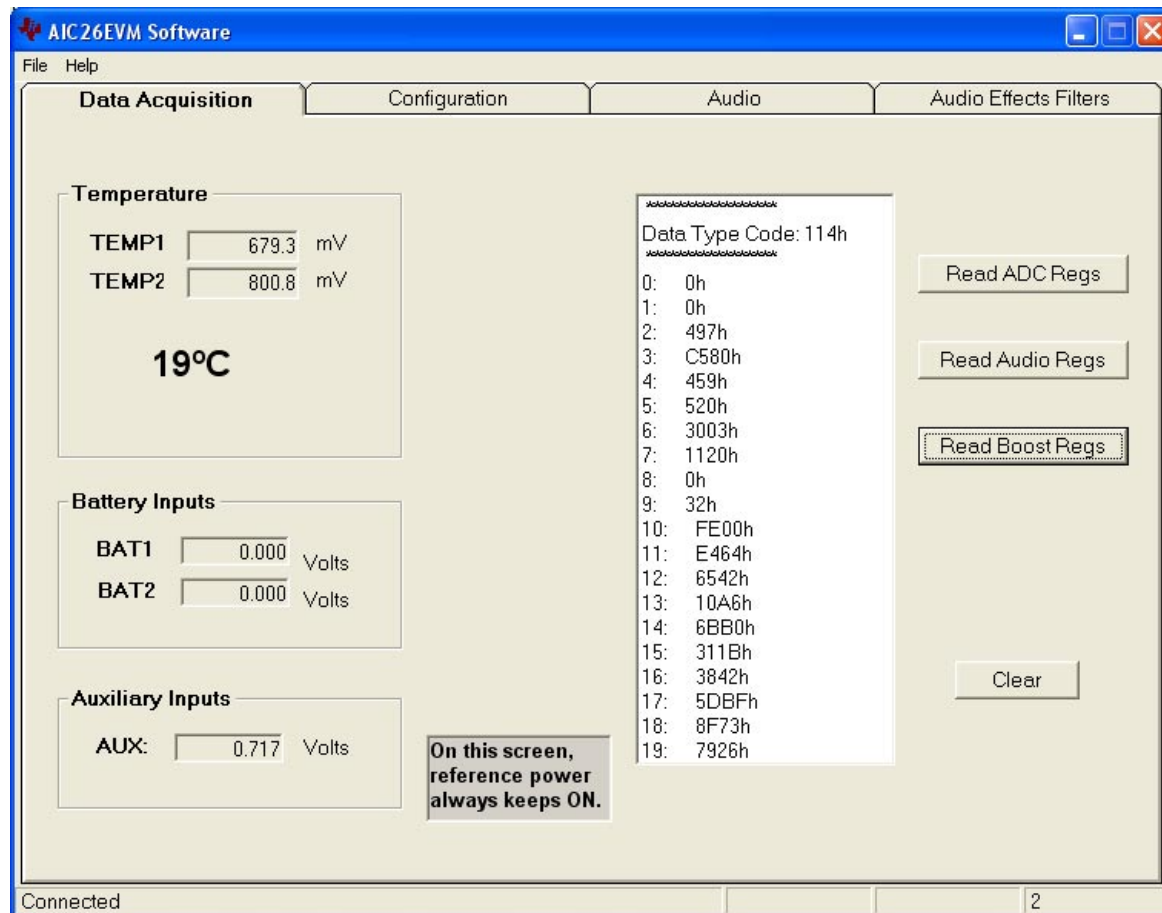


Figure 3–3. Data Acquisition Screen With Boost Filter Parameters

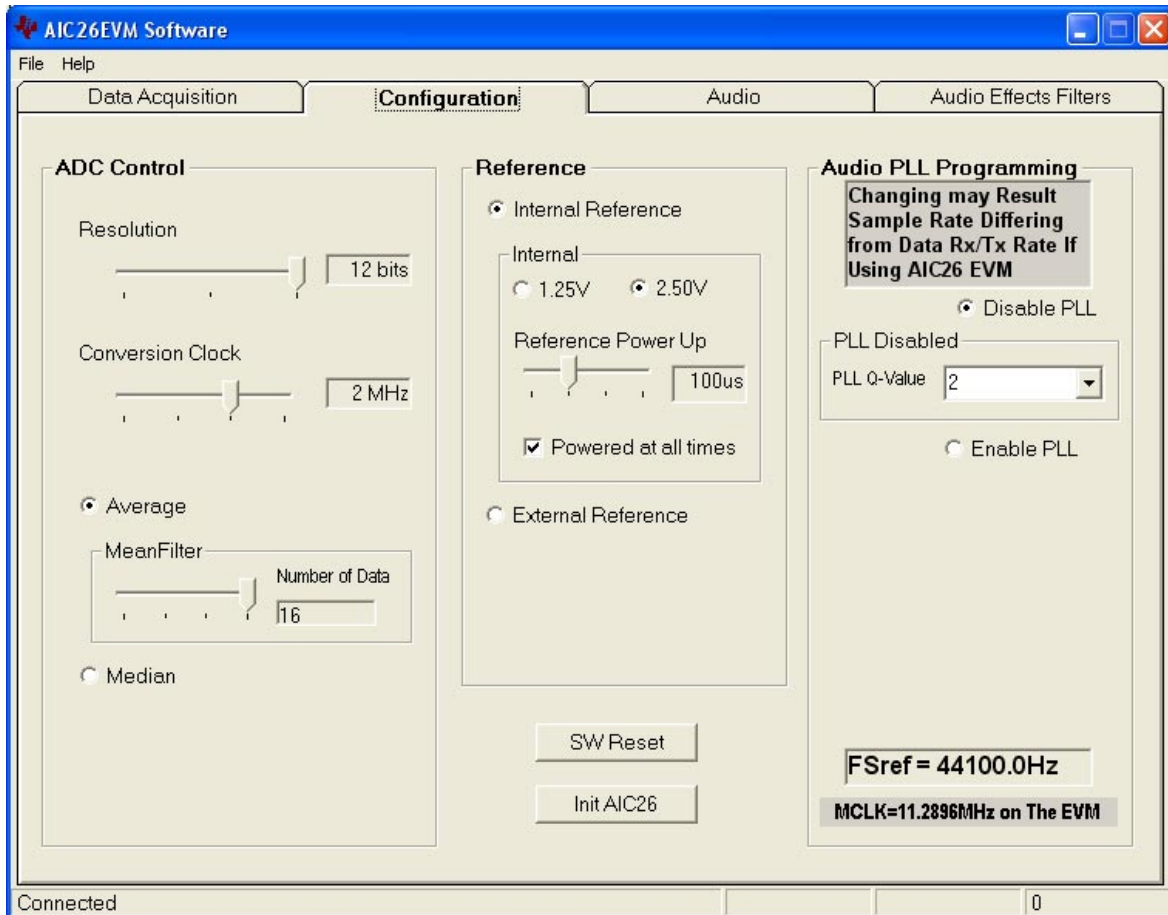


3.5.2 Configuration Screen

This screen provides access to all of the configurable settings for the AIC26's A/D converter and reference, as shown in Figure 3–4.

Located on the right hand side of the screen are the programmable phase lock loop (PLL) settings, which are not the A/D settings but the audio settings.

Figure 3–4. Configuration Screen



3.5.2.1 ADC Control Section

This section controls all of the parameters of the A/D converter. Each slider controls one parameter, whose value is shown next to the slider. Each slider is described below.

- Resolution

Selects between 8-, 10-, and 12-bit resolution.

- Conversion Clock

The internal clock which runs the A/D converter can run at 8, 4, 2, or 1 MHz. When running at 8 MHz, only 8-bit resolution is possible; when running at 4 MHz, 8- or 10-bit resolution is possible, but 12-bit is not. These restrictions are reflected in the operation of this program, since only 1- or 2-MHz clock rates allow 12-bit resolution to be chosen.

■ Average/Median

There are two ways to reduce noise effect to the ADC result. One is averaging where 2, 4, 8, or 16 readings are averaged, and another option is to find the median value among 5, 9, or 15 readings.

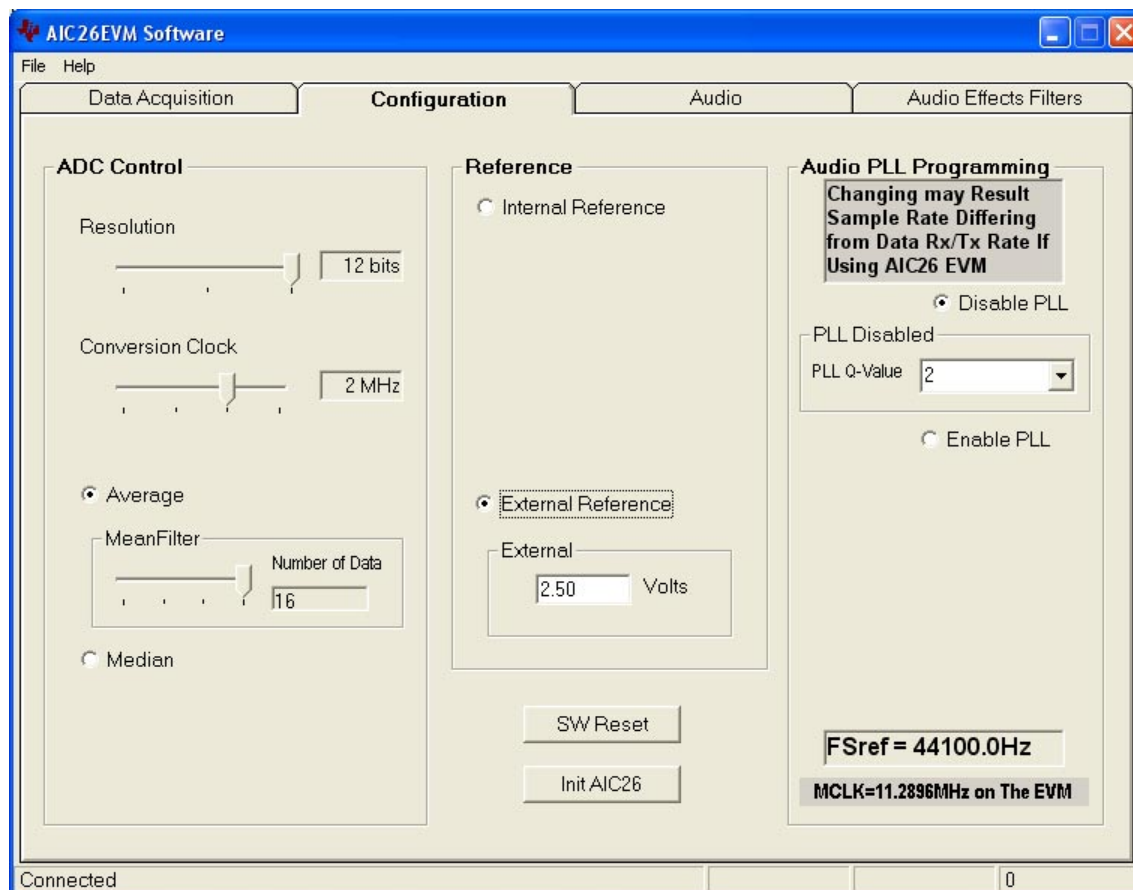
3.5.2.2 Reference Section

For all nonaudio A/D functions, a reference voltage is needed for the A/D converter. Figure 3–4 shows this section with the AIC26's internal reference chosen. This reference voltage can be set to either 1.25 V or 2.5 V.

The internal reference powers down between conversions to save power. Using the *Powered at all times* checkbox, this can be overridden and the reference does not power down. If the reference is allowed to power down, the AIC26 then must allow a delay time for the reference to power up when a conversion is to take place. This delay time can be set using the slider in this section.

If an external reference is to be used, it can be selected as shown in Figure 3–5. The value of the external reference should be entered in the text box shown.

Figure 3–5. Configuration Screen With External Reference Selection



3.5.2.3 Audio PLL Section

On the audio codec part of the AIC26, there is an on-chip phase-lock-loop (PLL). The PLL can be enabled or disabled, based on the given master clock (MCLK) to the AIC26 and the required reference frequency (FSref) for the codec. For more details on the PLL, refer to the AIC26 data sheet.

With the EVM board, the MCLK is at 11.2896 MHz, and the codec sample rate is also fixed at 44.1 kHz. So no PLL is necessary.

With the AIC26EVM, changing the PLL setting may cause audio distortions.

3.5.2.4 Reinitialization and Reset

There are two buttons on this screen that allow the user to reset and reinitialize the AIC26 by clicking these buttons.

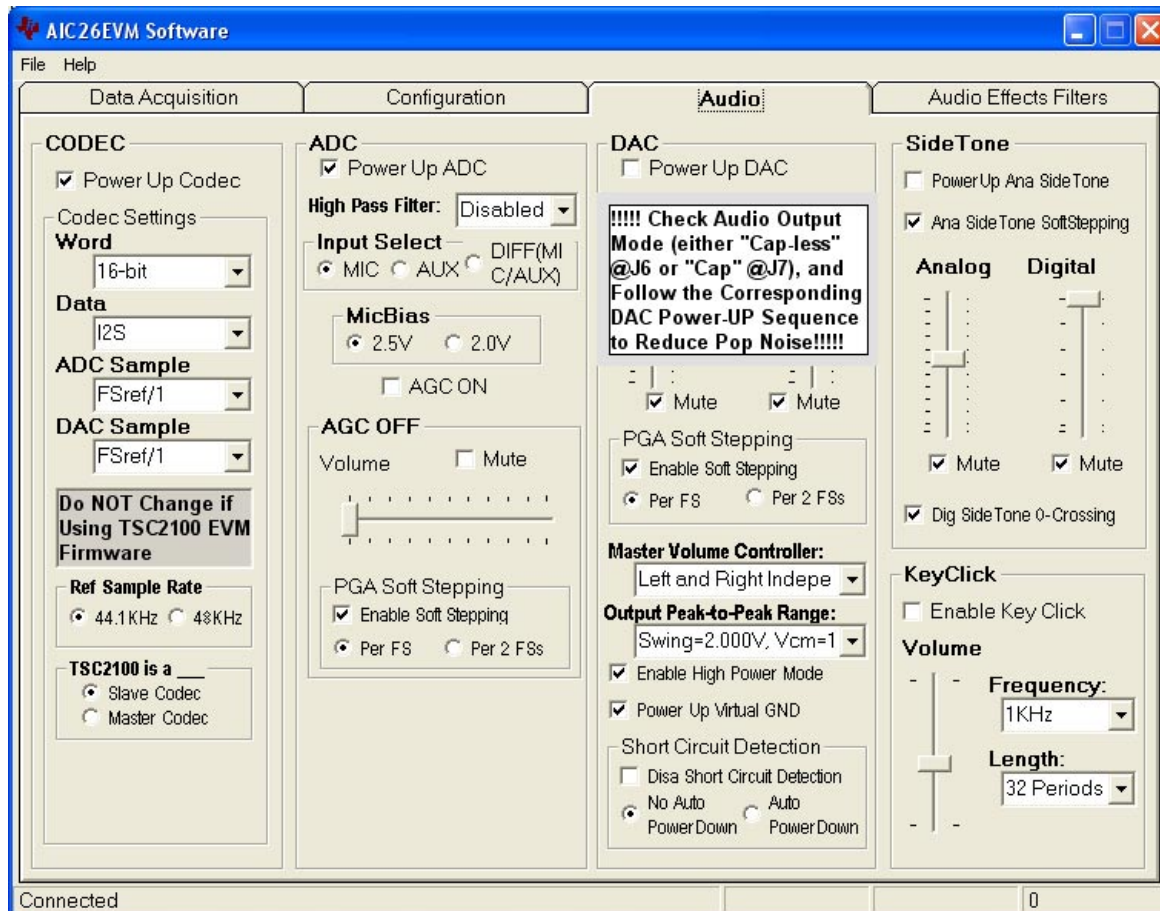
By clicking the button **SW Reset**, a software reset is issued. By clicking the button **Init AIC26**, the control registers (for ADC and audio) revert back to the startup (firmware) default settings.

To bring the AIC26 EVM back to its powerup status, you can clicking **SW Reset** and followed by **Init AIC26**.

3.5.3 Audio Screen

The audio functions of the AIC26 can be accessed using the Audio screen (besides the programmable PLL which is on the configuration screen) as shown in Figure 3–6.

Figure 3–6. Audio Screen



3.5.3.1 Codec Section

By checking Power Up Codec in the codec section, the audio codec is powered up.

In this EVM, the audio codec samples at 44.1 kHz in 16-bit I²S mode. Also, the AIC26 codec functions as a slave in the interface. Although the AIC26 device has much more flexibility, this EVM has these values fixed.

3.5.3.2 ADC Section

By checking Power Up ADC, audio ADC power is enabled.

The audio ADC also has a high-pass filter which is a submultiple of the sample rate, to remove dc or low frequency components from the input signal.

The input signal to the audio ADC can come from: 1) the pin MICIN, a single-ended input; 2) the pin AUX, also a single-ended input; or 3) the pin MIC2IN and AUX, a differential input, selectable through the Input Select box. Figure 3–6 shows the single-ended input from MICIN (if selected).

A microphone bias voltage of either 2.5 V or 2.0 V can also be generated by the AIC26 (refer to Figure 3–6). Note that to use the microphone bias voltage, jumper JMP2 should be set to position 2 to 3 (refer to Table 3–1 of this document for jumper settings).

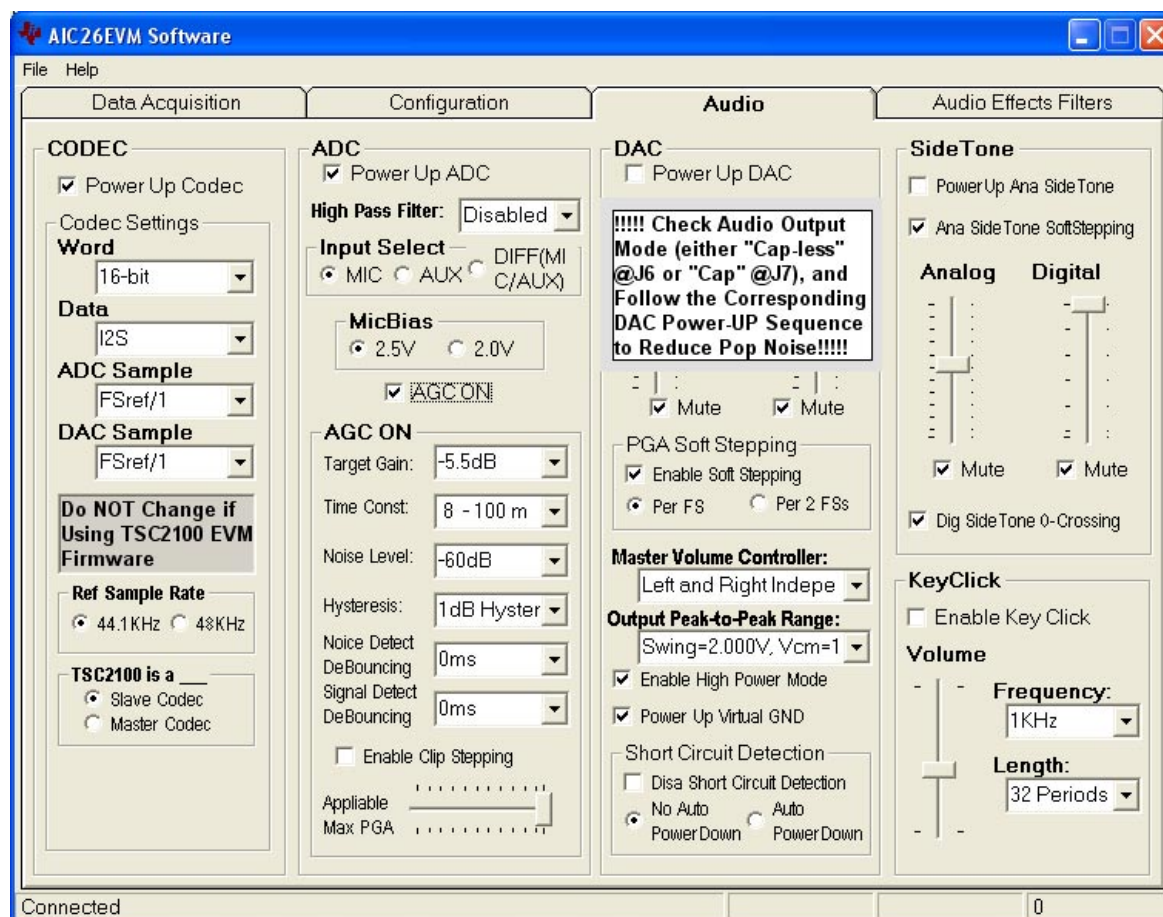
If the differential microphone inputs to the EVM (through the microphone jack J5) the JMP1 should be installed, and the input select should be set to DIFF (MIC/AUX) in this section.

In the ADC input path, there is a programmable EVM amplifier (ADC PGA), allowing analog input gain control from 0 dB to 59 dB. When not using automatic gain control (AGC OFF), moving the volume slide adjusts the PGA and checking the Mute box mutes the ADC signal.

When the gain changes from the current value to the programmed value, it changes in steps of 0.5 dB. Also, the change rate can be controlled if the PGA Soft Stepping box is checked, where the PGA changes 0.5 dB at either 1 step per sample or 1 step per 2 samples.

Automatic gain control (AGC) is another more sophisticated way to control the ADC gain. When the box by AGC ON is checked, AGC is enabled, as shown in Figure 3–7. Refer to the AIC26 data sheet for setting and using the AGC.

Figure 3–7. Audio Screen With AGC On



3.5.3.3 DAC Section

Like the ADC section, the AIC26 audio DAC can be powered on or off. By default, the DAC is powered off. Before a DAC power on, make sure to check the DAC output mode on the EVM board. If the audio output is connected to J6 or J13, the *virtual GND* should be powered up before the DAC powers up. Otherwise, if the audio output is connected to J7 (AC coupled plug), the *virtual GND* should be powered down before power up.

The stereo audio volumes can be controlled by the left (L) and right (R) volume control slides, in three different ways, selectable through setting the master volume controller: 1) independent, 2) right channel controlled, or 3) left channel controlled.

Like the audio ADC's gain controls the DAC's PGA gain can be changed in *soft stepping* either 0.5-dB per one sample, or 0.5-dB per 2 samples.

The audio DACs output swing range can be set from the list in the Output Peak-to-Peak Range pulldown. Refer to the AIC26 data sheet to find out the range. Note that the output peak-to-peak range is related to the analog driver power supply voltage.

By checking the Headphone Amp Enable box, the amp is enabled, which can directly be connected to a 16- Ω load. Otherwise, the headphone driver is bypassed and the device can have a load of 10 k Ω .

By checking the Power Up Virtual GND box, the virtual ground for the headphone output is powered up. The virtual ground should be powered up/down according to the DAC output mode. If the DAC output is in cap-decoupling mode, the virtual group can be powered down, otherwise the DAC output is in cap-less mode and the virtual ground should be powered up.

3.5.3.4 Sidetone Section

The AIC26 has an analog sidetone and a digital sidetone circuit. The audio output of the AIC26 includes a mix of the DAC and the sidetone channels, in proportion to their respective volume settings.

The analog sidetone is enabled when the PowerUp AnaSideTone box is checked, and available only if the single-ended MICIN or AUX Input Select is selected as input to the ADC. Its volume can be adjusted by the analog volume control slider, ranging from 12 dB to -34.5 dB in 0.5-dB steps. The analog sidetone is muted when the Mute box under the slider is checked. Additionally, similar to the audio ADC and DAC, the analog sidetone volume change can be in soft stepping mode if the corresponding box is checked.

The AIC26's digital sidetone has three settings. The volume is controlled by the digital slider, which changes from 0 dB to -48 dB in steps of 1.5 dB. The digital sidetone can be muted by checking the mute box under the volume control slider. The gain change is implemented with zero crossover, when enabled by checking the box below the sliders, and a possible pop sound may be avoided or reduced.

3.5.3.5 Keyclick Section

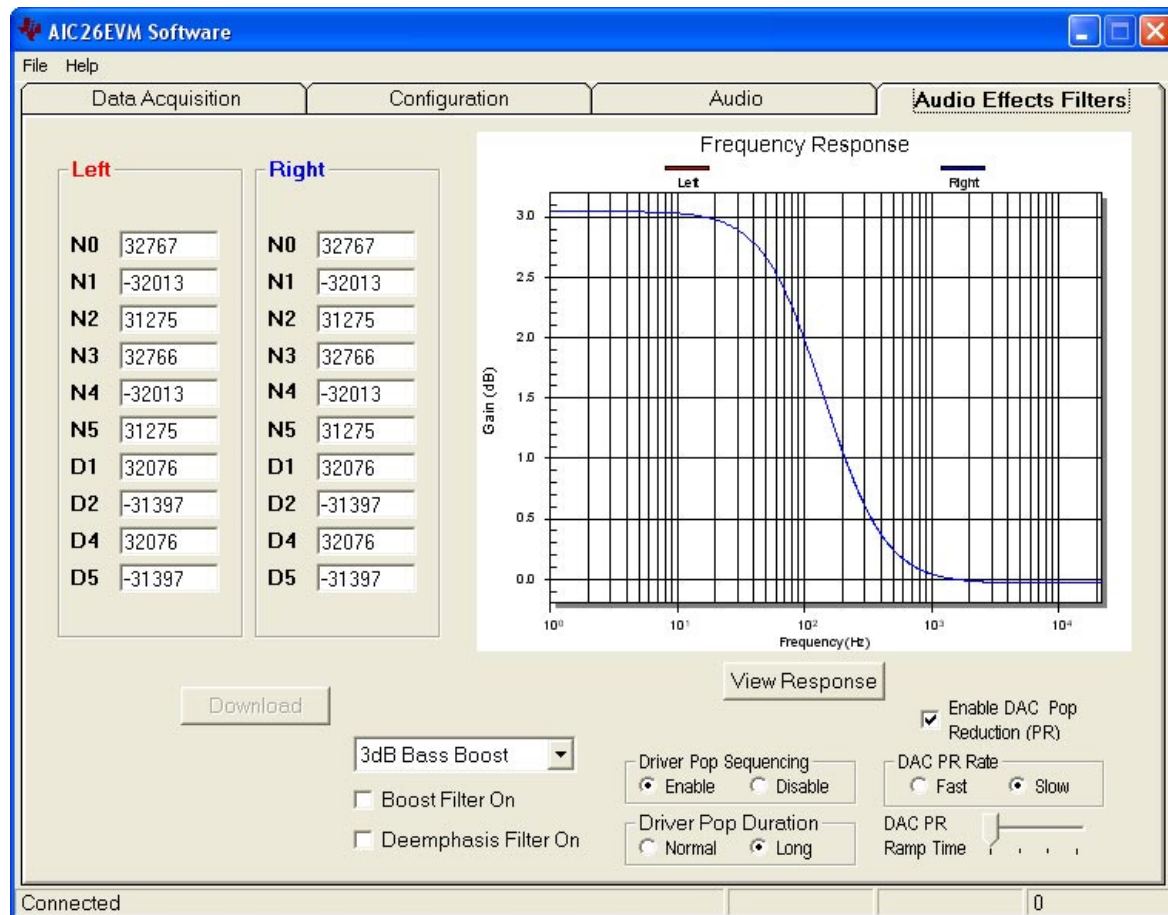
When the Enable Key Click box is checked, a clicking sound is heard whenever an audio related setting is selected or checked in the audio screen or in the PLL section of the configuration screen, or the settings on the Audio Effects Filters screen (see Figure 3-8).

The volume, frequency, and duration (length) of this keyclick can be adjusted using the corresponding slider and selectors shown in Figure 3-7.

3.5.4 Audio Effects Filters Screen

The Audio Effects Filters screen displays all of the coefficients for the audio effects filters of the AIC26, including the bass-boost and other filters, the de-emphasis filters and the power-up *pop* noise reduction functions. This screen is shown in Figure 3-8.

Figure 3–8. Audio Effects Filter Screen



Different filter coefficients can be loaded for left and right channels, though usually these are set the same. Six *preconfigured* filters are selectable using the drop-down list box of this screen. Selecting one of these updates the coefficients and causes the graph of the filter response to update. However, nothing is loaded into the AIC26 until the *Download* button is pressed.

If changes are made to coefficient values directly, the response can be viewed on the graph by pressing the *View Response* button. It is recommended that you view the response before downloading values to the AIC26, as some values can cause clipping or oscillation of the filter. The filter equation is described in the AIC26 data sheet.

Checking the Boost Filter On box enables the filter.

There is another digital filter, the de-emphasis filter, provided by the AIC26 for the audio DAC. Checking the Deemphasis Filter On box enables the filter.

Moreover, to reduce the AIC26's power-up pop noise, two pop-reduction functions were added to the AIC26 and are selectable on this screen. They are the audio output driver pop-reduction and the audio DAC pop-reduction. Refer to the data sheet for the details of the pop-reduction features.

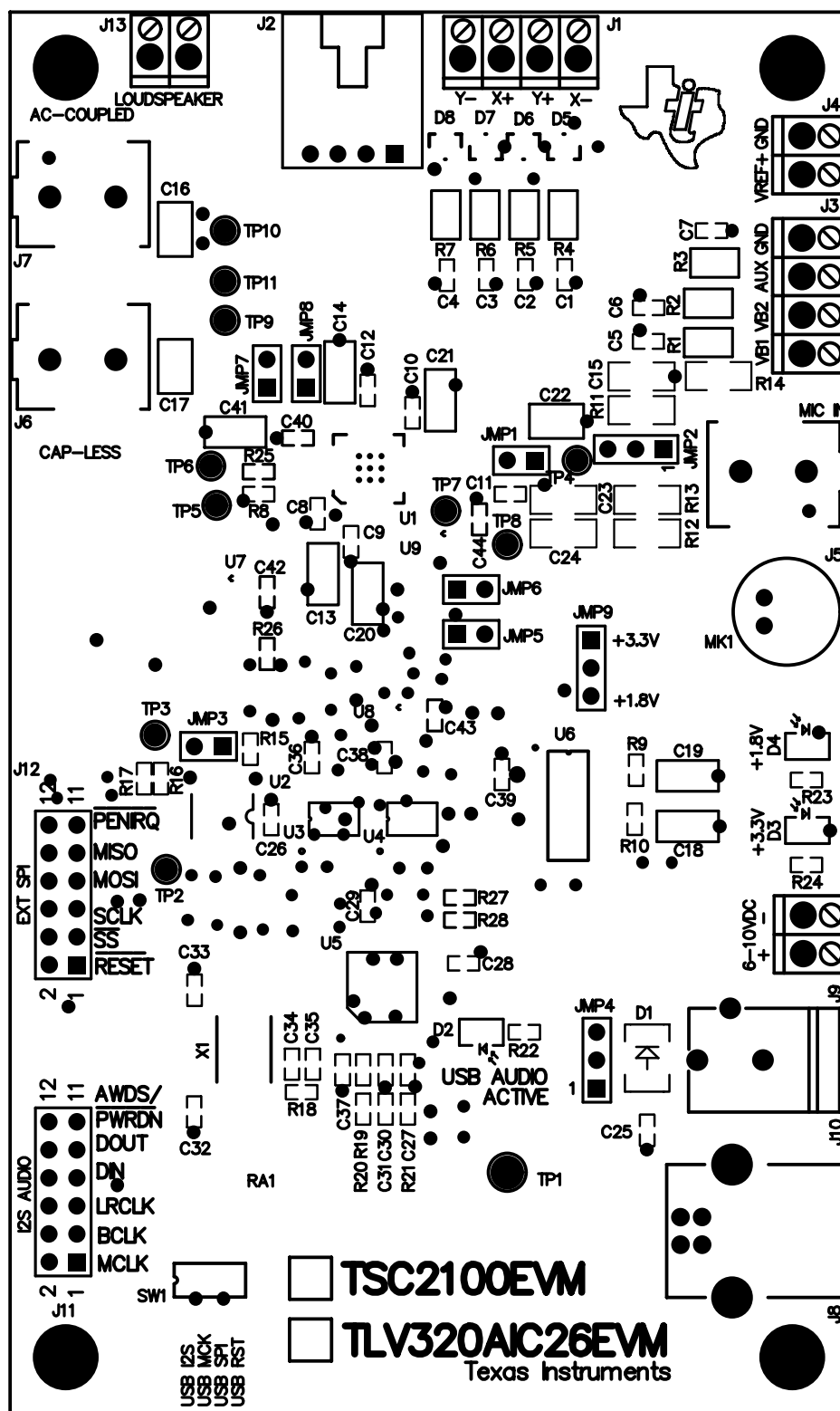
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Physical Description

This chapter contains the component locations, bill of materials, and the schematics.

Topic	Page
4.1 Component Locations	4-2
4.2 Bill of Materials	4-3
4.3 Schematics	4-6

4.1 Component Locations



4.2 Bill of Materials

Item No.	Qty	Value	Ref Des	Description	Vendor	Part number
1	1	0R0	R3	1/10W 5% Chip resistor	Panasonic	ERJ-6GEY0R00V
Not Installed	4	0R0	R4, R5, R6, R7	1/10W 5% Chip resistor	Panasonic	ERJ-6GEY0R00V
2	1	0R0	R12	1/4W 5% Chip resistor	Panasonic	ERJ-8GEY0R00V
3	1	10R	R23	1/16W 5% Chip resistor	Panasonic	ERJ-3GEYJ100V
4	2	27R4	R20, R21	1/16W 1% Chip resistor	Panasonic	ERJ-3EKF27R4V
5	1	220R	R24	1/16W 5% Chip resistor	Panasonic	ERJ-3GEYJ221V
6	2	220R	R1, R2	1/8W 5% Chip resistor	Panasonic	ERJ-6GEYJ221V
7	1	649R	R22	1/16W 1% Chip resistor	Panasonic	ERJ-3EKF6490V
8	1	680R	R14	1/4W 5% Chip resistor	Panasonic	ERJ-8GEYJ681V
9	1	1.5 K	R19	1/16W 5% Chip resistor	Panasonic	ERJ-3GEYJ152V
10	1	2.2 K	R13	1/4W 5% Chip resistor	Panasonic	ERJ-8GEYJ222V
11	3	2.7 K	R26, R27, R28	1/10W 5% Chip resistor	Panasonic	ERJ-3GEYJ272V
12	4	3.09 K	R15, R16, R17, R18	1/16W 1% Chip resistor	Panasonic	ERJ-3EKF3091V
13	3	100 K	R8, R9, R10, R25	1/16W 5% Chip resistor	Panasonic	ERJ-3GEYJ104V
Not Installed	1		R11	1/10W 5% Chip resistor	Panasonic	
14	1	10 K	RA1	1/8W Quad Isolated resistor array	CTS Corporation	744C083103JTR
15	2	33 pF	C32, C33	50 V Ceramic chip capacitor, $\pm 5\%$, NPO	Panasonic	ECJ-1VC1H330J
16	2	47 pF	C30, C31	50 V Ceramic chip capacitor, $\pm 5\%$, NPO	Panasonic	ECJ-1VC1H470J
17	1	100 pF	C34	50 V Ceramic chip capacitor, $\pm 5\%$, NPO	Panasonic	ECJ-1VC1H101J
18	1	1000 pF	C35	50 V Ceramic chip capacitor, $\pm 5\%$, NPO	Panasonic	ECJ-1VC1H102J
19	7	0.1 μ F	C8, C9, C10, C11, C12, C25, C40	16 V Ceramic chip capacitor, $\pm 10\%$, X7R	Panasonic	ECJ-1VB1C104K
20	1	0.1 μ F	C24	16 V Ceramic chip capacitor, $\pm 10\%$, X7R	Panasonic	ECJ-3VB1C104K
Not Installed	3	0.1 μ F	C5, C6, C7	16 V Ceramic chip capacitor, $\pm 10\%$, X7R	Panasonic	ECJ-1VB1C104K
21	1	0.33 μ F	C39	6.3 V Ceramic chip capacitor, $\pm 10\%$, X5R	Panasonic	ECJ-1VB0J334K
22	10	1 μ F	C26, C27, C28, C29, C36, C37, C38, C42, C43, C44	6.3 V Ceramic chip capacitor, $\pm 10\%$, X5R	Panasonic	ECJ-1VB0J105K

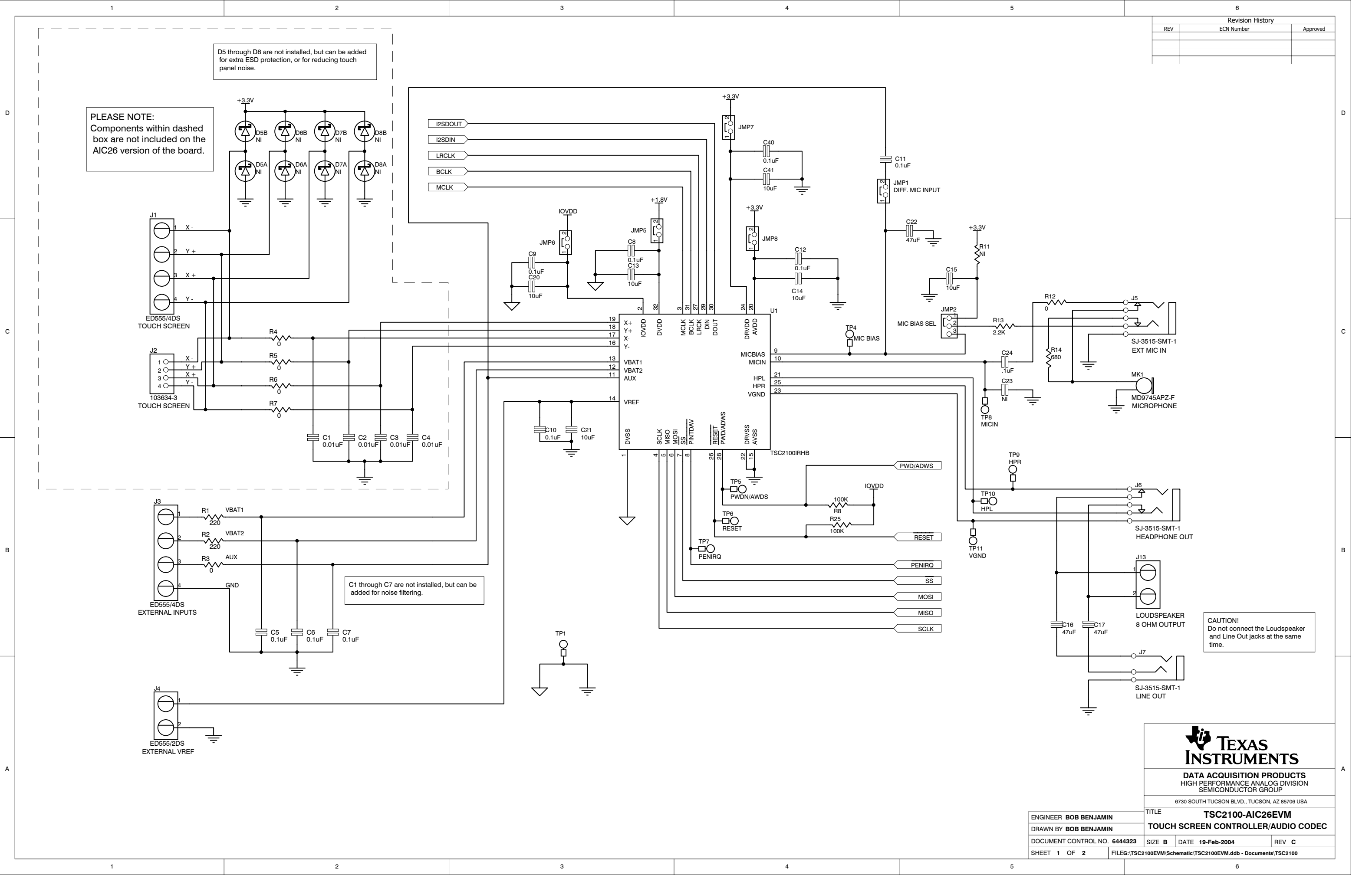
Bill of Materials

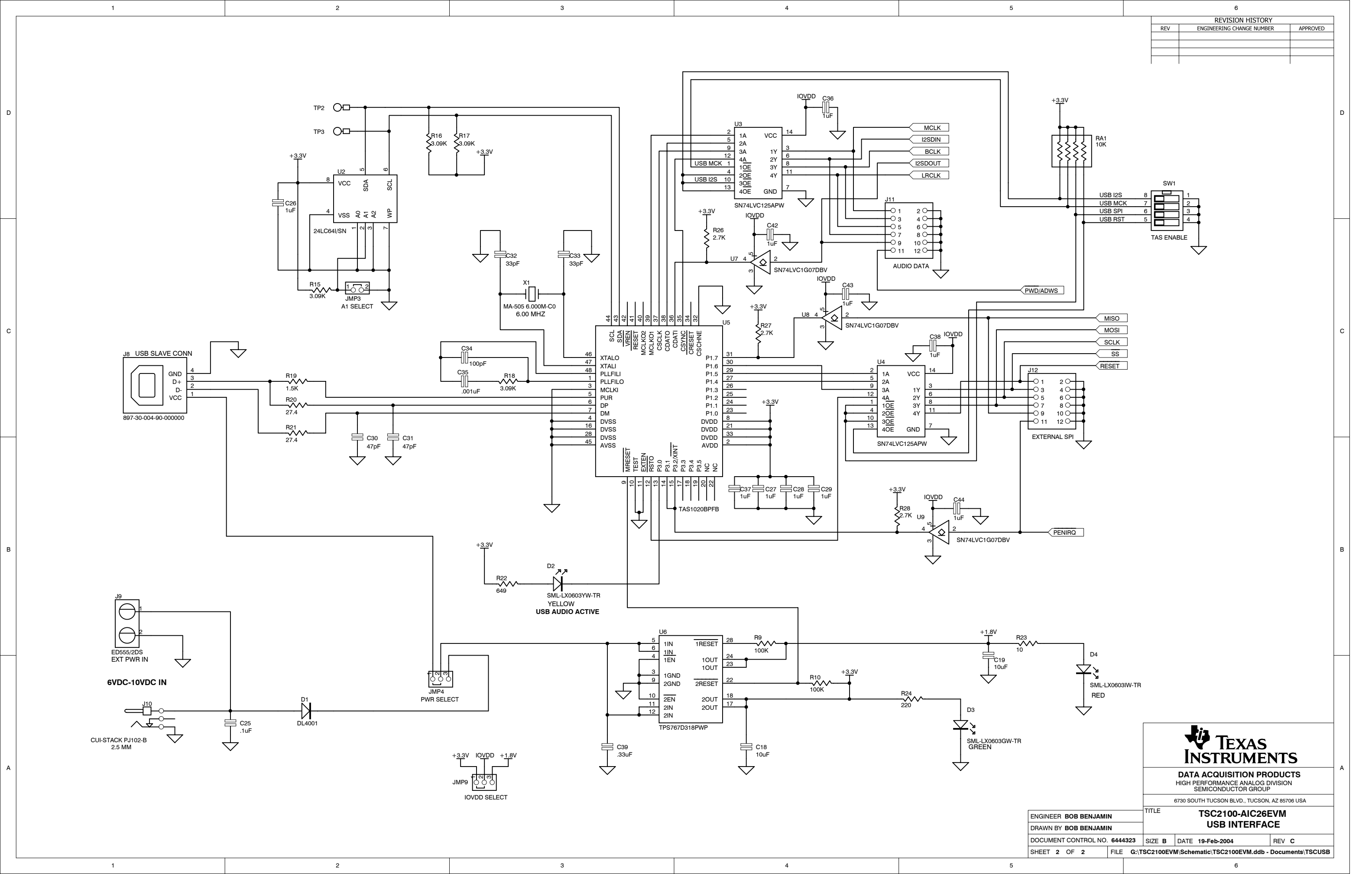
Item No.	Qty	Value	Ref Des	Description	Vendor	Part number
23	8	10 μ F	C13, C14, C15, C18, C19, C20, C21, C41	6.3 V Ceramic chip capacitor, $\pm 10\%$, X5R	Panasonic	ECJ-3YB0J106K
24	3	47 μ F	C16, C17, C22	6.3 V Ceramic chip capacitor, $\pm 20\%$, X5R	Panasonic	ECJ-4YB0J476M
Not Installed	1		C23	16 V Ceramic chip capacitor, $\pm 10\%$, X7R	Panasonic	
Not Installed	4	0.01 μ F	C1, C2, C3, C4	16 V Ceramic chip capacitor, $\pm 10\%$, X7R	Panasonic	ECJ-1VB1C103K
25	1		D1	50 V, 1A, Diode MELF SMD	Micro Commercial Components	DL4001
26	1		D2	Yellow light emitting diode	Lumex	SML-LX0603YW-TR
27	1		D3	Green light emitting diode	Lumex	SML-LX0603GW-TR
28	1		D4	Red light emitting diode	Lumex	SML-LX0603IW-TR
Not Installed	4		D5, D6, D7, D8	Schottky barrier diode, series configuration	Zetex	BAT54STA
29	1		MK1	Omnidirectional Microphone Cartridge	Knowles Acoustics	MD9745APZ-F
30	1		X1	6 MHz Crystal SMD	Epson	MA-505 6.000M-C0
31	1		U1	Stereo audio CODEC	Texas Instruments	TLV320AIC26IRHB
32	1		U5	USB streaming controller	Texas Instruments	TAS1020BPFB
33	1		U6	3.3 V/1.8 V dual output LDO regulator	Texas Instruments	TPS767D318PWP
34	2		U3, U4	Quad 3-state buffers	Texas Instruments	SN74LVC125APW
35	3		U7, U8, U9	Single IC buffer driver with open drain O/P	Texas Instruments	SN74LVC1G07DBVR
36	1		U2	64K 2-Wire Serial EEPROM I ² C	Microchip	24LC64I/SN
37	1		N/A	TSC2100EVM/AIC26EVM PWB	Texas Instruments	6444324
38	10		TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	Miniature test point terminal	Keystone Electronics	5000
39	1		TP1	Multipurpose test point terminal	Keystone Electronics	5011
Not Installed	1		J2	4 Pin right angle latching header	Tyco Electronics/AMP	103634-3
41	1		J8	USB Type B slave connector thru-hole	Mill-Max	897-30-004-90-000000
42	3		J4, J9, J13	2 Position terminal block	On Shore Technology	ED555/2DS

Item No.	Qty	Value	Ref Des	Description	Vendor	Part number
43	1		J3	4 Position terminal block	On Shore Technology	ED555/4DS
Not Installed	1		J1	4 Position terminal block	On Shore Technology	ED555/4DS
44	1		J10	2,5 mm Power connector	CUI Stack	PJ-102B
45	3		J5, J6, J7	3,5 mm Stereo audio jack SMT	CUI Stack	SJ-3515-SMT-1
46	2		J11, J12	12 Pin double row header (2x6) 0.1"	Samtec	TSW-106-07-L-D
47	2		JMP1, JMP3	2 Position Jumper , 0.1" spacing	Samtec	TSW-102-07-L-S
48	3		JMP2, JMP4, JMP9	3 Position Jumper , 0.1" spacing	Samtec	TSW-103-07-L-S
49	4		JMP5, JMP6, JMP7, JMP8	Bus wire		
50	1		SW1	SMT, Half-pitch 4 position switch	C & K Division, ITT	TDA04H0SK1
51	5		N/A	Jumper plug	Samtec	SNT-100-BK-T
52	4		N/A	0.25" x 0.625" Hex 4-40 threaded standoff	Keystone Electronics	1808
53	4		N/A	Pan head machine screw 4-40 x 1/2" Phillips	Building Fasteners	PMS 440 0050 PH

4.3 Schematics

Schematic diagrams of the AIC26EVM showing the AIC26 connections and the USB and connectors are shown on the following pages.





REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

**TEXAS
INSTRUMENTS**

DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

ENGINEER BOB BENJAMIN		TITLE TSC2100-AIC26EVM USB INTERFACE	
DRAWN BY BOB BENJAMIN			
DOCUMENT CONTROL NO. 6444323	SIZE B	DATE 19-Feb-2004	REV C
SHEET 2 OF 2	FILE G:\TSC2100EVM\Schematic\TSC2100EVM.ddb - Documents\TSCUSB		