Dual-Channel, 12-Bit, 80 MSPS ADC with Analog Input Signal Conditioning

AD13280

FEATURES

Dual 80 MSPS, minimum sample rate
Channel-to-channel matching, ±1% gain error
90 dB channel-to-channel isolation
DC-coupled signal conditioning
80 dB spurious-free dynamic range
Selectable bipolar inputs (±1 V and ±0.5 V ranges)
Integral single-pole, low-pass Nyquist filter
Twos complement output format
3.3 V compatible outputs
1.85 W per channel

APPLICATIONS

Radar processing (optimized for I/Q baseband operation)
Phased array receivers
Multichannel, multimode receivers
GPS antijamming receivers
Communications receivers

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 80 MSPS.
2. Input signal conditioning; gain and impedance match.
3. Single-ended, differential, or off-module filter option.
4. Fully tested/characterized full channel performance.

FUNCTIONAL BLOCK DIAGRAM

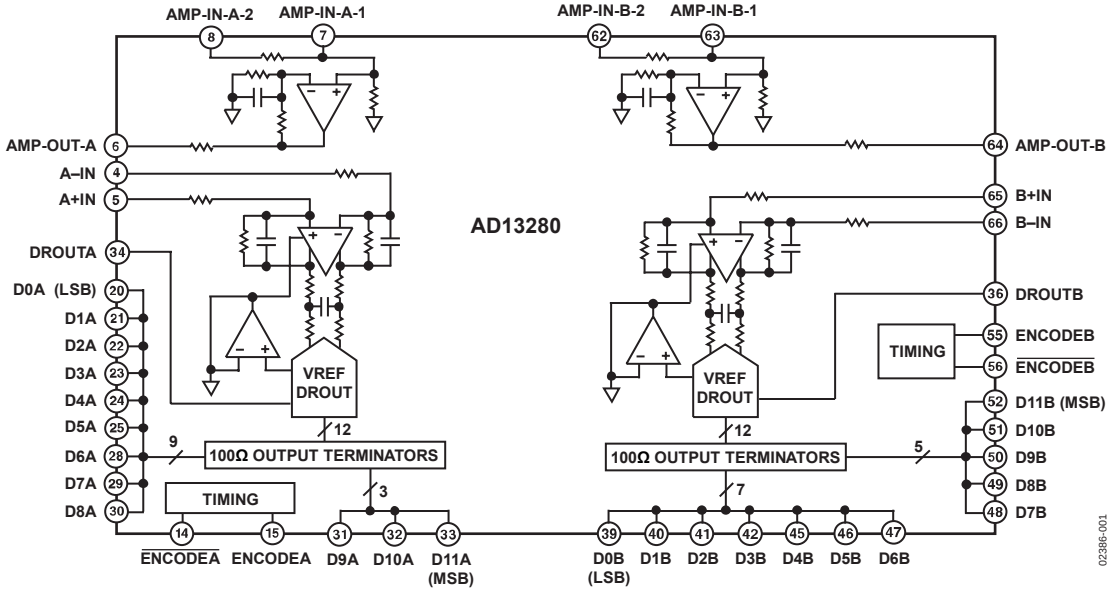


Figure 1.

Rev. C
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Product Highlights ... 1
Functional Block Diagram ... 1
Revision History ... 2
General Description ... 3
Specifications ... 4
  Timing Diagram ... 6
Absolute Maximum Ratings ... 7
  Explanation of Test Levels ... 7
  ESD Caution ... 7
Pin Configuration and Function Descriptions ... 8
Typical Performance Characteristics ... 10
Terminology ... 12
Input and Output Stages ... 13
Theory of Operation ... 14
  Using the Single-Ended Input ... 14
  Using the Differential Input ... 14
Applications Information ... 15
  Encoding the AD13280 ... 15
  Jitter Consideration ... 15
  Power Supplies ... 16
  Output Loading ... 16
Evaluation Board ... 17
  Layout Information ... 17
  Bill of Materials List for Evaluation Board ... 24
Outline Dimensions ... 25
  Ordering Guide ... 26

REVISION HISTORY

4/08—Rev. B to Rev. C

Updated Outline Dimensions ... 25
Changes to the Ordering Guide ... 26

11/05—Rev. A to Rev. B

Updated Format ... Universal
Changes to Features and Product Highlights ... 1
Changes to General Description ... 3
Changes to Table 1 ... 4
Changes to Figure 3 ... 8
Changes to Theory of Operation ... 14
Changes to Equation 1 ... 15
Changes to Table 5 ... 18
Changes to Figure 21 ... 19
Changes to Figure 22 ... 20
Changes to Figure 23 ... 21
Changes to Figure 28 and Figure 29 ... 24
Updated Outline Dimensions ... 25
Changes to the Ordering Guide ... 26

8/02—Rev. 0 to Rev. A

Edits to Specifications ... 2
Packages Updated ... 19

GENERAL DESCRIPTION

The AD13280 is a complete, dual-channel, signal processing solution that includes on-board amplifiers, references, ADCs, and output termination components to provide optimized system performance. The AD13280 has on-chip track-and-hold circuitry and uses an innovative multipass architecture to achieve 12-bit, 80 MSPS performance. The AD13280 uses innovative high density circuit design and laser-trimmed thin-film resistor networks to achieve exceptional channel matching, impedance control, and performance while maintaining excellent isolation and providing for significant board area savings.

Multiple options are provided for driving the analog input, including single-ended, differential, and optional series filtering. The AD13280 also offers users a choice of analog input signal ranges to further minimize additional external signal conditioning, while remaining general purpose.

The AD13280 operates with ±5.0 V for the analog signal conditioning with a separate 5.0 V supply for the analog-to-digital conversion and 3.3 V digital supply for the output stage. Each channel is completely independent, allowing operation with independent encode and analog inputs and maintaining minimal crosstalk and interference.

The AD13280 is available in a 68-lead, ceramic gull wing package. The components are manufactured using the Analog Devices, Inc., high speed complementary bipolar process (XFCB).

SPECIFICATIONS

AV_{CC} = +5 V, AV_{EE} = −5 V, DV_{CC} = +3.3 V; applies to each ADC with front-end amplifier, unless otherwise noted.

Table 1.

			AD13280AZ			
Parameter	**Temperature**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				12		Bits
DC ACCURACY[1]						
No Missing Codes	Full	IV		Guaranteed		
Offset Error	25°C	I	−2.2	±1.0	+2.2	% FS
	Full	VI	−2.2	±1.0	+2.2	% FS
Offset Error Channel Match	Full	VI	−1.0	±0.1	+1.0	%
Gain Error[2]	25°C	I	−3	−1.0	+1	% FS
	Full	VI	−5.0	±2.0	+5.0	% FS
Gain Error Channel Match	25°C	I	−1.5	±0.5	+1.5	%
	Max	VI	−3.0	±1.0	+3.0	%
	Min	VI	−5	±1.0	+5	%
SINGLE-ENDED ANALOG INPUT						
Input Voltage Range						
AMP-IN-X-1	Full	V		±0.5		V
AMP-IN-X-2	Full	V		±1.0		V
Input Resistance						
AMP-IN-X-1	Full	IV	99	100	101	Ω
AMP-IN-X-2	Full	IV	198	200	202	Ω
Capacitance	25°C	V		4.0	7.0	pF
Analog Input Bandwidth[3]	Full	V		143		MHz
DIFFERENTIAL ANALOG INPUT						
Analog Signal Input Range						
A+IN to A–IN and B+IN to B–IN[4]	Full	V		±1		V
Input Impedance	25°C	V		618		Ω
Analog Input Bandwidth	Full	V		50		MHz
ENCODE INPUT (ENCODE, $\overline{\text{ENCODE}}$)[1]						
Differential Input Voltage	Full	IV	0.4			V p-p
Differential Input Resistance	25°C	V		10		kΩ
Differential Input Capacitance	25°C	V		2.5		pF
SWITCHING PERFORMANCE						
Maximum Conversion Rate[5]	Full	VI	80			MSPS
Minimum Conversion Rate[5]	Full	IV			30	MSPS
Aperture Delay (t_A)	25°C	V		0.9		ns
Aperture Delay Matching	25°C	IV		250	500	ps
Aperture Uncertainty (Jitter)	25°C	V		0.3		ps rms
ENCODE Pulse Width High at Max Conversion Rate	25°C	IV	4.75	6.25	8	ns
ENCODE Pulse Width Low at Max Conversion Rate	25°C	IV	4.75	6.25	8	ns
Output Delay (t_{OD})	Full	V		5		ns
Encode, Rising to Data Ready, Rising Delay	Full	V		8.5		ns
SNR[1, 6]						
Analog Input @ 10 MHz	25°C	I	66.5	70		dBFS
	Min	II	64.5			dBFS
	Max	II	66.3			dBFS
Analog Input @ 21 MHz	25°C	I	66.5	70		dBFS
	Min	II	64			dBFS
	Max	II	66.3			dBFS

Parameter	Temperature	Test Level	AD13280AZ Min	Typ	Max	Unit
Analog Input @ 37 MHz	25°C	I	63	65		dBFS
	Min	II	61.5			dBFS
	Max	II	63			dBFS
SINAD[1, 7]						
Analog Input @ 10 MHz	25°C	I	66	69		dBFS
	Min	II	63.5			dBFS
	Max	II	66			dBFS
Analog Input @ 21 MHz	25°C	I	64	68.5		dBFS
	Min	II	63			dBFS
	Max	II	64			dBFS
Analog Input @ 37 MHz	25°C	I	54	59		dBFS
	Min	II	53			dBFS
	Max	II	54			dBFS
SPURIOUS-FREE DYNAMIC RANGE[1, 8]						
Analog Input @ 10 MHz	25°C	I	75	80		dBFS
	Min	II	70			
	Max	II	75			
Analog Input @ 21 MHz	25°C	I	68	75		dBFS
	Min	II	67			
	Max	II	67			
Analog Input @ 37 MHz	25°C	I	56	62		dBFS
	Min	II	55			
	Max	II	55			
SINGLE-ENDED ANALOG INPUT						
Pass-Band Ripple to 10 MHz	25°C	V		0.07		dB
Pass-Band Ripple to 25 MHz	25°C	V		0.12		dB
DIFFERENTIAL ANALOG INPUT						
Pass-Band Ripple to 10 MHz	25°C	V		0.3		dB
Pass-Band Ripple to 25 MHz	25°C	V		0.82		dB
TWO-TONE IMD REJECTION[9]						
f_{IN} = 9.1 MHz and 10.1 MHz (f_1 and f_2 are −7 dBFS)	25°C	I	75	80		dBc
	Min	II	71			
	Max	II	74			
f_{IN} = 19.1 MHz and 20.7 MHz (f_1 and f_2 are −7 dBFS)	25°C	V		77		dBc
f_{IN} = 36 MHz and 37 MHz (f_1 and f_2 are −7 dBFS)	25°C	V		60		dBc
CHANNEL-TO-CHANNEL ISOLATION[10]	25°C	IV	90			dB
TRANSIENT RESPONSE	25°C	V		25		ns
DIGITAL OUTPUTS[11]						
Logic Compatibility				CMOS		
DV_{CC} = 3.3 V						
Logic 1 Voltage	Full	I	2.5	DV_{CC} − 0.2		V
Logic 0 Voltage	Full	I		0.2	0.5	V
DV_{CC} = 5 V						
Logic 1 Voltage	Full	V		DV_{CC} − 0.3		V
Logic 0 Voltage	Full	V		0.35		V
Output Coding				Twos complement		
POWER SUPPLY						
AV_{CC} Supply Voltage[12]	Full	IV	4.85	5.0	5.25	V
I (AV_{CC}) Current	Full	I		313	364	mA
AV_{EE} Supply Voltage[12]	Full	IV	−5.25	−5.0	−4.75	V
I (AV_{EE}) Current	Full	I		38	49	mA
DV_{CC} Supply Voltage[12]	Full	IV	3.135	3.3	3.465	V

Parameter	Temperature	Test Level	AD13280AZ Min	Typ	Max	Unit
I (DV_{CC}) Current	Full	I		34	46	mA
I_{CC} (Total) Supply Current per Channel	Full	I		375	459	mA
Power Dissipation (Total)	Full	I		3.7	4.3	W
Power Supply Rejection Ratio (PSRR)	Full	V		0.01		% FSR/% VS

[1] All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially. Single-ended input: AMP-IN-x-1 = 1 V p-p, AMP-IN-x-2 = GND.
[2] Gain tests are performed on the AMP-IN-x-1 input voltage range.
[3] Full power bandwidth is the frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.
[4] For differential input: +IN = 1 V p-p and –IN = 1 V p-p (signals are 180 Ω out of phase). For single-ended input: +IN = 2 V p-p and –IN = GND.
[5] Minimum and maximum conversion rates allow for variation in encode duty cycle of 50% ± 5%.
[6] Analog input signal power at –1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed). Encode = 80 MSPS. SNR is reported in dBFS, related back to converter full scale.
[7] Analog input signal power at –1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 80 MSPS. SINAD is reported in dBFS, related back to converter full scale.
[8] Analog input signal at –1 dBFS; SFDR is the ratio of converter full scale to worst spur.
[9] Both input tones at –7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third-order intermodulation product.
[10] Channel-to-channel isolation tested with A channel grounded and a full-scale signal applied to B channel.
[11] Digital output logic levels: DV_{CC} = 3.3 V, C_{LOAD} = 10 pF. Capacitive loads >10 pF degrades performance.
[12] Supply voltage recommended operating range. AV_{CC} may be varied from 4.85 V to 5.25 V. However, rated ac (harmonics) performance is valid only over the range AV_{CC} = 5.0 V to 5.25 V.

TIMING DIAGRAM

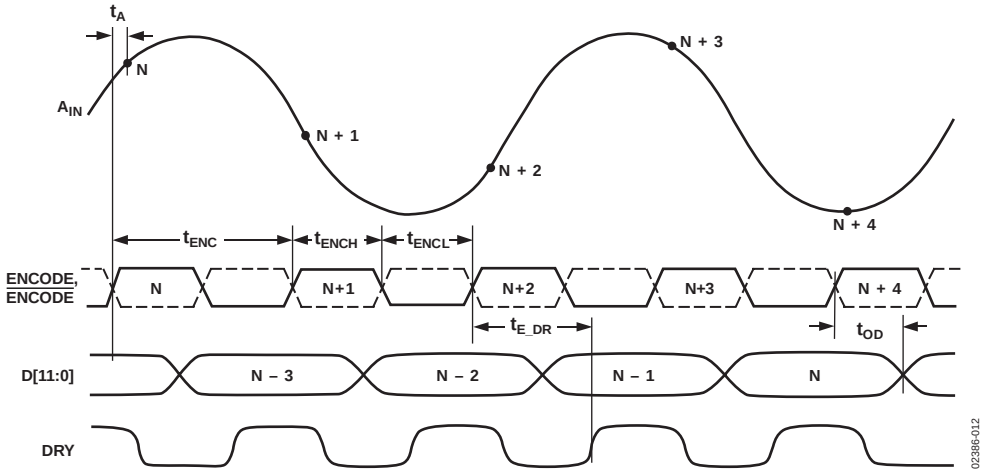


Figure 2.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
ELECTRICAL[1]	
AV_{CC} Voltage	0 V to 7 V
AV_{EE} Voltage	−7 V to 0 V
DV_{CC} Voltage	0 V to 7 V
Analog Input Voltage	V_{EE} to V_{CC}
Analog Input Current	−10 mA to +10 mA
Digital Input Voltage (ENCODE)	0 to V_{CC}
ENCODE, $\overline{\text{ENCODE}}$ Differential Voltage	4 V max
Digital Output Current	−10 mA to +10 mA
ENVIRONMENTAL[1]	
Operating Temperature Range (Case)	−40°C to +85°C
Maximum Junction Temperature	175°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

[1] Typical thermal impedance for ES package: θ_{JC} 2.2°C/W; θ_{JA} 24.3°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C, and sample tested at specified temperatures. AC testing done on a sample basis.

III. Sample tested only.

IV. Parameter guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested with temperature at 25°C, and sample tested at temperature extremes.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

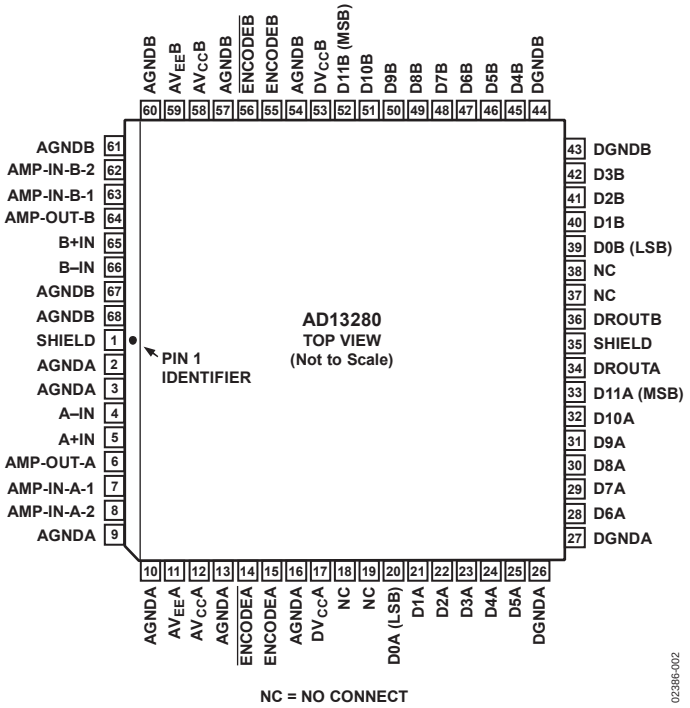


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 35	SHIELD	Internal Ground Shield Between Channels.
2, 3, 9, 10, 13, 16	AGNDA	A Channel Analog Ground. A and B grounds should be connected as close to the device as possible.
4	A−IN	Inverting Differential Input (Gain = +1).
5	A+IN	Noninverting Differential Input (Gain = +1).
6	AMP-OUT-A	Single-Ended Amplifier Output (Gain = +2).
7	AMP-IN-A-1	Analog Input for A Side ADC (Nominally ±0.5 V).
8	AMP-IN-A-2	Analog Input for A Side ADC (Nominally ±1.0 V).
11	AVEEA	A Channel Analog Negative Supply Voltage (Nominally −5.0 V or −5.2 V).
12	AVCCA	A Channel Analog Positive Supply Voltage (Nominally +5.0 V).
14	$\overline{\text{ENCODEA}}$	Complement of ENCODEA. Differential input.
15	ENCODEA	Encode Input. Conversion initiated on rising edge.
17	DVCCA	A Channel Digital Positive Supply Voltage (Nominally +5.0 V/+3.3 V).
18, 19, 37, 38	NC	No Connect.
20 to 25, 28 to 33	D0A to D11A	Digital Outputs for ADC A. D0 (LSB).
26, 27	DGNDA	A Channel Digital Ground.
34	DROUTA	Data Ready A Output.
36	DROUTB	Data Ready B Output.
39 to 42, 45 to 52	D0B to D11B	Digital Outputs for ADC B. D0 (LSB).
43, 44	DGNDB	B Channel Digital Ground.
53	DVCCB	B Channel Digital Positive Supply Voltage (Nominally +5.0 V/+3.3 V).

Pin No.	Mnemonic	Description
54, 57, 60, 61, 67, 68	AGNDB	B Channel Analog Ground. A and B grounds should be connected as close to the device as possible.
55	ENCODEB	Encode Input. Conversion initiated on rising edge.
56	$\overline{\text{ENCODEB}}$	Complement of ENCODEB. Differential input.
58	AVCCB	B Channel Analog Positive Supply Voltage (Nominally +5.0 V).
59	AVEEB	B Channel Analog Negative Supply Voltage (Nominally −5.0 V or −5.2 V).
62	AMP-IN-B-2	Analog Input for B Side ADC (Nominally ±1.0 V).
63	AMP-IN-B-1	Analog Input for B Side ADC (Nominally ±0.5 V).
64	AMP-OUT-B	Single-Ended Amplifier Output (Gain = +2).
65	B+IN	Noninverting Differential Input (Gain = +1).
66	B−IN	Inverting Differential Input (Gain = +1).

TYPICAL PERFORMANCE CHARACTERISTICS

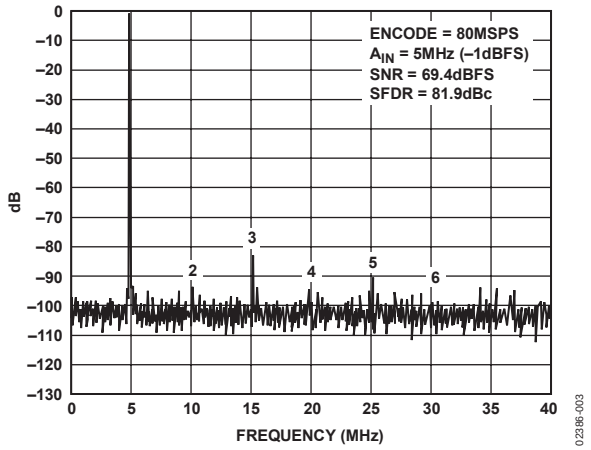


Figure 4. Single Tone @ 5 MHz

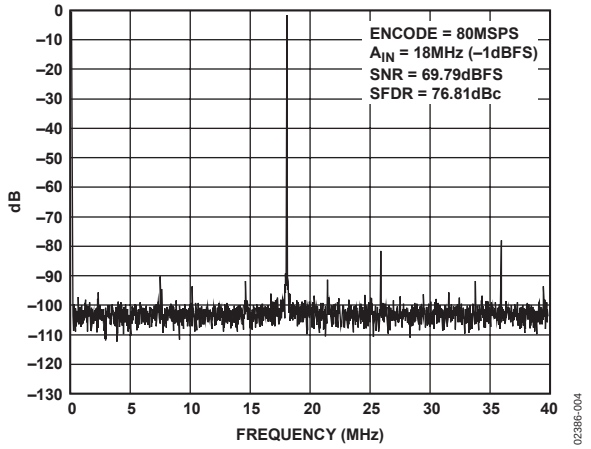


Figure 5. Single Tone @ 18 MHz

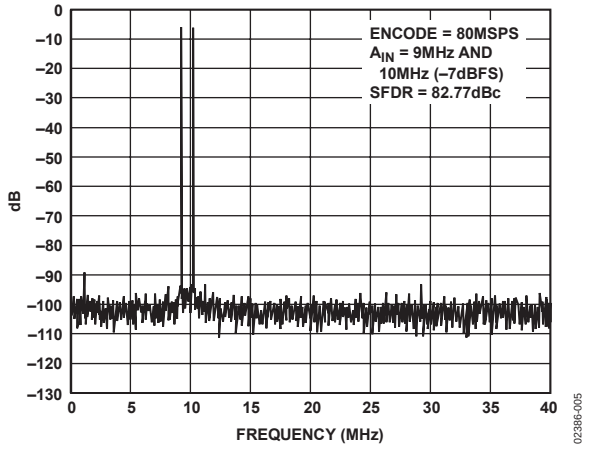


Figure 6. Two Tone @ 9 MHz and 10 MHz

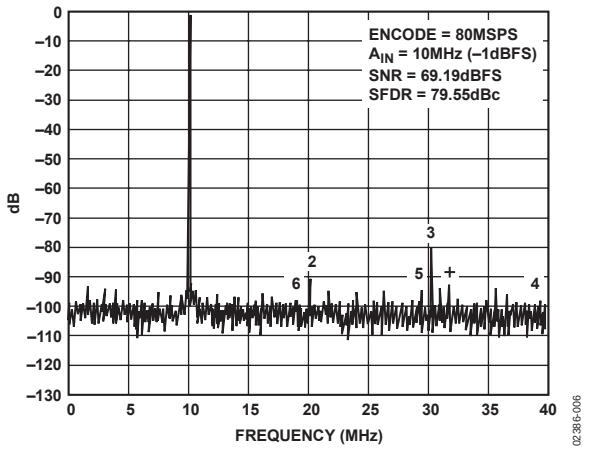


Figure 7. Single Tone @ 10 MHz

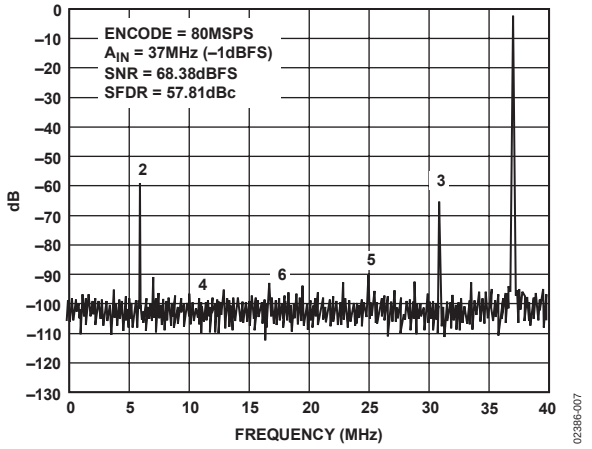


Figure 8. Single Tone @ 37 MHz

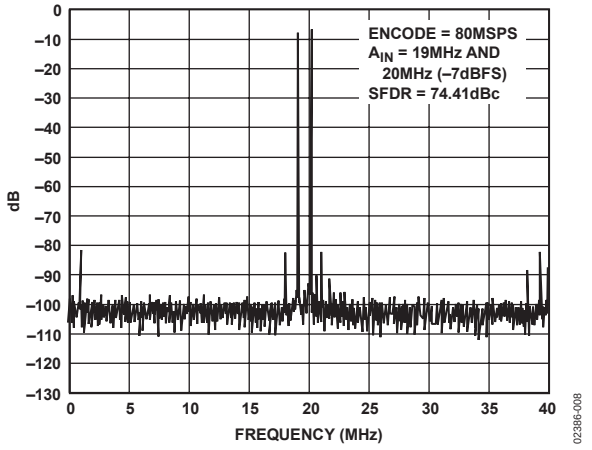


Figure 9. Two Tone @ 19 MHz and 20 MHz

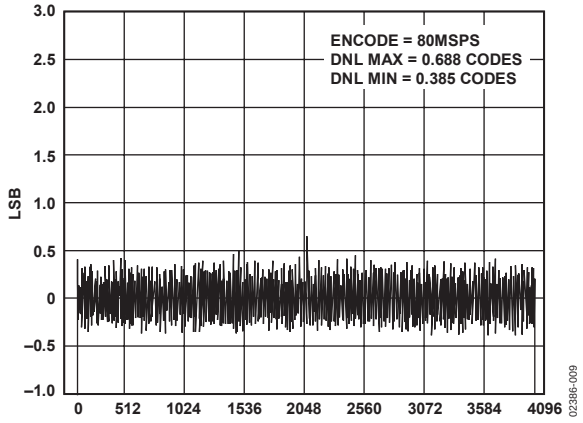


Figure 10. Differential Nonlinearity

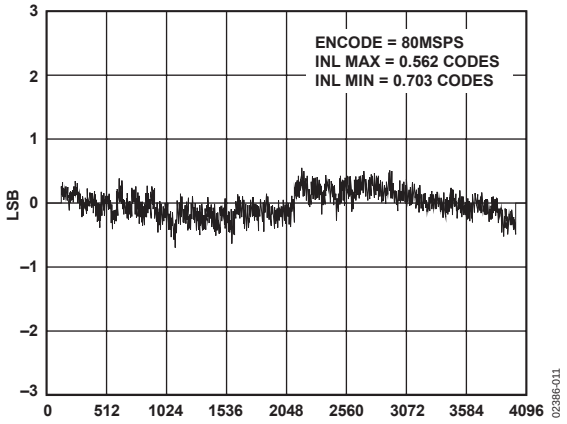


Figure 12. Integral Nonlinearity

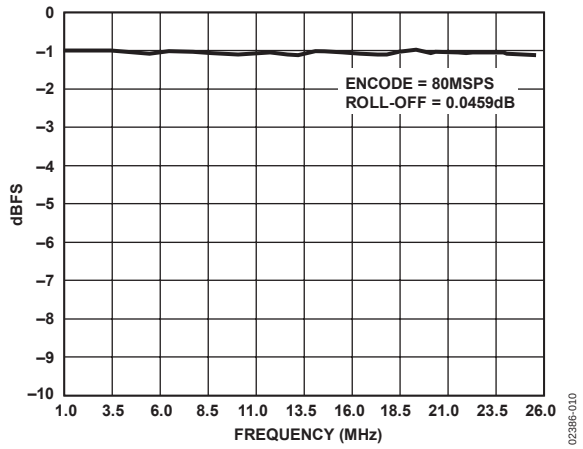


Figure 11. Pass-Band Ripple to 25 MHz

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of the ENCODEA signal and the $\overline{\text{ENCODEA}}$ signal and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically, and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the input phase 180 degrees and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

ENCODE Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the ENCODE pulse should be left in a Logic 1 state to achieve the rated performance. Pulse width low is the minimum time the ENCODE pulse should be left in a low state. At a given clock rate, these specifications define an acceptable encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of the ENCODEA signal and the $\overline{\text{ENCODEA}}$ signal and the time at which all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal of the specified percentage of full scale is reduced to midscale.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc. SINAD can be reported in dB (that is, degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Signal-to-Noise Ratio (SNR) (Without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc. SNR can be reported in dB (that is, degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Transient Response
The time required for the converter to achieve 0.02% accuracy when a one-half full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

INPUT AND OUTPUT STAGES

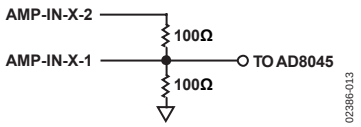


Figure 13. Single-Ended Input Stage

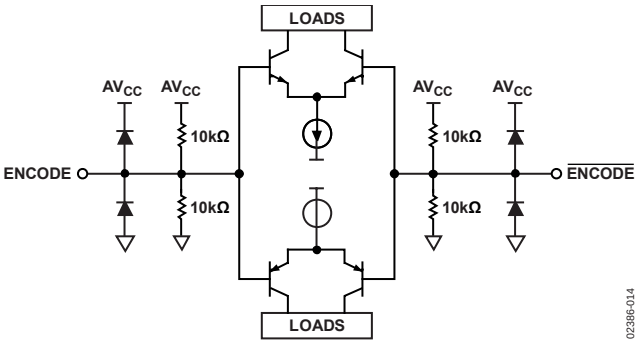


Figure 15. ENCODE Inputs

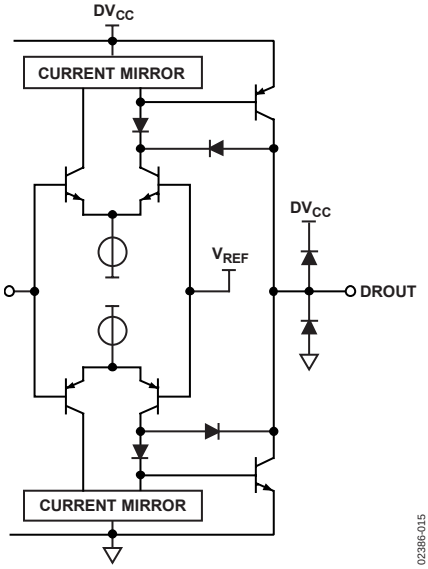


Figure 14. DR Digital Output Stage

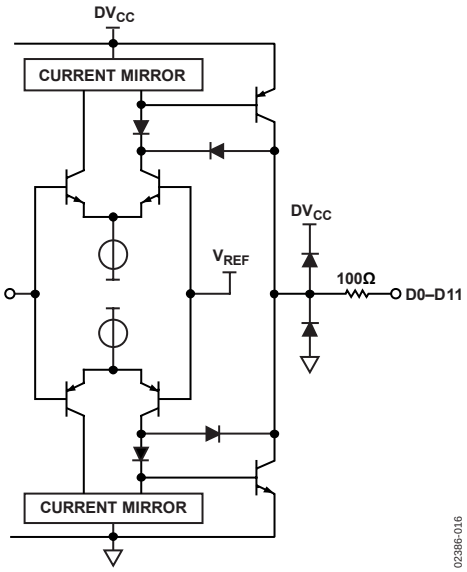


Figure 16. Digital Output Stage

THEORY OF OPERATION

The AD13280 is a high dynamic range 12-bit, 80 MHz pipeline delay (three pipelines) analog-to-digital converter (ADC). The custom analog input section provides input ranges of 1 V p-p and 2 V p-p and input impedance configurations of 50 Ω, 100 Ω, and 200 Ω.

The AD13280 employs four monolithic Analog Devices components per channel (AD8045, AD8138, AD8031, and a custom ADC IC), along with multiple passive resistor networks and decoupling capacitors to fully integrate a complete 12-bit analog-to-digital converter (ADC).

In the single-ended input configuration, the input signal is passed through a precision laser-trimmed resistor divider, allowing the user to externally select operation with a full-scale signal of ±0.5 V or ±1.0 V by choosing the proper input terminal for the application. The result of the resistor divider is to apply a full-scale input of approximately 0.4 V to the noninverting input of the internal AD8045 amplifier.

The AD13280 analog input includes an AD8045 amplifier featuring an innovative architecture that maximizes the dynamic range capability on the amplifier inputs and outputs. The AD8045 amplifier provides a high input impedance and gain for driving the AD8138 in a single-ended to differential amplifier configuration. The AD8138 has a −3 dB bandwidth at 300 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier. The AD8138 differential outputs help balance the differential inputs to the custom ADC, maximizing the performance of the device.

The AD8031 provides the buffer for the internal reference analog-to-digital converter. The internal reference voltage of the custom ADC is designed to track the offsets and drifts and is used to ensure matching over an extended temperature range of operation. The reference voltage is connected to the output common-mode input on the AD8138. This reference voltage sets the output common mode on the AD8138 at 2.4 V, which is the midsupply level for the ADC.

The custom ADC has complementary analog input pins, $\overline{\text{AIN}}$ and AIN. Each analog input is centered at 2.4 V and should swing ±0.55 V around this reference. Because AIN and $\overline{\text{AIN}}$ are 180 degrees out of phase, the differential analog input signal is 2.2 V peak-to-peak. Both analog inputs are buffered prior to the first track-and-hold.

The custom ADC digital outputs drive 100 Ω series resistors (see Figure 16). The result is a 12-bit, parallel digital CMOS-compatible word, coded as a twos complement.

USING THE SINGLE-ENDED INPUT

The AD13280 has been designed with user ease of operation in mind. Multiple input configurations have been included on-board to allow the user a choice of input signal levels and input impedance. The standard inputs are ±0.5 V and ±1.0 V. The user can select the input impedance of the AD13280 on any input by using the other inputs as alternate locations for the GND. The following is a summary of the impedance options available at each input location:

AMP-IN-x-1 = 100 Ω when AMP-IN-x-2 is open.

AMP-IN-x-1 = 50 Ω when AMP-IN-x-2 is shorted to GND.

AMP-IN-x-2 = 200 Ω when AMP-IN-x-1 is open.

Each channel has two analog inputs: AMP-IN-A-1 and AMP-IN-A-2 or AMP-IN-B-1 and AMP-IN-B-2. Use AMP-IN-A-1 or AMP-IN-B-1 when an input of ±0.5 V full scale is desired. Use AMP-IN-A-2 or AMP-IN-B-2 when ±1 V full scale is desired. Each channel has an AMP-OUT that must be tied to either a noninverting or inverting input of a differential amplifier with the remaining input grounded. For example, Side A, AMP-OUT-A (Pin 6) must be tied to A+IN (Pin 5) with A−IN (Pin 4) tied to ground for noninverting operation or AMP-OUT-A (Pin 6) tied to A−IN (Pin 4) with A+IN (Pin 5) tied to ground for inverting operation.

USING THE DIFFERENTIAL INPUT

Each channel of the AD13280 is designed with two optional differential inputs, A+IN, A−IN and B+IN, B−IN. The inputs provide system designers with the ability to bypass the AD8045 amplifier and drive the AD8138 directly. The AD8138 differential ADC driver can be deployed in either a single-ended or differential input configuration. The differential analog inputs have a nominal input impedance of 620 Ω and nominal full-scale input range of 1.2 V p-p. The AD8138 amplifier drives a differential filter and the custom analog-to-digital converter. The differential input configuration provides the lowest even-order harmonics and signal-to-noise (SNR) performance improvement of up to 3 dB (SNR = 73 dBFS). Exceptional care was taken in the layout of the differential input signal paths. The differential input transmission line characteristics are matched and balanced. Equal attention to system level signal paths must be provided in order to realize significant performance improvements.

APPLICATIONS INFORMATION

ENCODING THE AD13280

The AD13280 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 12-bit accuracy at 80 MSPS places a premium on encode clock phase noise. SNR performance can easily degrade 3 dB to 4 dB with 37 MHz input signals when using a high jitter clock source. See Analog Devices Application Note AN-501, *Aperture Uncertainty and ADC System Performance*, for complete details. For optimum performance, the AD13280 must be clocked differentially. The encode signal is usually ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 17 shows one preferred method for clocking the AD13280. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD13280 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD13280 and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limited resistor (typically 100 Ω) is placed in series with the primary.

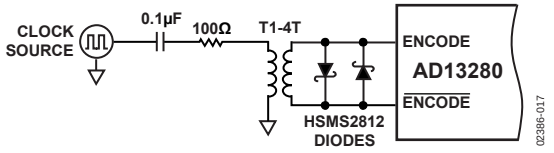


Figure 17. Crystal Clock Oscillator—Differential Encode

If a low jitter ECL/PECL clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown below. A device that offers excellent jitter performance is the MC100LVEL16 (or within the same family) from Motorola.

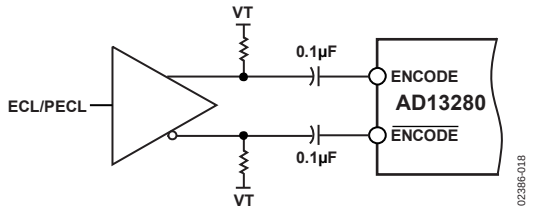


Figure 18. Differential ECL for Encode

JITTER CONSIDERATION

The signal-to-noise ratio for any ADC can be predicted. When normalized to ADC codes, Equation 1 accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$SNR = -20 \times \log\left[\left[\frac{1+\varepsilon}{2^N}\right]^2 + \left(2 \times \pi \times f_{ANALOG} \times t_{J\,rms}\right)^2 + \left(\frac{V_{NOISE\,rms}}{2^N}\right)^2\right]^{1/2} \quad (1)$$

where:

f_{ANALOG} is the analog input frequency.

$t_{J\,rms}$ is the rms jitter of the encode (rms sum of encode source and internal encode circuitry).

ε is the average DNL of the ADC (typically 0.50 LSB).

N is the number of bits in the ADC.

$V_{NOISE\,rms}$ is the analog input of the ADC (typically 5 LSB).

For a 12-bit analog-to-digital converter like the AD13280, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. The chart below shows a family of curves that demonstrates the expected SNR performance of the AD13280 as jitter increases. The chart is derived from Equation 1.

For a complete discussion of aperture jitter, consult Analog Devices Application Note AN-501, *Aperture Uncertainty and ADC System Performance.*

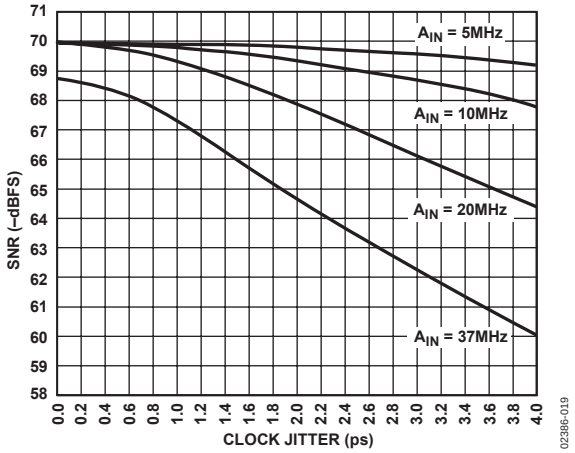


Figure 19. SNR vs. Jitter

POWER SUPPLIES

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that may be received by the AD13280. Each of the power supply pins should be decoupled as close as possible to the package using 0.1 µF chip capacitors.

The AD13280 has separate digital and analog power supply pins. The analog supplies are denoted AV_{CC}, and the digital supply pins are denoted DV_{CC}. AV_{CC} and DV_{CC} should be separate power supplies because the fast digital output swings can couple switching current back into the analog supplies.

Note that AV_{CC} must be held within 5% of 5 V. The AD13280 is specified for DV_{CC} = 3.3 V because this is a common supply for digital ASICs.

OUTPUT LOADING

Care must be taken when designing the data receivers for the AD13280. The digital outputs drive an internal series resistor (for example, 100 Ω) followed by a gate like 75LCX574. To minimize capacitive loading, there should be only one gate on each output pin. An example of this is shown in the evaluation board schematic (see Figure 20). The digital outputs of the AD13280 have a constant output slew rate of 1 V/ns.

A typical CMOS gate combined with a PCB trace has a load of approximately 10 pF. Therefore, as each bit switches, 10 mA (10 pF × 1 V ÷ 1 ns) of dynamic current per bit flows in or out of the device. A full-scale transition can cause up to 120 mA (12 bits × 10 mA/bit) of transient current through the output stages. These switching currents are confined between ground and the DVCC pin. Standard TTL gates should be avoided because they can appreciably add to the dynamic switching currents of the AD13280. It should also be noted that extra capacitive loading increases output timing and invalidates timing specifications. Digital output timing is guaranteed with 10 pF loads.

EVALUATION BOARD

The AD13280 evaluation board (see Figure 20) is designed to provide optimal performance for evaluation of the AD13280 analog-to-digital converter. The board encompasses everything needed to ensure the highest level of performance for evaluating the AD13280. The board requires an analog input signal, encode clock, and power supply inputs. The clock is buffered on-board to provide clocks for the latches. The digital outputs and out clocks are available at the standard 40-pin connectors J1 and J2.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the associated components and the analog section of the AD13280. The digital outputs of the AD13280 are powered via banana jacks with 3.3 V. Contact the factory if additional layout or applications assistance is required.

LAYOUT INFORMATION

The schematics of the evaluation board (Figure 21, Figure 22, and Figure 23) represent a typical implementation of the AD13280. The pinout of the AD13280 is very straightforward and facilitates ease of use and the implementation of high frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors can be standard, high quality ceramic chip capacitors.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and should connect directly to the receiving gate. Internal circuitry buffers the outputs of the ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.

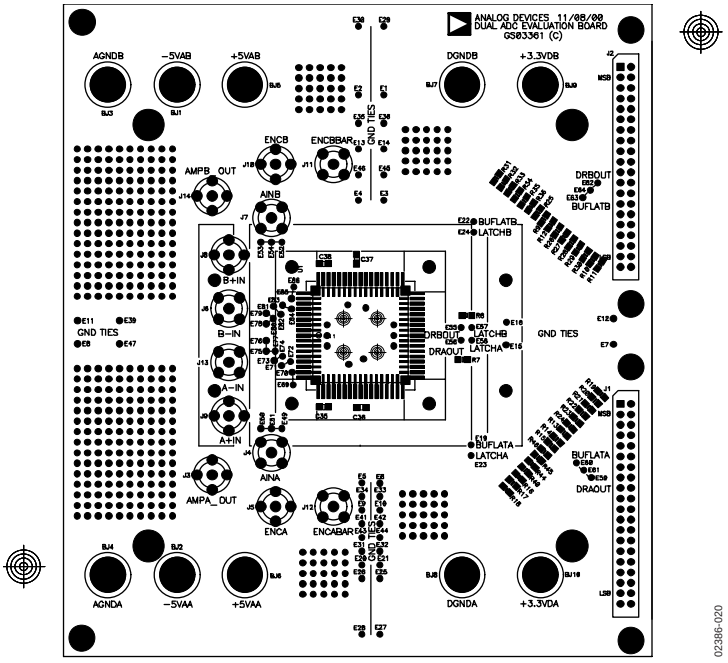


Figure 20. Evaluation Board Mechanical Layout

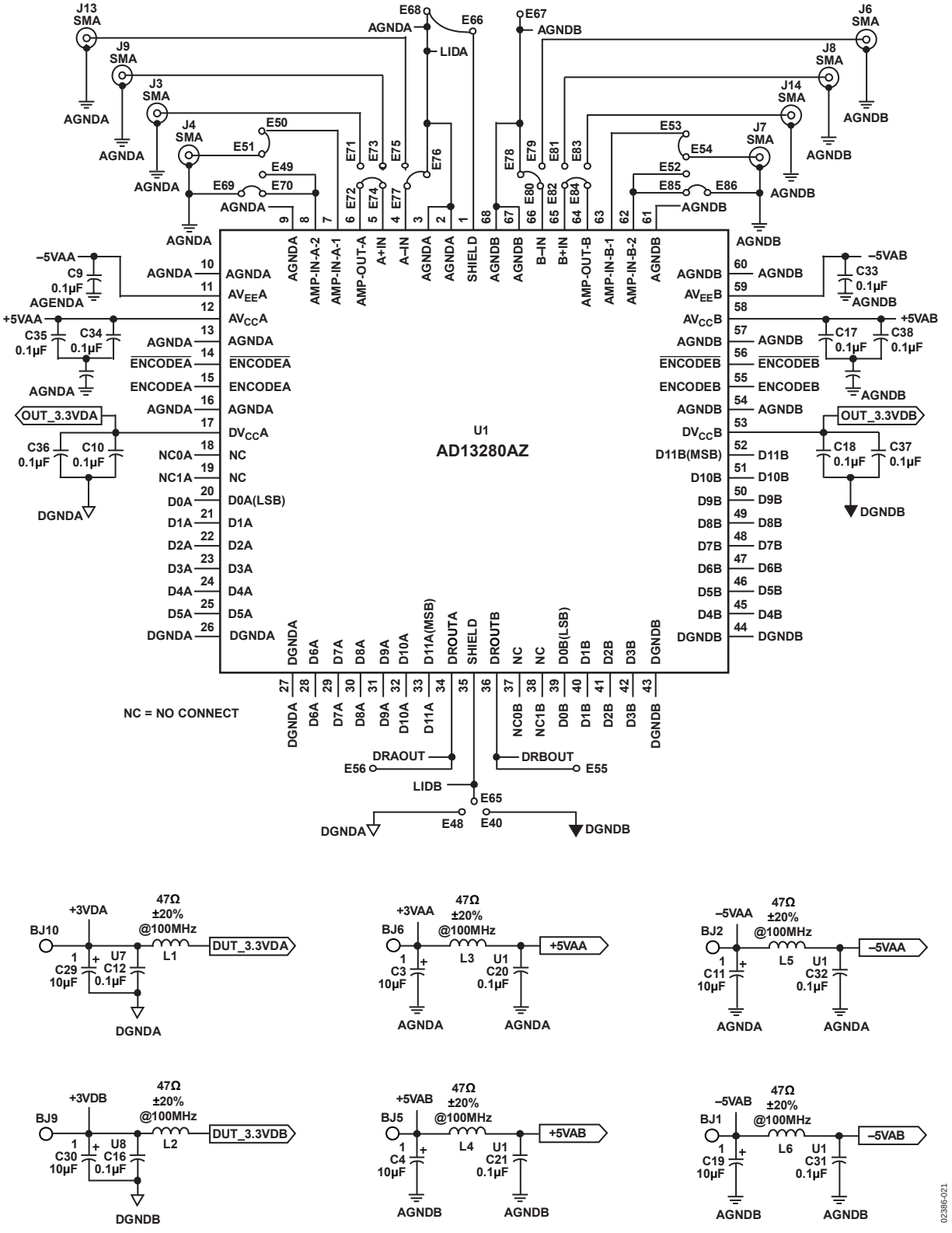


Figure 21. Evaluation Board

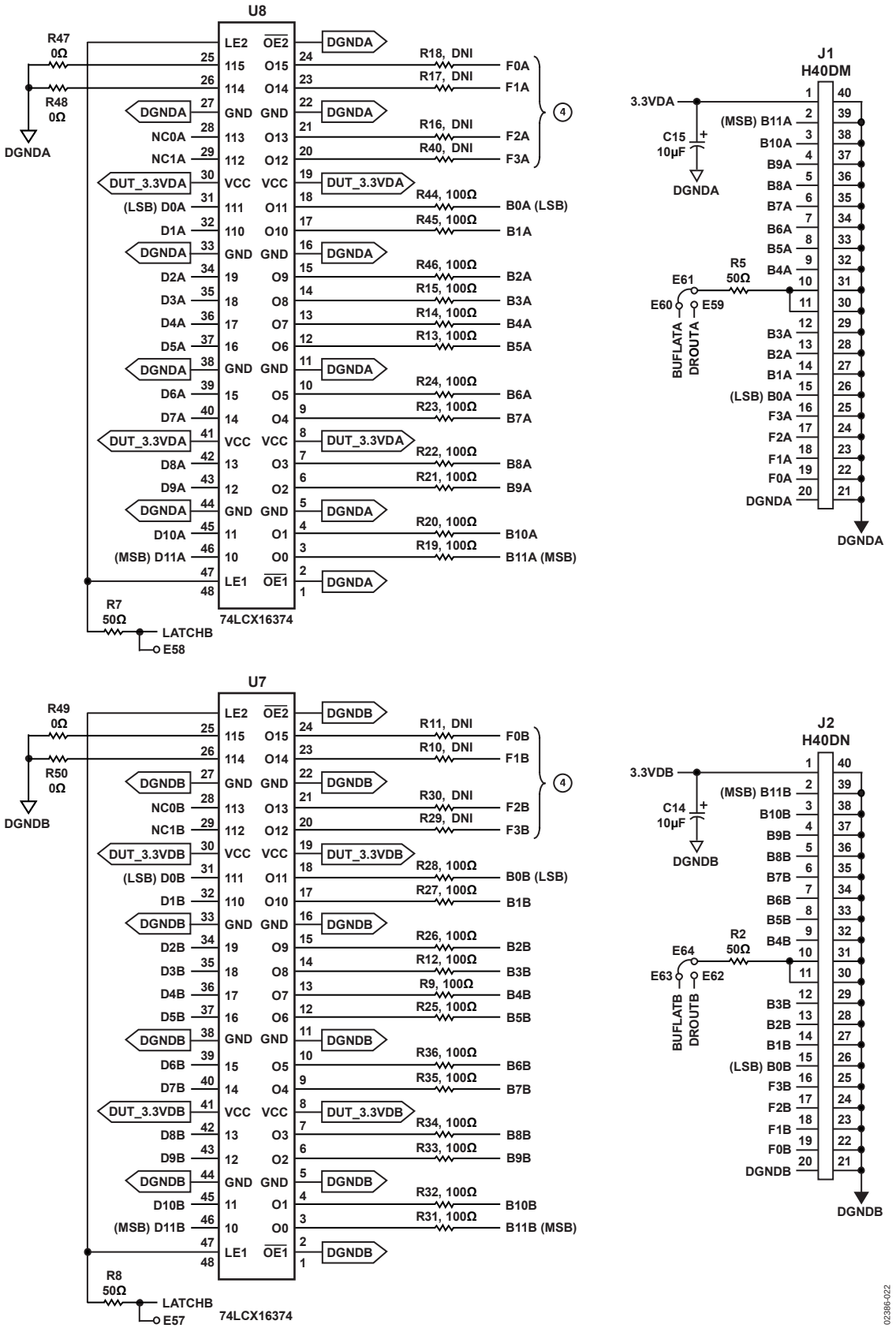


Figure 22. Evaluation Board

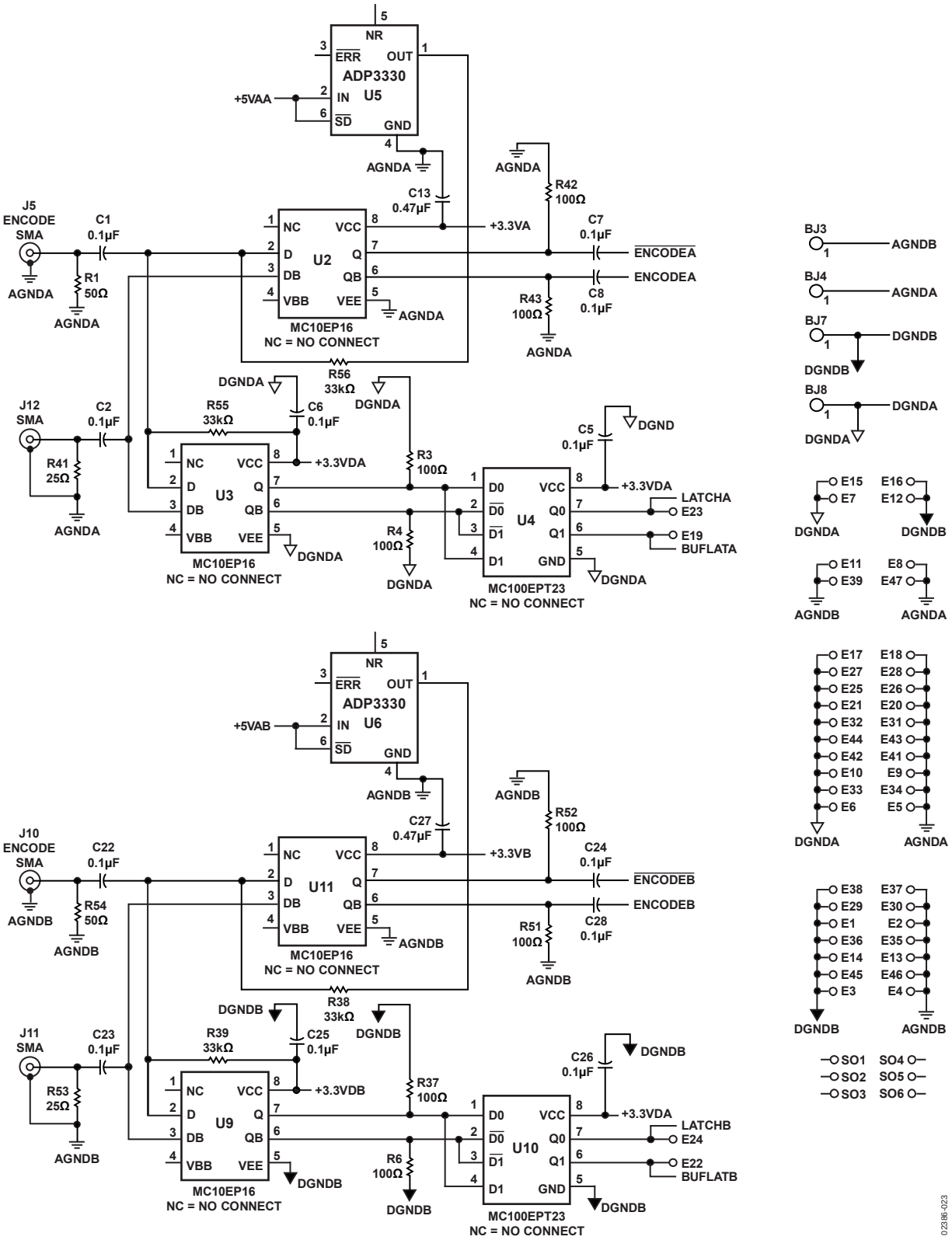


Figure 23. Evaluation Board

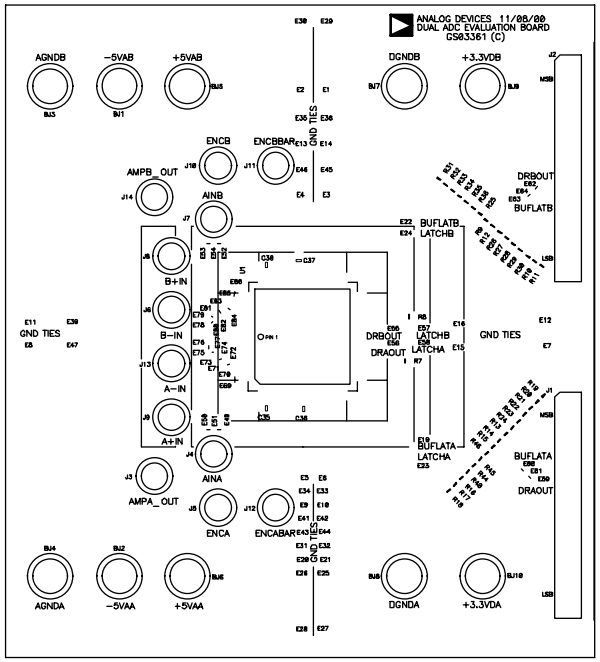


Figure 24. Top Silk

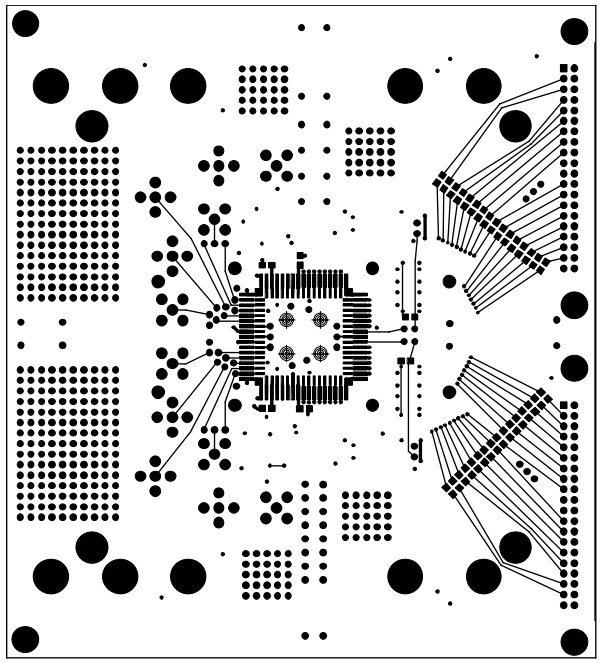


Figure 25. Top Layer

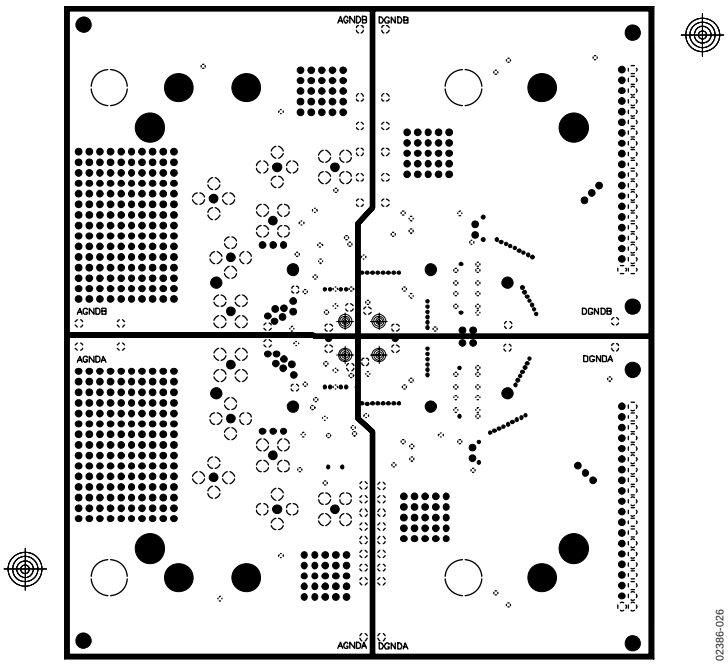


Figure 26. GND1

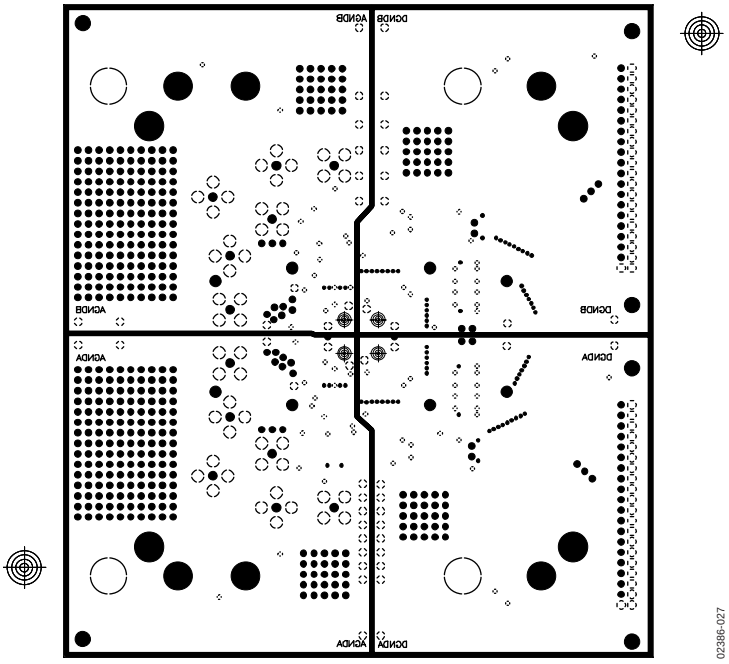


Figure 27. GND2

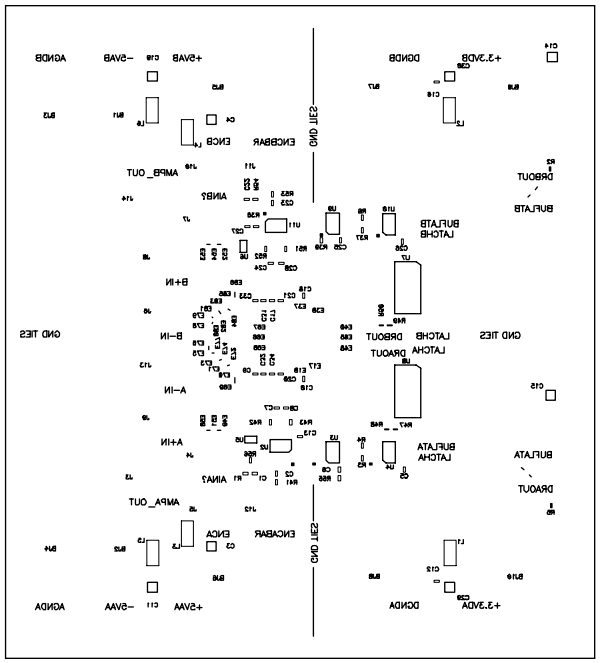


Figure 28. Bottom Silk

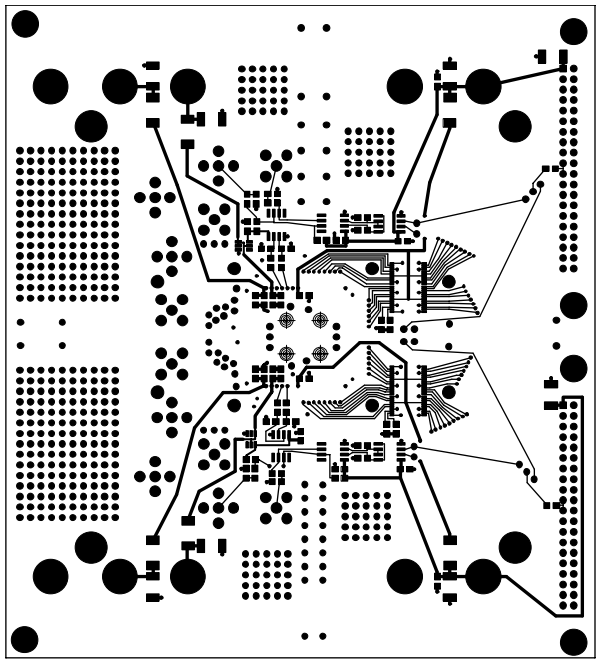


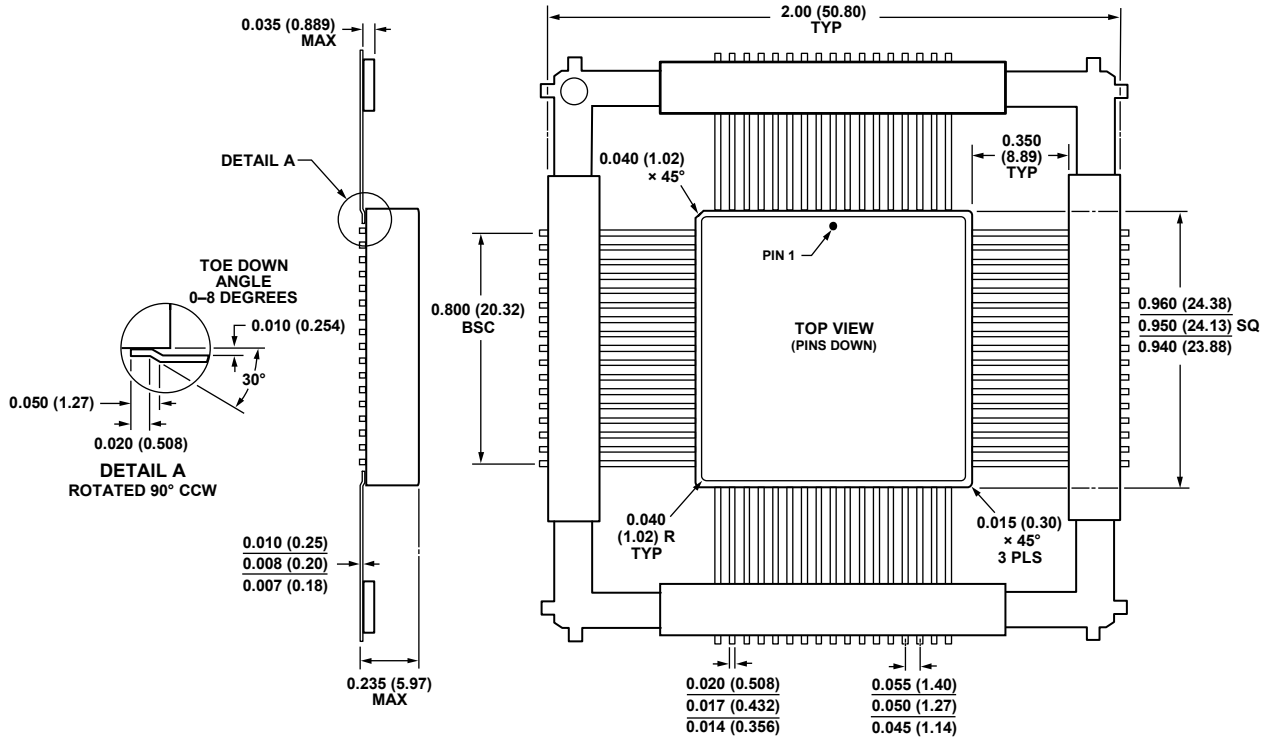
Figure 29. Bottom Layer

BILL OF MATERIALS LIST FOR EVALUATION BOARD

Table 4.

Qty	Component Name	Reference	Value	Description	Manufacturing Part Number
2	74LCX16374MTD	U7, U8		Latch	74LCX16374MTD (Fairchild)
1	AD13280AZ	U1		AD13280	AD13280AZ
2	ADP3330	U5, U6		Regulator	ADP3330ART-3.3RL7
10	BJACK	BJ1 to BJ10		Banana jacks	108-0740-001 (Johnson Components)
2	BRES0805	R41, R53	25 Ω	0805 SM resistor	ERJ-6GEYJ 240V (Panasonic)
4	BRES0805	R38, R39, R55, R56	33 kΩ	0805 SM resistor	ERJ-6GEYJ 333V (Panasonic)
28	CAP2	C1, C2, C5 to C10, C12, C16 to C18, C20 to C26, C28, C31 to C38	0.1 µF	0805 SM capacitor	GRM 40X7R104K025BL
2	CAP2	C13, C27	0.47 µF	0805 SM capacitor	VJ1206U474MFXMB (Vishay)
2	H40DM	J1, J2		2 × 20, 40-pin male connector	TSW-120-08-G-D
6	IND2	L1 to L6	47 Ω	SM inductor	2743019447
4	MC10EP16	U2, U3, U9, U11		Clock drivers	MC10EP16D (ON Semiconductor)
2	MC100EPT23	U4, U10		ECL/TTL clock drivers	SY100EP23L (ON Semiconductor)
8	POLCAP2	C3, C4, C11, C14, C15, C19, C29, C30	10 µF	Tantalum polar capacitor	T491C106M016AT (Kemet)
4	RES2	R47 to R50	0 Ω	0805 SM resistor	ERJ-6GEY OR 00V (Panasonic)
6	RES2	R1, R2, R5, R7, R8, R54	50 Ω	0805 SM resistor	ERJ-6GEYJ 510V (Panasonic)
32	RES2	R3, R4, R6, R9, R12 to R15, R19 to R28, R31 to R37, R42, R43, R44 to R46, R51, R52	100 Ω	0805 SM resistor	ERJ-6GEYJ 101V (Panasonic)
12	SMA	J3 to J14		SMA connectors	142-0701-201
4	Standoff			Standoff	313-2477-016 (Johnson Components)
4	Screws			Screws (standoff)	MPMS 004 0005 PH (Building Fasteners)
1	PCB			AD13280 evaluation board	GS03361

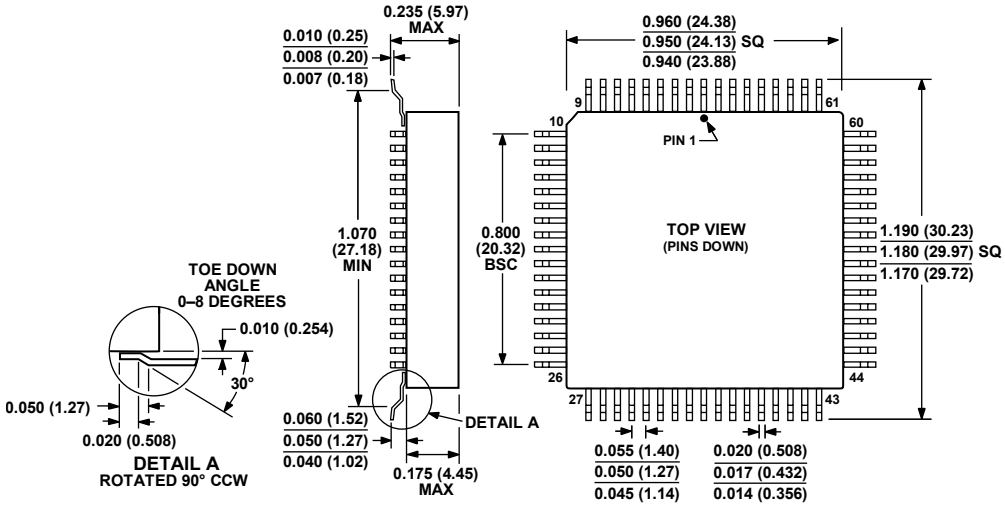
OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

022608-B

Figure 30. 68-Lead Ceramic Leaded Chip Carrier with Nonconductive Tie-Bar [CLCC]
(ES-68-1)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

012908A

Figure 31. 68-Lead Ceramic Leaded Chip Carrier [CLCC]
(ES-68-C)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option
AD13280AZ[2]	−25°C to +85°C	68-Lead Ceramic Leaded Chip Carrier [CLCC]	ES-68-C
AD13280AF	−25°C to +85°C	68-Lead Ceramic Leaded Chip Carrier with Nonconductive Tie-Bar [CLCC]	ES-68-1
AD13280/PCB		Evaluation Board with AD13280AZ	

[1] Referenced temperature is case temperature.
[2] Z is a package indicator; the part is not RoHS compliant.

NOTES

NOTES

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