

## 8-CHANNEL POWER-SUPPLY SEQUENCER AND MONITOR

### FEATURES

- Single Supply Voltage: 3.3 V
- Low Power Consumption
- Sequences and Monitors up to Eight Voltage Rails
- Rail Voltages Sampled Every 50  $\mu$ s With 3.2-mV Resolution
- Four Configurable Digital Outputs for Power-On Reset and Other Functions
- Configurable Rail-Enable Output Polarity
- Flexible Rail Sequencing: Timeline (ms), Parent Rail Regulation Window, Parent Rail Achieving Defined Threshold
- Under- and Overvoltage Thresholds: Settable Per-Rail
- Regulation Expiration Time: Settable Per-Rail
- Flexible Rail Shutdown: Parent Rail Shutdown Can Shut Down Child Rails, Independent Rail Configuration
- Per-Rail Alarm Conditions, With Timestamp: Under- and Overvoltage Glitch, Sustained Under- and/or Overvoltage, Rail Did Not Start
- I<sup>2</sup>C Interface for Configuration and Monitoring
- Microsoft® Windows® GUI for Configuration and Monitoring

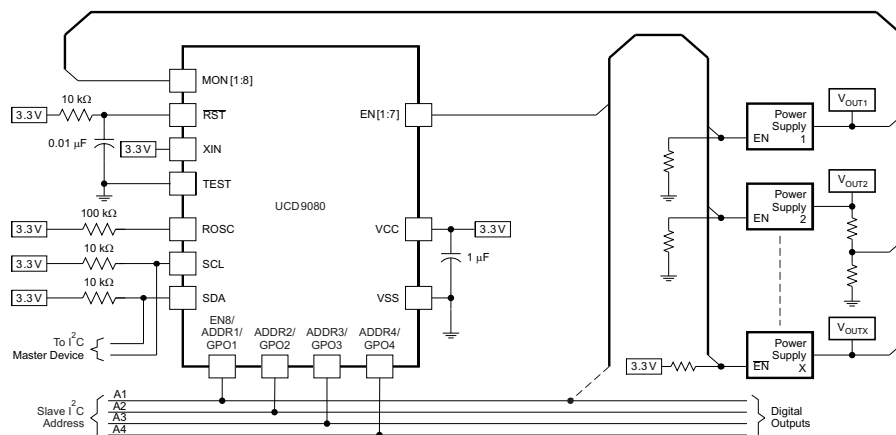
### APPLICATIONS

- Telecommunications Switches
- Servers
- Networking Equipment
- Test Equipment
- Any System Requiring Sequencing of Multiple Voltage Rails

### DESCRIPTION

The UCD9080 power-supply sequencer controls the enable sequence of up to eight independent voltage rails and provides four general-purpose digital outputs. The device operates from a 3.3-V supply, provides 3.2-mV resolution of voltage rails, and requires no external memory or clock. The UCD9080 monitors the voltage rails independently at more than a 20-kHz rate and has a high degree of rail sequence and rail error-response configurability. The sequencing of rails can be based on time or on time in conjunction with other rails achieving regulation or a voltage threshold. In addition, each rail is monitored for undervoltage and overvoltage glitches and thresholds. Each rail the UCD9080 monitors can be configured to shut down a user-defined set of other rails, and alarm conditions are monitored on a per-rail basis.

Figure 1 shows the UCD9080 power-supply sequencer in a typical application.



**Figure 1. Typical Application Diagram**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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# UCD9080

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|                                           | VALUE                         | UNIT |
|-------------------------------------------|-------------------------------|------|
| Voltage applied from VCC to VSS           | –0.3 to 4.1                   | V    |
| Voltage applied to any pin <sup>(2)</sup> | –0.3 to V <sub>CC</sub> + 0.3 | V    |
| Diode current at any device terminal      | ±2                            | mA   |
| T <sub>stg</sub> Storage temperature      | –40 to 85                     | °C   |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to VSS.

## RECOMMENDED OPERATING CONDITIONS

|                 |                                             | MIN | NOM | MAX | UNIT |
|-----------------|---------------------------------------------|-----|-----|-----|------|
| V <sub>CC</sub> | Supply voltage during operation             | 3   | 3.3 | 3.6 | V    |
|                 | Supply voltage during configuration changes | 3   | 3.3 | 3.6 |      |
| T <sub>A</sub>  | Operating free-air temperature range        | −40 |     | 85  | °C   |

## ELECTRICAL CHARACTERISTICS

These specifications are over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted

| PARAMETER                                                                                                   | TEST CONDITIONS       | MIN                 | NOM | MAX                   | UNIT |
|-------------------------------------------------------------------------------------------------------------|-----------------------|---------------------|-----|-----------------------|------|
| <b>SUPPLY CURRENT</b>                                                                                       |                       |                     |     |                       |      |
| I <sub>S</sub> Supply current into V <sub>CC</sub> , excluding external current                             | T <sub>A</sub> = 25°C |                     | 3   | 4                     | mA   |
| I <sub>C</sub> Supply current during configuration                                                          | 3.6 V                 | 3                   |     | 7                     | mA   |
| <b>STANDARD INPUTS (RST, TEST)</b>                                                                          |                       |                     |     |                       |      |
| V <sub>IL</sub> Low-level input voltage                                                                     | V <sub>CC</sub> = 3 V | V <sub>SS</sub>     |     | V <sub>SS</sub> + 0.6 | V    |
| V <sub>IH</sub> High-level input voltage                                                                    | V <sub>CC</sub> = 3 V | 0.8 V <sub>CC</sub> |     | V <sub>CC</sub>       | V    |
| <b>SCHMITT TRIGGER INPUTS (SDA, SCL, EN1, EN2, EN3, EN4, EN5, EN6, EN7, EN8/ADDR1, ADDR2, ADDR3, ADDR4)</b> |                       |                     |     |                       |      |
| V <sub>IT+</sub> Positive-going input threshold voltage                                                     | V <sub>CC</sub> = 3 V | 1.5                 |     | 1.9                   | V    |
| V <sub>IT–</sub> Negative-going input threshold voltage                                                     | V <sub>CC</sub> = 3 V | 0.9                 |     | 1.3                   | V    |
| V <sub>hys</sub> Input-voltage hysteresis, (V <sub>IT+</sub> – V <sub>IT–</sub> )                           | V <sub>CC</sub> = 3 V | 0.5                 |     | 1                     | V    |
| I <sub>ikg</sub> High-impedance leakage current                                                             |                       |                     |     | ±50                   | nA   |

## ELECTRICAL CHARACTERISTICS (continued)

These specifications are over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted

| PARAMETER                                                                                  |                                                                     | TEST CONDITIONS                                                                                              | MIN                                                                              | NOM                    | MAX             | UNIT   |
|--------------------------------------------------------------------------------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------------------|-----------------|--------|
| ANALOG INPUTS (MON1, MON2, MON3, MON4, MON5, MON6, MON7, MON8, ROSC)                       |                                                                     |                                                                                                              |                                                                                  |                        |                 |        |
| V <sub>CC</sub>                                                                            | Analog supply voltage                                               | V <sub>SS</sub> = 0 V                                                                                        | 3                                                                                |                        | 3.6             | V      |
| V <sub>(R&lt;1..8&gt;)</sub>                                                               | Analog input voltage                                                | Internal voltage reference                                                                                   | 0                                                                                |                        | 2.5             | V      |
|                                                                                            |                                                                     | External voltage reference (V <sub>CC</sub> = 3.3 V used as reference)                                       | 0                                                                                |                        | V <sub>CC</sub> |        |
| C <sub>I</sub> <sup>(1)</sup>                                                              | Input capacitance                                                   | Only one terminal can be selected at a time (MON1–MON8)                                                      |                                                                                  |                        | 27              | pF     |
| R <sub>I</sub> <sup>(1)</sup>                                                              | Input MUX ON resistance                                             | 0 V ≤ V <sub>(MONx)</sub> ≤ V <sub>CC</sub> , V <sub>CC</sub> = 3 V                                          |                                                                                  |                        | 2000            | Ω      |
| I <sub>lkg</sub>                                                                           | High-impedance leakage current                                      | MON1–MON8                                                                                                    |                                                                                  |                        | ±50             | nA     |
| V <sub>REF+</sub>                                                                          | Positive internal reference voltage output                          | REF2_5V = 1 for 2.5 V I <sub>(VREF+)</sub> ≤ I <sub>(VREF+)</sub> max, V <sub>CC</sub> = 3 V                 | 2.35                                                                             | 2.5                    | 2.65            | V      |
| V <sub>CC(min)</sub>                                                                       | V <sub>CC</sub> minimum voltage, positive built-in reference active | REF2_5V = 1, I <sub>(VREF+)</sub> ≤ 0.5 mA                                                                   | 3                                                                                |                        |                 | V      |
|                                                                                            |                                                                     | REF2_5V = 1, I <sub>(VREF+)</sub> ≤ 1 mA                                                                     | 3                                                                                |                        |                 | V      |
| V <sub>(acc)</sub>                                                                         | Accuracy of voltage sampling from rails                             | Internal reference (2.5 V)                                                                                   | ±6.8                                                                             | ±12                    | ±17.4           | mV     |
|                                                                                            |                                                                     | External reference (3.3 V/V <sub>CC</sub> )                                                                  | ±0.2                                                                             | ±1.6                   | ±6.8            |        |
| T <sub>REF+</sub> <sup>(1)</sup>                                                           | Temperature coefficient of built-in reference                       | I <sub>(VREF+)</sub> is a constant in the range of 0 mA ≤ I <sub>(VREF+)</sub> ≤ 1 mA, V <sub>CC</sub> = 3 V |                                                                                  |                        | ±100            | ppm/°C |
| MISCELLANEOUS                                                                              |                                                                     |                                                                                                              |                                                                                  |                        |                 |        |
| t <sub>retention</sub>                                                                     | Retention of configuration parameters                               | T <sub>J</sub> = 25°C                                                                                        | 100                                                                              |                        |                 | Years  |
| POR, Brownout, Reset <sup>(2)</sup> <sup>(3)</sup>                                         |                                                                     |                                                                                                              |                                                                                  |                        |                 |        |
| t <sub>d(BOR)</sub>                                                                        | Brownout                                                            | V <sub>CC</sub> /dt ≤ 3 V/s                                                                                  | 2000                                                                             |                        |                 | μs     |
| V <sub>CC(start)</sub>                                                                     |                                                                     |                                                                                                              | 0.7×V <sub>(B_IT-)</sub>                                                         |                        |                 | V      |
| V <sub>(B_IT-)</sub>                                                                       |                                                                     |                                                                                                              | 1.71                                                                             |                        |                 | V      |
| V <sub>hys(B_IT-)</sub>                                                                    |                                                                     |                                                                                                              | 70                                                                               | 130                    | 180             | mV     |
| t <sub>(reset)</sub>                                                                       |                                                                     |                                                                                                              | Pulse length needed at RST pin to accept reset internally, V <sub>CC</sub> = 3 V |                        | 2               |        |
| DIGITAL OUTPUTS (EN8/GPO1, GPO2, GPO3, GPO4, EN1, EN2, EN3, EN4, EN5, EN6, EN7, SDA, SCL ) |                                                                     |                                                                                                              |                                                                                  |                        |                 |        |
| V <sub>OH</sub>                                                                            | High-level output voltage                                           | I <sub>OH(max)</sub> = −1.5 mA, <sup>(4)</sup> V <sub>CC</sub> = 3 V                                         | V <sub>CC</sub> − 0.25                                                           |                        | V <sub>CC</sub> | V      |
|                                                                                            |                                                                     | I <sub>OH(max)</sub> = −6 mA, <sup>(5)</sup> V <sub>CC</sub> = 3 V                                           | V <sub>CC</sub> − 0.6                                                            |                        | V <sub>CC</sub> |        |
| V <sub>OL</sub>                                                                            | Low-level output voltage                                            | I <sub>OH(max)</sub> = −1.5 mA, <sup>(4)</sup> V <sub>CC</sub> = 3 V                                         | V <sub>SS</sub>                                                                  | V <sub>SS</sub> + 0.25 |                 | V      |
|                                                                                            |                                                                     | I <sub>OH(max)</sub> = −6 mA, <sup>(5)</sup> V <sub>CC</sub> = 3 V                                           | V <sub>SS</sub>                                                                  | V <sub>SS</sub> + 0.6  |                 |        |
| I <sub>lkg</sub>                                                                           | High-impedance leakage current                                      | V <sub>CC</sub> = 3 V                                                                                        |                                                                                  |                        | ±50             | nA     |

(1) Not production tested. Limits verified by design.

(2) The current consumption of the brownout module is already included in the I<sub>CC</sub> current-consumption data.

(3) During power up, device initialization starts subsequent to a period of t<sub>d(BOR)</sub> after V<sub>CC</sub> = V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub>.

(4) The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.

(5) The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

The UCD9080 is compatible with 3.3-V IO ports of microcontrollers, TMS320™ DSP family as well as ASICs. The UCD9080 is available in a plastic 32-pin QFN package (RHB).

## DIGITAL OUTPUTS (Only One Output Loaded at a Time)

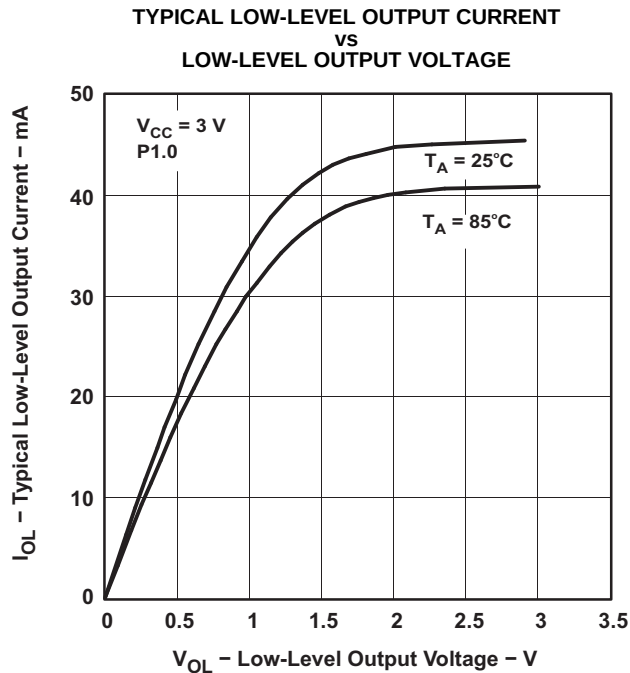


Figure 2.

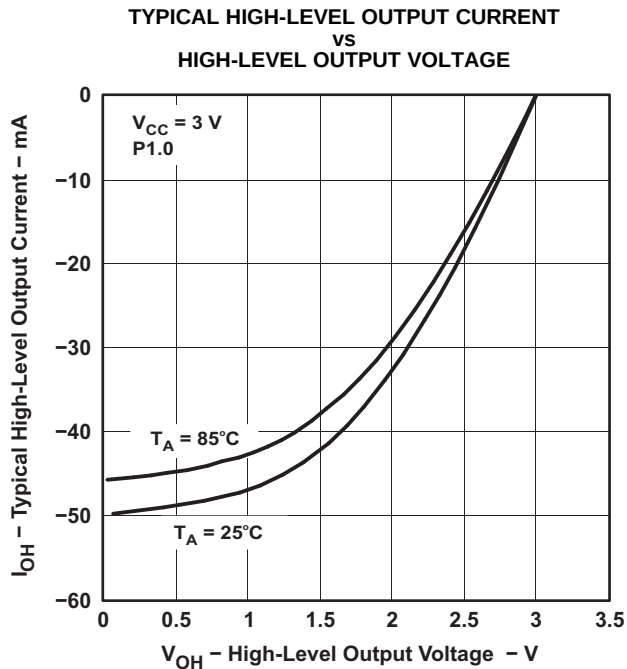


Figure 3.

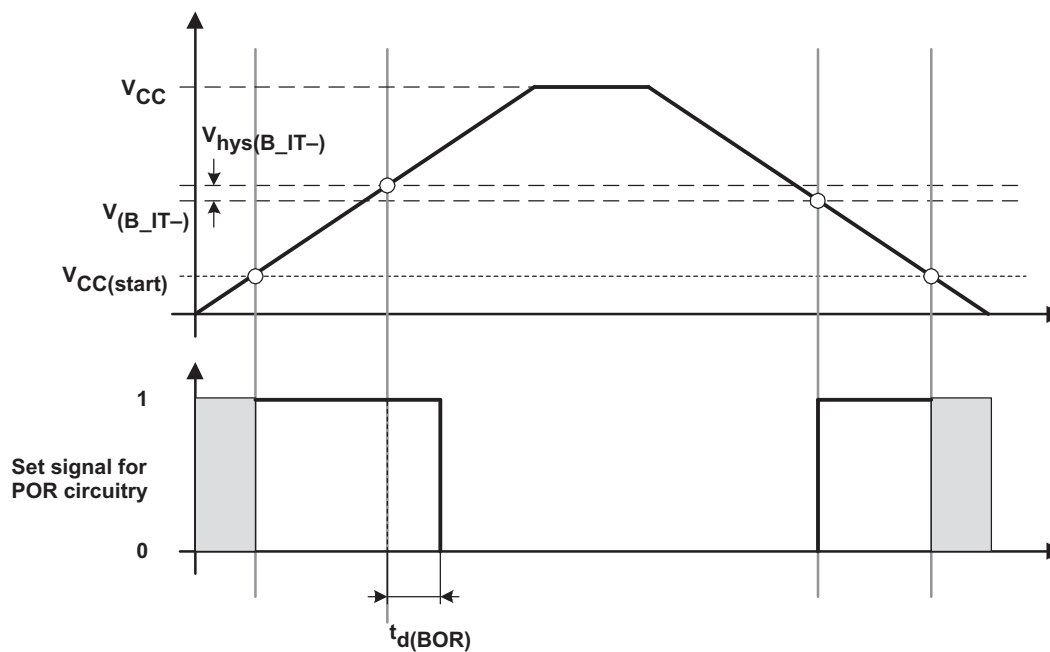


Figure 4. POR/Brownout Reset (BOR) vs Supply Voltage

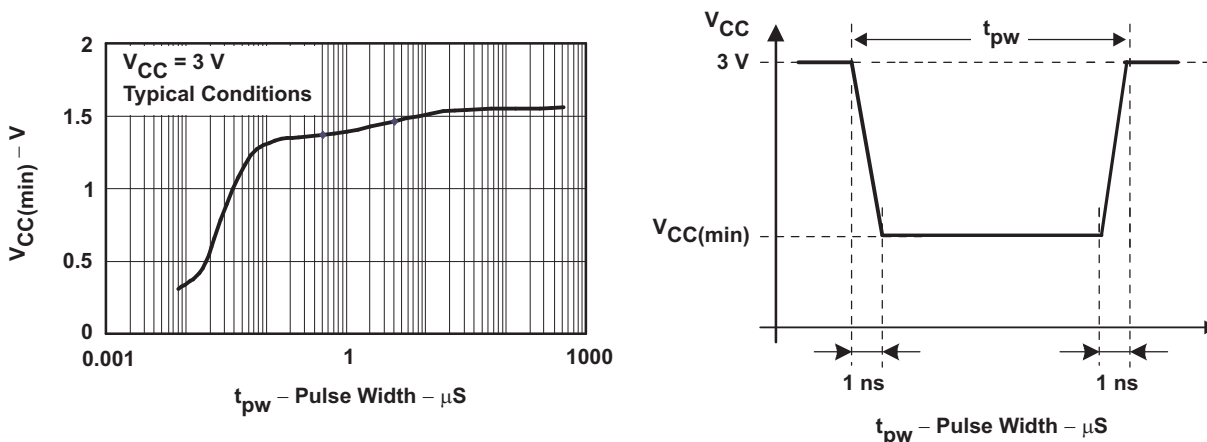


Figure 5.  $V_{CC(min)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

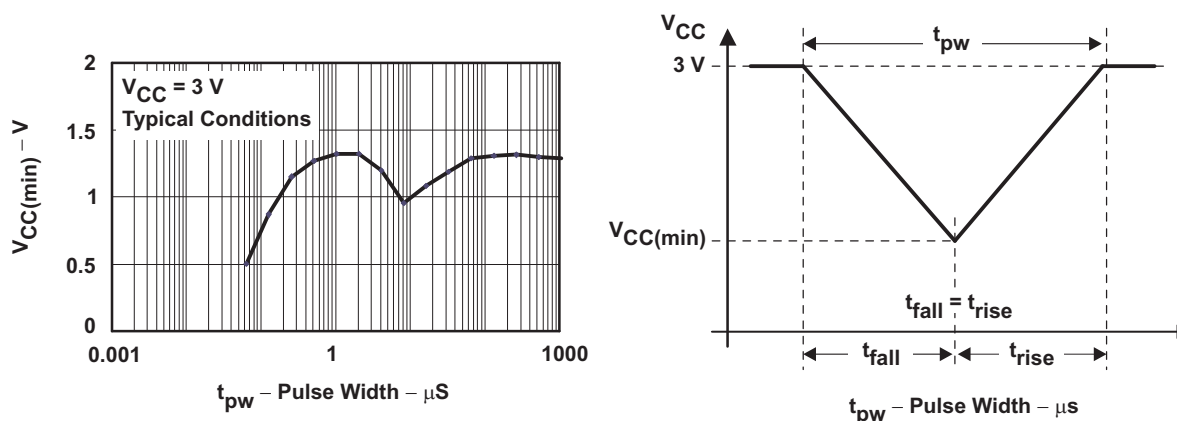


Figure 6.  $V_{CC(min)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

## I<sup>2</sup>C TIMING

The UCD9080 supports the same timing parameters as standard-mode I<sup>2</sup>C. See the following timing diagram and timing parameters for more information.

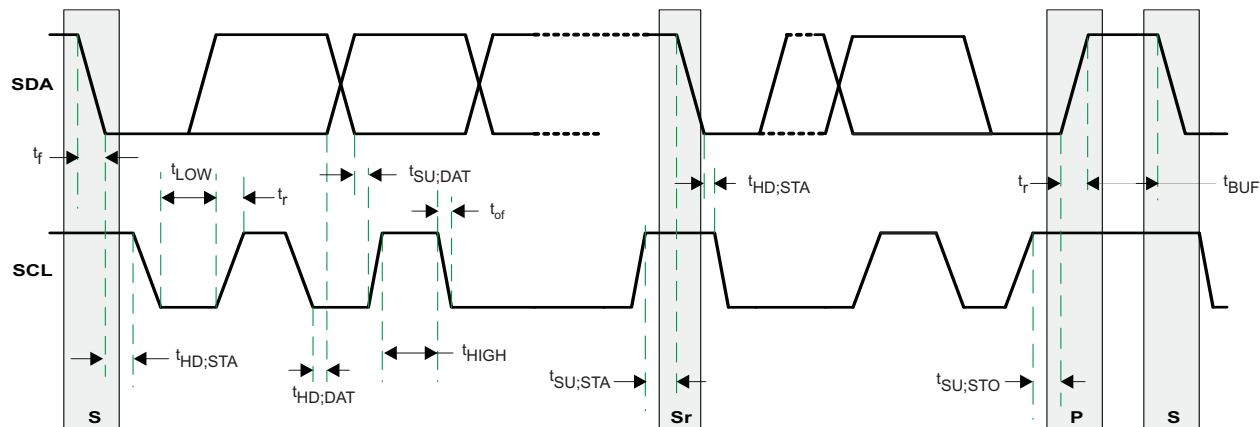


Figure 7. Timing Diagram for I<sup>2</sup>C Interface

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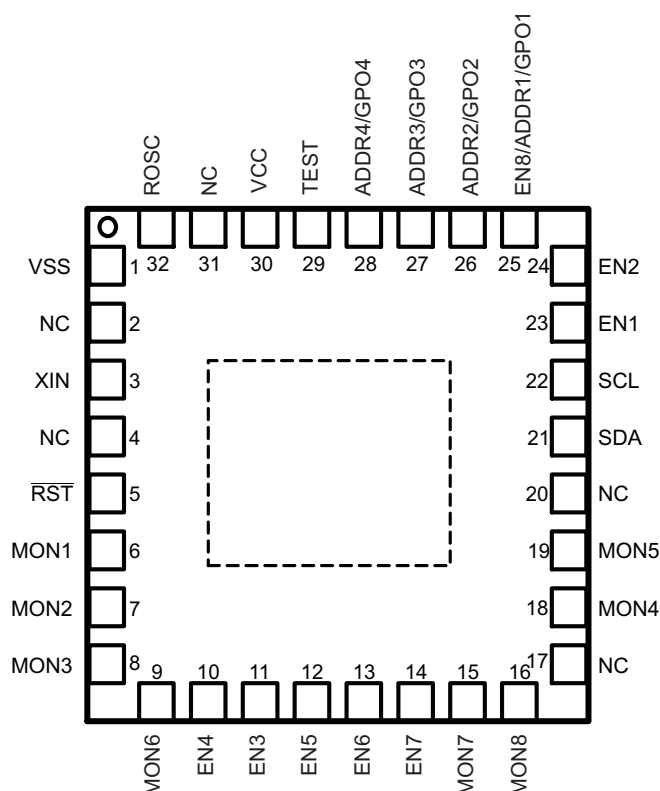
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## TIMING PARAMETERS FOR I<sup>2</sup>C INTERFACE

| PARAMETER    |                                                                                                       | MIN              | MAX                 | UNIT |
|--------------|-------------------------------------------------------------------------------------------------------|------------------|---------------------|------|
| $t_{of}$     | Output fall time from $V_{OH}$ to $V_{OL}$ <sup>(1)</sup> with a bus capacitance from 10 pF to 400 pF |                  | 250 <sup>(2)</sup>  | ns   |
| $C_I$        | Capacitance for each pin.                                                                             |                  | 10                  | pF   |
| $f_{SCL}$    | SCL clock frequency                                                                                   | 10               | 100                 | kHz  |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated.          | 4                |                     | μs   |
| $t_{HD;DAT}$ | Data hold time                                                                                        | 0 <sup>(3)</sup> | 3.45 <sup>(4)</sup> | μs   |
| $t_{LOW}$    | LOW period of the SCL clock                                                                           | 4.7              |                     | μs   |
| $t_{HIGH}$   | HIGH period of the SCL clock                                                                          | 4                |                     | μs   |
| $t_{SU;STA}$ | Set-up time for repeated start condition                                                              | 4.7              |                     | μs   |
| $t_{SU;DAT}$ | Data setup time                                                                                       | 250              |                     | ns   |
| $t_r$        | Rise time of both SDA and SCL signals                                                                 |                  | 1000                | ns   |
| $t_f$        | Fall time of both SDA and SCL signals                                                                 |                  | 300                 | ns   |
| $t_{SU;STO}$ | Setup time for STOP condition                                                                         | 4                |                     | μs   |
| $t_{BUF}$    | Bus free time between a STOP and START condition                                                      | 4.7              |                     | μs   |
| $C_{(b)}$    | Capacitive load for each bus line                                                                     |                  | 400                 | pF   |
| $V_{nL}$     | Noise margin at the LOW level for each connected device (including hysteresis)                        | 0.1 VDD          |                     | V    |
| $V_{nH}$     | Noise margin at the HIGH level for each connected device (including hysteresis)                       | 0.2 VDD          |                     | V    |

- (1) See the *Electrical Characteristics* section of this data sheet.
- (2) The maximum  $t_f$  for the SDA and SCL bus lines (300 ns) is longer than the specified maximum  $t_{of}$  for the output stages (250 ns). This allows series protection resistors ( $R_s$ ) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
- (4) The maximum  $t_{HD;DAT}$  must only be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.

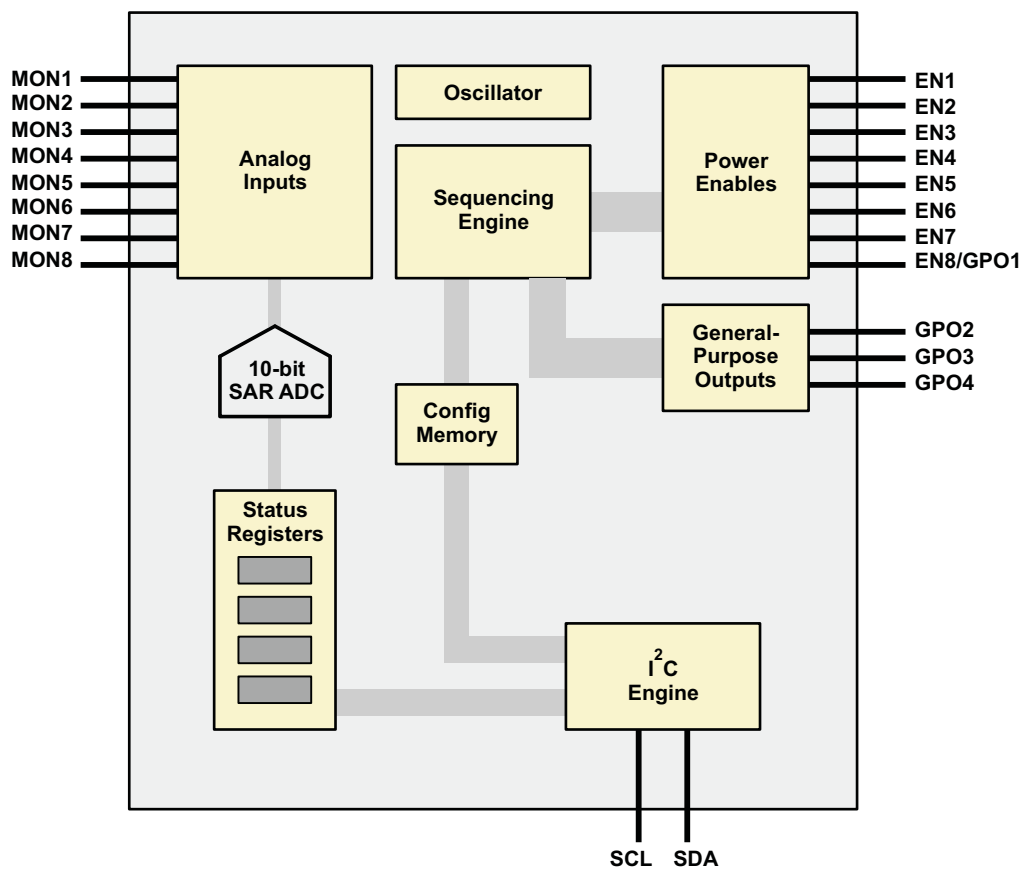
### RHB PACKAGE (TOP VIEW)



**Table 1. TERMINAL FUNCTIONS**

| TERMINAL           |                 | I/O | DESCRIPTION                                                                                                                              |
|--------------------|-----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------|
| NAME               | NO.             |     |                                                                                                                                          |
| ADDR2/GPO2         | 26              | I/O | I <sup>2</sup> C address select 2, general-purpose digital output 2                                                                      |
| ADDR3/GPO3         | 27              | I/O | I <sup>2</sup> C address select 3, general-purpose digital output 3                                                                      |
| ADDR4/GPO4         | 28              | I/O | I <sup>2</sup> C address select 4, general-purpose digital output 4                                                                      |
| EN1                | 23              | I/O | Voltage rail 1 enable (digital output)                                                                                                   |
| EN2                | 24              | I/O | Voltage rail 2 enable (digital output)                                                                                                   |
| EN3                | 11              | I/O | Voltage rail 3 enable (digital output)                                                                                                   |
| EN4                | 10              | I/O | Voltage rail 4 enable (digital output)                                                                                                   |
| EN5                | 12              | I/O | Voltage rail 5 enable (digital output)                                                                                                   |
| EN6                | 13              | I/O | Voltage rail 6 enable (digital output)                                                                                                   |
| EN7                | 14              | I/O | Voltage rail 7 enable (digital output)                                                                                                   |
| EN8/ADDR1/<br>GPO1 | 25              | I/O | Voltage rail 8 enable (digital output), I <sup>2</sup> C address select 1, general-purpose digital output 1                              |
| MON1               | 6               | I   | Analog input for voltage rail 1                                                                                                          |
| MON2               | 7               | I   | Analog input for voltage rail 2                                                                                                          |
| MON3               | 8               | I   | Analog input for voltage rail 3                                                                                                          |
| MON4               | 18              | I   | Analog input for voltage rail 4                                                                                                          |
| MON5               | 19              | I   | Analog input for voltage rail 5                                                                                                          |
| MON6               | 9               | I   | Analog input for voltage rail 6                                                                                                          |
| MON7               | 15              | I   | Analog input for voltage rail 7                                                                                                          |
| MON8               | 16              | I   | Analog input for voltage rail 8                                                                                                          |
| NC                 | 2               |     | Do not connect.                                                                                                                          |
| NC                 | 4,17,<br>20, 31 |     | Not connected internally. Connect to VSS.                                                                                                |
| ROSC               | 32              |     | Internal oscillator frequency adjust. Must use 100-kΩ pullup to VCC for minimum drift and maximum frequency when sampling voltage rails. |
| RST                | 5               | I   | Reset input                                                                                                                              |
| SCL                | 22              | I/O | I <sup>2</sup> C clock. A pullup resistor to 3.3 V is required.                                                                          |
| SDA                | 21              | I/O | I <sup>2</sup> C data (bidirectional). A pullup resistor to 3.3 V is required.                                                           |
| TEST               | 29              | I   | Connect to VSS                                                                                                                           |
| VCC                | 30              |     | Supply voltage                                                                                                                           |
| VSS                | 1               |     | Ground reference                                                                                                                         |
| XIN                | 3               |     | Connect to VCC                                                                                                                           |

## FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### POWER-SUPPLY SEQUENCING

The UCD9080 can be configured to sequence the power rails using the enable signals or the general-purpose outputs in one of three ways.

The first way is to specify a delay time after a UCD9080 RESET. The enable/GPO is asserted after the UCD9080 RESET plus a specified delay.

The second way is to specify a delay time after another (parent) rail has achieved regulation (that is,  $V_{\text{RAIL}}$  is within the specified under- and overvoltage settings). The enable/GPO is asserted after the (parent) rail is in regulation plus specified delay.

The third way is to specify a (parent) rail voltage. The enable/GPO is asserted after the (parent) rail voltage is greater than or equal to the specified voltage.

Of course, a rail does not have to be sequenced, as in the case of a backplane voltage that is not under the control of the UCD9080, but is being monitored.

### POWER-SUPPLY ENABLES

The UCD9080 can sequence up to eight power supplies using the ENx (EN1 to EN8) signals. These signals can be configured as active-high or active-low, supporting power supplies with either polarity.

EN8 can also be configured as a GPO (GPO1). EN8/ADDR1/GPO1 is also used for I<sup>2</sup>C address selection (ADDR1).

### GENERAL-PURPOSE OUTPUTS

The UCD9080 can control up to four general-purpose digital outputs using the same sequencing mechanisms as described in the [Power-Supply Enables](#) section. These general-purpose outputs (referred to as GPO1–GPO4) can be used for digital signals such as RESET or status. Note that these signals are multiplexed with other functions (primarily I<sup>2</sup>C address selection). See the [Terminal Functions](#) table to ensure that these signals are used properly by the application. Also note that the GPO1 signal is multiplexed with EN8, so both of these cannot be used at the same time.

### EXTERNAL CONSIDERATIONS FOR EN AND GPO PINS

During the UCD9080 RESET interval, all ENx and GPOx pins become Schmitt-trigger Inputs. A UCD9080 RESET occurs under the following conditions:

- External  $\overline{\text{RST}}$  pin is driven low.
- Power is applied to the device (power-on reset) or power is cycled.
- A sequence event occurs as a result of a configured rail-alarm event.
- The RESTART register is written with a value of 0 over the I<sup>2</sup>C bus.

All ENx and GPOx pins must be externally terminated to one of the following Schmitt-trigger input-logic states for proper sequencer operation.

- EN or GPO pin configured for ACTIVE-LOW polarity: the external resistor network must default the corresponding EN or GPO pin to a voltage greater than or equal to 1.9 V ( $V_{\text{IT+}}$ , MAX, positive-going input threshold voltage) during device reset.
- EN or GPO pin configured for ACTIVE-HIGH polarity: the external resistor network must default the corresponding EN or GPO pin to a voltage less than or equal to 0.9 V ( $V_{\text{IT-}}$ , MIN, negative-going input threshold voltage) during device reset.

#### NOTE:

The external resistor networks should not derive their voltage from a sequenced power supply, as this may cause the voltage level presented to the ENx or GPOx pin to be at the wrong level during device reset. It is best to use the UCD9080 VCC supply for the external resistor networks.

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The user must consider GPO polarity usage when programming the UCD9080 I<sup>2</sup>C address using the external GPOx (ADDRx) resistor networks. Acceptable ADDR<sub>x</sub> bit voltage levels are set according to Schmitt-trigger input specifications. The following GPOx/ADDR<sub>x</sub> combinations are acceptable:

- GPO<sub>x</sub> = Active-low polarity: Corresponding ADDR<sub>x</sub> bit set to Schmitt-trigger input logic level = 1
- GPO<sub>x</sub> = Active-high polarity: Corresponding ADDR<sub>x</sub> bit set to Schmitt-trigger input logic level = 0

### VOLTAGE REFERENCE

The UCD9080 has a voltage reference that is selectable via the I<sup>2</sup>C interface and parameter configuration section. The voltage reference can either be an internally generated 2.5-V reference or an external 3.3-V reference. If the external voltage reference is selected, then the 3.3-V reference is from the V<sub>CC</sub> supply to the UCD9080.

Depending on the voltage reference that is being used, the accuracy of reading voltages is affected. The internal reference is not as accurate as the external reference and affects the accuracy of the sampled voltages of the monitored rails. See the *Electrical Characteristics* for information on voltage reading accuracy for use with each of the references.

The [Configuring the UCD9080](#) section details how to select the internal or external voltage reference.

### VOLTAGE MONITORING

The UCD9080 can monitor eight voltage rails through the MON<sub>x</sub> terminals of the device (MON1–MON8). The UCD9080 samples these eight input channels using either the internal 2.5-V reference or V<sub>CC</sub> (3.3 V) as a voltage reference to convert the voltage to digital values. The eight digitally monitored voltage values are accessible via the I<sup>2</sup>C interface.

When monitoring a voltage rail that has a nominal voltage larger than 2.5 V (internal reference) or 3.3 V (external reference), a resistor divider network is typically used. The design must ensure that the source impedance of that resistor network is not too high, because it causes the UCD9080 analog-to-digital converter (ADC) to take longer to perform the sample-and-hold conversion. The extended conversion time causes the frequency of the sampling of voltage rails to slow below 20 kHz.

Using a higher-valued resistor network lowers the overall power dissipation of the solution, which is desirable. In order to keep the source impedance low, a buffer circuit is typically used. The UCD9080 analog inputs require that a source impedance of less than 20 kΩ be used in order to maintain the high sampling rate of the voltages.

The UCD9080 allows specification of overvoltage threshold, undervoltage threshold, and out-of-regulation or glitch duration for each monitored rail.

Each voltage rail can also be marked so that it is not monitored, in which case all checks and alarm conditions are disabled.

### RAIL SHUTDOWN

Rail shutdown is the act of setting the EN<sub>x</sub> pin associated with that rail to a state which disables the power supply output. Each UCD9080 rail can be configured to shut down based on a monitored alarm event (sustained overvoltage, sustained undervoltage, or rail did not start) and in a configurable manner.

The options for rail shutdown are as follows:

- Ignore
- Log only
- Sequence
- Retry 1 time
- Retry 0 times

If the system does not care whether a monitored rail enters a sustained error condition, the UCD9080 can be configured to either ignore or log the error event and take no subsequent action.

The UCD9080 can also be configured to sequence the entire system in response to a sustained error condition. When the UCD9080 monitors an alarm event on the configured rail, UCD9080 RESET occurs (all ENx and GPOx outputs go to the high-impedance state for ~4–5 ms). Next, a sequence of all configured enables and GPOs occurs, as defined by the current sequencer configuration. Note that for this configuration, a shutdown according to the values in the UnsequenceTime register does not occur prior to UCD9080 RESET.

The UCD9080 can also be configured to attempt to restart a rail once in response to a sustained error condition. When the UCD9080 monitors an alarm event on a configured rail, the rail is momentarily disabled and then re-enabled. The rail remains enabled according to the RampTime register setting (time), and if the rail does not properly achieve regulation, the system (rail and dependent rails) is shut down as defined by the current sequencer configuration (UnsequenceTime register).

The last option that the UCD9080 supports is to shut down (if specified as a dependency) and disable (Retry 0 times) a configured rail in response to a sustained error condition. When the UCD9080 monitors an alarm event on the configured rail, the system (dependent rails and GPOs) is shut down as defined by the current sequencer configuration (UnsequenceTime register). Only rails and GPOs marked as dependencies of the configured rail are shut down. If there are no rails or GPO dependencies marked, the configured rail is just disabled in response to the sustained error condition.

Each UCD9080 ENx and GPOx output can be marked to sequence after shutdown (as defined by the current sequencer configuration) if specified as a dependency in the DependencyMasks register. For example, if rail 1 is configured to sequence after shutdown (RESEQ bit set), and rail 2 has rail 1 set in its dependency mask, then if/when rail 2 is shut down, rail 1 shuts down and the system resequences.

## BROWNOUT

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

## I<sup>2</sup>C INTERFACE

The UCD9080 power-supply sequencer has a 100-kHz, slave-mode I<sup>2</sup>C interface for communication with an I<sup>2</sup>C master. The I<sup>2</sup>C master uses this interface to configure and monitor the UCD9080.

### I<sup>2</sup>C Address Selection

The UCD9080 supports 7-bit I<sup>2</sup>C addressing. The UCD9080 selects an I<sup>2</sup>C address by sampling the logic level of the four digital inputs to the device (ADDR1–ADDR4) during the UCD9080 RESET interval. When the UCD9080 is released from RESET, the ADDR<sub>x</sub> logic levels are latched and the I<sup>2</sup>C address is assigned as shown in [Figure 8](#).

|        |        |        |                 |                 |                 |                     |
|--------|--------|--------|-----------------|-----------------|-----------------|---------------------|
| A7 = 1 | A6 = 1 | A5 = 0 | A4 = ADDR4/GPO4 | A3 = ADDR3/GPO3 | A2 = ADDR2/GPO2 | A1 = EN8/ADDR1/GPO1 |
|--------|--------|--------|-----------------|-----------------|-----------------|---------------------|

**Figure 8. I<sup>2</sup>C ADDRESS = 0x60–0x6F**

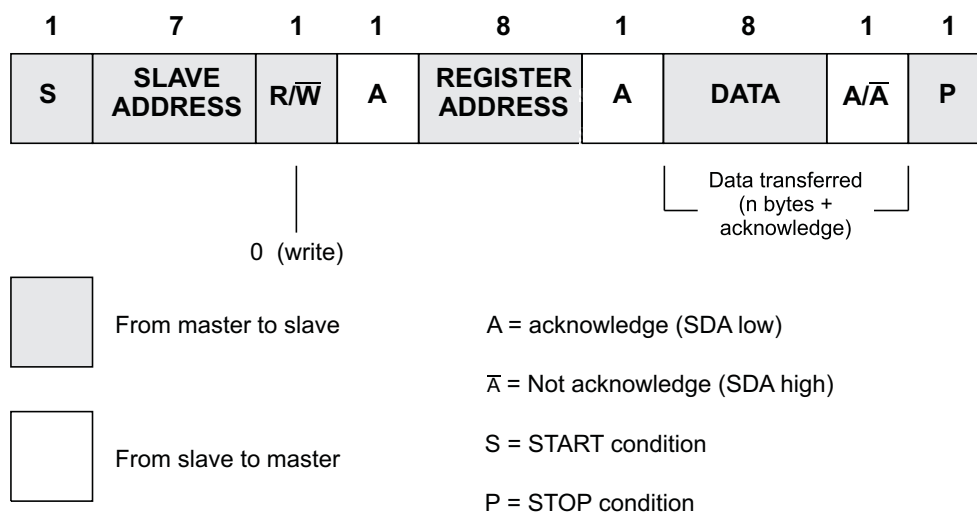
External pullup/pulldown resistors are required to configure the I<sup>2</sup>C address; the UCD9080 does not have internal bias resistors. Note that the 7-bit I<sup>2</sup>C address refers to the address bits only, not the read/write (8<sup>th</sup>) bit in the first byte of the I<sup>2</sup>C protocol. The base I<sup>2</sup>C address is 0x60 and the I<sup>2</sup>C general-call address (0x00) is not supported.

After the initialization process of the UCD9080 is complete, these four pins can be used as general-purpose outputs (GPOs). They can be programmed and sequenced as described in the [Configuring the UCD9080](#) section. GPO polarity must consider the external I<sup>2</sup>C address resistors as described in the [External Considerations for EN and GPO Pins](#) section.

### I<sup>2</sup>C Transactions

The UCD9080 can be configured and monitored via I<sup>2</sup>C memory-mapped registers. Registers that are configurable (can be written) via an I<sup>2</sup>C write operation are implemented using an I<sup>2</sup>C unidirectional data transfer, from the master to slave, with a stop bit between transactions.

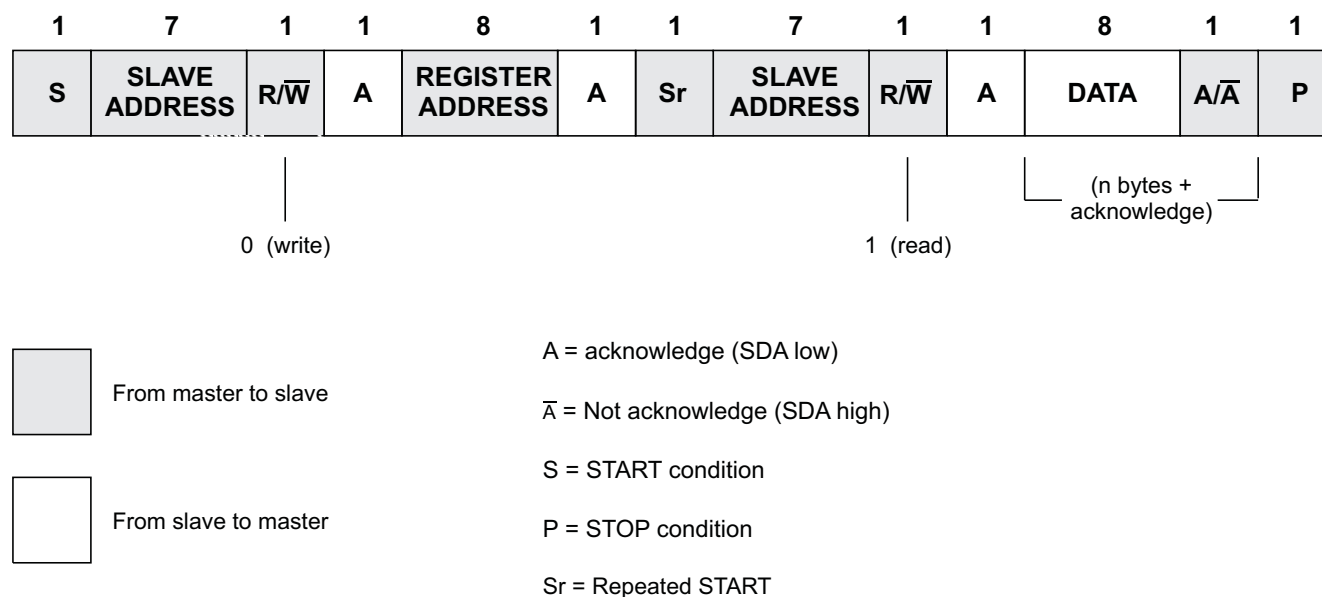
## I<sup>2</sup>C Unidirectional Transfer



**Figure 9. I<sup>2</sup>C Register Access With START/STOP**

Registers that can be read are implemented using an I<sup>2</sup>C read operation, which uses the I<sup>2</sup>C combined format that changes data direction during the transaction. This transaction uses an I<sup>2</sup>C repeated START during the direction change.

## I<sup>2</sup>C Combined Format



**Figure 10. I<sup>2</sup>C Register Access With Repeated START**

The UCD9080 also supports a feature that auto-increments the register address pointer for increased efficiency when accessing sequential blocks of data. It is not necessary to issue separate I<sup>2</sup>C transactions.

## CONFIGURING AND MONITORING THE UCD9080

The UCD9080 supports both configuration and monitoring using its I<sup>2</sup>C slave interface. A Microsoft Windows GUI is available for configuring and monitoring the UCD9080. See the *UCD9080 Power Supply Sequencer and Monitor EVM* user's guide ([SLVU184](#)).

For monitoring the sequencer, an I<sup>2</sup>C memory map allows an I<sup>2</sup>C host to perform memory-mapped reads (and in some cases writes) to obtain status information from the UCD9080. For instance, all rails can report their voltage through the I<sup>2</sup>C memory map. For information on which parameters are available via the I<sup>2</sup>C memory map, see the [Monitoring the UCD9080](#) section.

To change configuration parameters of the sequencer, a different mechanism is used. The entire set of configuration parameters must be written to the device at one time as one large transaction over the I<sup>2</sup>C interface to ensure that the configuration of the device is consistent at any given time. The process for configuring the UCD9080 is described in the [Configuring the UCD9080](#) section.

## MONITORING THE UCD9080

### Register Map

The UCD9080 allows all monitoring of the system through the I<sup>2</sup>C interface on the device. The following is the memory map of the supported registers in the system. The detail of each of these registers is given in the next section as well.

Note that the UCD9080 supports functionality to increment the I<sup>2</sup>C register address value automatically when a register is being accessed, to access blocks of like registers more efficiently. The following table also shows the amount that the register address is incremented for each register access.

| REGISTER NAME | ADDRESS | ACCESS | ADJUSTMENT AFTER ACCESS |
|---------------|---------|--------|-------------------------|
| RAIL1H        | 0x00    | r      | +1 (0x01)               |
| RAIL1L        | 0x01    | r      | +1 (0x02)               |
| RAIL2H        | 0x02    | r      | +1 (0x03)               |
| RAIL2L        | 0x03    | r      | +1 (0x04)               |
| RAIL3H        | 0x04    | r      | +1 (0x05)               |
| RAIL3L        | 0x05    | r      | +1 (0x06)               |
| RAIL4H        | 0x06    | r      | +1 (0x07)               |
| RAIL4L        | 0x07    | r      | +1 (0x08)               |
| RAIL5H        | 0x08    | r      | +1 (0x09)               |
| RAIL5L        | 0x09    | r      | +1 (0x0A)               |
| RAIL6H        | 0x0A    | r      | +1 (0x0B)               |
| RAIL6L        | 0x0B    | r      | +1 (0x0C)               |
| RAIL7H        | 0x0C    | r      | +1 (0x0D)               |
| RAIL7L        | 0x0D    | r      | +1 (0x0E)               |
| RAIL8H        | 0x0E    | r      | +1 (0x0F)               |
| RAIL8L        | 0x0F    | r      | –15 (0x00)              |
| ERROR1        | 0x20    | r      | +1 (0x21)               |
| ERROR2        | 0x21    | r      | +1 (0x22)               |
| ERROR3        | 0x22    | r      | +1 (0x23)               |
| ERROR4        | 0x23    | r      | +1 (0x24)               |
| ERROR5        | 0x24    | r      | +1 (0x25)               |
| ERROR6        | 0x25    | r      | –5 (0x20)               |
| STATUS        | 0x26    | r      | 0 (0x26)                |
| VERSION       | 0x27    | r      | 0 (0x27)                |
| RAILSTATUS1   | 0x28    | r      | +1 (0x29)               |
| RAILSTATUS2   | 0x29    | r      | –1 (0x28)               |
| FLASHLOCK     | 0x2E    | rw     | 0 (0x2E)                |
| RESTART       | 0x2F    | w      | 0 (0x2F)                |
| WADDR1        | 0x30    | rw     | +1 (0x31)               |
| WADDR2        | 0x31    | rw     | –1 (0x30)               |

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| REGISTER NAME | ADDRESS | ACCESS | ADJUSTMENT AFTER ACCESS |
|---------------|---------|--------|-------------------------|
| WDATA1        | 0x32    | rw     | +1 (0x33)               |
| WDATA2        | 0x33    | rw     | –1 (0x32)               |

## Register Descriptions

The following are the detailed descriptions of each of the UCD9080 I<sup>2</sup>C registers.

The following register bit conventions are used. Each register is shown with a key indicating the accessibility of each bit, and the initial condition after device initialization.

| KEY    | ACCESS                         |
|--------|--------------------------------|
| rw     | Read/write                     |
| r      | Read-only                      |
| r0     | Read as 0                      |
| r1     | Read as 1                      |
| w      | Write-only                     |
| w0     | Write as 0                     |
| w1     | Write as 1                     |
| rc     | Read clears bit after read     |
| rs     | Read sets bit after read       |
| -0, -1 | Condition after initialization |

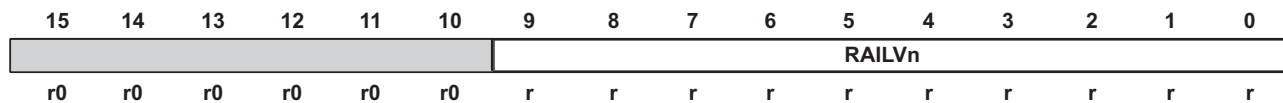
## RAIL

For each of eight voltage rails, the UCD9080 has two registers that contain the rolling average voltage for the associated rail as measured by the device. This average voltage is maintained in real-time by the UCD9080 and is calculated as the output of a 4-TAP FIR filter. There are two registers for each voltage rail. One holds the least-significant 8 bits of the voltage and the other the most-significant 2 bits of the voltage. This is shown in the following table.

| Register Name | Address | Register Contents       |
|---------------|---------|-------------------------|
| RAIL1H        | 0x00    | RAIL1 voltage, bits 9:8 |
| RAIL1L        | 0x01    | RAIL1 voltage, bits 7:0 |
| RAIL2H        | 0x02    | RAIL2 voltage, bits 9:8 |
| RAIL2L        | 0x03    | RAIL2 voltage, bits 7:0 |
| RAIL3H        | 0x04    | RAIL3 voltage, bits 9:8 |
| RAIL3L        | 0x05    | RAIL3 voltage, bits 7:0 |
| RAIL4H        | 0x06    | RAIL4 voltage, bits 9:8 |
| RAIL4L        | 0x07    | RAIL4 voltage, bits 7:0 |
| RAIL5H        | 0x08    | RAIL5 voltage, bits 9:8 |
| RAIL5L        | 0x09    | RAIL5 voltage, bits 7:0 |
| RAIL6H        | 0x0A    | RAIL6 voltage, bits 9:8 |
| RAIL6L        | 0x0B    | RAIL6 voltage, bits 7:0 |
| RAIL7H        | 0x0C    | RAIL7 voltage, bits 9:8 |
| RAIL7L        | 0x0D    | RAIL7 voltage, bits 7:0 |
| RAIL8H        | 0x0E    | RAIL8 voltage, bits 9:8 |
| RAIL8L        | 0x0F    | RAIL8 voltage, bits 7:0 |

A rail voltage is read with a 16-bit access. The auto-increment feature of the UCD9080 allows multiple rail voltages to be read with a single access.

A rail voltage is provided as a 10-bit value in an unsigned format:



The following formulas can be used to calculate the actual measured rail voltage:

Without external voltage divider:

$$V_{\text{RAILn}} = \frac{\text{RAILVn}}{1024} \times V_{\text{REF}} \quad (1)$$

With external voltage divider:

$$V_{\text{RAILn}} = \frac{\text{RAILVn}}{1024} \times V_{\text{REF}} \times \frac{R_{\text{PULLDOWN}} + R_{\text{PULLUP}}}{R_{\text{PULLDOWN}}} \quad (2)$$

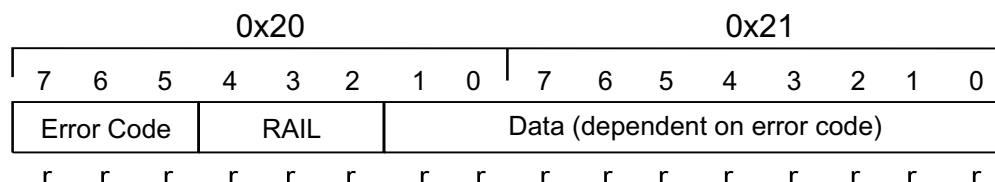
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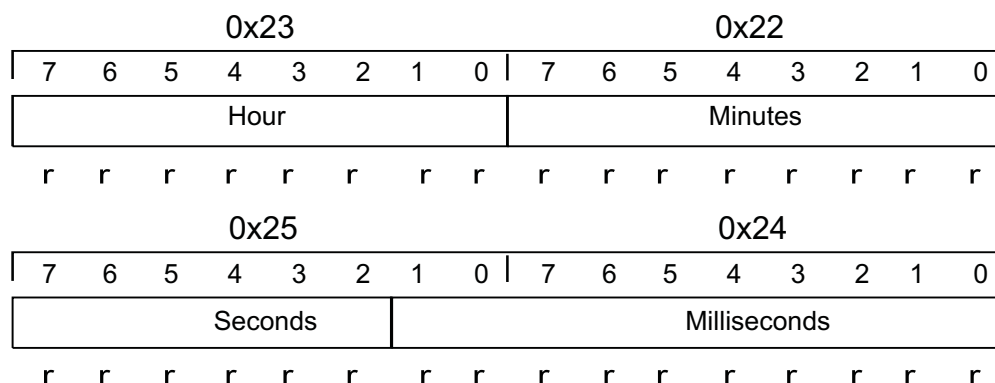
## ERROR

Error conditions are logged by the UCD9080 and are accessible to the user via reading the ERROR register. This is a 6-byte register with the following format:



| RAIL  | Meaning                         | Rail #(n) – 1, RAIL = 0 through 7 |
|-------|---------------------------------|-----------------------------------|
| 0 0 0 | Null alarm                      | 0x0000                            |
| 0 0 1 | Supply did not start            | Average voltage on rail           |
| 0 1 0 | Sustained overvoltage detected  | Average voltage on rail           |
| 0 1 1 | Sustained undervoltage detected | Average voltage on rail           |
| 1 0 0 | Overvoltage glitch detected     | Glitch voltage level on rail      |
| 1 0 1 | Undervoltage glitch detected    | Glitch voltage level on rail      |
| 1 1 0 | Reserved                        | Reserved                          |
| 1 1 1 | Reserved                        | Reserved                          |

**NOTE:** When error code = *Null Alarm*, then the Hours, Minutes, Seconds, and Milliseconds fields are zero.



Error conditions encountered during processing post error logs to this register with some exceptions. This register is internally managed as a FIFO (with a depth of 8). Errors are posted to the FIFO as they occur, and read out of the FIFO via I<sup>2</sup>C access. Due to the unknown latency of host extraction of the FIFO data, the UCD9080 only posts to the FIFO if there is room to write. There is no real-time impact to processing in the UCD9080 if this FIFO is full and cannot be posted to.

The values in registers 0x22 through 0x25 are reset to a value of 0 during UCD9080 RESET.

## STATUS

STATUS is an 8-bit read-only register. This register provides real-time status information about the state of the UCD9080. The following bits are defined.

| 7        | 6    | 5        | 4   | 3   | 2   | 1               | 0 |
|----------|------|----------|-----|-----|-----|-----------------|---|
| IICERROR | RAIL | NVERRLOG |     |     |     | Register Status |   |
| rc-0     | rc-0 | r        | r-0 | r-0 | r-0 | rc-0            |   |

| IICERROR Meaning |                                     |
|------------------|-------------------------------------|
| 0                | No I <sup>2</sup> C PHY layer error |
| 1                | I <sup>2</sup> C PHY layer error    |

| RAIL | Meaning               |
|------|-----------------------|
| 0    | No RAIL error pending |
| 1    | RAIL error pending    |

**NVERRLOG: Reserved**

| Register Status | Meaning            |
|-----------------|--------------------|
| 00              | No error           |
| 01              | Invalid address    |
| 10              | Read access error  |
| 11              | Write access error |

Reading of the STATUS register clears the register except for the NVERRLOG bit, which is maintained until the device is reset. Descriptions of the different errors follow.

The IICERROR bit is set when an I<sup>2</sup>C access fails. This is most often a case where the user has accessed an invalid address or performed an illegal number of operations for a given register (for example, reading 3 bytes from a 2-byte register). In the event of an I<sup>2</sup>C error when IICERROR is set, bits 1:0 of the STATUS register further define the nature of the error as shown in the preceding figure.

The RAIL error bit is set to alert the user to an issue with one of the voltage rails. When this bit is set, the user is advised to query the RAILSTATUS register to further ascertain which RAIL input(s) have an issue. The user may then query the ERROR registers to get further information about the nature of the error condition.

The NVERRLOG bit is reserved for future use.

When the IICERROR bit is set, the register status bits provide further information about the type of I<sup>2</sup>C error that has been detected, as indicated previously.

## RAILSTATUS

The RAILSTATUS1 and RAILSTATUS2 registers are two 8-bit read-only registers that provide a bit mask to represent the error status of the rails as indicated in the following diagram. The RAILSTATUS1 register is reserved.

| 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|------|------|------|------|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
|      |      |      |      |      |      |      |      | RAIL8 | RAIL7 | RAIL6 | RAIL5 | RAIL4 | RAIL3 | RAIL2 | RAIL1 |
| rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0  | rc-0  | rc-0  | rc-0  | rc-0  | rc-0  | rc-0  | rc-0  |

| RAILn | Meaning                    |
|-------|----------------------------|
| 0     | No alarm pending for RAILn |
| 1     | Alarm pending for RAILn    |

Bits 15:8 are RAILSTATUS1 and bits 7:0 are RAILSTATUS2. These are read as two 8-bit registers or as a single 16-bit register.

If a bit is set in these registers, then the ERROR register is read to further ascertain the specific error. Bits in the RAILSTATUS1 and RAILSTATUS2 registers are cleared when read.

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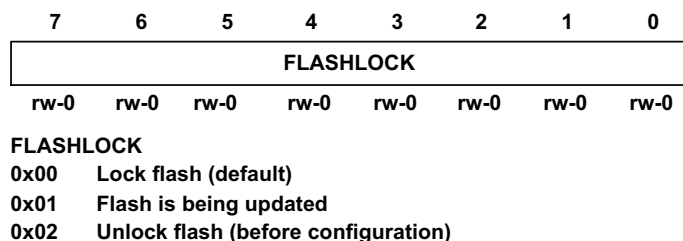
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## FLASHLOCK

The FLASHLOCK register is used to lock and unlock the configuration memory on the UCD9080 when updating the configuration. The [Configuring the UCD9080](#) section details this process.

The format for the FLASHLOCK register is as follows:



## RESTART

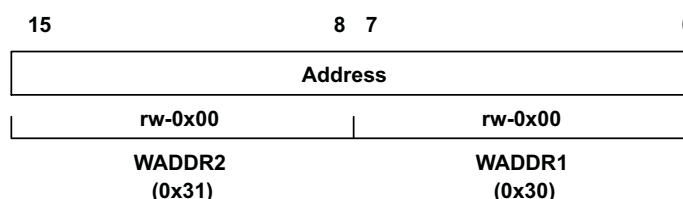
The RESTART register provides the capability for the I<sup>2</sup>C host to force a re-initialization and restart of the UCD9080. This is an 8-bit register, and when a value of 0 is written to the register, the UCD9080 is restarted and the rails are resequenced.

Note that in order to respond to this I<sup>2</sup>C request properly, there is a 50-μs delay before the system is restarted, so that the I<sup>2</sup>C ACK can take place.

## WADDR and WDATA

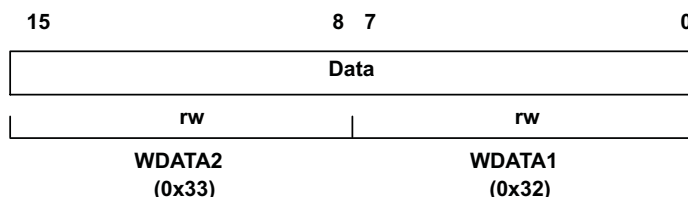
In order to update the configuration on the UCD9080, four registers are provided: WADDR2 (address bits 8–15), WADDR1 (address bits 0–7), WDATA2 (data bits 8–15), and WDATA1 (data bits 0–7). WADDR2 and WADDR1 specify the 16-bit memory address and WDATA2 and WDATA1 specify the 16-bit data written to or read from that memory address.

The format for the WADDR register is as follows:



To set the address of the memory that will be accessed, write the LSB of the address to the WADDR1 register and the MSB of the address to the WADDR2 register. For example, to write the address 0x1234 to the device, set WADDR1 = 0x34 and WADDR2 = 0x12. Note that because these addresses support the auto-increment feature, the user can perform a single 16-bit write to WADDR1 to write the entire address.

The format for the WDATA register is as follows:



To set the value of the data that will be written, write the LSB of the data to the WDATA1 register and the MSB of the data to the WDATA2 register. For example, to write the data 0xBEEF to the device, set WDATA1 = 0xEF and WDATA2 = 0xBE. Note that because these addresses support the auto-increment feature, the user can perform a single 16-bit write to WDATA1 to write the entire data. To read the value of the data at the specified address, read the LSB from WDATA1 and the MSB from WDATA2.

These registers are used for updating the UCD9080 configuration as explained in the [Configuring the UCD9080](#) section.

## CONFIGURING THE UCD9080

The UCD9080 has many different configurable parameters, such as sequencing policies, shutdown policies and dependency masks. The UCD9080 can configure all of its parameters via the I<sup>2</sup>C interface while the device is operational. Sequencing, shutdown, and rail monitoring are not performed during device configuration time.

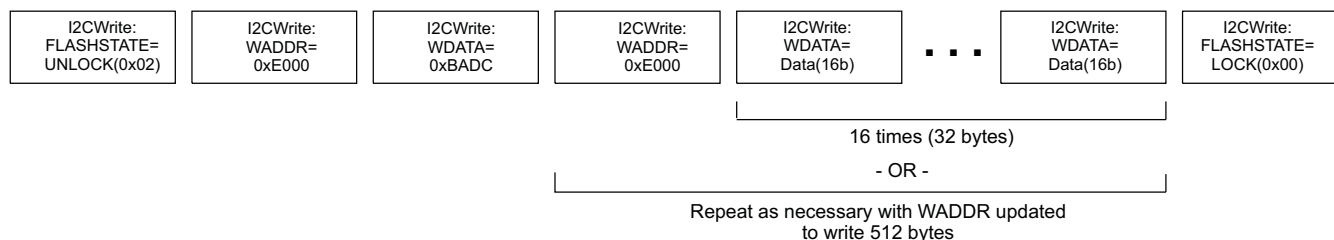
### NOTE:

During runtime, if the UCD9080 is configured, there is a delay in voltage monitoring while the new configuration parameters are applied to the device.

To configure the UCD9080, a large block of configuration information is sent to the device via the I<sup>2</sup>C interface. This block is 512 bytes and contains all the configuration information that the device requires for any function of the UCD9080.

This 512-byte block of configuration information is sent to the device in multiple segments. The segment size can range from 2 to 32 bytes at one time, and must be a power of 2 bytes. That is, a master can send 256 2-byte segments or 32 16-byte segments, and so on. All the segments must be sent back-to-back in the proper sequence, and this operation must be completed by sending the last segment so that the last byte of the 512-byte block is written. If this is not done, the UCD9080 is in an unknown state and does not function as designed.

The process for sending the configuration information to the UCD9080 is as shown in [Figure 11](#):



**Figure 11. Configuration Information**

As shown in [Figure 11](#), the process for updating the configuration of the UCD9080 is as follows:

1. Unlock flash memory by writing the FLASHLOCK register with a value of 0x02.
2. Write the address of the configuration section of memory (WADDR = 0xE000).
3. Write the constant 0xBADC to update memory (WDATA = 0xBADC).
4. Write the address of the configuration section of memory again (WADDR = 0xE000).

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5. Write the data (WDATA = <varies>). Repeat steps 4 and 5 as necessary, depending on the data segment size used, to write 512 bytes. Increment the address as necessary.
6. Lock flash memory after the last byte of the last segment is written by writing the FLASHLOCK register with a value of 0x00.

At the conclusion of this process, the configuration of the UCD9080 is updated with the configuration changes, as represented by the values from the data segments. The UCD9080 can then be reset by writing the RESTART register with a value of 0. The new sequencer configuration then starts.

The memory map for the 512-byte configuration segment is defined in the [Configuration Parameters Detail](#) section.

## User Data

User data (128 bytes) can be stored in the UCD9080 user-data area at memory location 0x1080 to 0x10FF. Access to the user-data area occurs by following the procedure outlined in the [Configuring the UCD9080](#) section.

## Configuration Parameters Memory Map

[Table 2](#) shows the 512-byte configuration parameters memory map. User-configurable bytes in bold are described in the [Configuration Parameters Detail](#) section; adjacent groups of user-configurable bytes are distinguished in the table by alternating use of italics. **Other bytes must remain exactly as shown in [Table 2](#).**

**Table 2. Configuration Parameters Memory Map**

| ADDRESS | +0          | +1          | +2          | +3          | +4          | +5          | +6          | +7          |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 0xE000  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE008  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE010  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE018  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE020  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE028  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE030  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE038  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE040  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE048  | 0xFF        | 0xFF        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE050  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE058  | 0xFF        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0xC0        | 0x02        |
| 0xE060  | 0x00        | 0x00        | 0x00        | 0x0F        | 0x00        | 0x02        | 0x00        | 0x02        |
| 0xE068  | 0xFF        | 0x0F        | 0x00        | 0x50        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE070  | 0x00        | 0x00        | 0xC0        | 0x20        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE078  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0xA8        | 0xDC        | 0xBA        |
| 0xE080  | <b>0x50</b> | <b>0x51</b> | <b>0x52</b> | <b>0x53</b> | <b>0x54</b> | <b>0x55</b> | <b>0x56</b> | <b>0x57</b> |
| 0xE088  | <b>0x00</b> | <b>0x49</b> | <b>0x4A</b> | <b>0x4B</b> | <b>0x01</b> | <b>0x00</b> | <b>0x01</b> | <b>0x04</b> |
| 0xE090  | <b>0x01</b> | <b>0x04</b> | <b>0x05</b> | <b>0x06</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> |
| 0xE098  | <b>0x05</b> | <b>0xE0</b> | <b>0x05</b> | <b>0xA0</b> | <b>0x32</b> | <b>0xE0</b> | <b>0x33</b> | <b>0xE0</b> |
| 0xE0A0  | <b>0x33</b> | <b>0xE0</b> | <b>0x35</b> | <b>0xE0</b> | <b>0x35</b> | <b>0xE0</b> | <b>0x00</b> | <b>0x00</b> |
| 0xE0A8  | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> |
| 0xE0B0  | 0xFF        | 0x7F        | 0xFF        | 0x7F        | 0xFF        | 0x7F        | 0xFF        | 0x7F        |
| 0xE0B8  | 0xFF        | 0x7F        | 0xFF        | 0x7F        | 0xFF        | 0x7F        | 0xFF        | 0x7F        |
| 0xE0C0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE0C8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE0D0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE0D8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE0E0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |

**Table 2. Configuration Parameters Memory Map (continued)**

| ADDRESS | +0          | +1          | +2          | +3          | +4          | +5          | +6          | +7          |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 0xE0E8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE0F0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE0F8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE100  | <b>0x7F</b> | <b>0x00</b> | <b>0x01</b> | <b>0x00</b> | <b>0x02</b> | <b>0x00</b> | <b>0x04</b> | <b>0x00</b> |
| 0xE108  | <b>0x08</b> | <b>0x00</b> | <b>0x10</b> | <b>0x00</b> | <b>0x20</b> | <b>0x00</b> | <b>0x40</b> | <b>0x00</b> |
| 0xE110  | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> |
| 0xE118  | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> |
| 0xE120  | <b>0x00</b> | <b>0x04</b> | <b>0x00</b> | <b>0x04</b> | <b>0x00</b> | <b>0x04</b> | <b>0x00</b> | <b>0x04</b> |
| 0xE128  | <b>0x00</b> | <b>0x04</b> | <b>0x00</b> | <b>0x04</b> | <b>0x00</b> | <b>0x04</b> | <b>0x00</b> | <b>0x04</b> |
| 0xE130  | <b>0xA0</b> | <b>0x0F</b> | <b>0xA0</b> | <b>0x0F</b> | <b>0xA0</b> | <b>0x0F</b> | <b>0xA0</b> | <b>0x0F</b> |
| 0xE138  | <b>0xA0</b> | <b>0x0F</b> | <b>0xA0</b> | <b>0x0F</b> | <b>0xA0</b> | <b>0x0F</b> | <b>0xA0</b> | <b>0x0F</b> |
| 0xE140  | <b>0x10</b> | <b>0x00</b> | <b>0x10</b> | <b>0x00</b> | <b>0x10</b> | <b>0x00</b> | <b>0x10</b> | <b>0x00</b> |
| 0xE148  | <b>0x10</b> | <b>0x00</b> | <b>0x10</b> | <b>0x00</b> | <b>0x10</b> | <b>0x00</b> | <b>0x10</b> | <b>0x00</b> |
| 0xE150  | <b>0xFF</b> | <b>0xC0</b> | <b>0xFF</b> | <b>0xC1</b> | <b>0xFF</b> | <b>0xC2</b> | <b>0xFF</b> | <b>0xC3</b> |
| 0xE158  | <b>0xFF</b> | <b>0xC4</b> | <b>0xFF</b> | <b>0xC5</b> | <b>0xFF</b> | <b>0xC6</b> | <b>0xFF</b> | <b>0xC7</b> |
| 0xE160  | <b>0x00</b> | <b>0x00</b> | <b>0x00</b> | <b>0xC0</b> | <b>0x00</b> | <b>0xC0</b> | <b>0x00</b> | <b>0xC0</b> |
| 0xE168  | <b>0x04</b> | <b>0x20</b> | <b>0x08</b> | <b>0x20</b> | <b>0x04</b> | <b>0x18</b> | <b>0x02</b> | <b>0x18</b> |
| 0xE170  | <b>0x08</b> | <b>0x18</b> | <b>0x10</b> | <b>0x18</b> | <b>0x20</b> | <b>0x18</b> | <b>0x10</b> | <b>0x20</b> |
| 0xE178  | <b>0x00</b> | <b>0x20</b> | <b>0x20</b> | <b>0x20</b> | <b>0x40</b> | <b>0x20</b> | <b>0x80</b> | <b>0x20</b> |
| 0xE180  | <b>0x00</b> | <b>0x00</b> | 0x00        | 0x04        | 0x94        | 0x02        | <b>0xF2</b> | <b>0x08</b> |
| 0xE188  | 0x10        | 0x03        | 0x05        | 0xC0        | 0x40        | 0x00        | <b>0xFF</b> | <b>0x08</b> |
| 0xE190  | 0x05        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE198  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1A0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1A8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1B0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1B8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1C0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1C8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1D0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1D8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1E0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1E8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1F0  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |
| 0xE1F8  | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        | 0x00        |

## CONFIGURATION PARAMETERS DETAIL

The following sections detail the format and meaning of the configuration parameters from the *Configuration Parameters Memory Map*, [Table 2](#).

### SequenceEventParameters

The SequenceEventParameters field in the configuration parameters specifies the rail identification, monitoring status, and sequencing options for each rail. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                                                      |
|---------|------|---------------|------------------------------------------------------------------|
| 0xE080  | 1    | 0x50          | Rail 1 identification, monitoring status and sequencing options  |
| 0xE081  | 1    | 0x51          | Rail 2 identification, monitoring status, and sequencing options |
| 0xE082  | 1    | 0x52          | Rail 3 identification, monitoring status, and sequencing options |
| 0xE083  | 1    | 0x53          | Rail 4 identification, monitoring status, and sequencing options |
| 0xE084  | 1    | 0x54          | Rail 5 identification, monitoring status, and sequencing options |
| 0xE085  | 1    | 0x55          | Rail 6 identification, monitoring status, and sequencing options |
| 0xE086  | 1    | 0x56          | Rail 7 identification, monitoring status, and sequencing options |
| 0xE087  | 1    | 0x57          | Rail 8 identification, monitoring status, and sequencing options |
| 0xE088  | 1    | 0x00          | GPO1 identification, sequencing options                          |
| 0xE089  | 1    | 0x49          | GPO2 identification, sequencing options                          |
| 0xE08A  | 1    | 0x4A          | GPO3 identification, sequencing options                          |
| 0xE08B  | 1    | 0x4B          | GPO4 identification, sequencing options                          |

The format of each register is as follows:

|        |   |   |     |          |   |   |   |
|--------|---|---|-----|----------|---|---|---|
| 7      | 6 | 5 | 4   | 3        | 2 | 1 | 0 |
| ENABLE |   | 0 | MON | RAIL/GPO |   |   |   |

#### RAIL

Rail #(n) – 1, RAIL = 0 through 7

#### GPO

GPO #(n) + 7, GPO = 8, 9, 0xA, 0xB

#### MON

##### Meaning

- 0 Do not monitor rail status (for event sequencing of GPOs)
- 1 Monitor rail status

#### ENABLE

##### Meaning

- 00 Sequence is disabled
- 01 Sequence is triggered after delay after sequence event
- 10 Sequence is triggered after parent rail achieves voltage level
- 11 Sequence is triggered after delay after parent rail achieves voltage regulation

## SequenceEventLink

The SequenceEventLink field allows a parent rail (monitored input) to be specified for each ENx and GPOx output. The RESEQ bit (sequence after shutdown) allows an enable or GPO to be marked to sequence the system (as defined by the current sequencer configuration) after it has been shut down. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                                            |
|---------|------|---------------|--------------------------------------------------------|
| 0xE08C  | 1    | 0x01          | Rail 1 parent rail identifier and resequence indicator |
| 0xE08D  | 1    | 0x00          | Rail 2 parent rail identifier and resequence indicator |
| 0xE08E  | 1    | 0x01          | Rail 3 parent rail identifier and resequence indicator |
| 0xE08F  | 1    | 0x04          | Rail 4 parent rail identifier and resequence indicator |
| 0xE090  | 1    | 0x01          | Rail 5 parent rail identifier and resequence indicator |
| 0xE091  | 1    | 0x04          | Rail 6 parent rail identifier and resequence indicator |
| 0xE092  | 1    | 0x05          | Rail 7 parent rail identifier and resequence indicator |
| 0xE093  | 1    | 0x06          | Rail 8 parent rail identifier and resequence indicator |
| 0xE094  | 1    | 0x00          | GPO1 parent rail identifier and resequence indicator   |
| 0xE095  | 1    | 0x00          | GPO2 parent rail identifier and resequence indicator   |
| 0xE096  | 1    | 0x00          | GPO3 parent rail identifier and resequence indicator   |
| 0xE097  | 1    | 0x00          | GPO4 parent rail identifier and resequence indicator   |

The format of each register is as follows:

|   |       |   |   |           |   |   |   |
|---|-------|---|---|-----------|---|---|---|
| 7 | 6     | 5 | 4 | 3         | 2 | 1 | 0 |
| 0 | RESEQ | 0 | 0 | PARENTAIL |   |   |   |

**RESEQ**
**Meaning**

|   |                                 |
|---|---------------------------------|
| 0 | Do not sequence after shutdown. |
| 1 | Sequence after shutdown.        |

**PARENTAIL**
**Meaning**

|        |                                                               |
|--------|---------------------------------------------------------------|
| 0x0000 | Sequence is dependent on RAIL1 achieving the specified event. |
| 0x0001 | Sequence is dependent on RAIL2 achieving the specified event. |
| 0x0010 | Sequence is dependent on RAIL3 achieving the specified event. |
| 0x0011 | Sequence is dependent on RAIL4 achieving the specified event. |
| 0x0100 | Sequence is dependent on RAIL5 achieving the specified event. |
| 0x0101 | Sequence is dependent on RAIL6 achieving the specified event. |
| 0x0110 | Sequence is dependent on RAIL7 achieving the specified event. |
| 0x0111 | Sequence is dependent on RAIL8 achieving the specified event. |

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## SequenceEventData

The SequenceEventData field in the configuration parameters specifies the rail and GPO sequencing and shutdown parameters. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                               |
|---------|------|---------------|-------------------------------------------|
| 0xE098  | 2    | 0xE005        | Rail 1 sequencing and shutdown parameters |
| 0xE09A  | 2    | 0xA005        | Rail 2 sequencing and shutdown parameters |
| 0xE09C  | 2    | 0xE032        | Rail 3 sequencing and shutdown parameters |
| 0xE09E  | 2    | 0xE033        | Rail 4 sequencing and shutdown parameters |
| 0xE0A0  | 2    | 0xE033        | Rail 5 sequencing and shutdown parameters |
| 0xE0A2  | 2    | 0xE035        | Rail 6 sequencing and shutdown parameters |
| 0xE0A4  | 2    | 0xE035        | Rail 7 sequencing and shutdown parameters |
| 0xE0A6  | 2    | 0x0000        | Rail 8 sequencing and shutdown parameters |
| 0xE0A8  | 2    | 0x0000        | GPO1 sequencing and shutdown parameters   |
| 0xE0AA  | 2    | 0x0000        | GPO2 sequencing and shutdown parameters   |
| 0xE0AC  | 2    | 0x0000        | GPO3 sequencing and shutdown parameters   |
| 0xE0AE  | 2    | 0x0000        | GPO4 sequencing and shutdown parameters   |

The format for each register is as follows. The value in the ENABLE field of the SequenceEventParameters register determines the measure represented by the value in the RAILDATA field of the SequenceEventData register.



| SEQPARAM | Meaning       | ENABLE<br>(SequenceEventParameters) | RAILDATA Meaning                      |
|----------|---------------|-------------------------------------|---------------------------------------|
| 000      | Log only      |                                     |                                       |
| 001      | Sequence      | 01                                  | Delay (in units of ms)                |
| 010      | Reserved      | 10                                  | Voltage (in units of Vref/1024 volts) |
| 011      | Reserved      | 11                                  | Delay (in units of ms)                |
| 100      | Reserved      |                                     |                                       |
| 101      | Retry 1 times |                                     |                                       |
| 110      | Retry 0 times |                                     |                                       |
| 111      | Reserved      |                                     |                                       |

## DependencyMasks

The DependencyMasks field in the configuration parameters defines the rail dependency masks used for rail and GPO shutdown. This mask represents the set of other rails and GPOs that should be shut down when this rail shuts down. Note that because only rails are monitored, the table only has entries for the shutdown of rails. In the dependency mask itself, there are bits that allow for GPO shutdown.

The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                |
|---------|------|---------------|----------------------------|
| 0xE100  | 2    | 0x007F        | Dependency mask for rail 1 |
| 0xE102  | 2    | 0x0001        | Dependency mask for rail 2 |
| 0xE104  | 2    | 0x0002        | Dependency mask for rail 3 |
| 0xE106  | 2    | 0x0004        | Dependency mask for rail 4 |
| 0xE108  | 2    | 0x0008        | Dependency mask for rail 5 |
| 0xE10A  | 2    | 0x0010        | Dependency mask for rail 6 |
| 0xE10C  | 2    | 0x0020        | Dependency mask for rail 7 |
| 0xE10E  | 2    | 0x0040        | Dependency mask for rail 8 |

The format for each register is as follows:

|    |    |    |    |      |      |      |      |       |       |       |       |       |       |       |       |
|----|----|----|----|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| 15 | 14 | 13 | 12 | 11   | 10   | 9    | 8    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| 0  | 0  | 0  | 0  | GPO4 | GPO3 | GPO2 | GPO1 | RAIL8 | RAIL7 | RAIL6 | RAIL5 | RAIL4 | RAIL3 | RAIL2 | RAIL1 |

### RAILn or GPOn Meaning

- 0 Shutdown of this rail does not shut down RAILn or GPOn.
- 1 Shutdown of this rail shuts down RAILn or GPOn.

## UnderVoltageThresholds

The UnderVoltageThresholds field in the configuration parameters specifies each rail undervoltage threshold that is used when monitoring this rail. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                       |
|---------|------|---------------|-----------------------------------|
| 0xE110  | 2    | 0x0000        | Undervoltage threshold for rail 8 |
| 0xE112  | 2    | 0x0000        | Undervoltage threshold for rail 7 |
| 0xE114  | 2    | 0x0000        | Undervoltage threshold for rail 6 |
| 0xE116  | 2    | 0x0000        | Undervoltage threshold for rail 5 |
| 0xE118  | 2    | 0x0000        | Undervoltage threshold for rail 4 |
| 0xE11A  | 2    | 0x0000        | Undervoltage threshold for rail 3 |
| 0xE11C  | 2    | 0x0000        | Undervoltage threshold for rail 2 |
| 0xE11E  | 2    | 0x0000        | Undervoltage threshold for rail 1 |

The format for each register is as follows:

|    |    |    |    |    |      |   |   |   |   |   |   |   |   |   |   |
|----|----|----|----|----|------|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0  | 0  | 0  | 0  | 0  | Vraw |   |   |   |   |   |   |   |   |   |   |

The voltage conversion is dependent upon the configured voltage reference, and the pullup/pulldown resistors used on the board for each rail. The voltage reference is selected as either 2.5 V (internal) or V<sub>CC</sub> (external). The formula to convert the desired rail UnderVoltageThreshold to Vraw follows:

Without external rail voltage divider:

$$V_{\text{raw}} = \frac{1024 \times V_{\text{RAILUV}}}{V_{\text{REF}}} \quad (3)$$

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With external rail voltage divider:

$$V_{\text{raw}} = \frac{1024 \times V_{\text{RAILUV}}}{V_{\text{REF}}} \times \frac{R_{\text{PULLDOWN}}}{R_{\text{PULLDOWN}} + R_{\text{PULLUP}}} \quad (4)$$

### OverVoltageThresholds

The OverVoltageThresholds field in the configuration parameters specifies each rail overvoltage threshold that is used when monitoring this rail. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                      |
|---------|------|---------------|----------------------------------|
| 0xE120  | 2    | 0x0400        | Overvoltage threshold for rail 8 |
| 0xE122  | 2    | 0x0400        | Overvoltage threshold for rail 7 |
| 0xE124  | 2    | 0x0400        | Overvoltage threshold for rail 6 |
| 0xE126  | 2    | 0x0400        | Overvoltage threshold for rail 5 |
| 0xE128  | 2    | 0x0400        | Overvoltage threshold for rail 4 |
| 0xE12A  | 2    | 0x0400        | Overvoltage threshold for rail 3 |
| 0xE12C  | 2    | 0x0400        | Overvoltage threshold for rail 2 |
| 0xE12E  | 2    | 0x0400        | Overvoltage threshold for rail 1 |

The format for each register is as follows:

|    |    |    |    |    |      |   |   |   |   |   |   |   |   |   |   |
|----|----|----|----|----|------|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0  | 0  | 0  | 0  | 0  | Vraw |   |   |   |   |   |   |   |   |   |   |

The voltage conversion is dependent upon the configured voltage reference, and the pullup/pulldown resistors used on the board for each rail. The voltage reference is selected as either 2.5 V (internal) or V<sub>CC</sub> (external). The formula to convert the desired rail OverVoltageThreshold to Vraw follows:

Without external rail voltage divider:

$$V_{\text{raw}} = \frac{1024 \times V_{\text{RAILOV}}}{V_{\text{REF}}} \quad (5)$$

With external voltage divider:

$$V_{\text{raw}} = \frac{1024 \times V_{\text{RAILOV}}}{V_{\text{REF}}} \times \frac{R_{\text{PULLDOWN}}}{R_{\text{PULLDOWN}} + R_{\text{PULLUP}}} \quad (6)$$

### RampTime

The RampTime field in the configuration parameters specifies the maximum amount of time for each rail to achieve regulation. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                          |
|---------|------|---------------|--------------------------------------|
| 0xE130  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 1 |
| 0xE132  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 2 |
| 0xE134  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 3 |
| 0xE136  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 4 |
| 0xE138  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 5 |
| 0xE13A  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 6 |
| 0xE13C  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 7 |
| 0xE13E  | 2    | 0x0FA0        | Maximum voltage ramp time for rail 8 |

|    |    |    |    |          |    |   |   |   |   |   |   |   |   |   |   |
|----|----|----|----|----------|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11       | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0  | 0  | 0  | 0  | RAMPTIME |    |   |   |   |   |   |   |   |   |   |   |

RAMPTIME = RAILn RailTime (in units of ms).

## OutOfRegulationWidth

The OutOfRegulationWidth field in the configuration parameters specifies the maximum amount of time that the rail is allowed to be out of regulation before an error is declared (glitch duration). The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                                                                  |
|---------|------|---------------|------------------------------------------------------------------------------|
| 0xE140  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 1 |
| 0xE142  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 2 |
| 0xE144  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 3 |
| 0xE146  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 4 |
| 0xE148  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 5 |
| 0xE14A  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 6 |
| 0xE14C  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 7 |
| 0xE14E  | 2    | 0x0010        | The out-of-regulation duration permissible without flagging error for rail 8 |

The contents of this register are as follows:

|    |    |    |    |      |    |   |   |   |   |   |   |   |   |   |   |
|----|----|----|----|------|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11   | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0  | 0  | 0  | 0  | OORW |    |   |   |   |   |   |   |   |   |   |   |

OORW = RAILn out-of-regulation glitch width (in units of 1/10 ms).

## UnsequenceTime

The UnsequenceTime field in the configuration parameters specifies the amount of time that each rail should delay before unsequencing. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                 |
|---------|------|---------------|-----------------------------|
| 0xE150  | 2    | 0xC0FF        | Unsequence delay for rail 1 |
| 0xE152  | 2    | 0xC1FF        | Unsequence delay for rail 2 |
| 0xE154  | 2    | 0xC2FF        | Unsequence delay for rail 3 |
| 0xE156  | 2    | 0xC3FF        | Unsequence delay for rail 4 |
| 0xE158  | 2    | 0xC4FF        | Unsequence delay for rail 5 |
| 0xE15A  | 2    | 0xC5FF        | Unsequence delay for rail 6 |
| 0xE15C  | 2    | 0xC6FF        | Unsequence delay for rail 7 |
| 0xE15E  | 2    | 0xC7FF        | Unsequence delay for rail 8 |
| 0xE160  | 2    | 0x0000        | Unsequence delay for GPO1   |
| 0xE162  | 2    | 0xC000        | Unsequence delay for GPO2   |
| 0xE164  | 2    | 0xC000        | Unsequence delay for GPO3   |
| 0xE166  | 2    | 0xC000        | Unsequence delay for GPO4   |

The contents of this register are as follows:

|              |    |    |    |        |    |   |   |   |   |   |   |   |   |   |   |
|--------------|----|----|----|--------|----|---|---|---|---|---|---|---|---|---|---|
| 15           | 14 | 13 | 12 | 11     | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COPYSEQPARAM |    |    | 0  | USTIME |    |   |   |   |   |   |   |   |   |   |   |

COPYSEQPARAM = Copy SEQPARAM bit value  
(bits 15:13) in SequenceEvent Data register

USTIME = RAILn UnsequenceTime (in units of ms).

# UCD9080

SLVS692E–SEPTEMBER 2006–REVISED MAY 2008

[www.ti.com](http://www.ti.com)

## EnablePolarity

The EnablePolarity field in the configuration parameters specifies whether each power-supply enable or GPO is to be configured active-high or active-low. The address map for these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION                |
|---------|------|---------------|----------------------------|
| 0xE168  | 2    | 0x2004        | Polarity for rail 1 enable |
| 0xE16A  | 2    | 0x2008        | Polarity for rail 2 enable |
| 0xE16C  | 2    | 0x1804        | Polarity for rail 3 enable |
| 0xE16E  | 2    | 0x1802        | Polarity for rail 4 enable |
| 0xE170  | 2    | 0x1808        | Polarity for rail 5 enable |
| 0xE172  | 2    | 0x1810        | Polarity for rail 6 enable |
| 0xE174  | 2    | 0x1820        | Polarity for rail 7 enable |
| 0xE176  | 2    | 0x2010        | Polarity for rail 8 enable |
| 0xE178  | 2    | 0x2000        | Polarity for GPO1          |
| 0xE17A  | 2    | 0x2020        | Polarity for GPO2          |
| 0xE17C  | 2    | 0x2040        | Polarity for GPO3          |
| 0xE17E  | 2    | 0x2080        | Polarity for GPO4          |

The contents of this register are as follows:

|            |                                        |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------|----------------------------------------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15         | 14                                     | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>POL</b> | DEFAULT VALUES as specified previously |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| POL | Meaning                            |
|-----|------------------------------------|
| 0   | Rail enable or GPO is active-low.  |
| 1   | Rail enable or GPO is active-high. |

## ReferenceSelect

The ReferenceSelect field in the configuration parameters specifies which voltage reference is used on the UCD9080. The selected reference can be internal (2.5-V), or external via V<sub>CC</sub> (3.3 V). The register address is 0xE186 and contents are as follows:

|               |    |    |          |              |    |   |   |   |   |   |   |   |   |   |   |
|---------------|----|----|----------|--------------|----|---|---|---|---|---|---|---|---|---|---|
| 15            | 14 | 13 | 12       | 11           | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>SELREF</b> |    |    | <b>0</b> | <b>0x8F2</b> |    |   |   |   |   |   |   |   |   |   |   |

| SELREF | Meaning                             |
|--------|-------------------------------------|
| 000    | External reference selected (VCC)   |
| 001    | Internal reference selected (2.5 V) |

The default value for this register is 0x08F2, which selects the external reference.

## LastUnusedSeq

The LastUnusedSeq field in the configuration parameters specifies the amount of time for the last rail to be shut down without creating an error. The register address is 0xE18E and contents are as follows:

|        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LUTIME |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

LUTIME = Maximum value USTIME + 255 (in units of ms)

The default value for this register is 0x08FF.

## APPLICATION INFORMATION

### Typical Application Diagram

Figure 12 illustrates a typical power-supply sequencing configuration. Power Supply 1 and Power Supply X require active-low enables, whereas Power Supply 2 and Power Supply 3 require active-high enables.  $V_{OUT1}$  and  $V_{OUT3}$  exceed the selected A/D reference voltage, so these outputs are divided before being sampled by the MON1 and MON3 inputs.  $V_{OUT2}$  and  $V_{OUTX}$  are within the selected A/D reference voltage, so these outputs can be sampled directly by the MON2 and MON7 inputs. Figure 12 illustrates the use of the GPO digital output pins to provide status and power-on reset to other system devices.

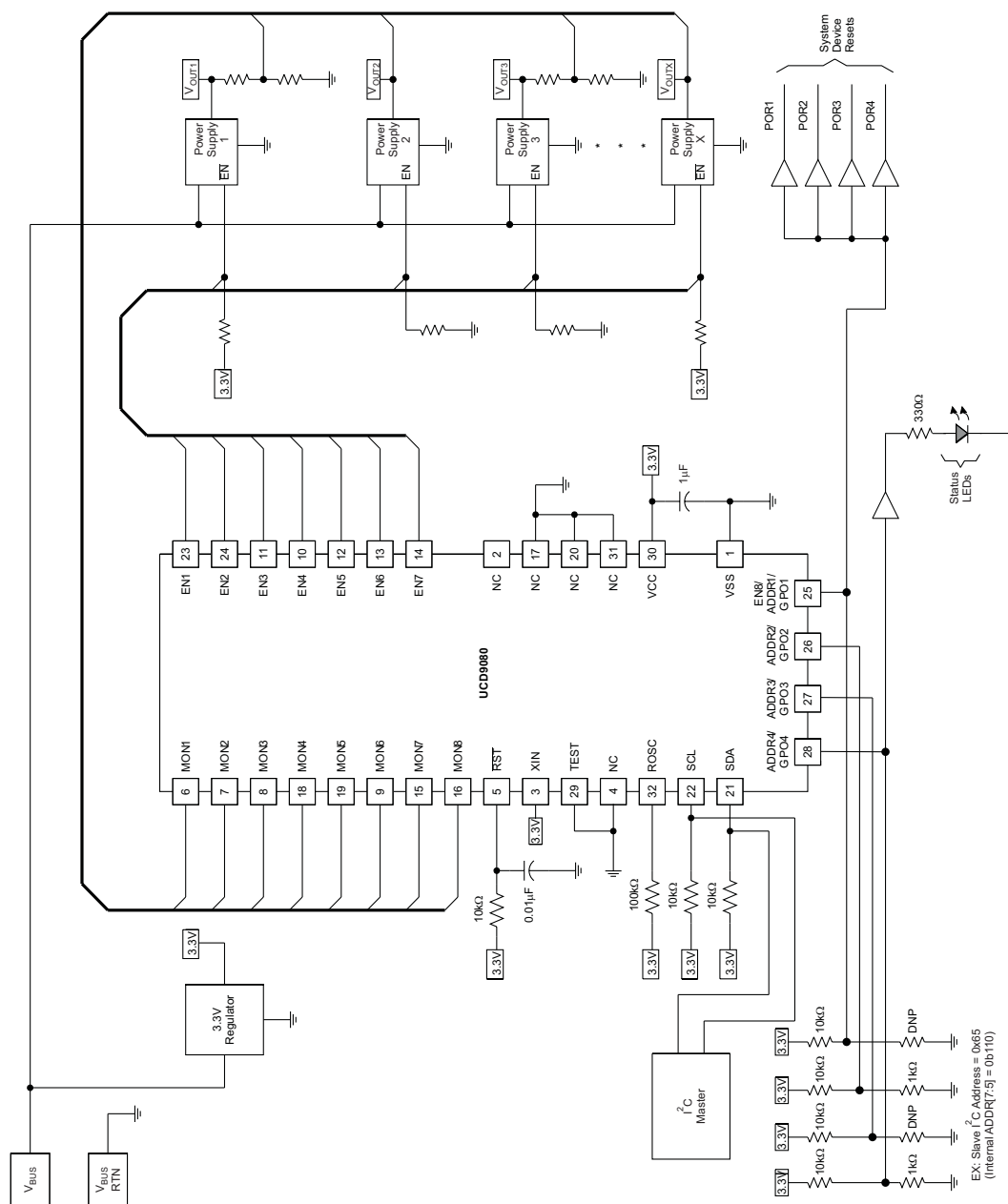


Figure 12. Typical Power-Supply Sequencing Application

| Changes from Revision D (December 2007) to Revision E                                                                                                    | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Deleted ordering information table.....                                                                                                                | 2    |
| • Changed NOM and MAX supply current specifications.....                                                                                                 | 2    |
| • Updated Schmitt-trigger input signal list to add the ENx pins (inputs during reset) .....                                                              | 2    |
| • Removed signal list from high-impedance leakage current specification .....                                                                            | 2    |
| • Updated the digital output signal list to include the SCL pin (for clock stretching).....                                                              | 3    |
| • Updated the directionality for the ENx and SCL pins .....                                                                                              | 7    |
| • Clarified wording .....                                                                                                                                | 9    |
| • Clarified wording in several sentences and removed note at end of paragraph .....                                                                      | 9    |
| • Moved this section to follow the Power-Supply Enables section. Minor wording change .....                                                              | 9    |
| • Added new section to describe ENx and GPOx behavior during device reset, and to describe I <sup>2</sup> C address and GPOx polarity relationship ..... | 9    |
| • Clarified wording in sequence paragraph .....                                                                                                          | 10   |
| • Clarified wording in several paragraphs .....                                                                                                          | 11   |
| • Clarified device time counter reset .....                                                                                                              | 16   |
| • Clarified FLASHLOCK wording .....                                                                                                                      | 18   |
| • Clarified RESTART wording .....                                                                                                                        | 18   |
| • Clarified WDATA/WADDR wording.....                                                                                                                     | 18   |
| • Clarified wording in several steps .....                                                                                                               | 19   |
| • Changed pin names from <b>NIC</b> to <b>NC</b> for pins 2, 4, 17, 20, 31.....                                                                          | 29   |

| Changes from Revision C (January 2007) to Revision D                                                                                                                                                            | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed minimum analog supply and positive built-in reference active V <sub>CC</sub> (min) voltage. Removed minimum sampling voltage, 1.5-V internal reference, and DCO OPERATING PERIOD specifications. .... | 3    |
| • Added specification for data hold time, t <sub>HD,DAT</sub> and notes 3 and 4.....                                                                                                                            | 6    |
| • Changed pin #2 from "connect to VSS" to "do not connect" .....                                                                                                                                                | 7    |
| • Removed critica-rail-specification sentence from paragraph 4.....                                                                                                                                             | 10   |
| • Added Ignore option and updated available retry options. Updated descriptions of options .....                                                                                                                | 10   |
| • Added version register and changed WDATA access type from <b>w</b> to <b>rw</b> .....                                                                                                                         | 13   |
| • Removed reference to flash and non-volatile error log feature in NVERRLOG bit description.....                                                                                                                | 17   |
| • Change WDATA access type from <b>w</b> to <b>rw</b> .....                                                                                                                                                     | 19   |
| • Removed <i>Resetting the Flash Error Logs</i> section .....                                                                                                                                                   | 19   |
| • Added the <i>UserData</i> section.....                                                                                                                                                                        | 20   |
| • Updated factory byte values .....                                                                                                                                                                             | 20   |
| • Updated factory byte values .....                                                                                                                                                                             | 21   |
| • Removed retry 2, retry 3, retry 4, and retry continuously options.....                                                                                                                                        | 24   |
| • Removed SaveRailLog register description.....                                                                                                                                                                 | 28   |
| • Removed pin-2 connection to ground.....                                                                                                                                                                       | 29   |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| UCD9080RHBR      | ACTIVE        | VQFN         | RHB                | 32   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 85    | UCD<br>9080             | <a href="#">Samples</a> |
| UCD9080RHBRG4    | ACTIVE        | VQFN         | RHB                | 32   | 3000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 85    | UCD<br>9080             | <a href="#">Samples</a> |
| UCD9080RHBT      | ACTIVE        | VQFN         | RHB                | 32   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 85    | UCD<br>9080             | <a href="#">Samples</a> |
| UCD9080RHBTG4    | ACTIVE        | VQFN         | RHB                | 32   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-2-260C-1 YEAR  | -40 to 85    | UCD<br>9080             | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UCD9080RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| UCD9080RHBT | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UCD9080RHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| UCD9080RHBT | VQFN         | RHB             | 32   | 250  | 210.0       | 185.0      | 35.0        |

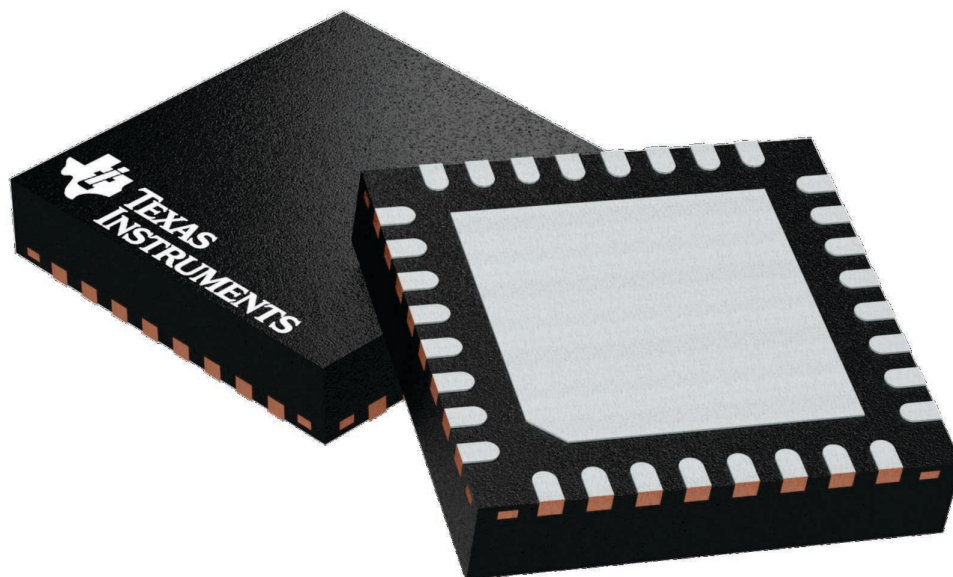
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

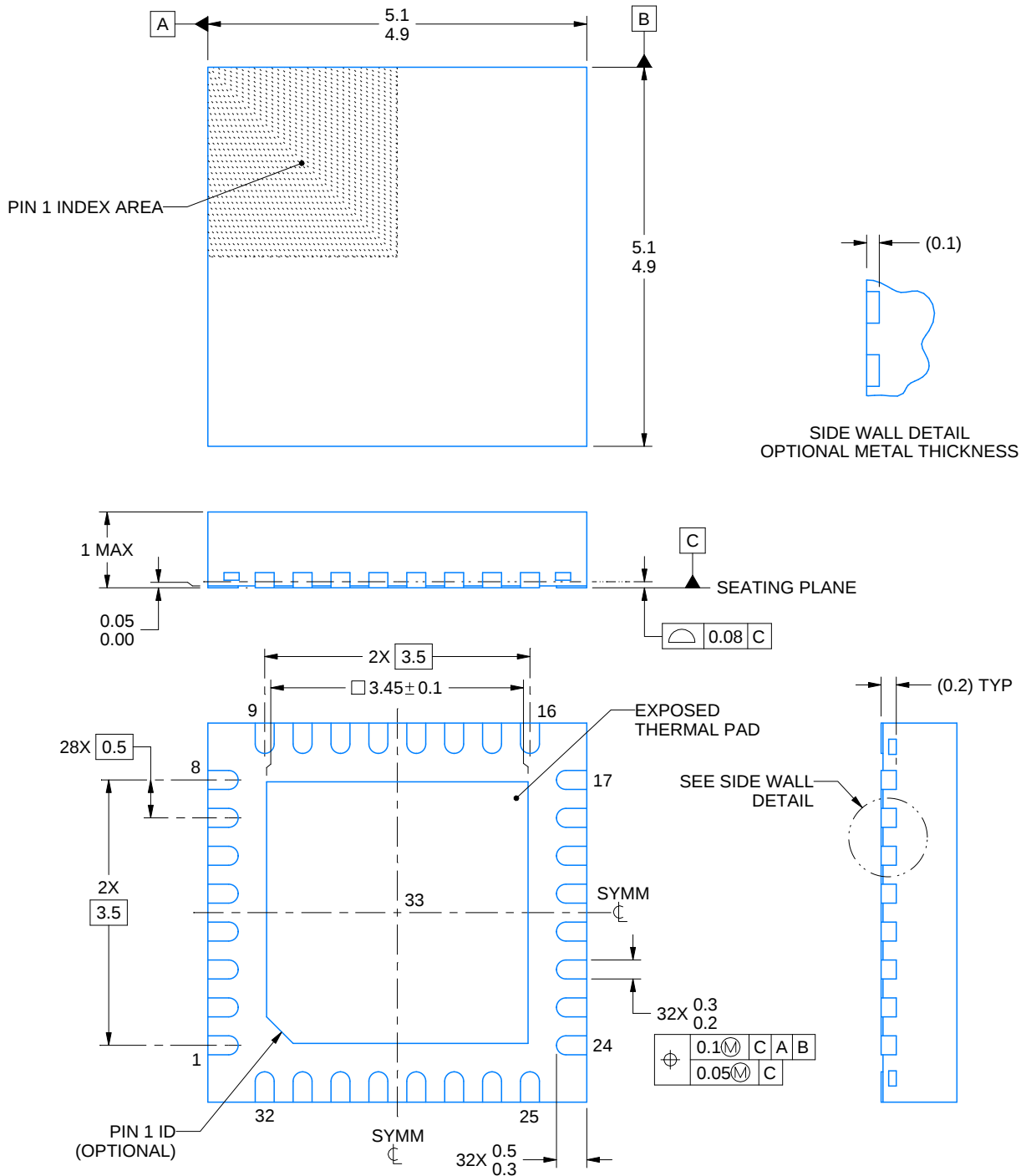
4224745/A

**RHB0032E**

## PACKAGE OUTLINE

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4223442/B 08/2019

NOTES:

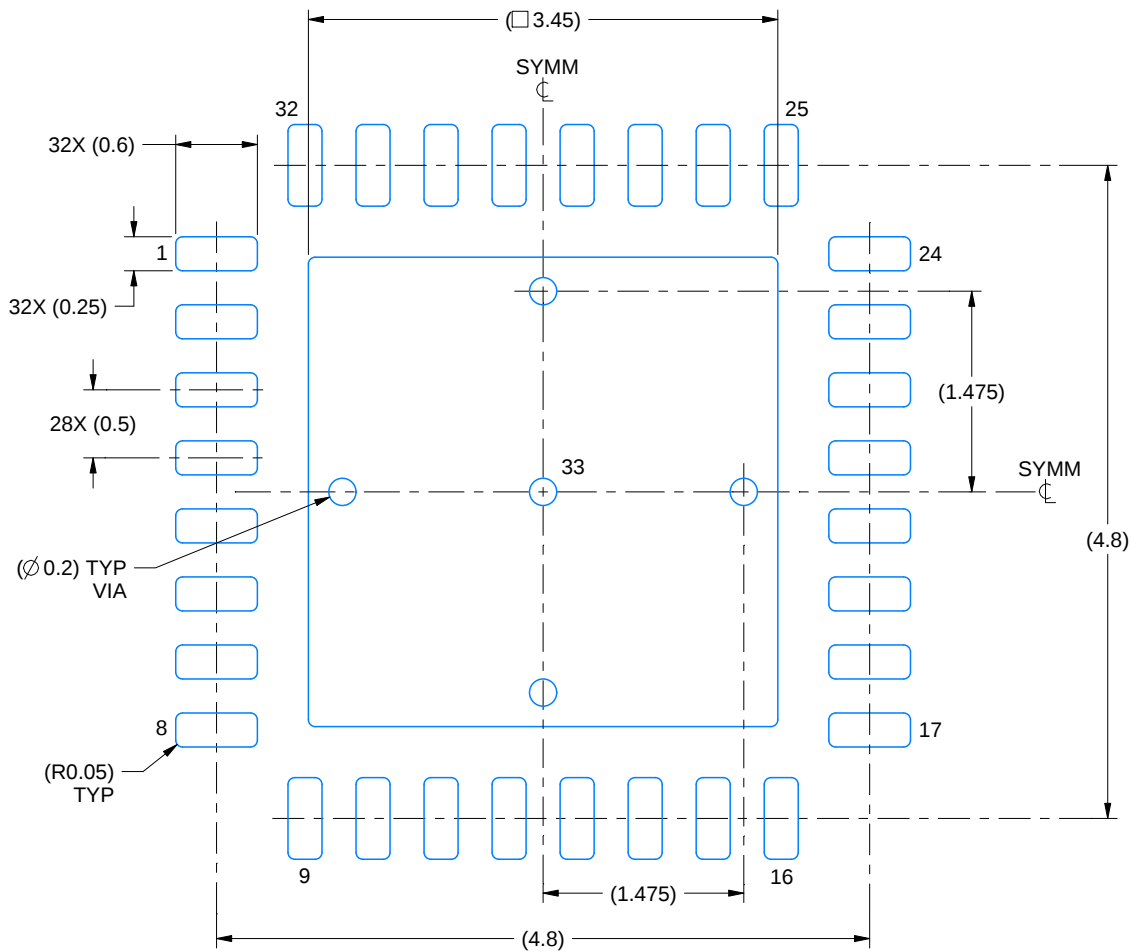
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

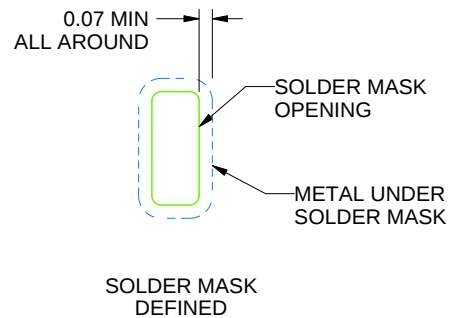
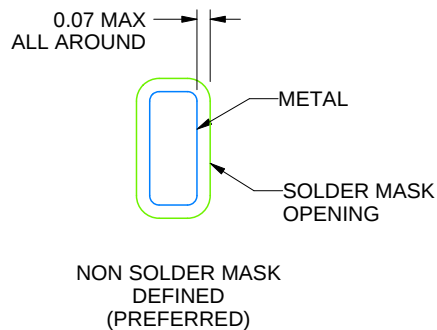
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

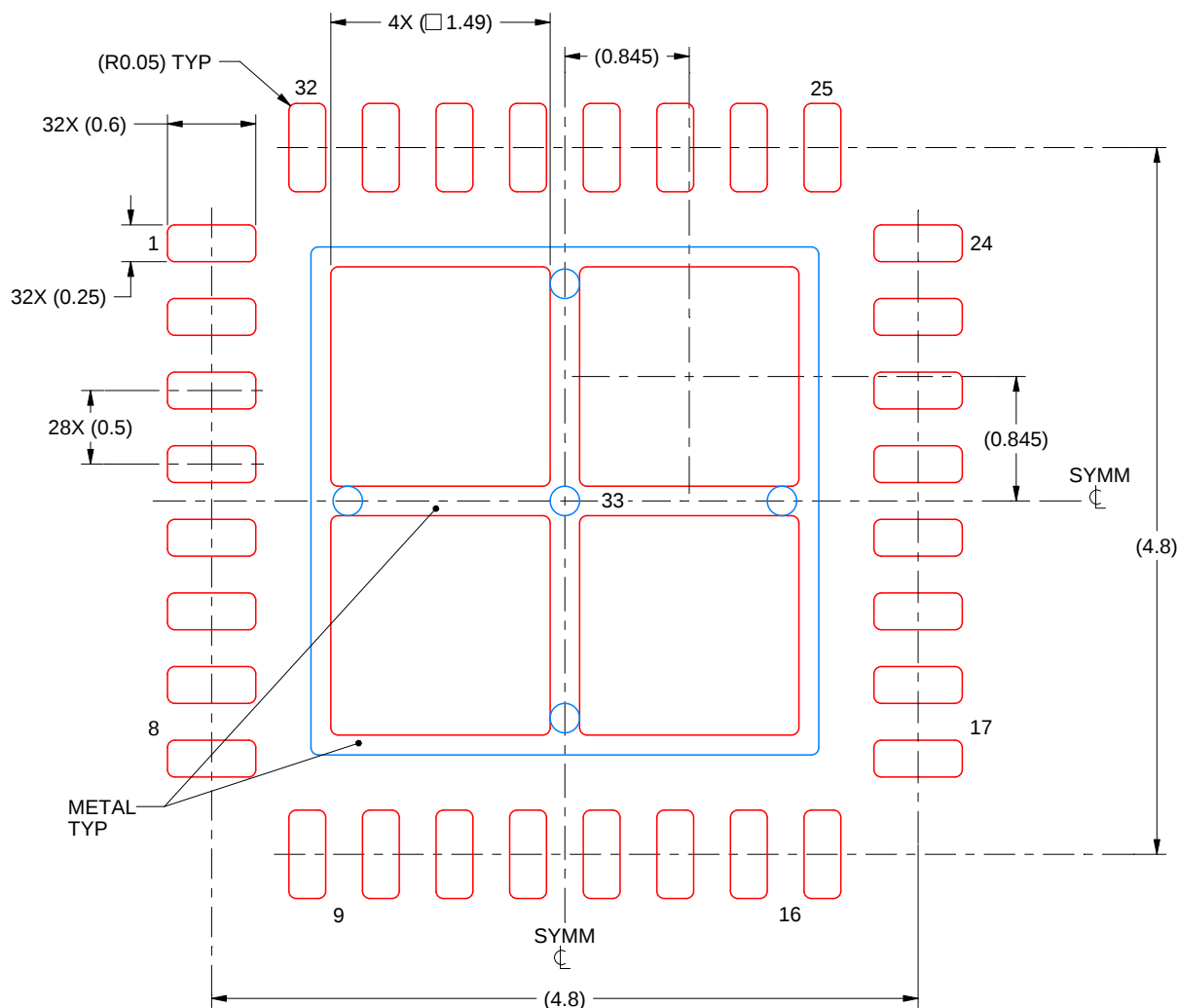
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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