TEXAS INSTRUMENTS

TPS61098, TPS610981
TPS610982, TPS610985, TPS610986, TPS610987

SLVS873D – JUNE 2015 – REVISED APRIL 2016

TPS61098x Ultra-Low Quiescent Current Synchronous Boost with Integrated LDO/Load Switch

1 Features

- 300 nA Ultra-Low I_Q in Low Power mode
- Startup into Load at 0.7 V Input Voltage
- Operating Input Voltage from 0.7 V to 4.5 V
- Selectable Output Voltages Up to 4.3 V
- Minimum 350 mA Switch Peak Current Limit
- Integrated LDO/Load Switch
- Two Modes Controlled by MODE Pin
  - Active Mode: Dual Outputs at Set Values
  - Low Power Mode: LDO/Load Switch Off; Boost Keeps On
- Automatic Pass-Through
- Up to 88% Efficiency at 10 µA Load from 2 V to 3.3 V Conversion (Low Power Mode)
- Up to 93% Efficiency at 5 mA ~ 100 mA Load from 2 V to 3.3 V Conversion
- 1.5 mm x 1.5 mm WSON Package

2 Applications

- Smart Remote Control
- BLE Tag
- Wearable Applications
- Low Power Wireless Applications
- Portable Consumer or Medical Products
- Single Coin Cell, Single or Two-Cell Alkaline Powered Applications

3 Description

The TPS61098x is an ultra low power solution for products powered by either a one-cell or two-cell alkaline, NiCd or NiMH, one-cell coin cell or one-cell Li-Ion or Li-polymer battery. It integrates either a Low-dropout Linear Regulator (LDO) or a load switch with a boost converter and provides two output rails. The boost output $V_{(MAIN)}$ is designed as an always-on supply for a main system, and the LDO or load switch output $V_{(SUB)}$ is to power peripheral devices.

The TPS61098x has two modes controlled by MODE pin: Active mode and Low Power mode. In Active mode, both outputs are enabled with enhanced response performance. In Low Power mode, the LDO or load switch is disabled to disconnect peripherals. The TPS61098x consumes only 300 nA quiescent current and can achieve up to 88% efficiency at 10 µA load in Low Power mode.

The TPS61098x supports automatic pass-through function. When input voltage is higher than a pass-through threshold, the boost converter stops switching and passes the input voltage to VMAIN rail; when input voltage is lower than the threshold, the boost works in boost mode and regulates output at the target value. The TPS61098x provides different versions for different output set values.

The TPS61098x can provide up to 50 mA total output current at 0.7 V input to 3.3 V output conversion. The boost is based on a hysteretic controller topology using synchronous rectifier to obtain maximum efficiency at minimal quiescent current.

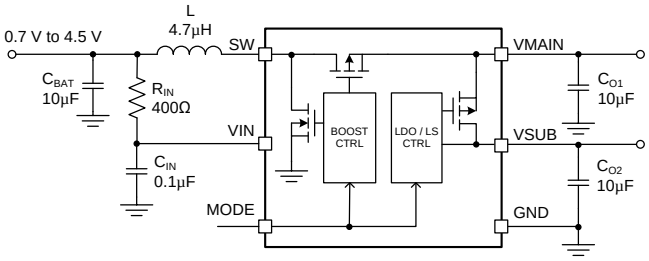
The TPS61098x is available in 1.5 mm x 1.5 mm WSON package to enable small circuit layout size.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61098x	6 pin WSON	1.50 mm x 1.50 mm

(1) For all available packages, see the orderable addendum at the end of this document.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2015) to Revision D — **Page**

- Added device TPS610987 ... 1
- Added TPS610987DSE in the Device Comparison Table. ... 4
- Added TPS610987 device to Electrical Characteristics table. ... 6
- Changed devices listed in the Conditions notes From:: TPS61098, '1, '5, '6 To: TPS61098, '1, '5, '6, '7 on graphs affected by adding TPS610987 device. ... 8
- Changed devices listed in the Conditions note From:: TPS61098 To: TPS61098, '7 in Figure 18, and Figure 19 ... 9

Changes from Revision B (July 2015) to Revision C — **Page**

- Added devices TPS610985 and TPS610986 to the data sheet ... 1
- Removed "Product Preview from devices TPS610985DSE and TPS610986DSE in the *Device Comparison Table* ... 4
- Added $R_{DS(on)\_LS}$ for device TPS610985 and TPS610986 in the *Electrical Characteristics* ... 6
- Added $R_{DS(on)\_HS}$ for device TPS610985 and TPS610986 in the *Electrical Characteristics* ... 6
- Added $R_{(LS)}$ for device TPS610985 and TPS610986 in the *Electrical Characteristics* ... 6
- Added $V_{(MAIN)}$ for device TPS610985 and TPS610986 in the *Electrical Characteristics* ... 7
- Added $V_{(PSTH)}$ for device TPS610985 and TPS610986 in the *Electrical Characteristics* ... 7
- Changed devices listed in the Conditions notes From: TPS61098/TPS610981 To: TPS61098, '1, '5, '6 in Figure 1 and Figure 2 ... 8
- Added Figure 13 to Figure 16 ... 9
- Added Figure 24 to Figure 27 ... 10
- Added Figure 34 to Figure 37 ... 12
- Added Figure 47 to Figure 48 ... 14
- Added a paragraph to the *Capacitor Selection* section: "For load switch version,..." ... 25
- Added Figure 65, Figure 66, and Figure 67 ... 26
- Added Figure 80 ... 29

Changes from Revision A (July 2015) to Revision B **Page**

- Added devices TPS610985DSE and TPS610986DSE to the *Device Comparison Table* ... 4
- Added device TPS610982 to the *Electrical Characteristics* ... 6
- Added Figure 3 and Figure 4 ... 8
- Added Figure 11 and Figure 12 ... 8
- Added Figure 22 and Figure 23 ... 10
- Added Figure 32 and Figure 33 ... 12
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- Added Figure 51 and Figure 52 ... 15
- Added text to the *Overview* section: "The TPS610982 is an exception..." ... 17
- Added text to the *Low Power Mode* Section: "The TPS610982 is an exception..." ... 21
- Added Figure 88, Figure 89, Figure 90 and Figure 92 ... 33
- Added Figure 94 and Figure 95 ... 33

Changes from Original (June 2015) to Revision A **Page**

- Changed text in the *Description* From: "can achieve 80% efficiency" To: " can achieve up to 88% efficiency" ... 1
- Changed "LDO / LS CRTL" with LDO / LS CTRL" and 4.7 µF To 4.7 µH in the *Simplified Schematic* ... 1
- Changed V_{IN} = 1.2 V To V_{IN} = 1.5 V and V_{IN} = 2 V to V_{IN} = 2.5 V in Figure 19 ... 10
- Changed "Boost Efficiency" To: "Boost Output Voltage" in Figure 28 To Figure 31 ... 11
- Changed text "below the programmed threshold," To: "below the programmed threshold with a hysteresis," in *Thermal Shutdown* ... 20
- Changed text "unstable operation at IC temperatures at the overtemperature threshold." To: "unstable operation at the overtemperature threshold." in *Thermal Shutdown* ... 20
- Changed text "sense or transfer signals" To: sense or transmit signals" in *VMAIN to Power MCU and VSUB to Power Subsystem* ... 22
- Changed 4.7 µF To 4.7 µH in Figure 57 ... 22
- Changed text "TPS610981 enters into sleep mode" To: "TPS610981 enters into Low Power mode" in *Control Sequence* ... 25
- Changed 4.7 µF To 4.7 µH in Figure 81 ... 30
- Changed text "a boost converter and an LDO are needed: To: "a boost converter with an LDO is needed" in *Figure 85* . 32
- Changed 4.7 µF To 4.7 µH in Figure 85 ... 32

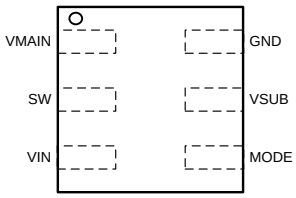
5 Device Comparison Table

PART NUMBER	INTEGRATED LDO OR LOAD SWITCH	VMAIN (ACTIVE MODE)	VMAIN (LOW POWER MODE)	VSUB (ACTIVE MODE)	VSUB (LOW POWER MODE)	VSUB ACTIVE DISCHARGE IN LOW POWER MODE
TPS61098DSE(1)	LDO	4.3 V	2.2 V	3.1 V	OFF	No
TPS610981DSE	LDO	3.3 V	3.3 V	3.0 V	OFF	Yes
TPS610982DSE	LDO	3.3 V	3.3 V	2.8 V	2.8 V	No
TPS610985DSE	Load Switch	3.0 V	3.0 V	ON	OFF	Yes
TPS610986DSE	Load Switch	3.3 V	3.3 V	ON	OFF	Yes
TPS610987DSE	LDO	4.3 V	2.2 V	3.1 V	OFF	Yes

(1) The DSE package is available taped and reeled. Add R suffix to device type (e.g., TPS61098DSER) to order quantities of 3000 devices per reel. Add T suffix to device type (e.g., TPS61098DSET) to order quantities of 250 devices per reel. For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

6 Pin Configuration and Functions

DSE Package
6-Pin WSON
Top View



Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
VMAIN	1	PWR	Boost converter output
SW	2	PWR	Connection for inductor
VIN	3	I	IC power supply input
MODE	4	I	Mode selection pin. 1: Active mode; 0: Low Power mode. Must be actively tied high or low. Do not leave floating.
VSUB	5	PWR	LDO or load switch output
GND	6	PWR	IC ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, SW, VMAIN, VSUB	-0.3	4.7	V
	MODE	-0.3	5.0	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged Device Model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM rating allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM rating allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	0.7		4.5	V
$V_{(MAIN)}$	Boost converter output voltage range	2.2		4.3	V
$V_{(SUB)}$	Load switch / LDO outut voltage range	1.8		3.7	V
L	Effective inductance range	1.54	4.7	6.11	µH
C_{BAT}	Effective input capacitance range at input(1)	5			µF
C_{O1}	Effective output capacitance range at VMAIN pin for boost converter output(1)	5	10	22	µF
C_{O2}	Effective output capacitance range at VSUB pin for LDO output(1)	1(2)	5	10	µF
	Effective output capacitance range at VSUB pin for load switch output(1)(3)		1	2.2	µF
T_J	Operating virtual junction temperature	–40		125	°C

(1) Effective value. Ceramic capacitor's derating effect under bias should be considered. Choose the right nominal capacitance by checking capacitor DC bias characteristics.
(2) If LDO output current is lower than 20 mA, the minimum effective output capacitance value can be lower to 0.5 µF.
(3) With load switch version, the output capacitor at VSUB pin is only required if smaller voltage ripple is needed.

7.4 Thermal Information

THERMAL METRIC(1)		TPS61098x DSE 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	118.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	136.4	
ψ_{JT}	Junction-to-top characterization parameter	8.3	
ψ_{JB}	Junction-to-board characterization parameter	136.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 0.7 V to 4.5 V. Typical values are at V_{IN} = 1.5 V, T_J = 25°C, unless otherwise noted.

PARAMETER		VERSION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply							
V_{IN}	Input voltage range	TPS61098x		0.7		4.5	V
$V_{IN(start)}$	Minimum input voltage at startup	TPS61098x	R_{Load} ≥ 3 kΩ (1)			0.7	V
$I_{Q(VIN)}$	Quiescent current into VIN pin in Active Mode	TPS61098x	MODE = High, Boost or Pass-through No Load, No Switching T_J = -40 °C to 85 °C		2	4	µA
	Quiescent current into VIN pin in Low Power Mode	TPS61098x	MODE = Low, Boost or Pass-through No Load, No Switching		5	90	nA
$I_{Q(VMAIN)}$	Quiescent current into VMAIN pin in Active Mode	TPS61098/1/5/6/7	MODE = High, Boost or Pass-through No Load, No Switching T_J = -40 °C to 85 °C		15	23	µA
		TPS610982	MODE = High, Boost or Pass-through No Load, No Switching T_J = -40 °C to 85 °C		18	23	µA
	Quiescent current into VMAIN pin in Low Power Mode	TPS61098/1/7	MODE = Low, Boost or Pass-through No Load, No Switching T_J = 25 °C		300	400	nA
		TPS61098/1/5/6/7	MODE = Low, Boost or Pass-through No Load, No Switching T_J = -40 °C to 85 °C		300	800	nA
		TPS610982	MODE = Low, Boost or Pass-through No Load, No Switching T_J = -40 °C to 85 °C		4	10	µA
$I_{LKG(SW)}$	Leakage current of SW pin (from SW pin to GND pin)	TPS61098x	$V_{(MAIN)}$ = $V_{(SW)}$ = 4.7 V, No Load T_J = -40 °C to 85 °C		5	100	nA
$I_{LKG(MAIN)}$	Leakage current of VMAIN pin (from VMAIN pin to SW pin)	TPS61098x	$V_{(MAIN)}$ = 4.7 V, $V_{(SW)}$ = 0 V, No Load T_J = -40 °C to 85 °C		10	200	nA
$I_{LKG(SUB)}$	Leakage current of VSUB pin (from VMAIN pin to VSUB pin)	TPS61098/1/5/6/7	MODE = Low, $V_{(MAIN)}$ = 4.7 V, $V_{(SUB)}$ = 0 V T_J = -40 °C to 85 °C		10	150	nA
$I_{LKG(MODE)}$	Leakage current into MODE pin	TPS61098x	$V_{(MODE)}$ = 5 V T_J = -40 °C to 85 °C		5	30	nA
Power Switch							
$R_{DS(on)\_LS}$	Low side switch on resistance	TPS61098/7	MODE = Low		600	1000	mΩ
			MODE = High		300	600	mΩ
		TPS610981/2/6	MODE = Low / High		350	650	mΩ
		TPS610985	MODE = Low / High		400	700	mΩ
$R_{DS(on)\_HS}$	Rectifier on resistance	TPS61098/7	MODE = Low		700	1000	mΩ
			MODE = High		450	700	mΩ
		TPS610981/2/6	MODE = Low / High		500	700	mΩ
		TPS610985	MODE = Low / High		550	750	mΩ
$R_{(LS)}$	Load switch on resistance	TPS610985/6			1.2	2	Ω
$V_{(Dropout)}$	LDO dropout voltage	TPS61098/1/2/7	I_{SUB} = 50 mA		60	100	mV
I_{LH}	Inductor current ripple	TPS61098x			100		mA
$I_{LIM(BST)}$	Boost switch current limit	TPS61098x	0.7 V < V_{IN} < $V_{(MAIN)}$	350	500	650	mA
$I_{LIM(SUB)}$	VSUB output current limit	TPS61098x	T_J = -20 °C to 125 °C	200			mA
$I_{(DISCH)}$	Discharge current from VSUB pin to GND pin	TPS610981/5/6/7	MODE = Low, $V_{(SUB)}$ = 3 V	5	8		mA

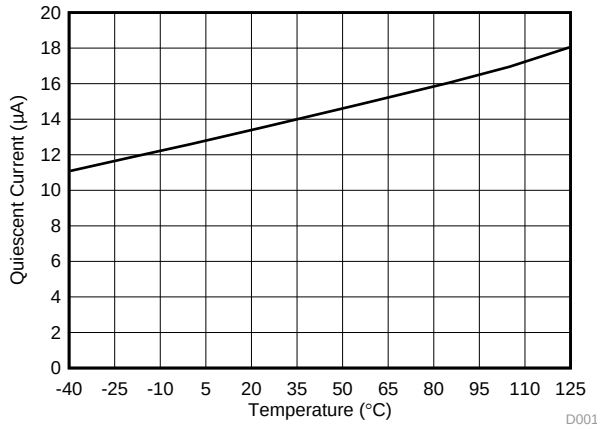
(1) TPS61098x is able to drive R_{Load} > 150 Ω after V_{MAIN} is established over 1.8 V.

Electrical Characteristics (continued)

T_J = -40°C to 125°C and V_{IN} = 0.7 V to 4.5 V. Typical values are at V_{IN} = 1.5 V, T_J = 25°C, unless otherwise noted.

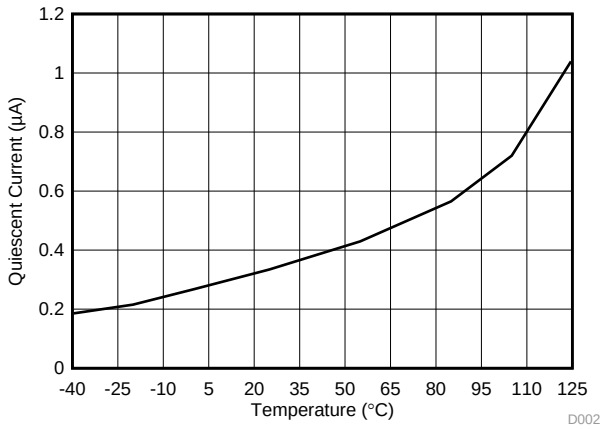
PARAMETER		VERSION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output							
$V_{(MAIN)}$	Boost converter output voltage	TPS61098/7	MODE = High, V_{IN} < $V_{(PSTH)}$ Burst mode, open loop		4.45		V
			MODE = High, V_{IN} < $V_{(PSTH)}$ PWM mode, open loop	4.142	4.27	4.398	V
			MODE = Low, V_{IN} < $V_{(PSTH)}$ Burst mode, open loop		2.3		V
			MODE = Low, V_{IN} < $V_{(PSTH)}$ PWM mode, open loop	2.163	2.23	2.297	V
		TPS610981	MODE = High / Low, V_{IN} < $V_{(PSTH)}$ Burst mode, open loop		3.4		V
			MODE = High / Low, V_{IN} < $V_{(PSTH)}$ PWM mode, open loop	3.201	3.3	3.399	V
		TPS610982	MODE = High / Low, V_{IN} < $V_{(PSTH)}$ Burst mode, open loop		3.4		V
			MODE = High / Low, V_{IN} < $V_{(PSTH)}$ PWM mode, open loop	3.201	3.3	3.399	V
		TPS610985	MODE = High / Low, V_{IN} < $V_{(PSTH)}$ Burst mode, open loop		3.1		V
			MODE = High / Low, V_{IN} < $V_{(PSTH)}$ PWM mode, open loop	2.91	3.0	3.09	V
		TPS610986	MODE = High / Low, V_{IN} < $V_{(PSTH)}$ Burst mode, open loop		3.4		V
			MODE = High / Low, V_{IN} < $V_{(PSTH)}$ PWM mode, open loop	3.201	3.3	3.399	V
$V_{(SUB)}$	LDO output voltage (LDO version)	TPS61098/7	MODE = High	3.038	3.1	3.162	V
		TPS610981	MODE = High	2.94	3.0	3.06	V
		TPS610982	MODE = High / Low	2.744	2.8	2.856	V
$V_{(PSTH)}$	Pass-through mode threshold	TPS61098/7	MODE = High, V_{IN} rising		4.4		V
			MODE = High, Hysteresis		0.1		V
			MODE = Low, V_{IN} rising		2.25		V
			MODE = Low, Hysteresis		0.1		V
		TPS610981	MODE = High / Low, V_{IN} rising		3.35		V
			MODE = High / Low, Hysteresis		0.1		V
		TPS610982	MODE = High / Low, V_{IN} rising		3.35		V
			MODE = High / Low, Hysteresis		0.1		V
		TPS610985	MODE = High / Low, V_{IN} rising		3.05		V
			MODE = High / Low, Hysteresis		0.1		V
		TPS610986	MODE = High / Low, V_{IN} rising		3.35		V
			MODE = High / Low, Hysteresis		0.1		V
PSRR	Power-supply rejection ratio from LDO input to output	TPS61098/1/2/7	f = 1kHz, C_{O2} = 10 µF, I_{SUB} = 10 mA MODE = High		40		dB
		TPS610982	f = 1kHz, C_{O2} = 10 µF, I_{SUB} = 10 mA MODE = Low		28		dB
t_{stup_LDO}	VSUB startup time (LDO version and load switch version)	TPS61098x	No Load Time from MODE high to 90% of $V_{(SUB)}$		1		ms
Control Logic							
V_{IL}	MODE input low voltage	TPS61098x				0.4	V
V_{IH}	MODE input high voltage	TPS61098x		1.2			V
	Overtemperature protection	TPS61098x			150		°C
	Overtemperature hysteresis	TPS61098x			25		°C

7.6 Typical Characteristics



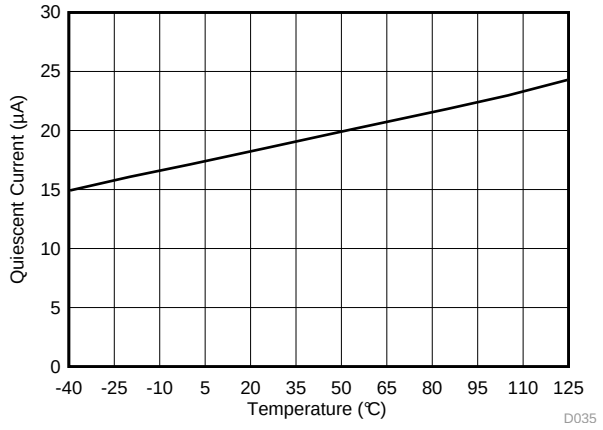
TPS61098, '1, '5, '6 MODE = High

Figure 1. I_Q into VMAIN Pin at Active Mode vs Temperature



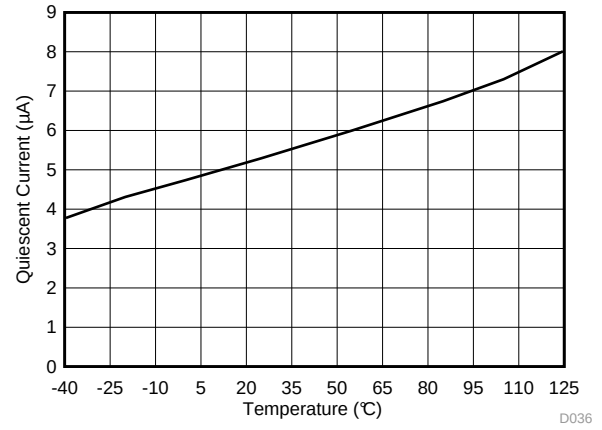
TPS61098, '1, '5, '6 MODE = Low

Figure 2. I_Q into VMAIN Pin at Low Power Mode vs Temperature



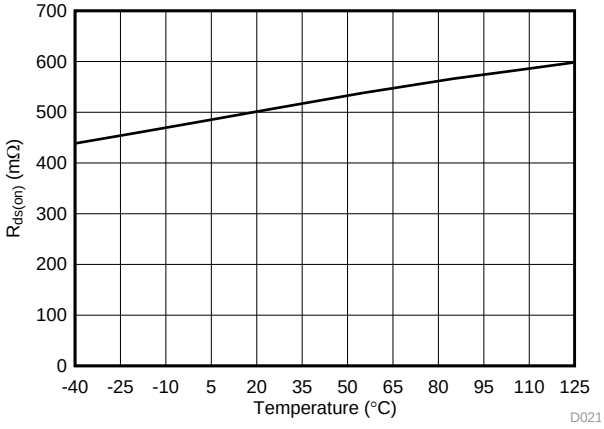
TPS610982 MODE = High

Figure 3. I_Q into VMAIN Pin at Active Mode vs Temperature



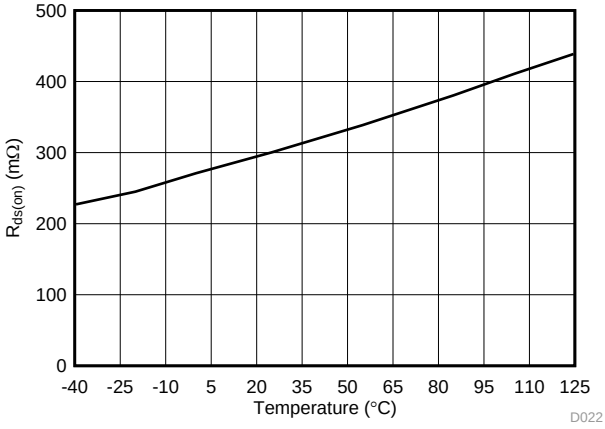
TPS610982 MODE = Low

Figure 4. I_Q into VMAIN Pin at Low Power Mode vs Temperature



TPS61098, '7 MODE = High

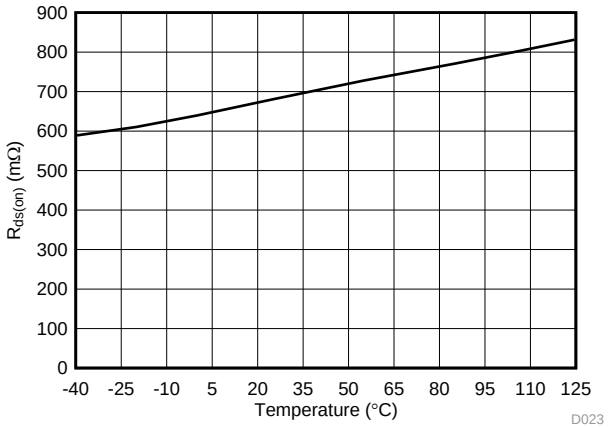
Figure 5. Rectifier On Resistance vs Temperature



TPS61098, '7 MODE = High

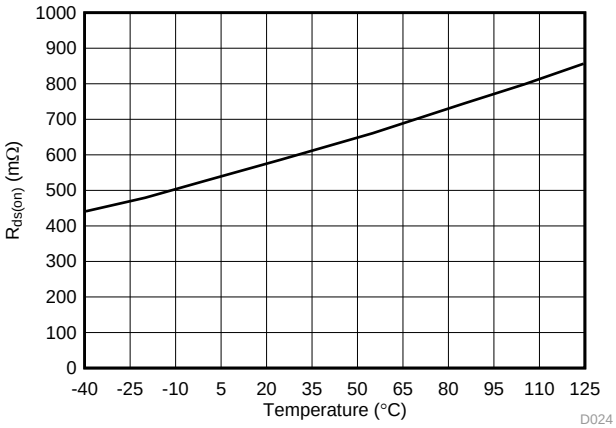
Figure 6. Low Side Switch On Resistance vs Temperature

Typical Characteristics (continued)



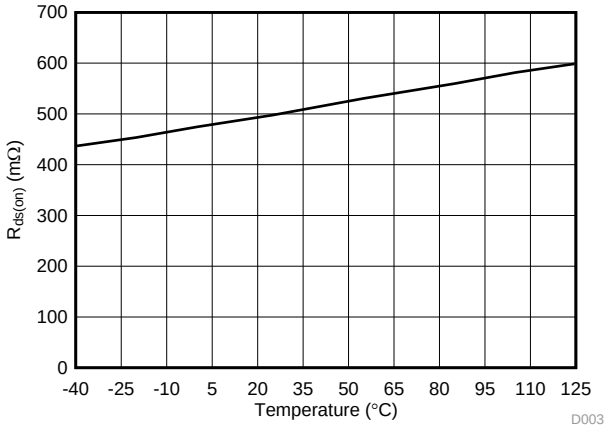
TPS61098, '7 MODE = Low

Figure 7. Rectifier On Resistance vs Temperature



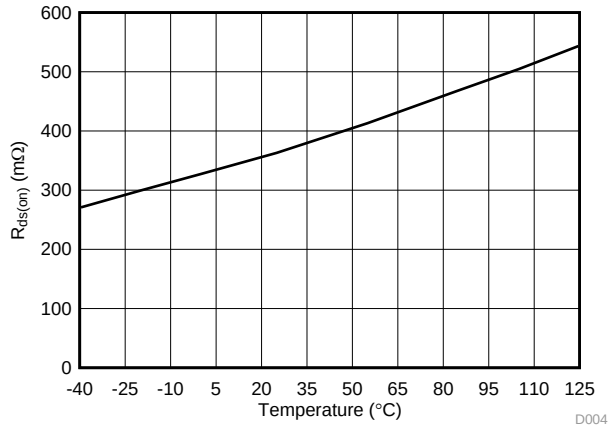
TPS61098, '7 MODE = Low

Figure 8. Low Side Switch On Resistance vs Temperature



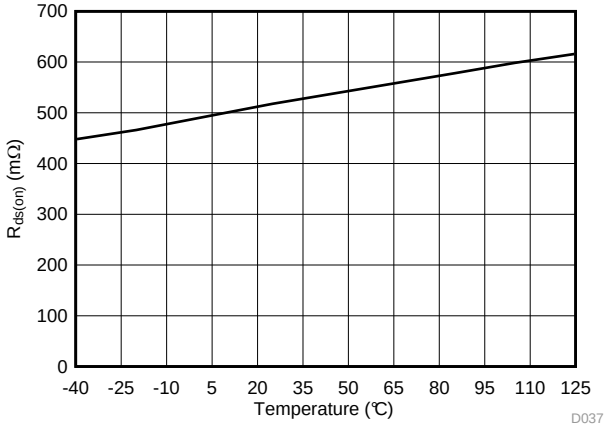
TPS610981 MODE = High / Low

Figure 9. Rectifier On Resistance vs Temperature



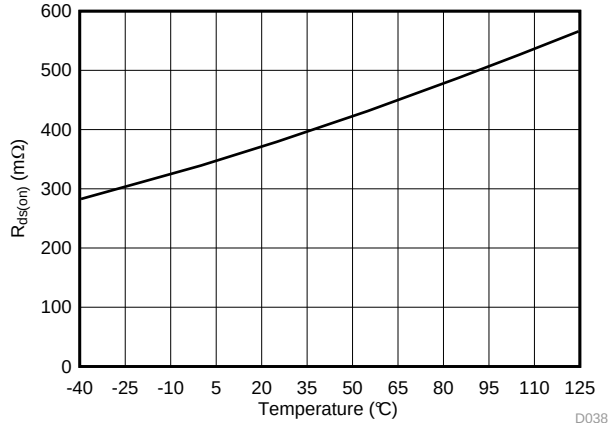
TPS610981 MODE = High / Low

Figure 10. Low Side Switch On Resistance vs Temperature



TPS610982 MODE = High / Low

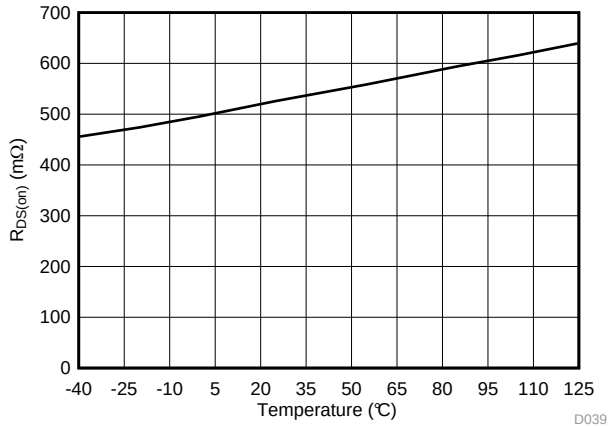
Figure 11. Rectifier On Resistance vs Temperature



TPS610982 MODE = High / Low

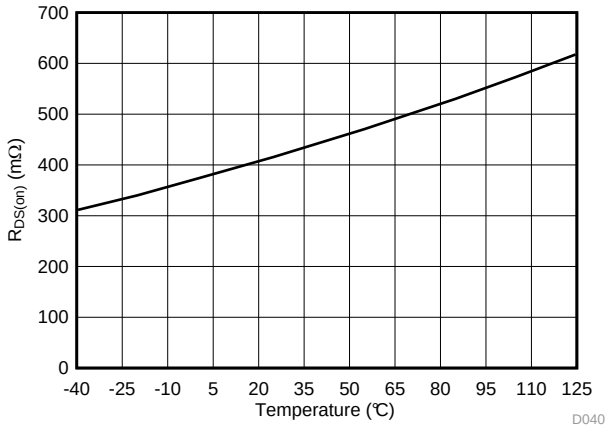
Figure 12. Low Side Switch On Resistance vs Temperature

Typical Characteristics (continued)



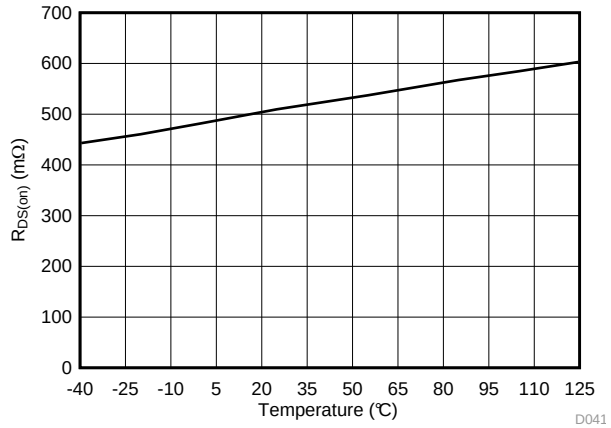
TPS610985 MODE = High / Low

Figure 13. Rectifier on Resistance vs Temperature



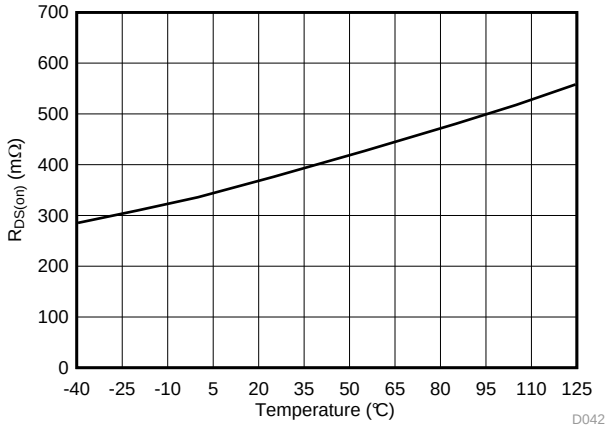
TPS610985 MODE = High / Low

Figure 14. Low Side Switch On Resistance vs Temperature



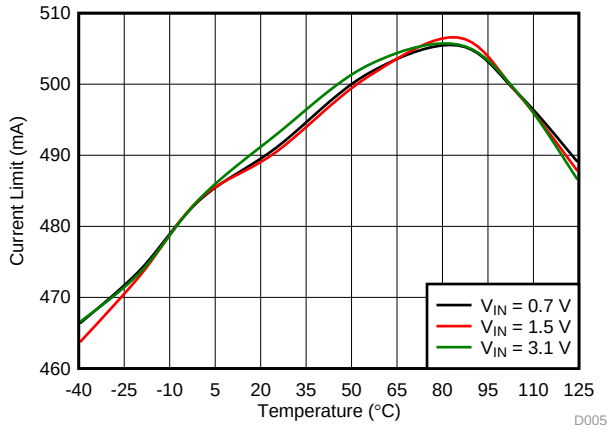
TPS610986 MODE = High / Low

Figure 15. Rectifier on Resistance vs Temperature



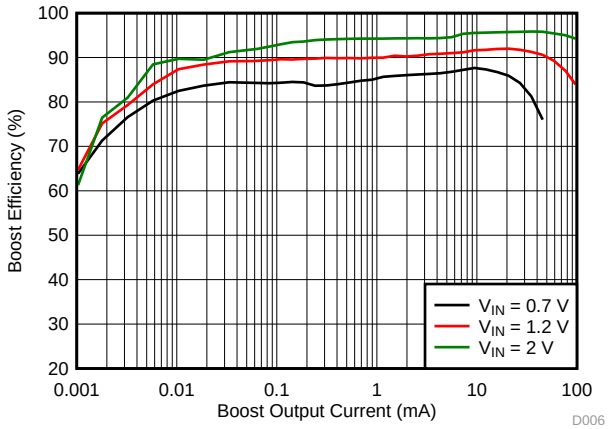
TPS610986 MODE = High / Low

Figure 16. Low Side Switch on Resistance vs Temperature



TPS61098x $V_{IN} < V_{(MAIN)}$

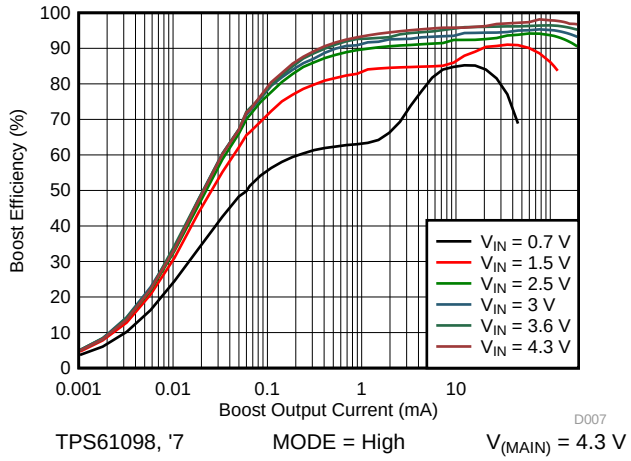
Figure 17. Current Limit vs Temperature



TPS61098, '7 MODE = Low $V_{(MAIN)}$ = 2.2 V

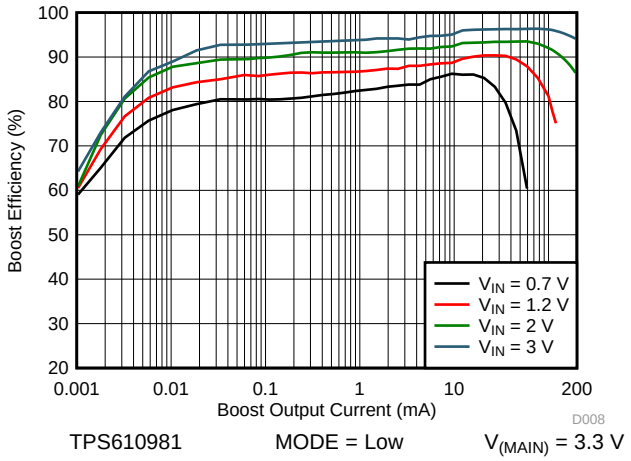
Figure 18. Boost Efficiency vs Output Current (Low Power Mode)

Typical Characteristics (continued)



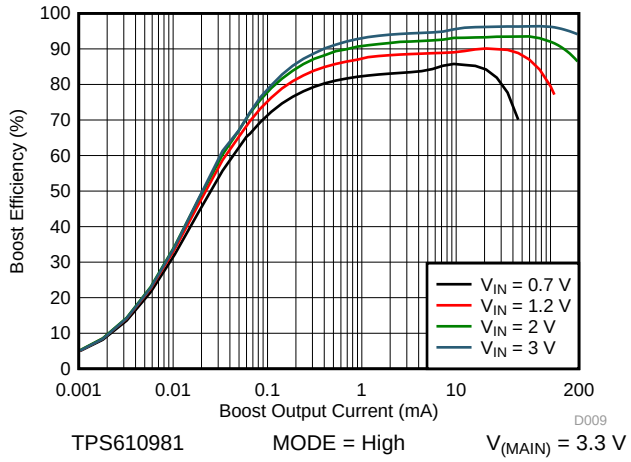
TPS61098, '7 MODE = High $V_{(MAIN)}$ = 4.3 V

Figure 19. Boost Efficiency vs Output Current (Active Mode)



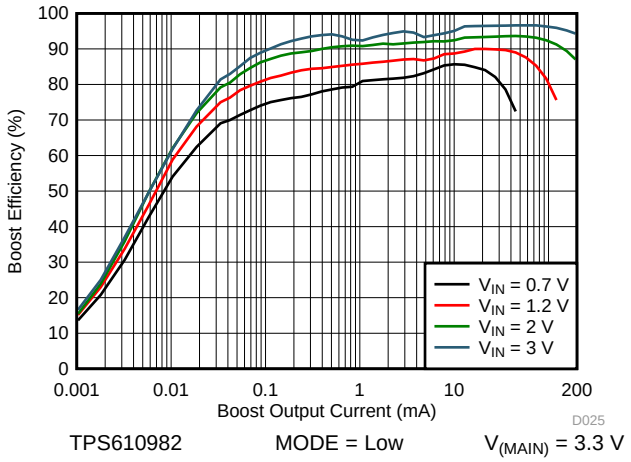
TPS610981 MODE = Low $V_{(MAIN)}$ = 3.3 V

Figure 20. Boost Efficiency vs Output Current (Low Power Mode)



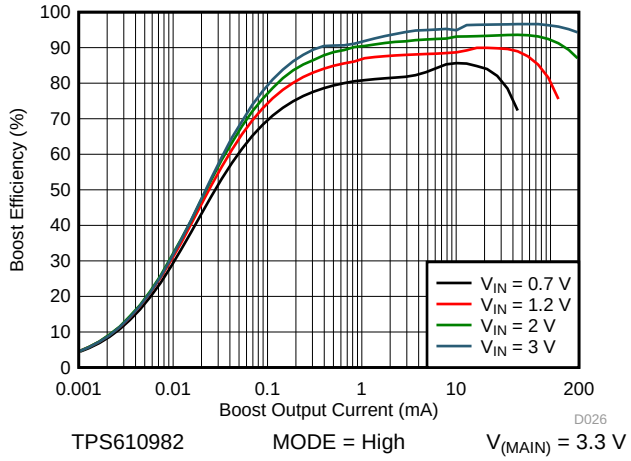
TPS610981 MODE = High $V_{(MAIN)}$ = 3.3 V

Figure 21. Boost Efficiency vs Output Current (Active Mode)



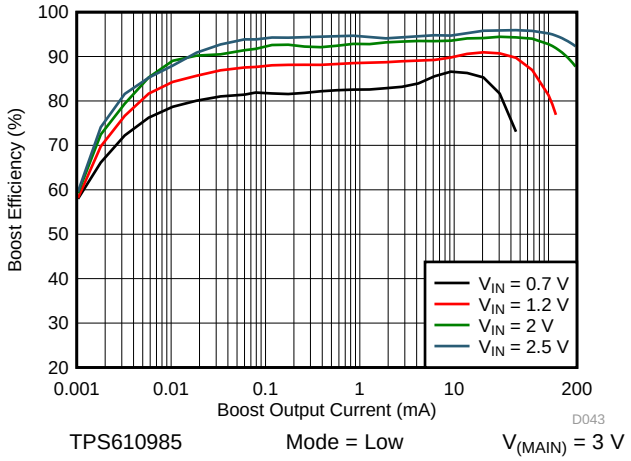
TPS610982 MODE = Low $V_{(MAIN)}$ = 3.3 V

Figure 22. Boost Efficiency vs Output Current (Low Power Mode)



TPS610982 MODE = High $V_{(MAIN)}$ = 3.3 V

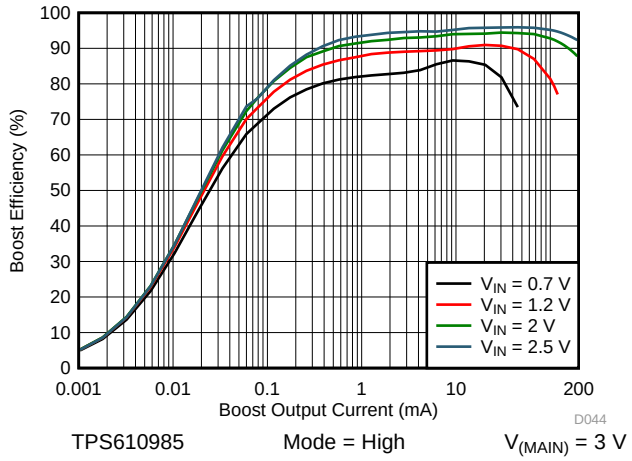
Figure 23. Boost Efficiency vs Output Current (Active Mode)



TPS610985 Mode = Low $V_{(MAIN)}$ = 3 V

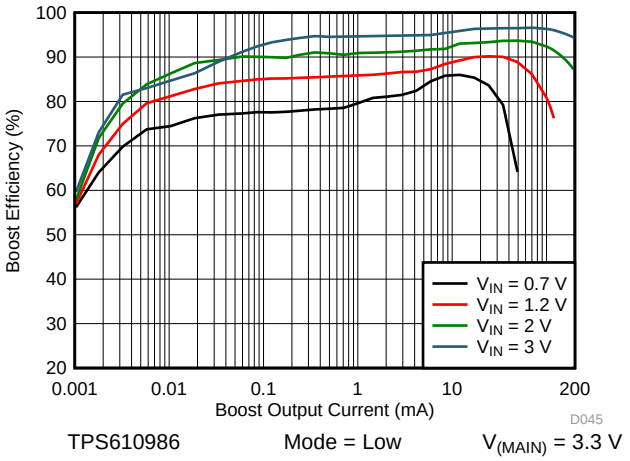
Figure 24. Boost Efficiency vs Output Current (Low Power Mode)

Typical Characteristics (continued)



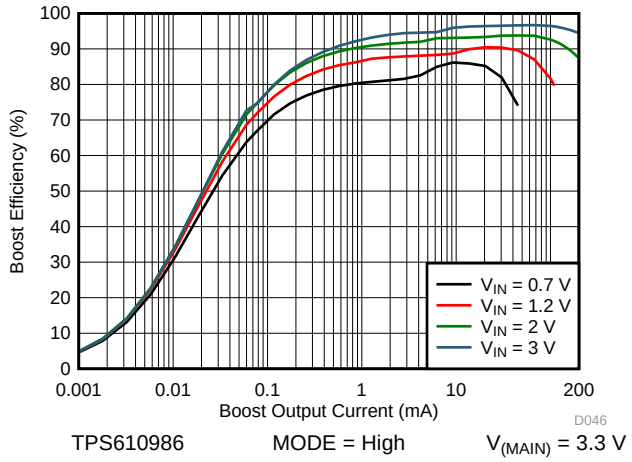
TPS610985 Mode = High $V_{(MAIN)}$ = 3 V

Figure 25. Boost Efficiency vs Output Current (Active Mode)



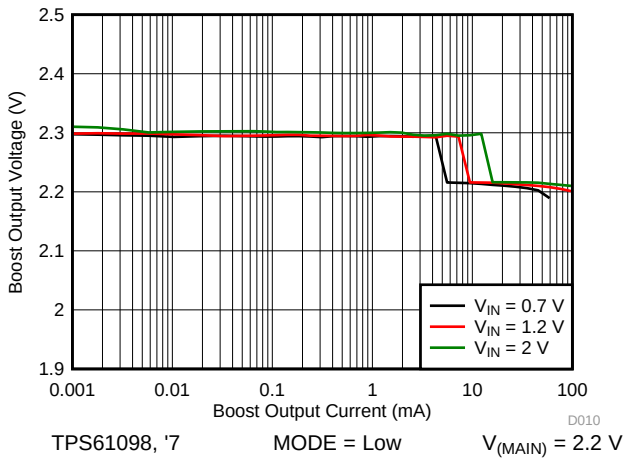
TPS610986 Mode = Low $V_{(MAIN)}$ = 3.3 V

Figure 26. Boost Efficiency vs Output Current (Low Power Mode)



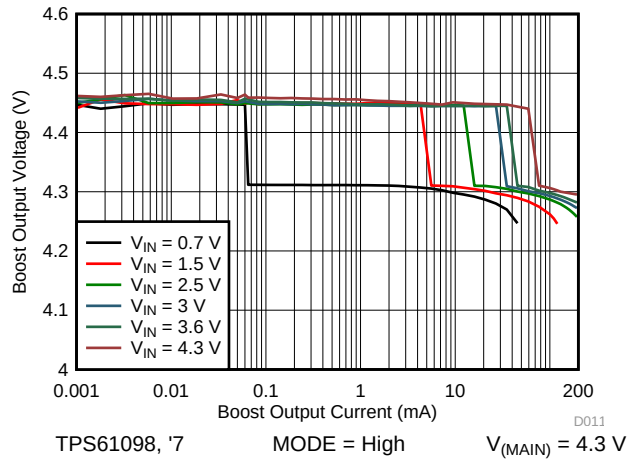
TPS610986 MODE = High $V_{(MAIN)}$ = 3.3 V

Figure 27. Boost Efficiency vs Output Current (Active Mode)



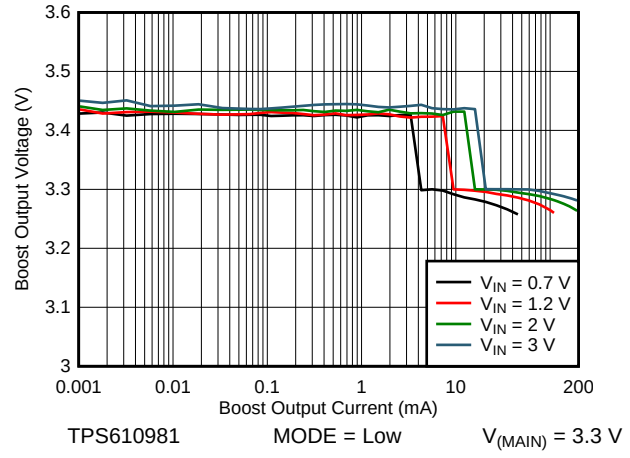
TPS61098, '7 MODE = Low $V_{(MAIN)}$ = 2.2 V

Figure 28. Boost Load Regulation (Low Power Mode)



TPS61098, '7 MODE = High $V_{(MAIN)}$ = 4.3 V

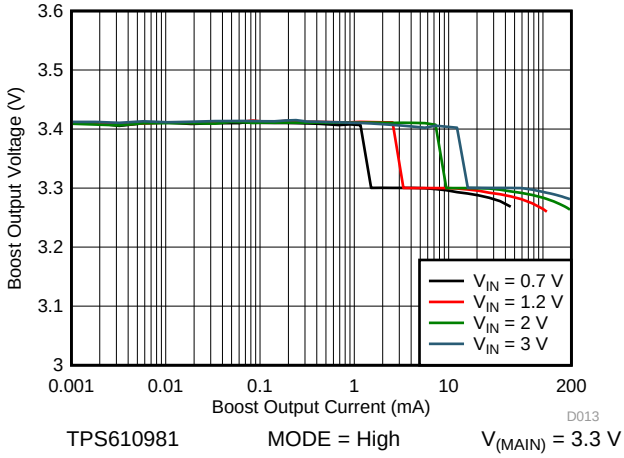
Figure 29. Boost Load Regulation (Active Mode)



TPS610981 MODE = Low $V_{(MAIN)}$ = 3.3 V

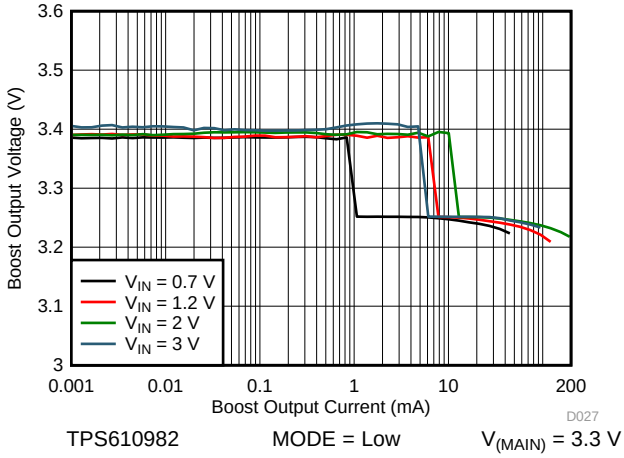
Figure 30. Boost Load Regulation (Low Power Mode)

Typical Characteristics (continued)



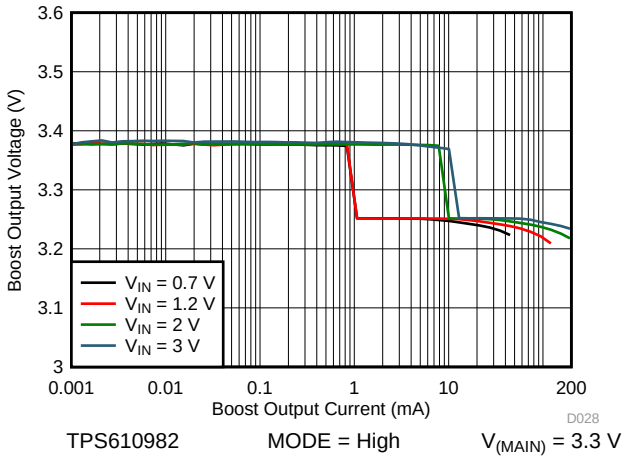
TPS610981 MODE = High $V_{(MAIN)}$ = 3.3 V

Figure 31. Boost Load Regulation (Active Mode)



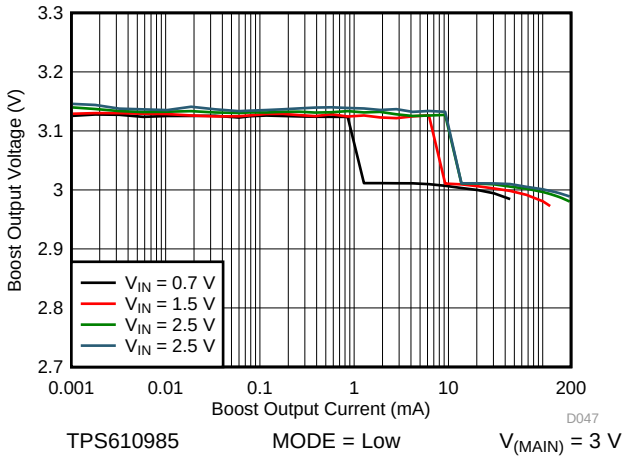
TPS610982 MODE = Low $V_{(MAIN)}$ = 3.3 V

Figure 32. Boost Load Regulation (Low Power Mode)



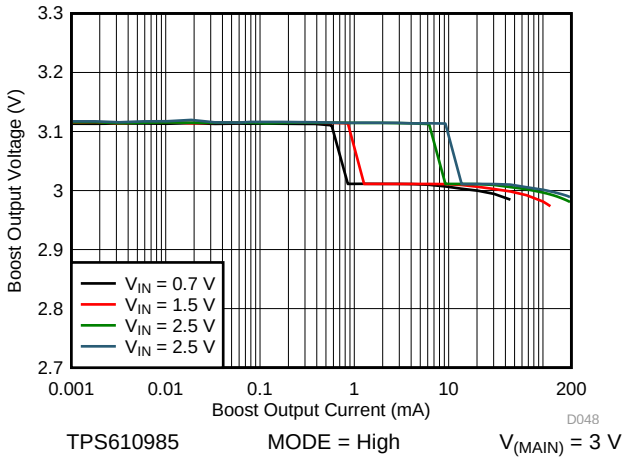
TPS610982 MODE = High $V_{(MAIN)}$ = 3.3 V

Figure 33. Boost Load Regulation (Active Mode)



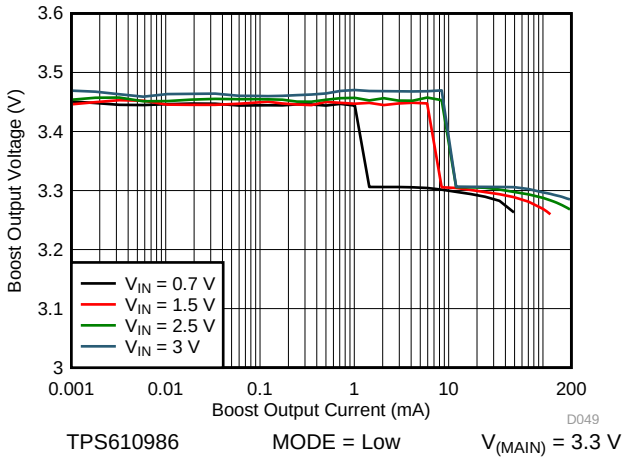
TPS610985 MODE = Low $V_{(MAIN)}$ = 3 V

Figure 34. Boost Load Regulation (Low Power Mode)



TPS610985 MODE = High $V_{(MAIN)}$ = 3 V

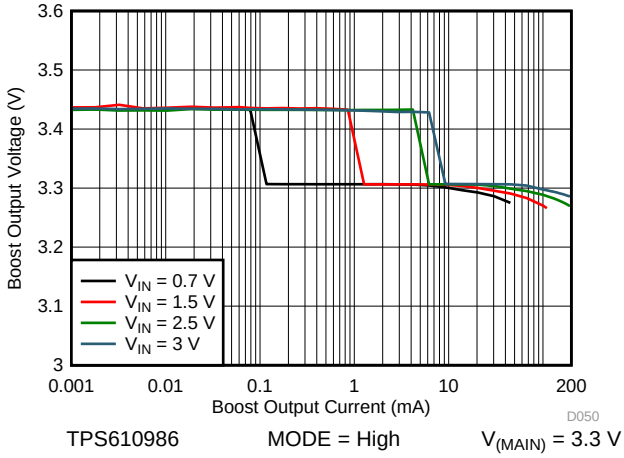
Figure 35. Boost Load Regulation (Active Mode)



TPS610986 MODE = Low $V_{(MAIN)}$ = 3.3 V

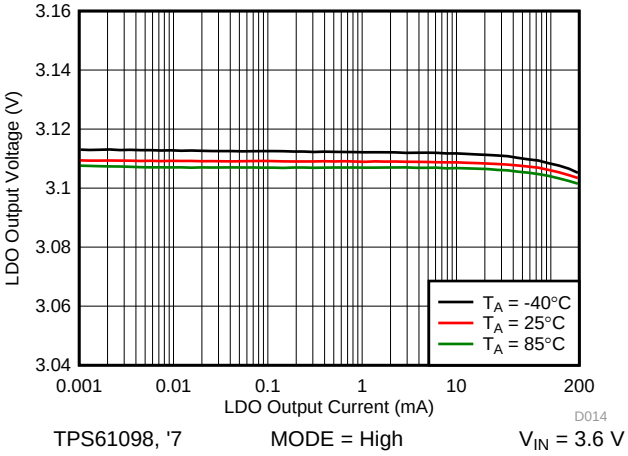
Figure 36. Boost Load Regulation (Low Power Mode)

Typical Characteristics (continued)



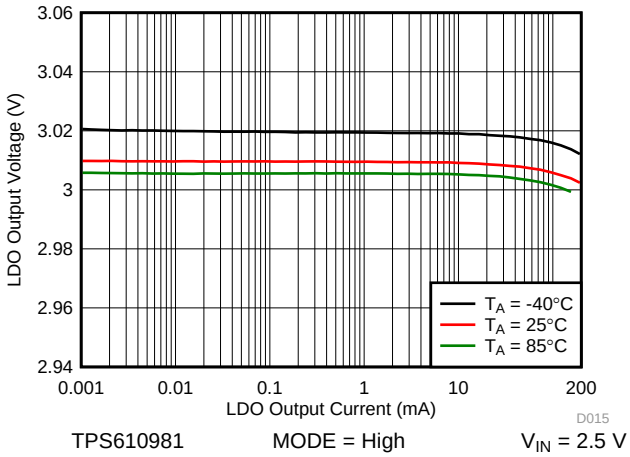
TPS610986 MODE = High $V_{(MAIN)}$ = 3.3 V

Figure 37. Boost Load Regulation (Active Mode)



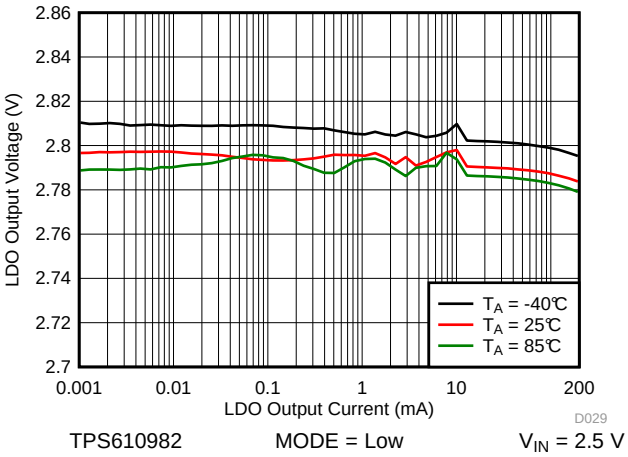
TPS61098, '7 MODE = High V_{IN} = 3.6 V

Figure 38. LDO Load Regulation



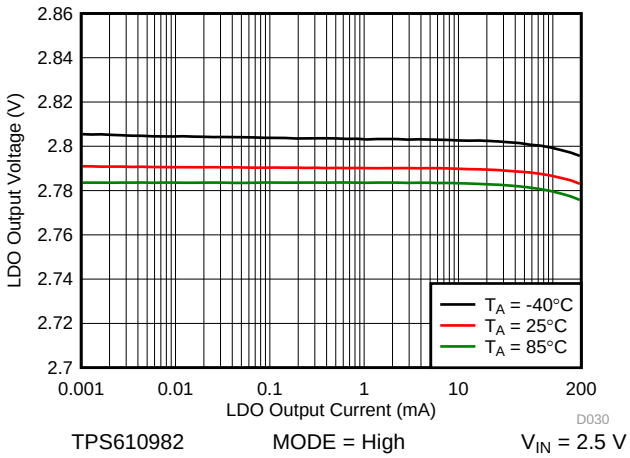
TPS610981 MODE = High V_{IN} = 2.5 V

Figure 39. LDO Load Regulation



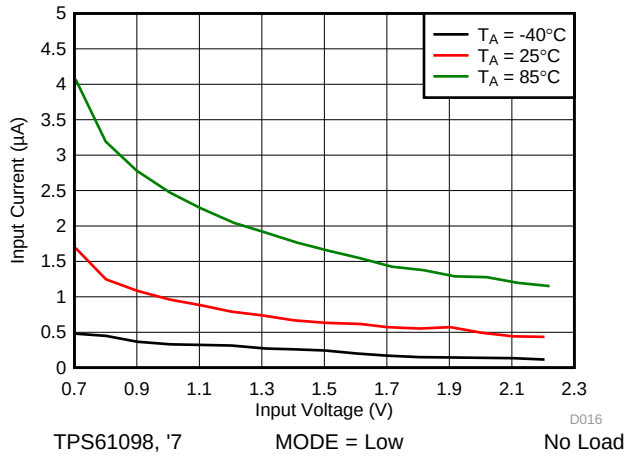
TPS610982 MODE = Low V_{IN} = 2.5 V

Figure 40. LDO Load Regulation (Low Power Mode)



TPS610982 MODE = High V_{IN} = 2.5 V

Figure 41. LDO Load Regulation (Active Mode)



TPS61098, '7 MODE = Low No Load

Figure 42. Input Current vs Input Voltage (Low Power Mode)

Typical Characteristics (continued)

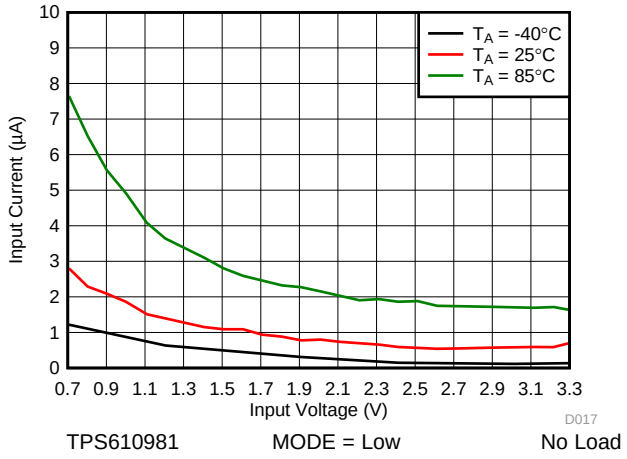


Figure 43. Input Current vs Input Voltage (Low Power Mode)

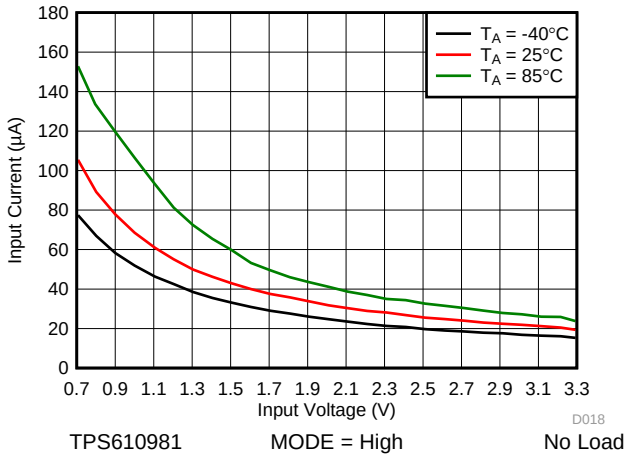


Figure 44. Input Current vs Input Voltage (Active Mode)

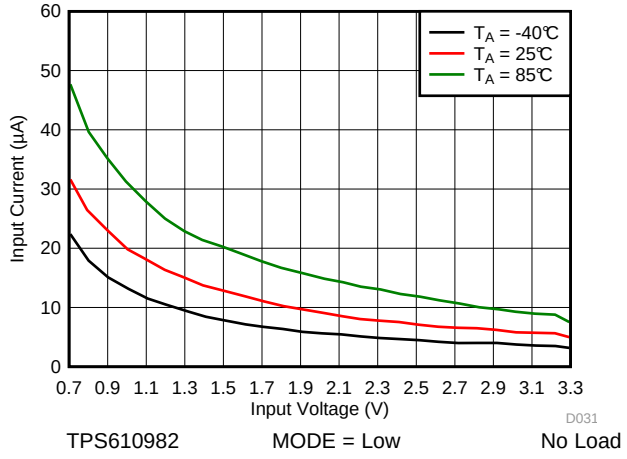


Figure 45. No Load Input Current vs Input Voltage (Low Power Mode)

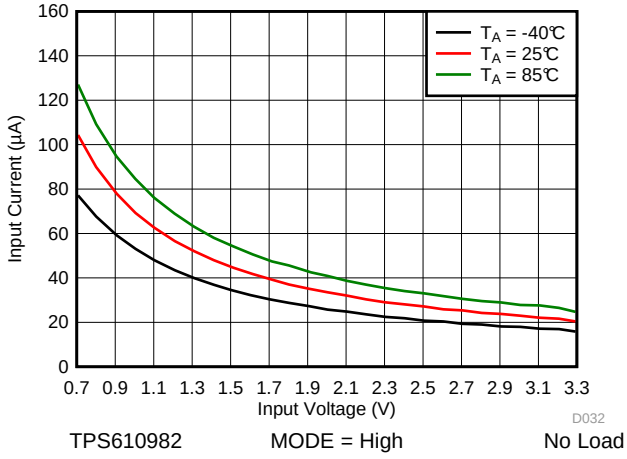


Figure 46. No Load Input Current vs Input Voltage (Active Mode)

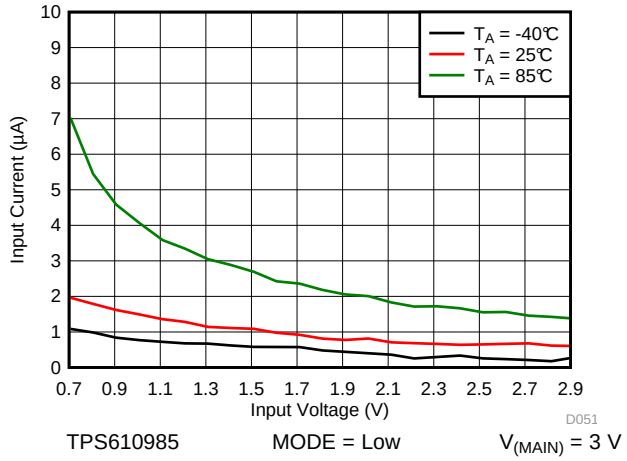


Figure 47. Input Current vs Input Voltage (Low Power Mode)

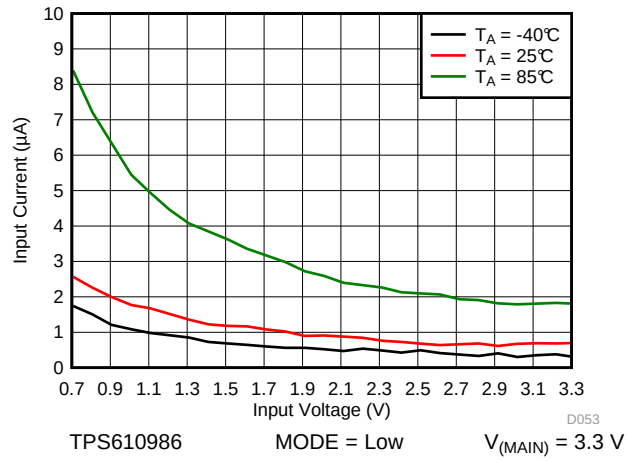
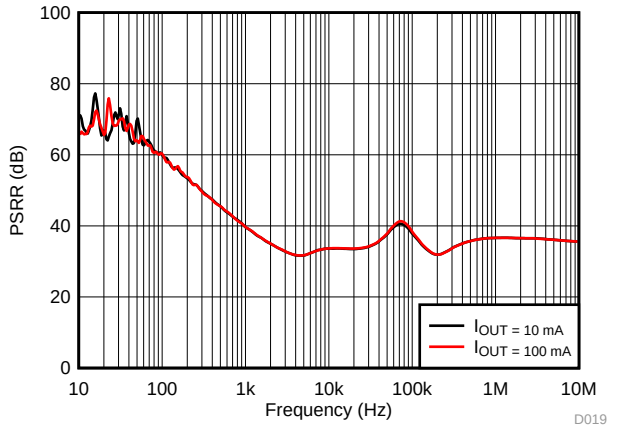


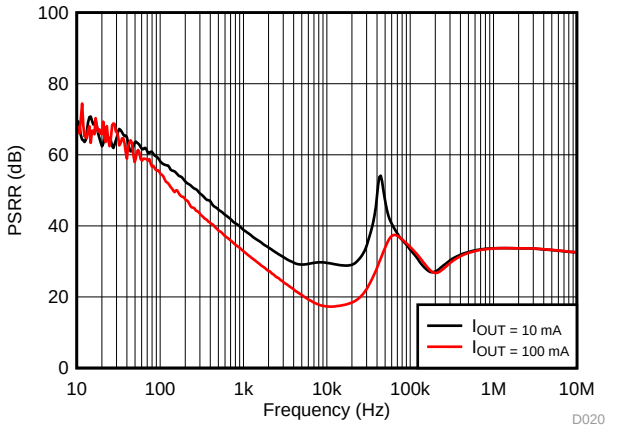
Figure 48. Input Current vs Input Voltage (Low Power Mode)

Typical Characteristics (continued)



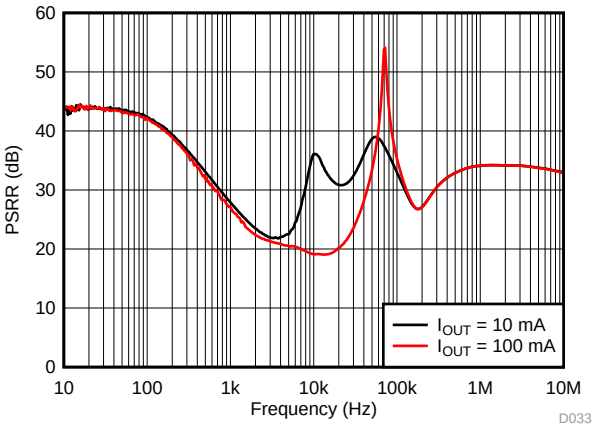
TPS61098. '7 MODE = High C_{O2} = 10 µF
V_{IN} - V_{OUT} = 4.3 V - 3.1 V = 1.2 V

Figure 49. LDO PSRR vs Frequency



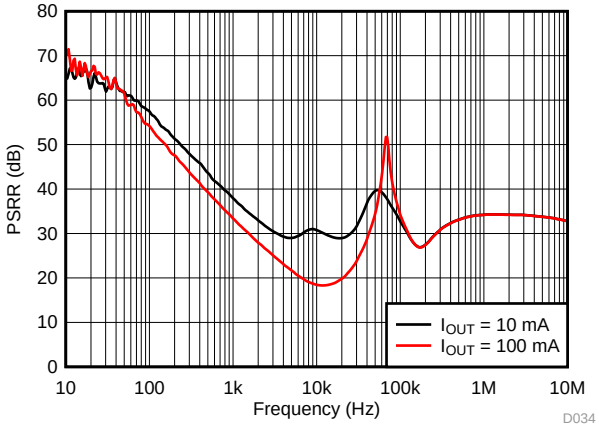
TPS610981 MODE = High C_{O2} = 10 µF
V_{IN} - V_{OUT} = 3.3 V - 3 V = 0.3 V

Figure 50. LDO PSRR vs Frequency



TPS610982 MODE = Low C_{O2} = 10 µF
V_{IN} - V_{OUT} = 3.3 V - 2.8 V = 0.5 V

Figure 51. LDO PSRR vs Frequency (Low Power Mode)



TPS610982 MODE = High C_{O2} = 10 µF
V_{IN} - V_{OUT} = 3.3 V - 2.8 V = 0.5 V

Figure 52. LDO PSRR vs Frequency (Active Mode)

8 Detailed Description

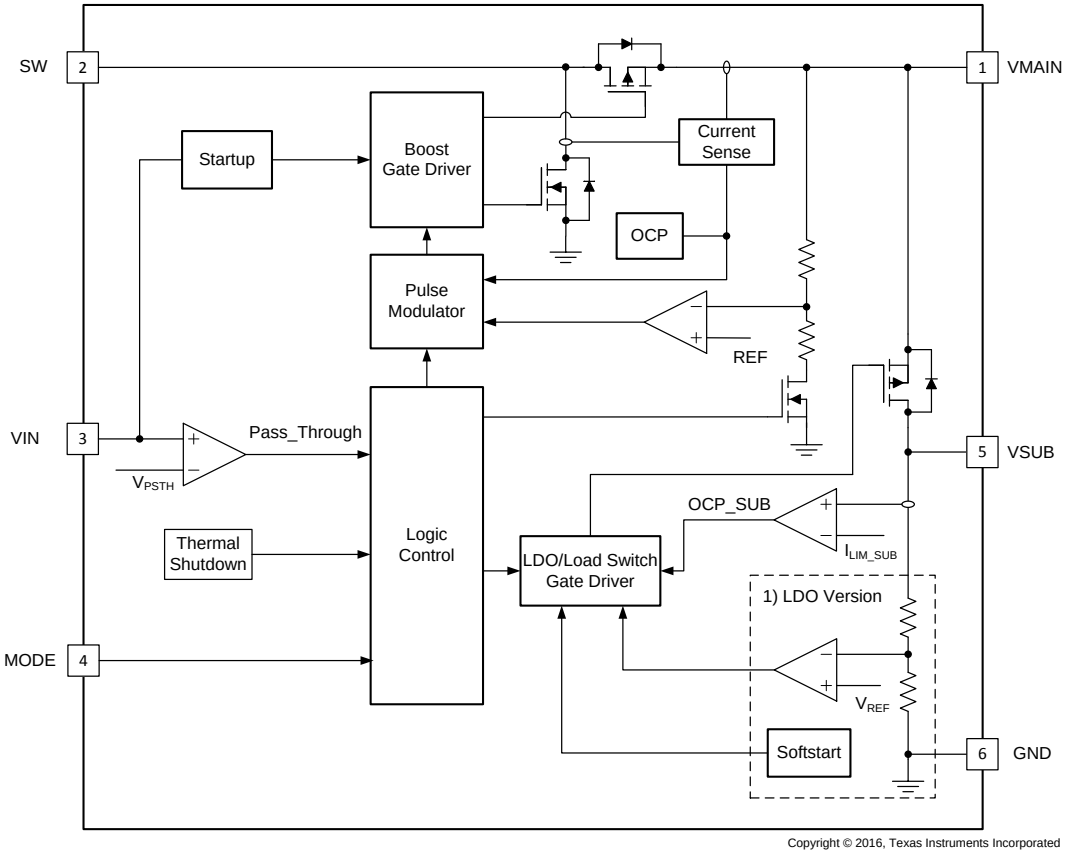
8.1 Overview

The TPS61098x is an ultra low power solution optimized for products powered by either a one-cell or two-cell alkaline, NiCd or NiMH, one-cell coin cell battery or one-cell Li-Ion or Li-polymer battery. To simplify system design and save PCB space, the TPS61098x integrates an LDO or load switch with a boost converter (different configurations for different versions) to provide two output rails in a compact package. The boost output $V_{(MAIN)}$ is designed as an always-on supply to power a main system, and the LDO or load switch output $V_{(SUB)}$ is designed to power peripheral devices and can be turned off.

The TPS61098x features two modes controlled by MODE pin: Active mode and Low Power mode. In Active mode, both outputs are enabled, and the transient response performance of the boost converter and LDO/load switch are enhanced, so it is able to respond load transient quickly. In Low Power mode, the LDO/load switch is disabled, so the peripherals can be disconnected to minimize the battery drain. Besides that, the boost consumes only 300 nA quiescent current in Low Power mode, so up to 88% efficiency at 10 µA load can be achieved to extend the battery run time. The TPS610982 is an exception. Its LDO is always on in both Active mode and Low Power mode. The main differences between the two modes of the TPS610982 are the quiescent current and performance. Refer to *Operation Modes by MODE Pin* for details.

The TPS61098x supports automatic pass-through function in both Active mode and Low Power mode. When V_{IN} is detected higher than a pass-through threshold, which is around the target $V_{(MAIN)}$ voltage, the boost converter stops switching and passes the input voltage through inductor and internal rectifier switch to $V_{(MAIN)}$, so $V_{(MAIN)}$ follows V_{IN}; when V_{IN} is lower than the threshold, the boost works in boost mode and regulates $V_{(MAIN)}$ at the target value. The TPS61098x can support different $V_{(MAIN)}$ target values in Active mode and Low Power mode to meet various requirements. For example, for TPS61098, the set value of $V_{(MAIN)}$ is 4.3 V in Active mode but 2.2 V in Low Power mode.

8.2 Functional Block Diagrams



(1) Implemented in versions with LDO configuration.

8.3 Feature Description

8.3.1 Boost Controller Operation

The TPS61098x boost converter is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 100 mA and adjusting the offset of this inductor current depending on the output load. Since the input voltage, output voltage and inductor value all affect the rising and falling slopes of inductor ripple current, the switching frequency is not fixed and is decided by the operation condition. If the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current goes discontinuous to keep the efficiency high under light load conditions. Figure 53 illustrates the hysteretic current operation. If the load is reduced further, the boost converter enters into Burst mode. In Burst mode, the boost converter ramps up the output voltage with several pulses and it stops operating once the output voltage exceeds a set threshold, and then it goes into a sleep status and consumes less quiescent current. It resumes switching when the output voltage is below the set threshold. It exits the Burst mode when the output current can no longer be supported in this mode. Refer to Figure 54 for Burst mode operation details.

To achieve high efficiency, the power stage is realized as a synchronous boost topology. The output voltage $V_{(MAIN)}$ is monitored via an internal feedback network which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly.

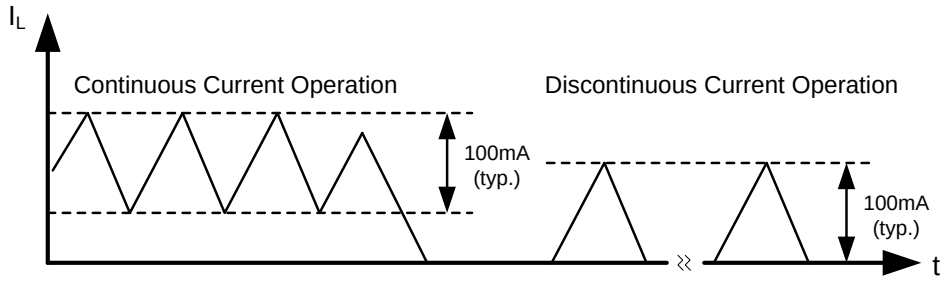


Figure 53. Hysteretic Current Operation

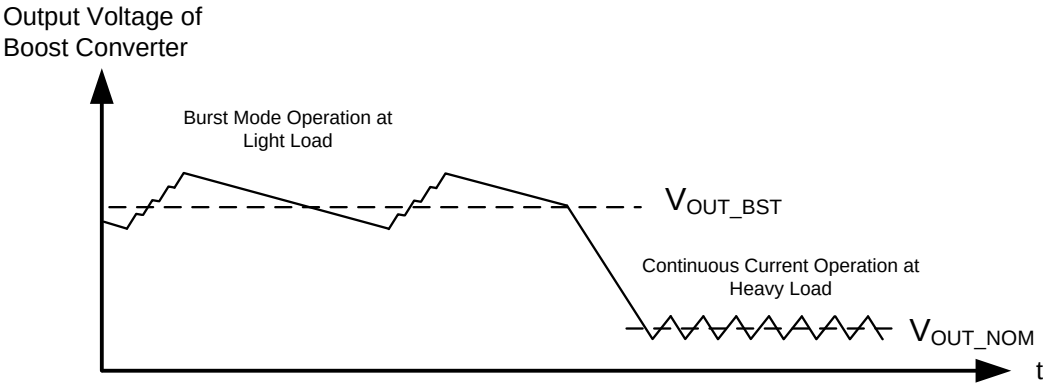


Figure 54. Burst Mode Operation

8.3.2 Pass-Through Operation

The TPS61098x supports automatic pass-through function for the boost converter. When the input voltage is detected higher than the pass-through threshold $V_{(PSTH)}$, which is around $V_{(MAIN)}$ set value, the boost converter enters into pass-through operation mode. In this mode, the boost converter stops switching, the rectifier is constantly turned on and the low side switch is turned off. The input voltage passes through external inductor and the internal rectifier to the output. The output voltage in this mode depends on the resistance between the input and the output, calculated as Equation 1:

$$V_{MAIN} = V_{IN} - (I_{MAIN} + I_{SUB}) \times (R_L + R_{DSon\_HS}) \quad (1)$$

where R_L is the DCR of external inductor, and $R_{DS(on)\_HS}$ is the resistance of internal rectifier.

Feature Description (continued)

When the input voltage is lower than $V_{(PSTH)}$, the boost converter resumes switching to regulate the output at target value.

The TPS61098x can support automatic pass-through function in both Active mode and Low Power mode.

8.3.3 LDO / Load Switch Operation

The TPS61098x uses a PMOS as a pass element of its integrated LDO / load switch. The input of the PMOS is connected to the output of the boost converter. When the MODE pin is pulled logic high, the PMOS is enabled to output a voltage on VSUB pin.

For load switch version, the PMOS pass element is fully turned on when enabled, no matter the boost converter works in boost operation mode or pass-through operation mode. So the output voltage at VSUB pin is decided by the output voltage at VMAIN pin and the current passing through the PMOS as Equation 2:

$$V_{SUB} = V_{MAIN} - I_{SUB} \times R_{LS} \quad (2)$$

where $I_{(SUB)}$ is the load of VSUB rail and the R_{LS} is the resistance of the PMOS when it is fully turned on.

For LDO version, the output voltage $V_{(SUB)}$ is regulated at the set value when the voltage difference between its input and output is higher than the dropout voltage $V_{(Dropout)}$, no matter the boost converter works in boost operation mode or pass-through operation mode. The $V_{(SUB)}$ is monitored via an internal feedback network which is connected to the voltage error amplifier. To regulate $V_{(SUB)}$, the voltage error amplifier compares the feedback voltage to the internal voltage reference and adjusts the gate voltage of the PMOS accordingly. When the voltage drop across the PMOS is lower than the dropout voltage, the PMOS will be fully turned on and the output voltage at $V_{(SUB)}$ is decided by Equation 2.

When the MODE pin is pulled low, the LDO or load switch is turned off to disconnect the load at VSUB pin. For some versions, active discharge function at VSUB pin is offered, which can discharge the $V_{(SUB)}$ to ground after MODE pin is pulled low, to avoid any bias condition to downstream devices. For versions without the active discharge function, the VSUB pin is floating after MODE pin is pulled low, and its voltage normally drops down slowly due to leakage. Refer to the *Device Comparison Table* for version differences.

When MODE pin is toggled from low to high, soft-start is implemented for the LDO versions to avoid inrush current during LDO startup. The start up time of LDO is typically 1 ms. For load switch versions, the load switch is turned on faster, so the output capacitor at VSUB pin is suggested 10X smaller than the output capacitor at VMAIN pin to avoid obvious voltage drop of $V_{(MAIN)}$ during load switch turning on process.

8.3.4 Start Up and Power Down

The boost converter of the TPS61098x is designed always-on, so there is no enable or disable control of it. The boost converter starts operation once input voltage is applied. If the input voltage is not high enough, a low voltage startup oscillator operates the switches first. During this phase, the switching frequency is controlled by the oscillator, and the maximum switch current is limited. Once the converter has built up the output voltage $V_{(MAIN)}$ to approximately 1.8 V, the device switches to the normal hysteretic current mode operation and the VMAIN rail starts to supply the internal control circuit. If the input voltage is too low or the load during startup is too heavy, which makes the converter unable to build up 1.8 V at $V_{(MAIN)}$ rail, the boost converter can't start up successfully. It will keep in this status until the input voltage is increased or removed.

The TPS61098x is able to startup with 0.7 V input voltage with ≥ 3 kΩ load. The startup time depends on input voltage and load conditions. After the $V_{(MAIN)}$ reaches 1.8 V to start the normal hysteretic current mode operation, an internal ramp-up reference controls soft-start time of the boost converter until $V_{(MAIN)}$ reaches its set value.

The TPS61098x does not support undervoltage lockout function. When the input voltage drops to a low voltage and can't provide the required energy to the boost converter, the $V_{(MAIN)}$ drops. When and to what extent $V_{(MAIN)}$ drops are dependent on the input and load conditions. When the boost converter is unable to maintain 1.8 V at VMAIN rail to supply the internal circuit, the TPS61098x powers down and enters into startup process again.

Feature Description (continued)

8.3.5 Over Load Protection

The boost converter of the TPS61098x supports a cycle-by-cycle current limit function in boost mode operation. If the peak inductor current reaches the internal switch current limit threshold, the main switch is turned off to stop a further increase of the input current. In this case the output voltage will decrease since the device cannot provide sufficient power to maintain the set output voltage. If the output voltage drops below the input voltage, the backgate diode of the rectifying switch gets forward biased and current starts to flow through it. Because this diode cannot be turned off, the load current is only limited by the remaining DC resistance. After the overload condition is removed, the converter automatically resumes normal operation.

The overload protection is not active in pass-through mode operation, in which the load current is only limited by the DC resistance.

The integrated LDO / load switch also supports over load protection. When the load current of VSUB rail reaches the I_{LIM_SUB}, the $V_{(SUB)}$ output current will be regulated at this limit value and will not increase further. In this case the $V_{(SUB)}$ voltage will decrease since the device cannot provide sufficient power to the load.

8.3.6 Thermal Shutdown

The TPS61098x has a built-in temperature sensor which monitors the internal junction temperature in boost mode operation. If the junction temperature exceeds the threshold (150°C typical), the device stops operating. As soon as the junction temperature has decreased below the programmed threshold with a hysteresis, it starts operating again. There is a built-in hysteresis (25°C typical) to avoid unstable operation at the overtemperature threshold. The over temperature protection is not active in pass-through mode operation.

8.4 Device Functional Modes

8.4.1 Operation Modes by MODE Pin

The TPS61098x features two operation modes controlled by MODE pin: the Active mode and Low Power mode. It can provide quick transient response in Active mode and ultra-low quiescent current in Low Power mode. So a low power system can easily use the TPS61098x to get high performance in its active mode and meantime minimize its power consumption to extend the battery run time in its sleep mode.

The MODE pin is usually controlled by an I/O pin of a controller, and should not be left floating.

8.4.1.1 Active Mode

The TPS61098x works in Active mode when MODE pin is logic high. In Active mode, both of the boost converter and the integrated LDO/load switch are enabled, and the TPS61098x can provide dual outputs simultaneously. The transient response performance of the boost converter is enhanced in Active mode, and the device consumes around 15 µA quiescent current. It is able to respond load transient quickly.

When MODE pin is toggled from low to high, soft-start is implemented for the LDO versions to avoid inrush current during startup. For load switch versions, the load switch is turned on faster, so the output capacitor at VSUB pin is suggested 10X smaller than the output capacitor at VMAIN pin to avoid obvious voltage drop of $V_{(MAIN)}$ during turning on process.

8.4.1.2 Low Power Mode

The TPS61098x works in Low Power mode when MODE pin is logic low. In Low Power mode, the LDO/load switch is turned off, so the peripherals can be disconnected to minimize the battery drain. The VSUB pin either outputs high impedance or is pulled to ground by internal active discharge circuit, depending on different versions. The boost converter consumes only 300 nA quiescent current typically, and can achieve up to 88% efficiency at 10 µA load.

The Low Power mode is designed to keep the load device powered with minimum power consumption. For example, it can be used to keep powering the main system, like an MCU, in a system's sleep mode even under < 0.7 V input voltage condition.

Figure 55 and Figure 56 illustrate the outputs of the TPS61098 and TPS610981 under different input voltages in Active mode and Low Power mode.

Device Functional Modes (continued)

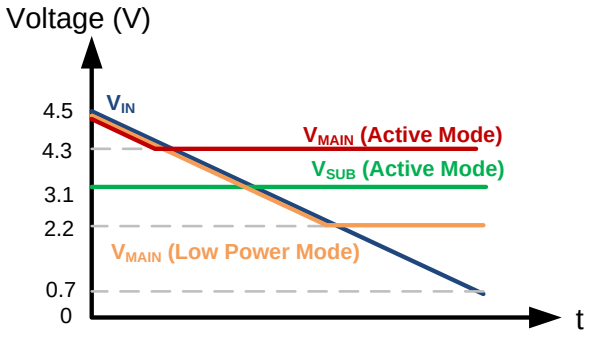


Figure 55. TPS61098 Output under Different Input Voltages

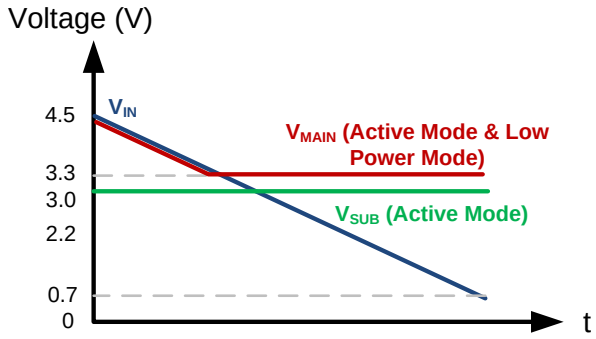


Figure 56. TPS610981 Output under Different Input Voltages

The TPS610982 is an exception. Its LDO is always on in both Active mode and Low Power mode with higher quiescent current consumption than other versions. The TPS610982 can be used to replace discrete boost and LDO solutions where the LDO output is always on, and its two modes provide users two options of different quiescent current consumption and performance. Refer to the *Device Comparison Table*, *Specifications* and *Typical Characteristics* for details.

8.4.2 Burst Mode Operation under Light Load Condition

The boost converter of TPS61098x enters into Burst Mode operation under light load condition. Refer to *Boost Controller Operation* for details.

8.4.3 Pass-Through Mode Operation

The boost converter of TPS61098x automatically enters into pass-through mode operation when input voltage is higher than the target output voltage. Refer to *Pass-Through Operation* for details.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61098x is an ultra low power solution for products powered by either a one-cell or two-cell alkaline, NiCd or NiMH, one-cell coin cell or one-cell Li-Ion or Li-polymer battery. It integrates either a Low-dropout Linear Regulator (LDO) or a load switch with a boost converter and provides dual output rails. The $V_{(MAIN)}$ rail is the output of the boost converter. It is an always-on output and can only be turned off by removing input voltage. The $V_{(SUB)}$ rail is the output of the integrated LDO or load switch, and it can be turned off by pulling the MODE pin low.

9.2 Typical Applications

9.2.1 VMAIN to Power MCU and VSUB to Power Subsystem

The TPS61098x suits for low power systems very well, especially for the system which spends the most of time in sleep mode and wakes up periodically to sense or transmit signals. For this kind of application, the boost output $V_{(MAIN)}$ can be used as an always-on supply for the main system, such as an MCU controller, and the LDO or load switch output $V_{(SUB)}$ is used to power peripheral devices or subsystem.

As shown in Figure 57, the MCU can control both of the subsystem and the TPS61098x. When the system goes into sleep mode, the MCU can disable the subsystem first, and then force the TPS61098x enter into Low Power mode, where the VSUB rail is disconnected but the $V_{(MAIN)}$ rail still powers the MCU with only 300 nA quiescent current. When the system wakes up, the MCU pulls the MODE pin of TPS61098x high first to turn on the VSUB rail, and then enables the subsystem. In this way, the system can benefit both of the enhanced transient response performance in active mode and the ultra-low quiescent current in sleep mode.

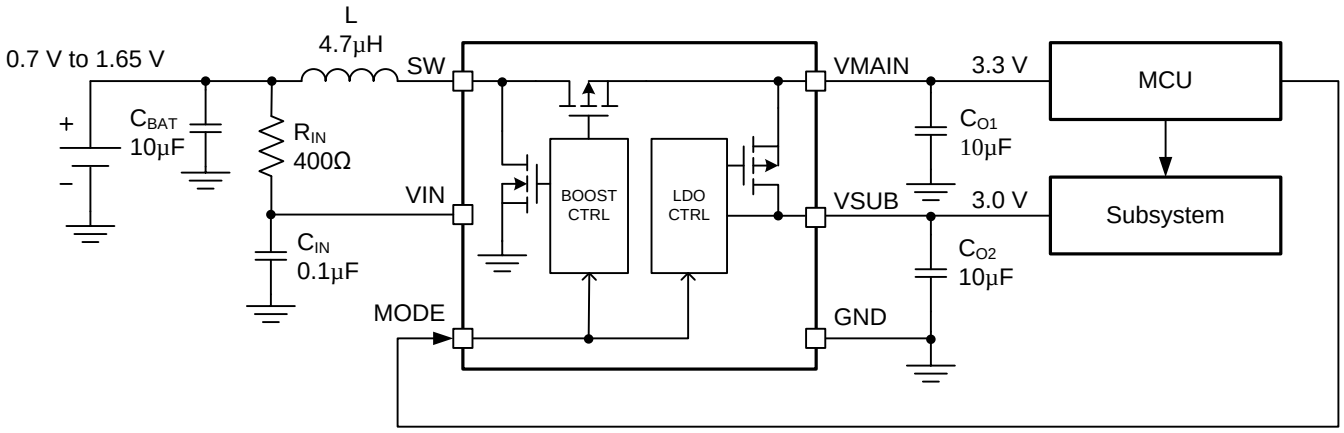


Figure 57. Typical Application of TPS610981 to Power Low Power System

9.2.1.1 Design Requirements

- 3.3 V $V_{(MAIN)}$ rail to power MCU with 15 mA load current, 3 V $V_{(SUB)}$ rail to power subsystem with 10 mA load current
- Power source, single-cell alkaline battery (0.7 V to 1.65 V range)
- Greater than 90% conversion efficiency

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Device Choice

In the TPS61098x family, different versions are provided. Refer to *Device Comparison Table* for version details and select the right version for target applications. It is OK to use only one output rail, either $V_{(MAIN)}$ or $V_{(BUS)}$, as long as it suits the application.

In this example, dual rails of 3.3 V and 3 V are required to power both MCU and subsystem, so the TPS610981 is selected.

9.2.1.2.2 Maximum Output Current

For the boost converter, it provides output current for both $V_{(MAIN)}$ and $V_{(SUB)}$ rails. Its maximum output capability is determined by the input to output ratio and the current limit of the boost converter and can be estimated by Equation 3.

$$I_{OUT(max)} = \frac{V_{IN} \times (I_{LIM\_BST} - 50mA) \times \eta}{V_{MAIN}} \quad (3)$$

where η is the boost converter power efficiency estimation, and 50 mA is half of the inductor current ripple value. Minimum input voltage, maximum boost output voltage and minimum current limit I_{LIM_BST} should be used as the worst case condition for the estimation.

Internal current limit is also implemented for the integrated LDO/load switch. So the maximum output current of VSUB rail should be lower than I_{LIM_SUB}, which has 200 mA minimum value. For LDO version, the maximum output current is also limited by its input to output headroom, that is $V_{(MAIN)}$ - $V_{(SUB)}$. Make sure the headroom voltage is enough to support the load current. Please refer to *Electrical Characteristics* for the dropout voltage information.

In this example, assume the power efficiency is 80% (lower than typical value for the worst case estimation), so the calculated maximum output current of the boost converter is 50.9 mA, which satisfies the application requirements (15 mA + 10 mA). The load of VSUB rail is 10 mA, which is well below the $V_{(SUB)}$ rail current limit and the dropout voltage is also within the headroom.

9.2.1.2.3 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The TPS61098x is designed to work with inductor values between 2.2 µH and 4.7 µH. The inductance values affects the switching frequency *f* in continuous current operation, which is proportional to 1/L as shown in Equation 4.

$$f = \frac{1}{L \times 100mA} \times \frac{V_{IN} \times (V_{MAIN} - V_{IN} \times \eta)}{V_{MAIN}} \quad (4)$$

The inductor current ripple is fixed to 100mA typical value by internal design, but it can be affected by the inductor value indirectly. Normally when a smaller inductor value is applied, the inductor current ramps up and down more quickly, so the current ripple becomes bigger because the internal current comparator has some delay to respond. So if smaller inductor peak current is required in applications, a higher inductor value can be tried. However, the TPS61098x is optimized to work within a range of L and C combinations. The LC output filter inductance and capacitance must be considered together. The output capacitor sets the corner frequency of the converter while the inductor creates a Right-Half-Plane-Zero degrading the stability of the converter. Consequently with a larger inductor, a bigger capacitor normally should be used to ensure the same L/C ratio thus a stable loop.

Having selected an inductance value, the peak current for the inductor in steady-state operation varies as a function of the load, the input and output voltages and can be estimated using Equation 5.

Typical Applications (continued)

$$I_{L,MAX} = \frac{V_{MAIN} \times (I_{MAIN} + I_{SUB})}{V_{IN} \times \eta} + 50mA; \quad \text{continuous current operation}$$
$$I_{L,MAX} = 100mA; \quad \text{discontinuous current operation} \tag{5}$$

where, 80% can be used for the boost converter power efficiency estimation, 100 mA is the typical inductor current ripple value and 50mA is half of the ripple value, which may be affected a little bit by inductor value. Equation 5 provides a suitable inductor current rating by using minimum input voltage, maximum boost output voltage and maximum load current for the calculation. Load transients and error conditions may cause higher inductor currents.

Equation 6 provides an easy way to estimate whether the device will work in continuous or discontinuous operation depending on the operating points. As long as the Equation 6 is true, continuous operation is typically established. If Equation 6 becomes false, discontinuous operation is typically established.

$$\frac{V_{MAIN} \times (I_{MAIN} + I_{SUB})}{V_{IN} \times \eta} > 50mA \tag{6}$$

Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce it's reliability.

In this example, the maximum load for the boost converter is 25 mA, and the minimum input voltage is 0.7 V, and the efficiency under this condition can be estimated at 80%, so the boost converter works in continuous operation by the calculation. The inductor peak current is calculated as 197 mA. To leave some margin, a 4.7 µH inductor with at least 250 mA saturation current is recommended for this application.

Table 1 also lists the recommended inductor for the TPS61098x device.

Table 1. List of Inductors

INDUCTANCE [µH]	ISAT [A]	IRMS [A]	DC RESISTANCE [mΩ]	PART NUMBER	MANUFACTURER
4.7	0.86	1.08	168	VLF302510MT-4R7M	TDK
4.7	0.57	0.95	300	VLF252010MT-4R7M	TDK
2.2	1.23	1.5	84	VLF302510MT-2R2M	TDK
2.2	0.83	0.92	120	VLF252010MT-2R2M	TDK

9.2.1.2.4 Capacitor Selection

For best output and input voltage filtering, low ESR X5R or X7R ceramic capacitors are recommended.

The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. An input capacitor value of at least 10 µF is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended. For applications where line transient is expected, an input filter composed of 400-Ω resistor and 0.1-µF capacitor as shown in Figure 57 is mandatory to avoid interference to internal pass-through threshold comparison circuitry.

For the output capacitor of VMAIN pin, small ceramic capacitors are recommended, placed as close as possible to the VMAIN and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, the use of a small ceramic capacitor with a capacitance value of around 2.2 µF in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VMAIN and GND pins of the IC. The recommended typical output capacitor values are 10 µF and 22 µF (nominal values).

For LDO version, like all low dropout regulators, VSUB rail requires an output capacitor connected between VSUB and GND pins to stabilize the internal control loop. Ceramic capacitor of 10 µF (nominal value) is recommended for most applications. If the $V_{(SUB)}$ drop during load transient is much cared, higher capacitance value up to 22 µF is recommended to provide better load transient performance. Capacitor below 10 µF is only recommended for light load operation. For load switch version, capacitor of 10x smaller value than capacitor at VMAIN pin is recommended to minimize the voltage drop caused by charge sharing when the load switch is turned on.

When selecting capacitors, ceramic capacitor's derating effect under bias should be considered. Choose the right nominal capacitance by checking capacitor's DC bias characteristics. In this example, GRM188R60J106ME84D, which is a 10 µF ceramic capacitor with high effective capacitance value at DC biased condition, is selected for both VMAIN and VSUB rails. The load transient response performance is shown in Application Curves section.

For load switch version, VSUB rails requires an output capacitor connected between VSUB and GND pins. Ceramic capacitor of 1 µF (nominal value) is recommended for most applications.

9.2.1.2.5 Control Sequence

In this example, the MCU is powered by the boost output $V_{(MAIN)}$ and the subsystem is powered by the LDO $V_{(SUB)}$. MCU controls both of the TPS610981 and subsystem. The control sequence as shown in Figure 58 is recommended.

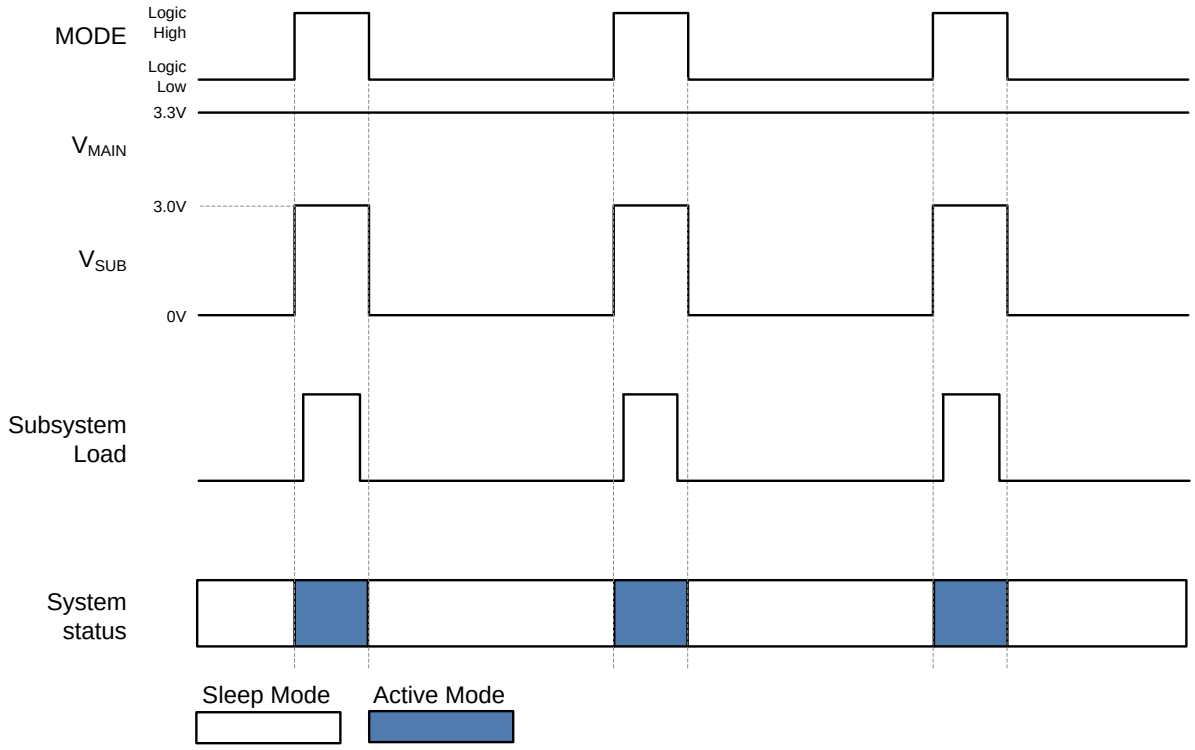
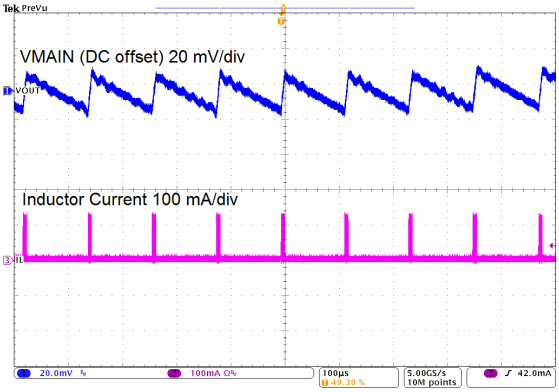


Figure 58. System Control Sequence

When the system is waking up, the MCU wakes up itself first, and it then pulls the MODE pin of TPS610981 to high to turned on the $V_{(SUB)}$ rail. TPS610981 enters into Active mode and gets ready to provide power to the subsystem. Then the MCU enables the subsystem.

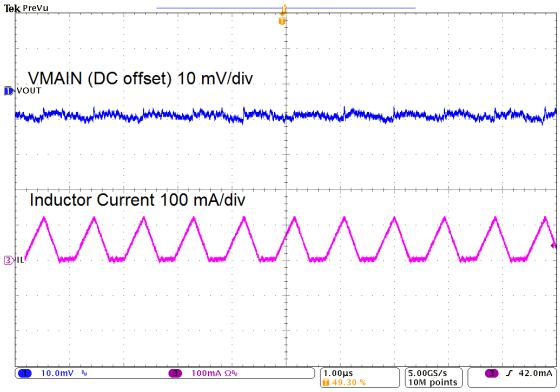
When the system is entering into sleep mode, the MCU disables the subsystem first and then pulls the MODE pin to low to turn off the $V_{(SUB)}$, so the subsystem is disconnected from the supply to minimize the current drain. TPS610981 enters into Low Power mode and the VMAIN rail still powers the MCU with only 300 nA quiescent current. The MCU enters into sleep mode itself finally.

9.2.1.3 Application Curves



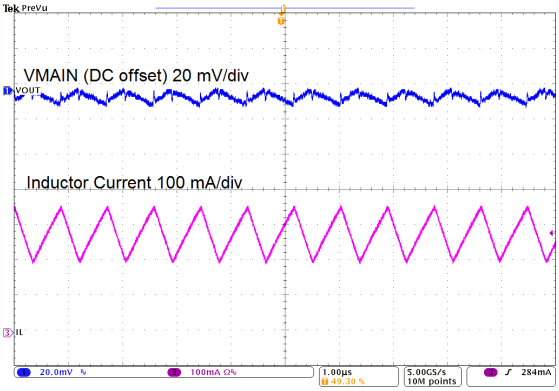
TPS610981 $I_{(MAIN)}$ = 1 mA $I_{(SUB)}$ = 0 mA
MODE = L VI_N = 1.5 V

Figure 59. Switching Waveforms



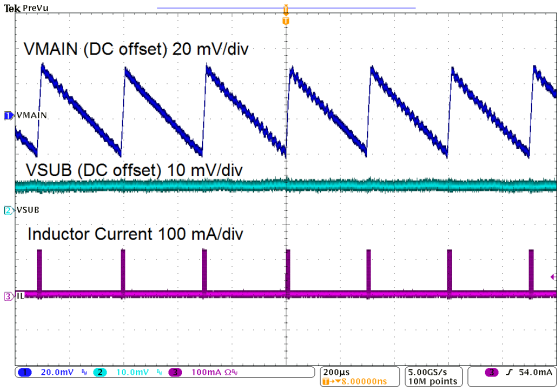
TPS610981 $I_{(MAIN)}$ = 10 mA $I_{(SUB)}$ = 0 mA
MODE = L V_{IN} = 1.5 V

Figure 60. Switching Waveforms



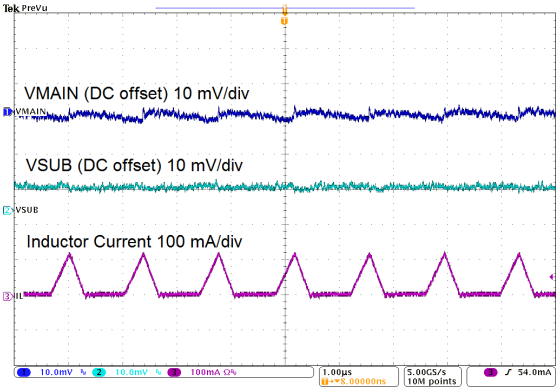
TPS610981 $I_{(MAIN)}$ = 100 mA $I_{(SUB)}$ = 0 mA
MODE = L V_{IN} = 1.5 V

Figure 61. Switching Waveforms



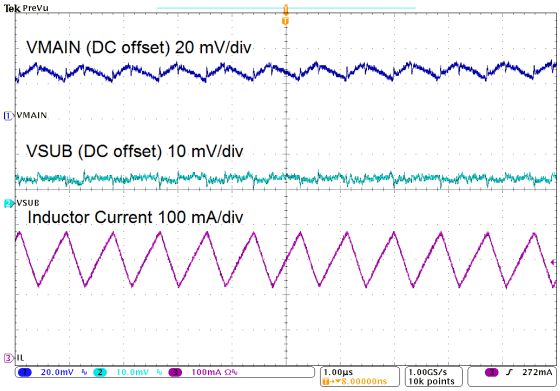
TPS610981 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 1 mA
MODE = H V_{IN} = 1.5 V

Figure 62. Switching Waveforms



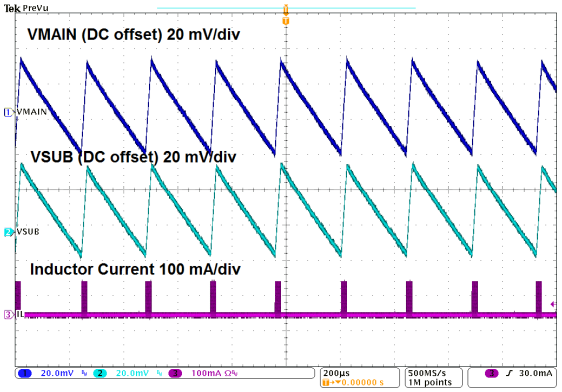
TPS610981 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 10 mA
MODE = H V_{IN} = 1.5 V

Figure 63. Switching Waveforms



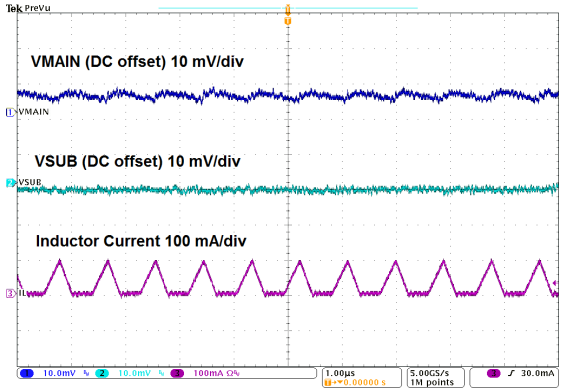
TPS610981 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 100 mA
MODE = H V_{IN} = 1.5V

Figure 64. Switching Waveforms



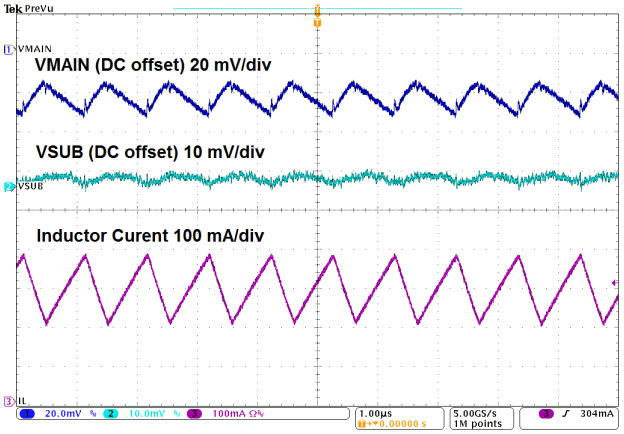
TPS610896 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 1 mA
MODE = H V_{IN} = 1.5V

Figure 65. Switching Waveforms



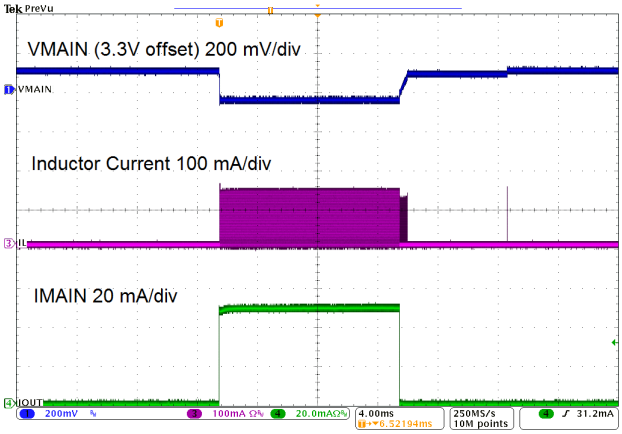
TPS610896 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 10 mA
MODE = H V_{IN} = 1.5V

Figure 66. Switching Waveforms



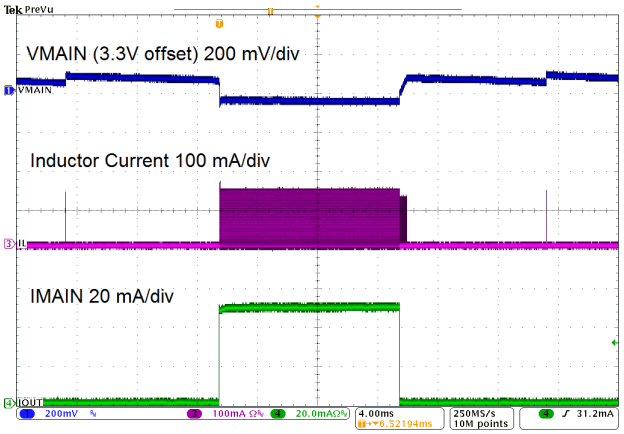
TPS610896 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 100 mA
MODE = H V_{IN} = 1.5V

Figure 67. Switching Waveforms



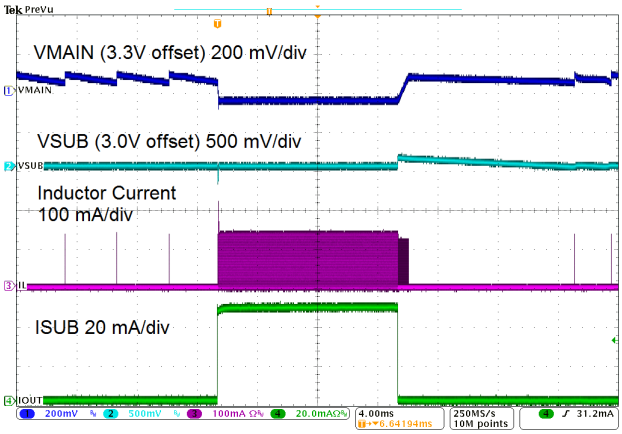
TPS610981 V_{IN} = 2.5 V $I_{(SUB)}$ = 0 mA
MODE = L $I_{(MAIN)}$ = 0 mA to 50 mA, 5 µs rising/falling edge

Figure 68. Load Transient Response



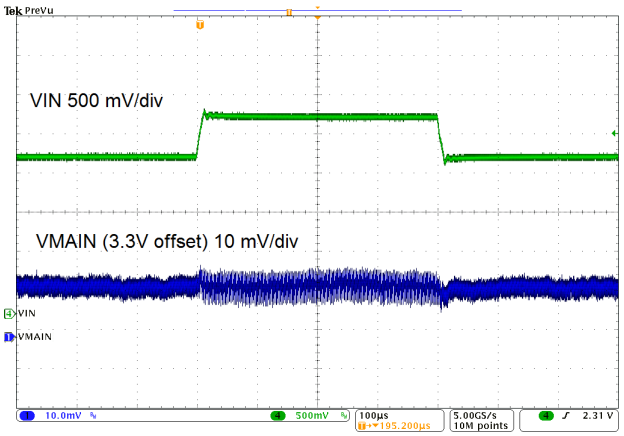
TPS610981 V_{IN} = 2.5 V $I_{(SUB)}$ = 0 mA
MODE = H $I_{(MAIN)}$ = 0 mA to 50 mA, 5 µs rising/falling edge

Figure 69. Load Transient Response



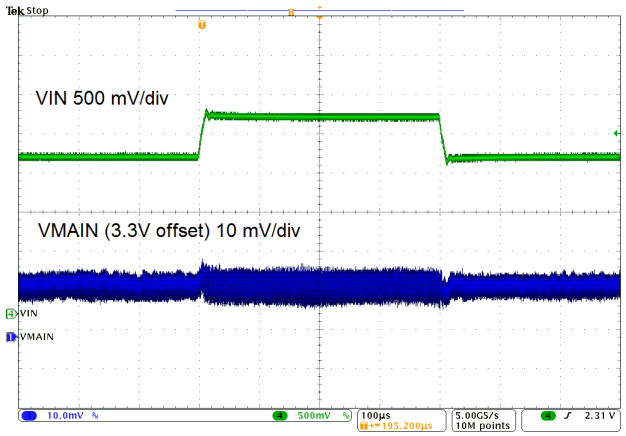
TPS610981 V_{IN} = 2.5 V $I_{(MAIN)}$ = 0 mA
MODE = H $I_{(SUB)}$ = 0 mA to 50 mA, 5 µs rising/falling edge

Figure 70. LDO Load Transient Response



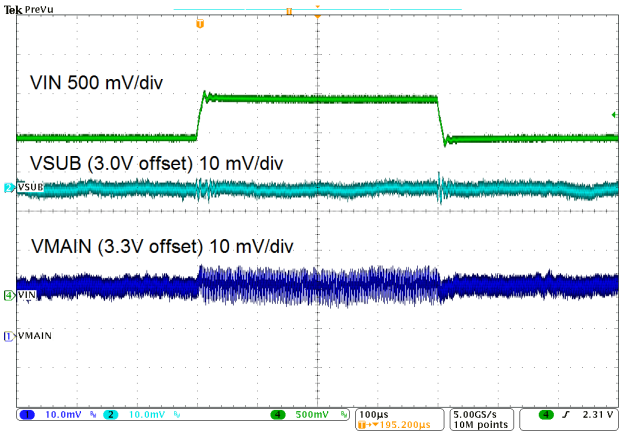
TPS610981 $I_{(MAIN)}$ = 20 mA $I_{(SUB)}$ = 0 mA
MODE = L V_{IN} = 2 V to 2.5 V, 10 µs rising/falling edge

Figure 71. Line Transient Response



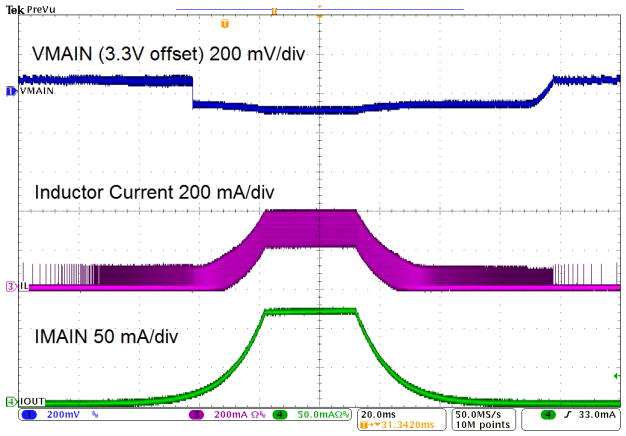
TPS610981 $I_{(MAIN)}$ = 20 mA $I_{(SUB)}$ = 0 mA
MODE = H V_{IN} = 2 V to 2.5 V, 10 µs rising/falling edge

Figure 72. Line Transient Response



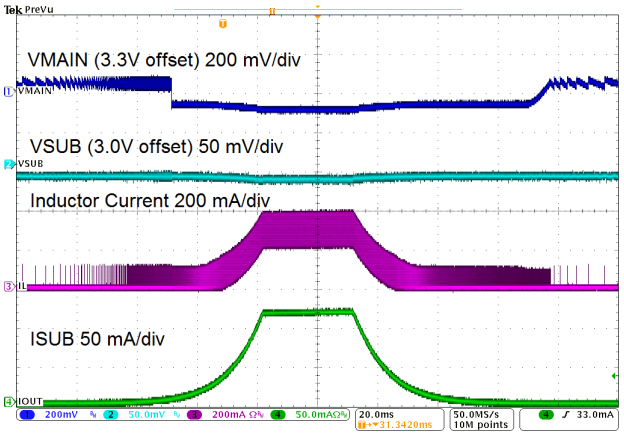
TPS610981 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 20 mA
MODE = H V_{IN} = 2 V to 2.5 V, 10 µs rising/falling edge

Figure 73. Line Transient Response



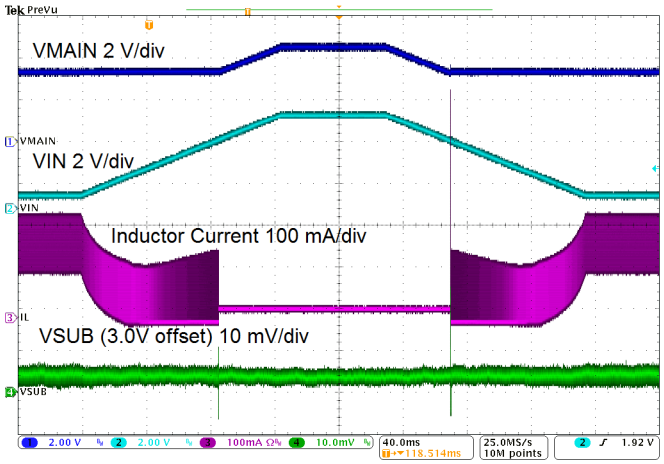
TPS610981 V_{IN} = 1.5 V $I_{(SUB)}$ = 0 mA
MODE = L $I_{(MAIN)}$ = 0 mA to 120 mA to 0 mA, ramp up and down

Figure 74. Load Regulation



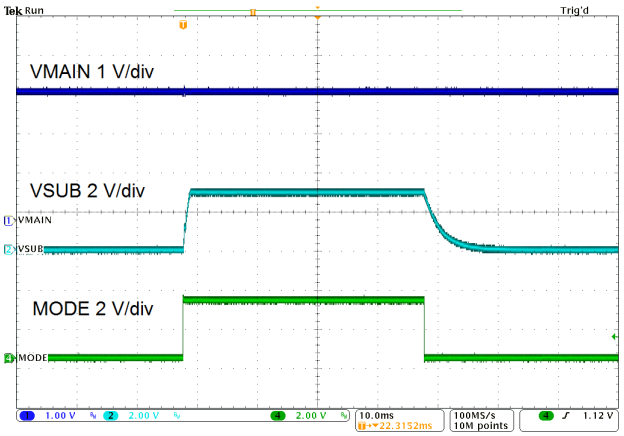
TPS610981 V_{IN} = 1.5 V $I_{(MAIN)}$ = 0 mA
MODE = H $I_{(SUB)}$ = 0 mA to 120 mA to 0 mA, ramp up and down

Figure 75. Load Regulation



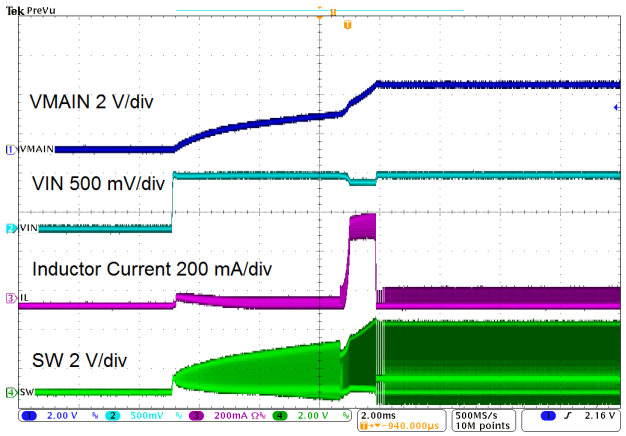
TPS610981 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 30 mA
MODE = H V_{IN} = 0.7 V to 4.5 V, ramp up and down

Figure 76. Line Regulation



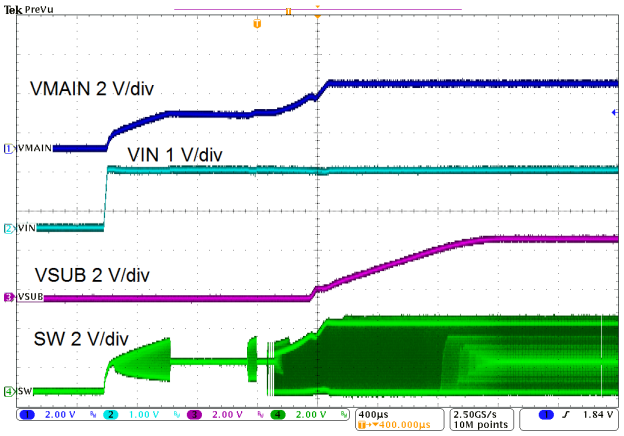
TPS610981 $R_{(MAIN)}$ = 1 kΩ $R_{(SUB)}$ = open load
MODE pin toggling

Figure 77. Mode Toggling



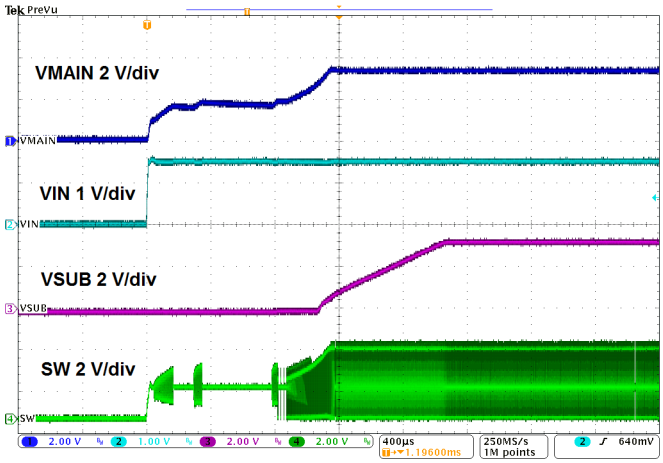
TPS610981 $R_{(MAIN)}$ = 3 kΩ V_{IN} = 0.7 V
MODE connected to GND

Figure 78. Startup



TPS610981 $R_{(MAIN)}$ = 1 kΩ $R_{(SUB)}$ = 1 kΩ
V_{IN} = 1.5 V MODE connected to VMAIN

Figure 79. Startup



TPS610896 $R_{(MAIN)}$ = 1 kΩ $R_{(SUB)}$ = 1 kΩ
V_{IN} = 1.5 V $C_{(SUB)}$ = 1 µF
MODE connected to VMAIN

Figure 80. Startup

9.2.2 VMAIN to Power the System in Low Power Mode

If only one power supply is needed for the whole system, users can easily leave the VSUB pin float and only use the VMAIN rail as the power supply. In this case, the TPS61098x functions as a standard boost converter. If enhanced load transient performance is needed when the system works in Active mode, the controller can control the MODE pin to switch the TPS61098x between the Active mode and Low Power mode. If the ultra-low Iq is critical for the application, users can connect the MODE pin to GND so the TPS61098x keeps working in Low Power mode with only 300 nA quiescent current. Below shows a typical application where the TPS61098 is used in Low Power mode to generate 2.2 V with only 300 nA Iq to power the whole system.

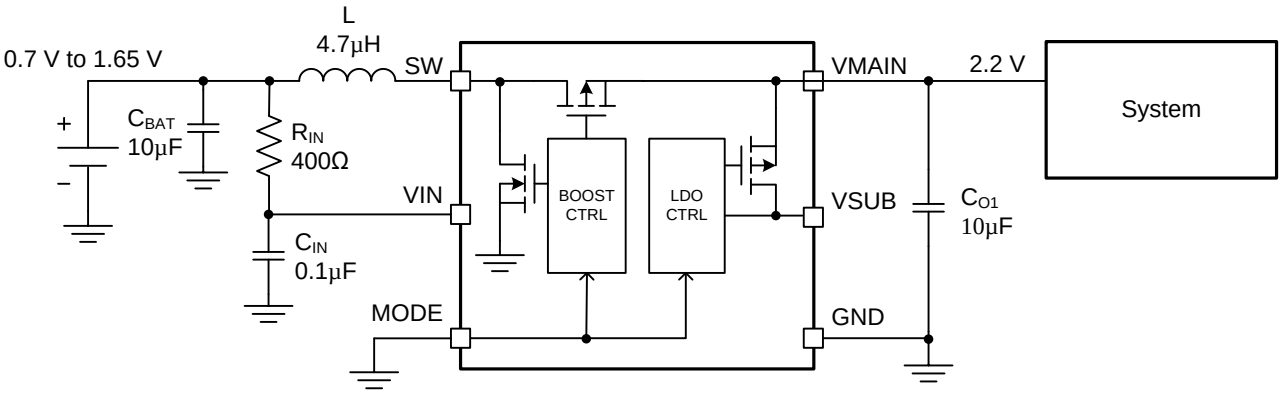


Figure 81. Typical Application of TPS61098 VMAIN to Power the System in Low Power Mode

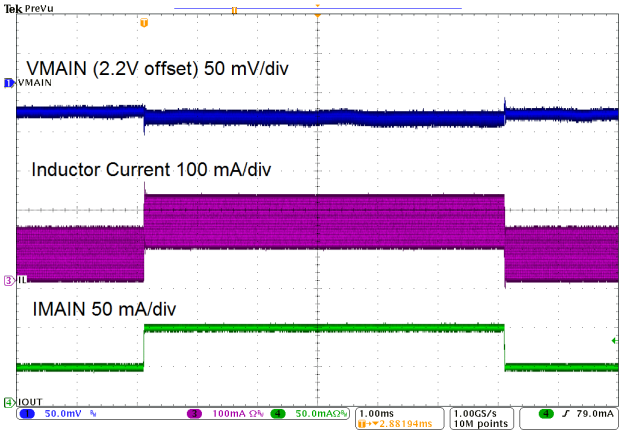
9.2.2.1 Design Requirements

- 2.2 V $V_{(MAIN)}$ to power the whole system
- Power source, single-cell alkaline battery (0.7 V to 1.65 V range)
- ≥ 80% conversion efficiency at 10 µA load

9.2.2.2 Detailed Design Procedure

Refer to the *Detailed Design Procedure* section for the detailed design steps.

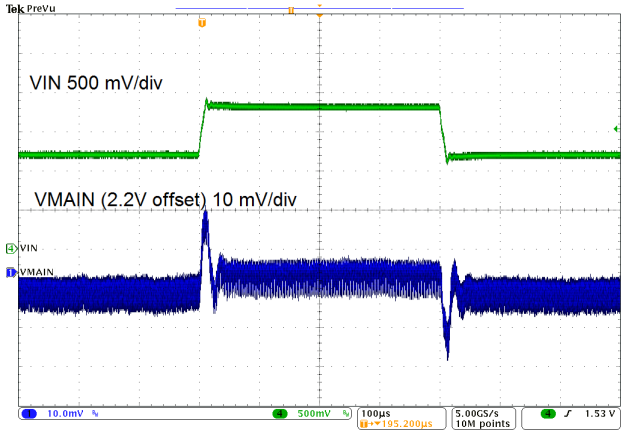
9.2.2.3 Application Curves



TPS61098
MODE = L

V_{IN} = 1.5 V
$I_{(MAIN)}$ = 50 mA to 100 mA, 5 µs rising/falling edge

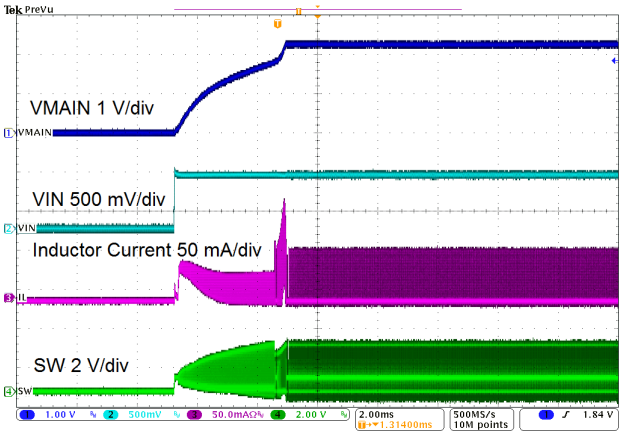
Figure 82. Load Transient Response



TPS61098
MODE = L

$I_{(MAIN)}$ = 100 mA $I_{(SUB)}$ = 0 mA
V_{IN} = 1.2 V to 1.8 V, 10 µs rising/falling edge

Figure 83. Line Transient Response



TPS61098
MODE connected to GND

$R_{(MAIN)}$ = 3 kΩ
V_{IN} = 0.7 V

Figure 84. Startup

9.2.3 VSUB to Power the System in Active Mode

In some applications, the system controller can be powered by the battery directly, but a buck-boost or a boost converter with an LDO is needed to provide a quiet power supply for a subsystem like a sensor. In this type of application, the TPS61098x can be used to replace the discrete boost converter and the LDO, providing a compact solution to simplify the system design and save the PCB space. The LDO can be turned on and off by the MODE pin. When the MODE pin is pulled low, the LDO is turned off to disconnect the load, and the TPS61098x also enters into Low Power mode to save power consumption. Figure 85 shows an application where the VSUB of the TPS61098 is used to supply the 3.1 V for a sensor in a system. The boost converter of the TPS61098 outputs 4.3 V and provides enough headroom for the LDO operation.

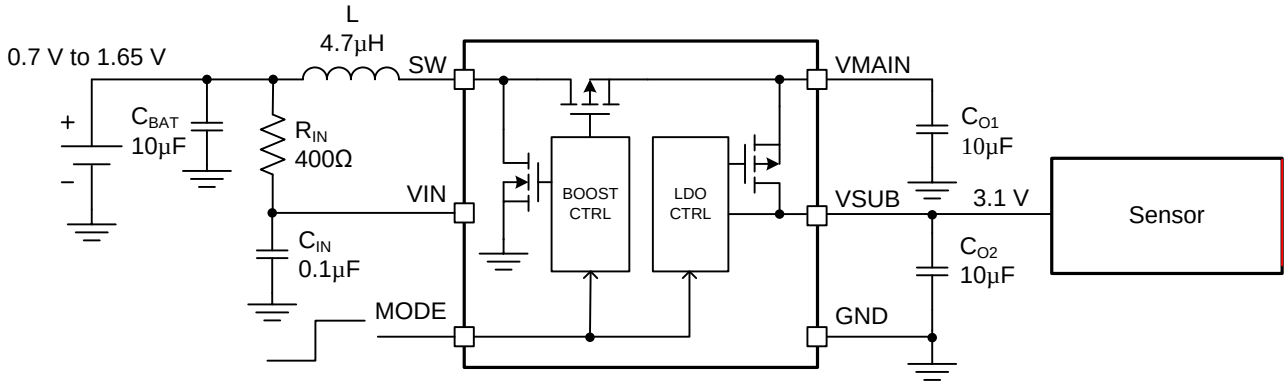


Figure 85. Typical Application of TPS61098 VSUB to Power the System in Active Mode

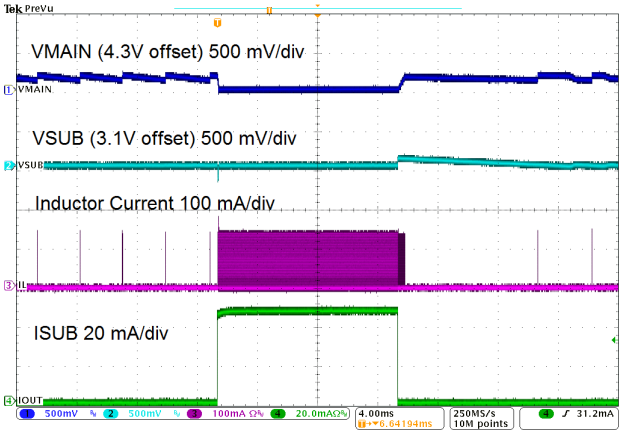
9.2.3.1 Design Requirements

- 3.1 V rail to power a sensor
- Power source, single-cell li-ion battery (2.7 V to 4.3 V range)

9.2.3.2 Detailed Design Procedure

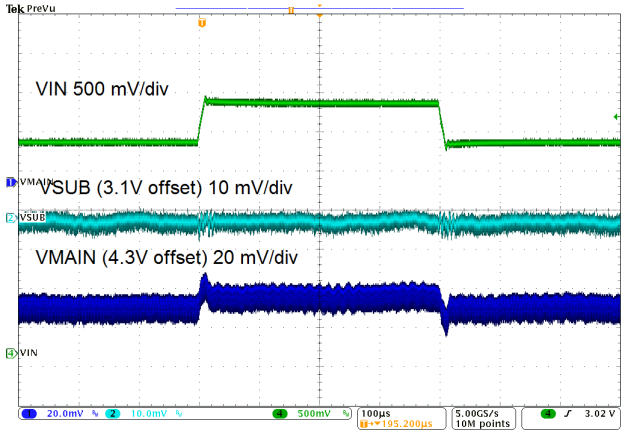
Refer to the *Detailed Design Procedure* section for the detailed design steps.

9.2.3.3 Application Curves



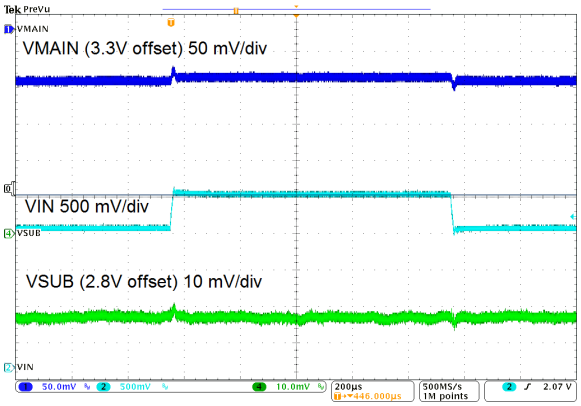
TPS61098 V_{IN} = 3.6 V $I_{(MAIN)}$ = 0 mA
MODE = H $I_{(SUB)}$ = 0 mA to 50 mA , 5 µs rising/falling edge

Figure 86. LDO Load Transient Response



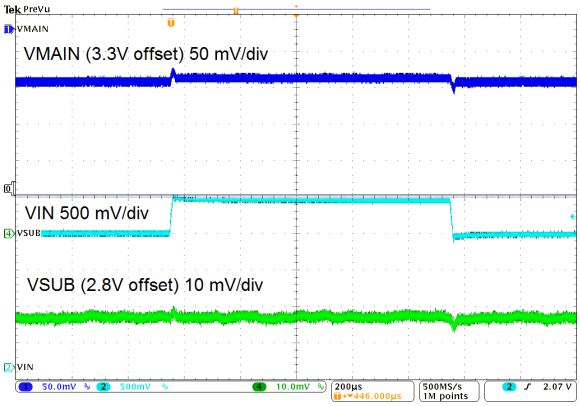
TPS61098 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 100 mA
MODE = H V_{IN} = 2.7 V to 3.2 V, 5 µs rising/falling edge

Figure 87. Line Transient Response



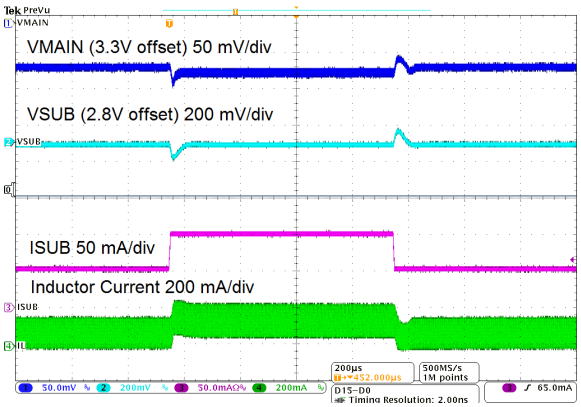
TPS610982 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 100 mA
MODE = L V_{IN} = 2 V to 2.5 V, 10 µs rising/falling edge

Figure 88. Line Transient Response



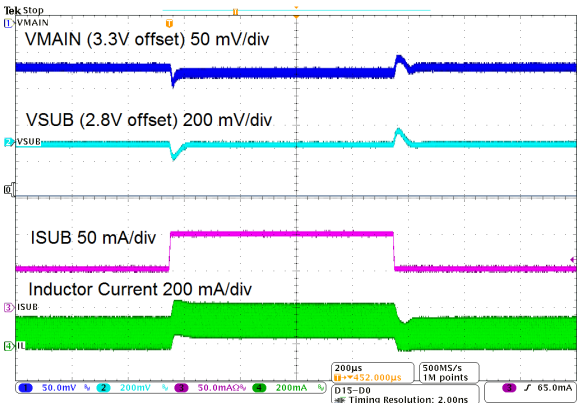
TPS610982 $I_{(MAIN)}$ = 0 mA $I_{(SUB)}$ = 100 mA
MODE = H V_{IN} = 2 V to 2.5 V, 10 µs rising/falling edge

Figure 89. Line Transient Response



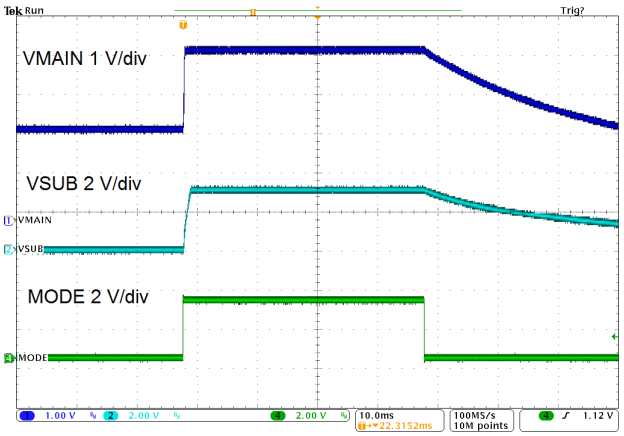
TPS610982 V_{IN} = 2.5 V $I_{(MAIN)}$ = 0 mA
MODE = L $I_{(SUB)}$ = 50 mA to 100 mA , 5 µs rising/falling edge

Figure 90. LDO Load Transient Response



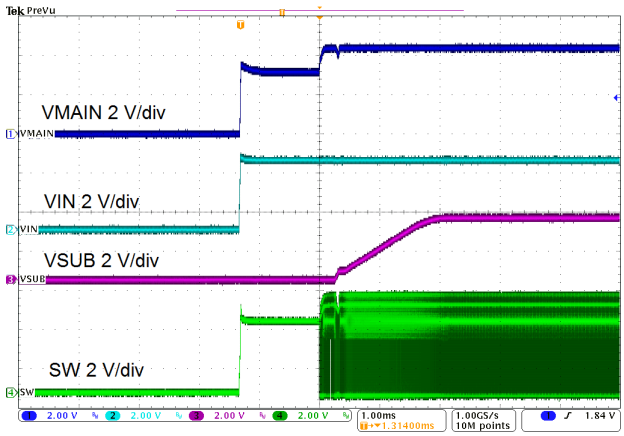
TPS610982 V_{IN} = 2.5 V $I_{(MAIN)}$ = 0 mA
MODE = H $I_{(SUB)}$ = 50 mA to 100 mA , 5 µs rising/falling edge

Figure 91. LDO Load Transient Response



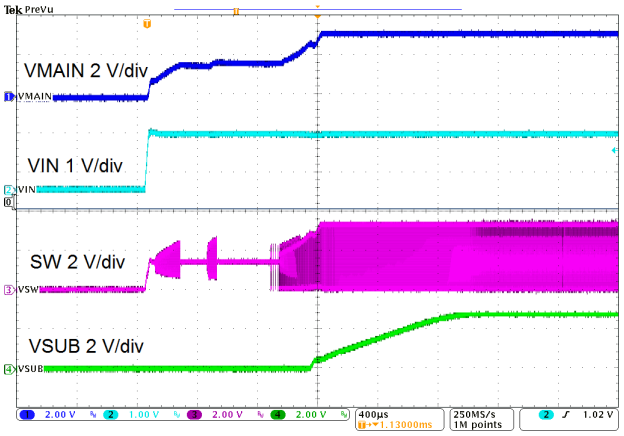
TPS61098 $R_{(MAIN)}$ = 10 kΩ $R_{(SUB)}$ = 3 kΩ
MODE pin toggling

Figure 92. MODE Toggling



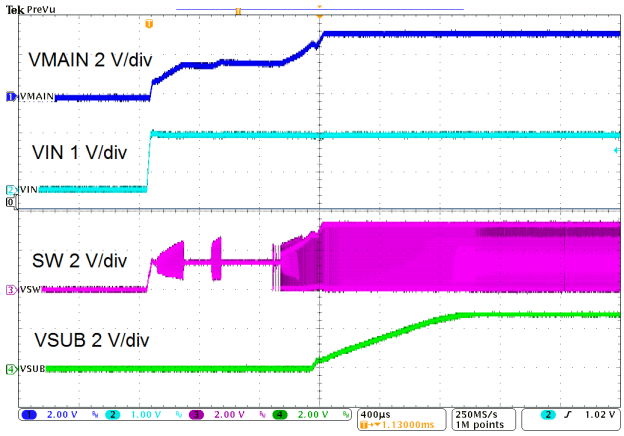
TPS61098 $R_{(MAIN)}$ = 1 kΩ $R_{(SUB)}$ = 1 kΩ
MODE connected to VMAIN V_{IN} = 3.6 V

Figure 93. Startup



TPS610982 $R_{(MAIN)}$ = 1 kΩ $R_{(SUB)}$ = 1 kΩ
MODE connected to GND V_{IN} = 1.5 V

Figure 94. Startup



TPS610982 $R_{(MAIN)}$ = 1 kΩ $R_{(SUB)}$ = 1 kΩ
MODE connected to VMAIN V_{IN} = 1.5 V

Figure 95. Startup

10 Power Supply Recommendations

The TPS61098x family is designed to operate from an input voltage supply range between 0.7 V to 4.5 V. The power supply can be either a one-cell or two-cell alkaline, NiCd or NiMH, one-cell coin cell or one-cell Li-Ion or Li-polymer battery. The input supply should be well regulated with the rating of TPS61098x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

11.2 Layout Example

The bottom layer is a large GND plane connected by vias.

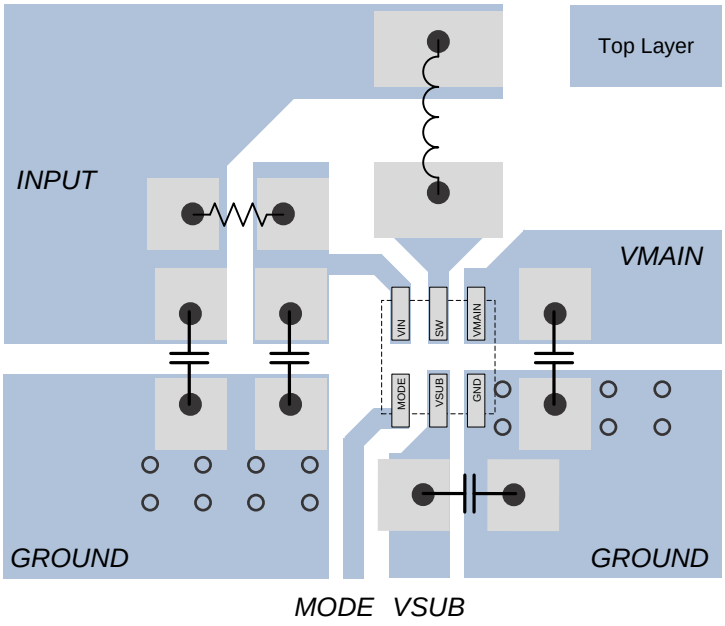


Figure 96. Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

Performing Accurate PFM Mode Efficiency Measurements, SLVA236

Accurately measuring efficiency of ultralow-IQ devices, SLYT558

IQ: What it is, what it isn't, and how to use it, SLYT412

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61098	Click here	Click here	Click here	Click here	Click here
TPS610981	Click here	Click here	Click here	Click here	Click here
TPS610982	Click here	Click here	Click here	Click here	Click here
TPS610985	Click here	Click here	Click here	Click here	Click here
TPS610986	Click here	Click here	Click here	Click here	Click here
TPS610987	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS610981DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GM	Samples
TPS610981DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GM	Samples
TPS610982DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	G8	Samples
TPS610982DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	G8	Samples
TPS610985DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1G	Samples
TPS610985DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1G	Samples
TPS610986DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1H	Samples
TPS610986DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1H	Samples
TPS610987DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3X	Samples
TPS610987DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3X	Samples
TPS61098DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GL	Samples
TPS61098DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

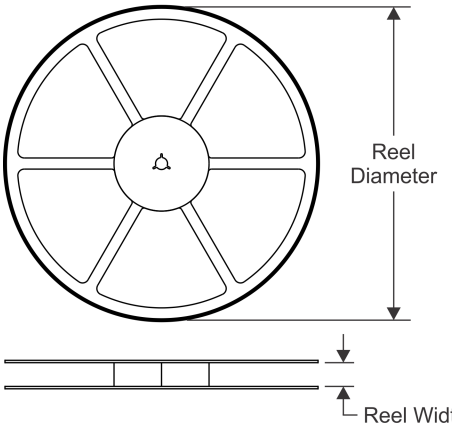
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

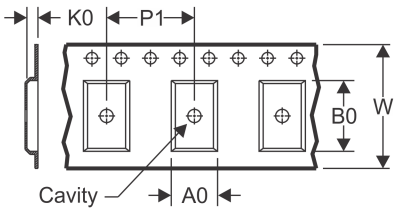
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

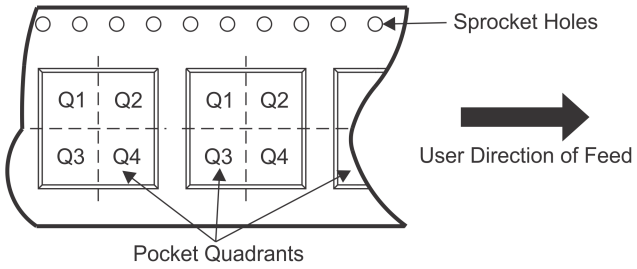


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

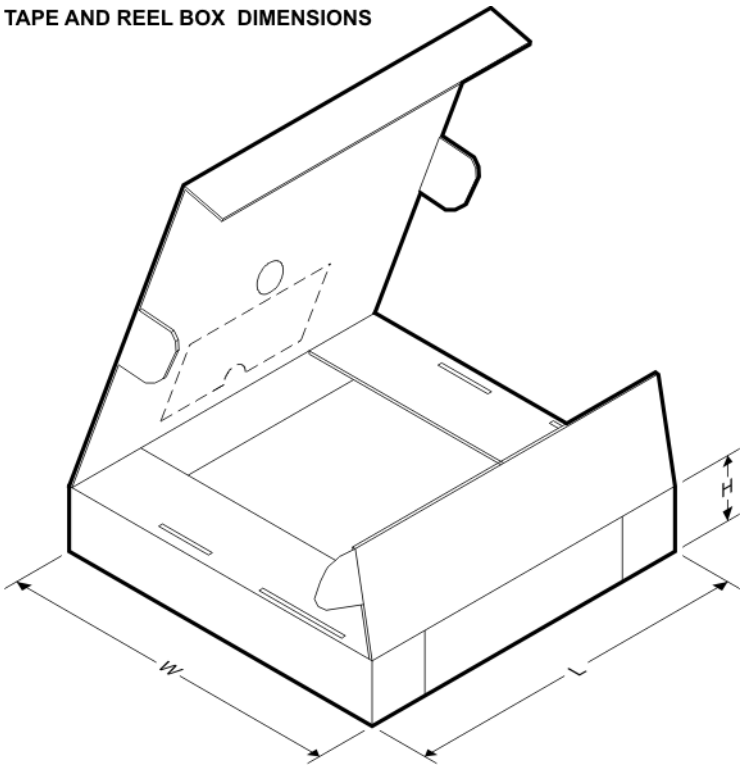
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS610981DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610981DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610982DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610982DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610985DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610985DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610986DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610986DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610987DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS610987DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS61098DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS61098DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

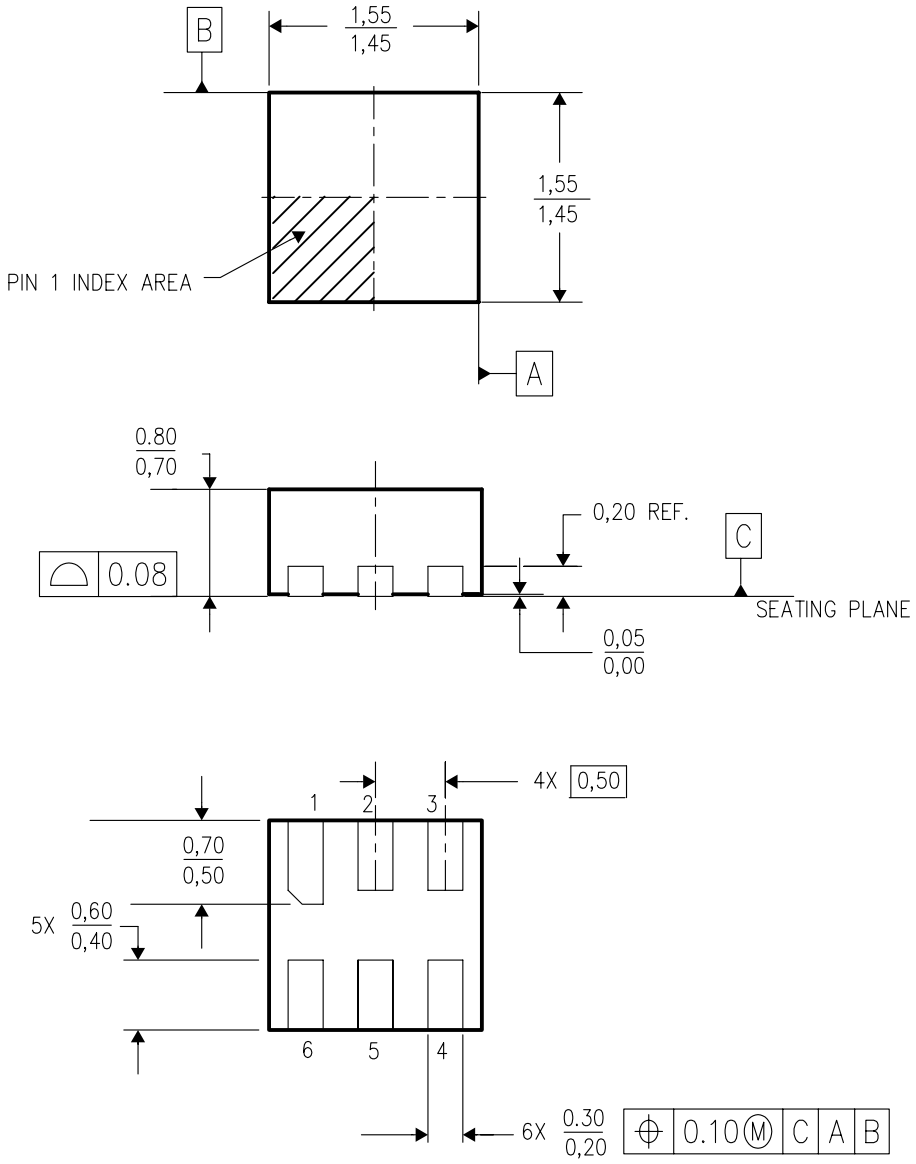
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS610981DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS610981DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS610982DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS610982DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS610985DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS610985DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS610986DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS610986DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS610987DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS610987DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS61098DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS61098DSET	WSON	DSE	6	250	205.0	200.0	33.0

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



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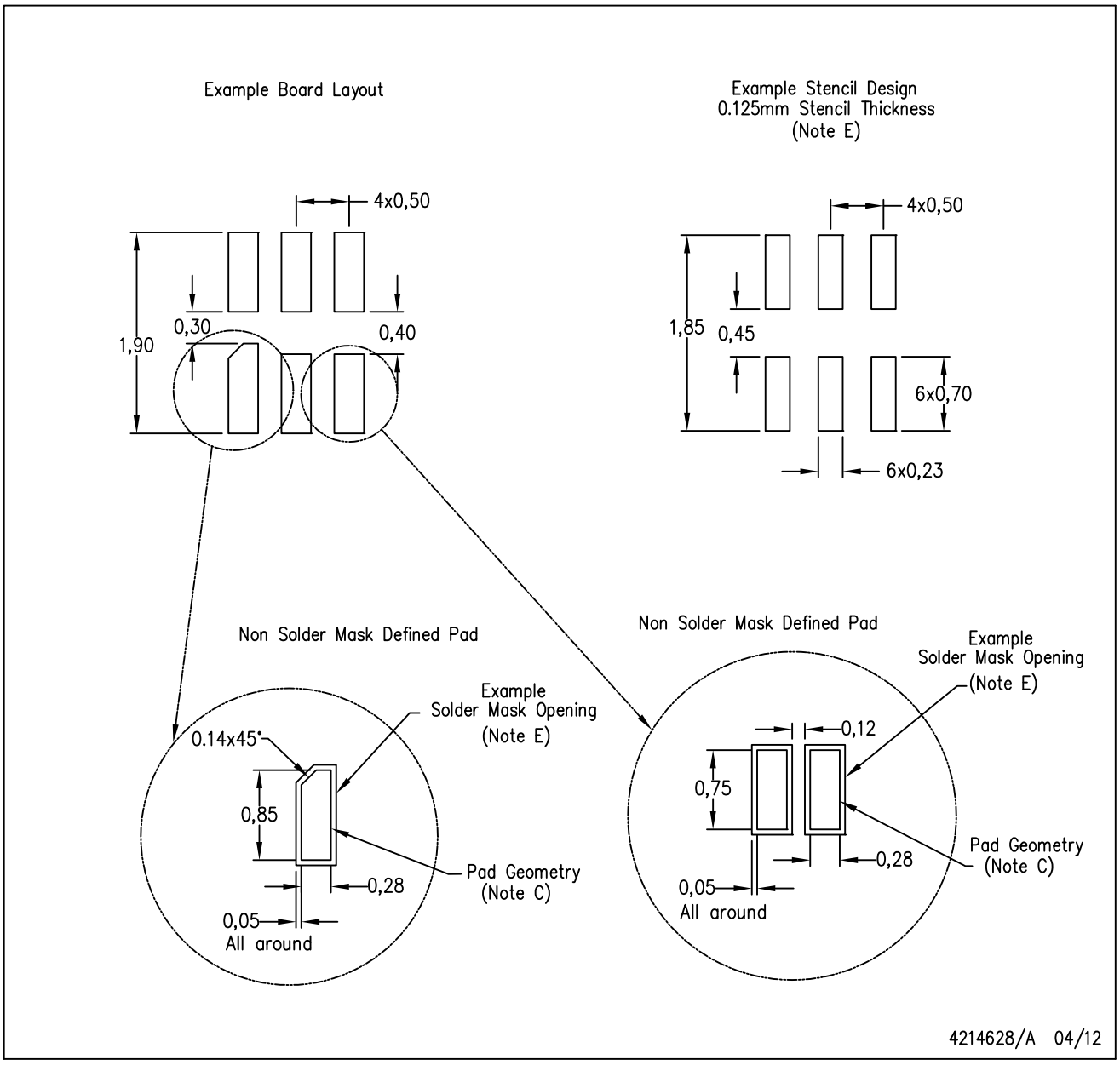
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

DSE (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for solder mask tolerances.

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