

## LMC6482-MIL CMOS Dual Rail-to-Rail Input and Output Operational Amplifier

### 1 Features

- Typical Unless Otherwise Noted
- Rail-to-Rail Input Common-Mode Voltage Range (Ensured Over Temperature)
- Rail-to-Rail Output Swing (Within 20-mV of Supply Rail, 100-k $\Omega$  Load)
- Ensured 3-V, 5-V, and 15-V Performance
- Excellent CMRR and PSRR: 82 dB
- Ultralow Input Current: 20 fA
- High Voltage Gain (R<sub>L</sub> = 500 k $\Omega$ ): 130 dB
- Specified for 2-k $\Omega$  and 600- $\Omega$  Loads
- Power-Good Output
- Available in VSSOP Package

### 2 Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

### 3 Description

The LMC6482-MIL device provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers. The device is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482-MIL is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

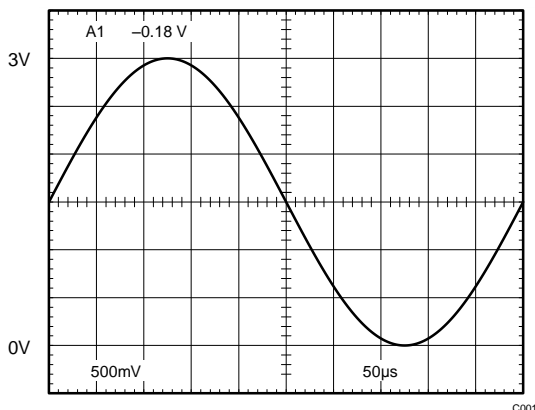
Maximum dynamic signal range is assured in low voltage and single supply systems by the rail-to-rail output swing of the LMC6482-MIL. The rail-to-rail output swing is ensured for loads down to 600  $\Omega$  of the device. Ensured low-voltage characteristics and low-power dissipation make the LMC6482-MIL especially well-suited for battery-operated systems. LMC6482-MIL is also available in a VSSOP package, which is almost half the size of a SOIC-8 device. See the LMC6484 data sheet for a quad CMOS operational amplifier with these same features.

#### Device Information<sup>(1)</sup>

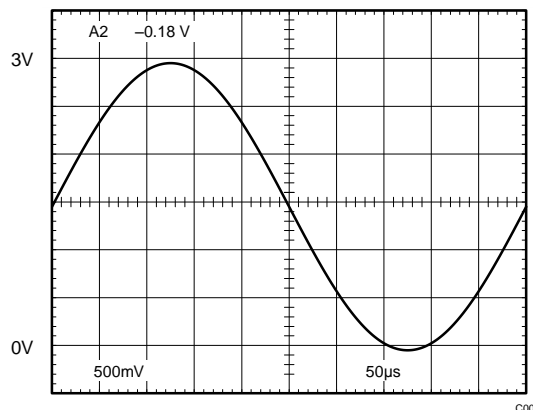
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMC6482-MIL	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	PDIP (8)	9.81 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Rail-to-Rail Input**



**Rail-to-Rail Output**



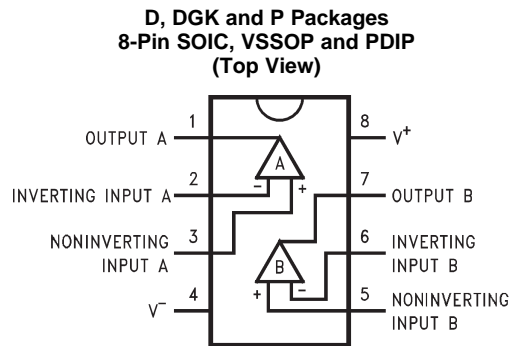
## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Pin Configuration and Functions</b> ..... 3 <b>6 Specifications</b> ..... 3 6.1 Absolute Maximum Ratings ..... 3 6.2 ESD Ratings..... 4 6.3 Recommended Operating Conditions ..... 4 6.4 Thermal Information ..... 4 6.5 Electrical Characteristics for $V^+ = 5\text{ V}$ ..... 4 6.6 Electrical Characteristics for $V^+ = 3\text{ V}$ ..... 6 6.7 Typical Characteristics ..... 7 <b>7 Detailed Description</b> ..... 16 7.1 Overview ..... 16	7.2 Functional Block Diagram ..... 16 7.3 Feature Description..... 16 7.4 Device Functional Modes..... 17 <b>8 Application and Implementation</b> ..... 18 8.1 Application Information..... 18 8.2 Typical Applications ..... 20 <b>9 Power Supply Recommendations</b> ..... 27 <b>10 Layout</b> ..... 27 10.1 Layout Guidelines ..... 27 10.2 Layout Example ..... 27 <b>11 Device and Documentation Support</b> ..... 29 11.1 Trademarks ..... 29 11.2 Electrostatic Discharge Caution..... 29 11.3 Glossary ..... 29 <b>12 Mechanical, Packaging, and Orderable Information</b> ..... 29
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## 4 Revision History

DATE	REVISION	NOTES
	*	Initial release.

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTPUT A	O	Output for Amplifier A
2	INVERTING INPUT A	I	Inverting input for Amplifier A
3	NONINVERTING INPUT A	I	Noninverting input for Amplifier A
4	V <sup>-</sup>	P	Negative supply voltage input
5	NONINVERTING INPUT B	I	Noninverting input for Amplifier B
6	INVERTING INPUT B	I	Inverting input for Amplifier B
7	OUTPUT B	O	Output for Amplifier B
8	V <sup>+</sup>	P	Positive supply voltage input

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
Differential Input Voltage		±Supply Voltage	
Voltage at Input/Output Pin	(V <sup>-</sup> ) -0.3	(V <sup>+</sup> ) +0.3	V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )		16	V
Current at Input Pin <sup>(3)</sup>	-5	5	mA
Current at Output Pin <sup>(4)(5)</sup>	-30	30	mA
Current at Power Supply Pin		40	mA
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature <sup>(6)</sup>		150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- (5) Do not short circuit output to V<sup>+</sup>, when V<sup>+</sup> is greater than 13 V or reliability will be adversely affected.
- (6) The maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly into a PC board.

## 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1500 V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage		3	15.5	V
Junction Temperature Range	LMC6482M	-55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMC6482-MIL	LMC6482-MIL	LMC6482-MIL	UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155	194	90	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics for $V^+ = 5\text{ V}$

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}$ .

PARAMETER	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			At Temperature Extremes <sup>(1)</sup>			UNIT
		MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
<b>DC Electrical Characteristics</b>								
$V_{OS}$	Input Offset Voltage		0.11	3			3.8	mV
$TCV_{OS}$	Input Offset Voltage Average Drift		1					$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Current	See <sup>(4)</sup>	0.02				10	pA
$I_{OS}$	Input Offset Current	See <sup>(4)</sup>	0.01				5	pA
$C_{IN}$	Common-Mode Input Capacitance		3					pF
$R_{IN}$	Input Resistance		10					Tera $\Omega$
CMRR	Common-Mode Rejection Ratio	$0\text{ V} \leq V_{CM} \leq 15\text{ V}$ $V^+ = 15\text{ V}$	65	82	60			dB
		$0\text{ V} \leq V_{CM} \leq 5\text{ V}$ $V^+ = 5\text{ V}$	65	82	60			
+PSRR	Positive Power Supply Rejection Ratio	$5\text{ V} \leq V^+ \leq 15\text{ V}$ , $V^- = 0\text{ V}$ $V_O = 2.5\text{ V}$	65	82	60			dB
-PSRR	Negative Power Supply Rejection Ratio	$-5\text{ V} \leq V^- \leq -15\text{ V}$ , $V^+ = 0\text{ V}$ $V_O = -2.5\text{ V}$	65	82	60			dB

(1) See [Recommended Operating Conditions](#) for operating temperature ranges.

(2) Typical Values represent the most likely parametric norm.

(3) All limits are specified by testing or statistical analysis.

(4) Ensured limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

**Electrical Characteristics for  $V^+ = 5\text{ V}$  (continued)**

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}$ .

PARAMETER	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			At Temperature Extremes <sup>(1)</sup>			UNIT	
		MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>		
$V_{CM}$	Input Common-Mode Voltage Range	$V^+ = 5\text{ V}$ and $15\text{ V}$ For $CMRR \geq 50\text{ dB}$			$V^- - 0.3$		$-0.25$	0	V
		$V^+ + 0.25$	$V^+ + 0.3$		$V^+$				
$A_V$	Large Signal Voltage Gain	$R_L = 2\text{ k}\Omega$ <sup>(5)(4)</sup>	Sourcing	120	666		60	V/mV	
			Sinking	35	75		18		
		$R_L = 600\ \Omega$ <sup>(5)(4)</sup>	Sourcing	50	300		25		
			Sinking	15	35		8		
$V_O$	Output Swing	$V^+ = 5\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$		4.8	4.9		4.7	V	
						0.1	0.18		0.24
		$V^+ = 5\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$		4.5	4.7		4.24	V	
					0.3	0.5		0.65	
		$V^+ = 15\text{ V}$ $R_L = 2\text{ k}\ \Omega$ to $V^+/2$		14.4	14.7		14.2	V	
					0.16	0.32		0.45	
		$V^+ = 15\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$		13.4	14.1		13	V	
					0.5	1		1.3	
$I_{SC}$	Output Short Circuit Current $V^+ = 5\text{ V}$	Sourcing, $V_O = 0\text{ V}$	16	20		10	mA		
		Sinking, $V_O = 5\text{ V}$	11	15		8			
$I_{SC}$	Output Short Circuit Current $V^+ = 15\text{ V}$	Sourcing, $V_O = 0\text{ V}$	28	30		20	mA		
		Sinking, $V_O = 12\text{ V}$ <sup>(6)</sup>	30	30		22			
$I_S$	Supply Current	Both Amplifiers $V^+ = +5\text{ V}$ , $V_O = V^+/2$		1	1.4		1.9	mA	
		Both Amplifiers $V^+ = 15\text{ V}$ , $V_O = V^+/2$		1.3	1.6		2		
<b>AC Electrical Characteristics</b>									
SR	Slew Rate	See <sup>(7)</sup>	0.9	1.3		0.54		V/ $\mu\text{s}$	
GBW	Gain-Bandwidth Product	$V^+ = 15\text{ V}$		1.5				MHz	
$\phi_m$	Phase Margin			50				Deg	
$G_m$	Gain Margin			15				dB	
	Amp-to-Amp Isolation	See <sup>(8)</sup>		150				dB	
$e_n$	Input-Referred Voltage Noise	$F = 1\text{ kHz}$ $V_{cm} = 1\text{ V}$		37				nV/ $\sqrt{\text{Hz}}$	
$I_n$	Input-Referred Current Noise	$F = 1\text{ kHz}$		0.03				pA/ $\sqrt{\text{Hz}}$	
T.H.D.	Total Harmonic Distortion	$F = 10\text{ kHz}$ , $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 4.1\text{ V}_{PP}$		0.01%					
		$F = 10\text{ kHz}$ , $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 8.5\text{ V}_{PP}$ $V^+ = 10\text{ V}$		0.01%					

(5)  $V^+ = 15\text{ V}$ ,  $V_{CM} = 7.5\text{ V}$  and  $R_L$  connected to  $7.5\text{ V}$ . For Sourcing tests,  $7.5\text{ V} \leq V_O \leq 11.5\text{ V}$ . For Sinking tests,  $3.5\text{ V} \leq V_O \leq 7.5\text{ V}$ .

(6) Do not short circuit output to  $V^+$ , when  $V^+$  is greater than  $13\text{ V}$  or reliability will be adversely affected.

(7)  $V^+ = 15\text{ V}$ . Connected as Voltage Follower with  $10\text{ V}$  step input. Number specified is the slower of either the positive or negative slew rates.

(8) Input referred,  $V^+ = 15\text{ V}$  and  $R_L = 100\text{ k}\Omega$  connected to  $7.5\text{ V}$ . Each amp excited in turn with  $1\text{ kHz}$  to produce  $V_O = 12\text{ V}_{PP}$ .

## 6.6 Electrical Characteristics for $V^+ = 3\text{ V}$

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS	$T_J = 25^\circ\text{C}$			At Temperature Extremes <sup>(1)</sup>			UNIT
			MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
<b>DC Electrical Characteristics</b>									
$V_{\text{OS}}$	Input Offset Voltage			0.9	3			3.8	mV
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift			2					$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current			0.02					pA
$I_{\text{OS}}$	Input Offset Current			0.01					pA
CMRR	Common Mode Rejection Ratio	$0\text{ V} \leq V_{\text{CM}} \leq 3\text{ V}$	60	74					dB
PSRR	Power Supply Rejection Ratio	$3\text{ V} \leq V^+ \leq 15\text{ V}$ , $V^- = 0\text{ V}$	60	80					dB
$V_{\text{CM}}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{ dB}$		$V^- - 0.25$	0				V
				$V^+ - 0.25$					V
$V_O$	Output Swing	$R_L = 2\text{ k}\Omega$ to $V^+/2$		2.8					V
				0.2					V
		$R_L = 600\ \Omega$ to $V^+/2$	2.5	2.7					V
			0.37	0.6					V
$I_S$	Supply Current	Both Amplifiers	0.825	1.2			1.6	mA	
<b>AC Electrical Characteristics</b>									
SR	Slew Rate	See <sup>(4)</sup>		0.9					V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product			1					MHz
T.H.D.	Total Harmonic Distortion	$F = 10\text{ kHz}$ , $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 2\text{ V}_{\text{PP}}$		0.01%					

(1) See [Recommended Operating Conditions](#) for operating temperature ranges.

(2) Typical Values represent the most likely parametric norm.

(3) All limits are specified by testing or statistical analysis.

(4) Connected as voltage Follower with 2-V step input. Number specified is the slower of either the positive or negative slew rates.

### 6.7 Typical Characteristics

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

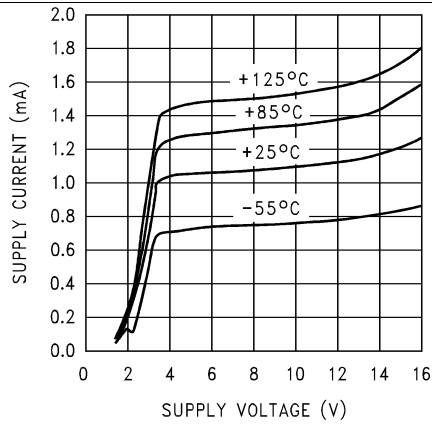


Figure 1. Supply Current vs. Supply Voltage

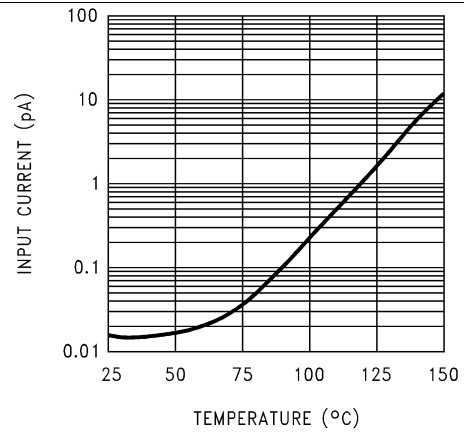


Figure 2. Input Current vs. Temperature

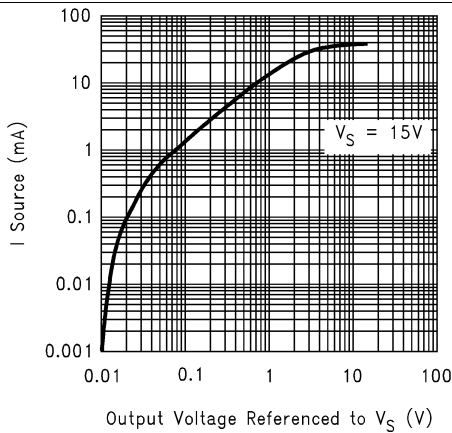


Figure 3. Sourcing Current vs. Output Voltage

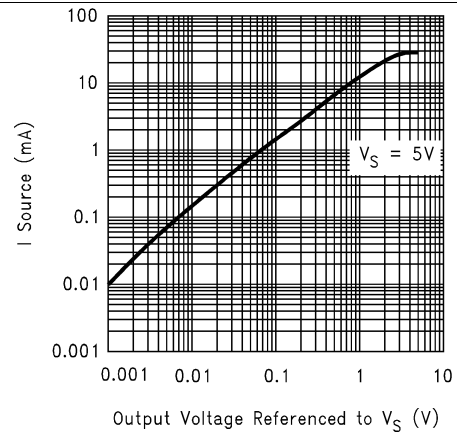


Figure 4. Sourcing Current vs. Output Voltage

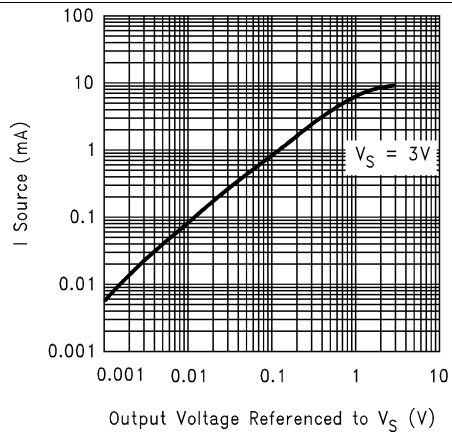


Figure 5. Sourcing Current vs. Output Voltage

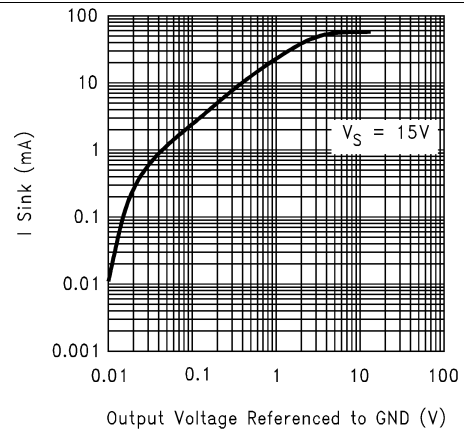
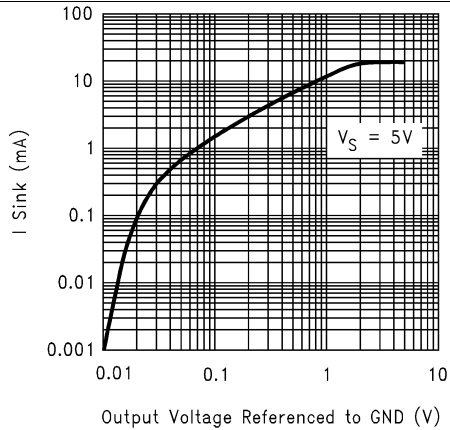


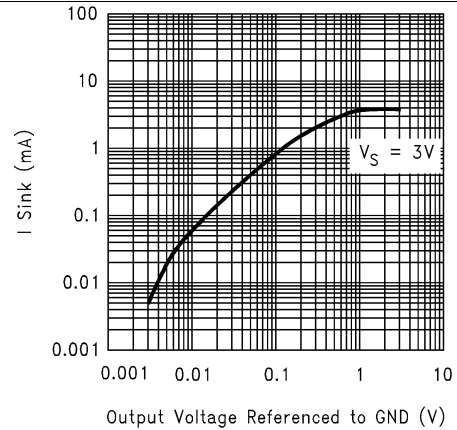
Figure 6. Sinking Current vs. Output Voltage

### Typical Characteristics (continued)

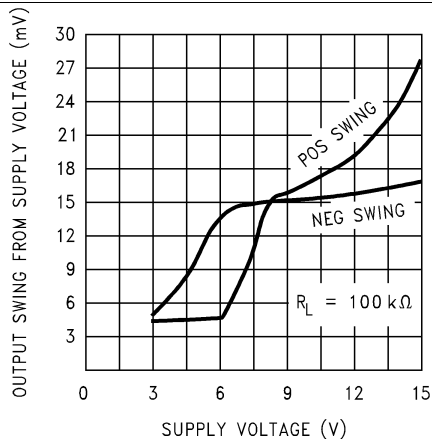
$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified



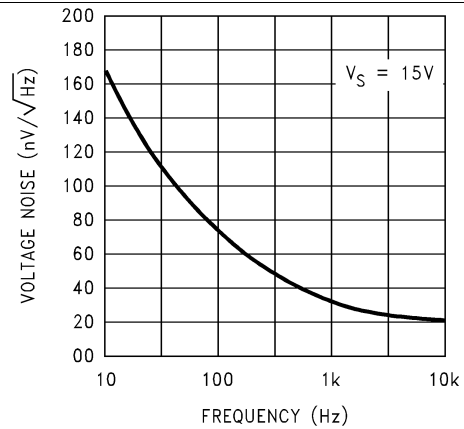
**Figure 7. Sinking Current vs. Output Voltage**



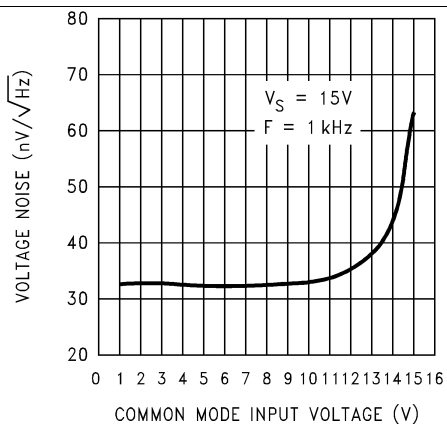
**Figure 8. Sinking Current vs. Output Voltage**



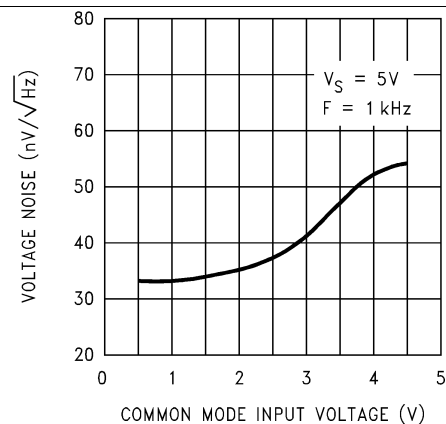
**Figure 9. Output Voltage Swing vs. Supply Voltage**



**Figure 10. Input Voltage Noise vs. Frequency**



**Figure 11. Input Voltage Noise vs. Input Voltage**



**Figure 12. Input Voltage Noise vs. Input Voltage**



Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

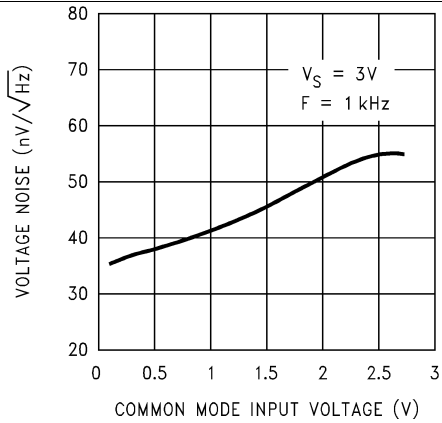


Figure 13. Input Voltage Noise vs. Input Voltage

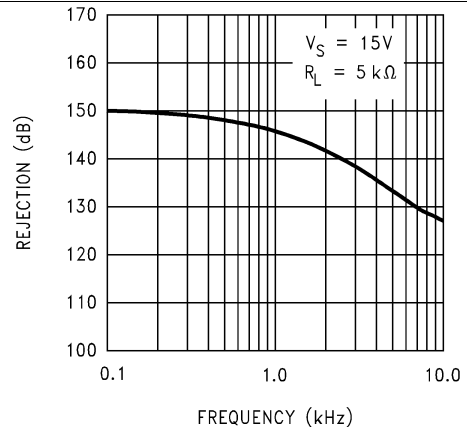


Figure 14. Crosstalk Rejection vs. Frequency

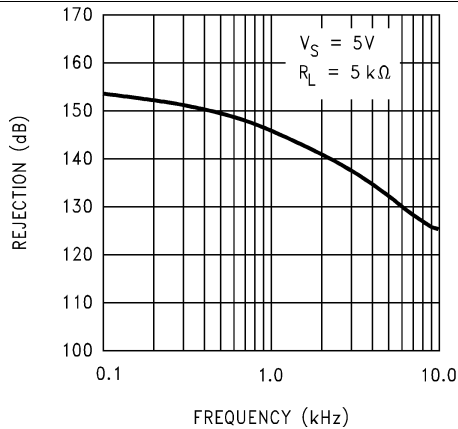


Figure 15. Crosstalk Rejection vs. Frequency

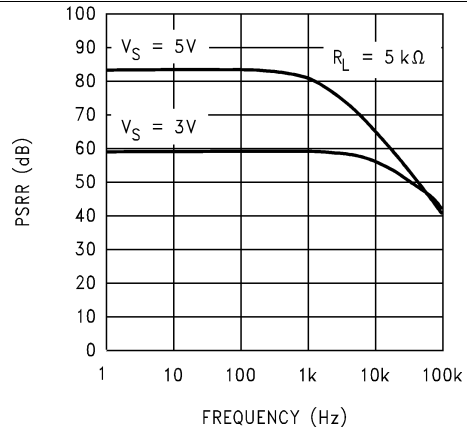


Figure 16. Positive PSRR vs. Frequency

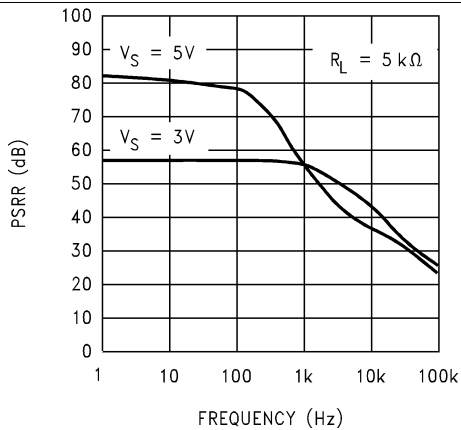


Figure 17. Negative PSRR vs. Frequency

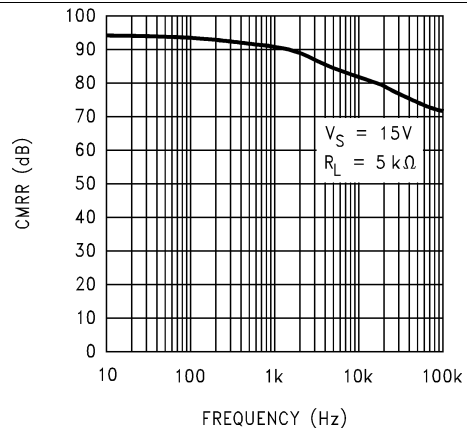


Figure 18. CMRR vs. Frequency

### Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

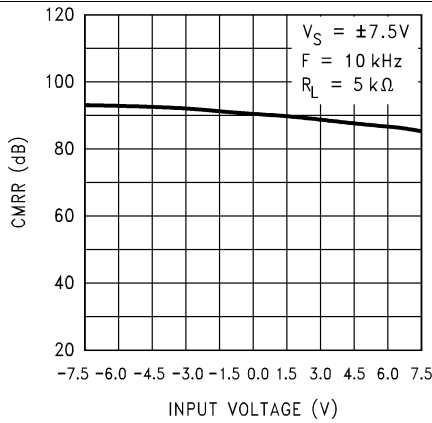


Figure 19. CMRR vs. Input Voltage

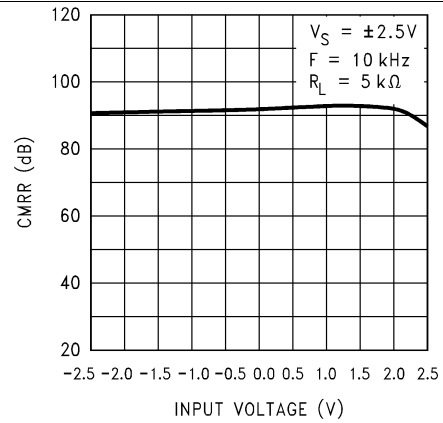


Figure 20. CMRR vs. Input Voltage

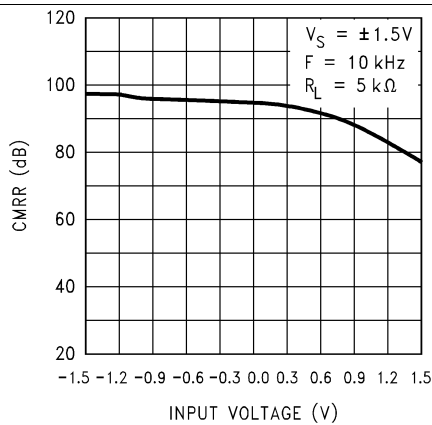


Figure 21. CMRR vs. Input Voltage

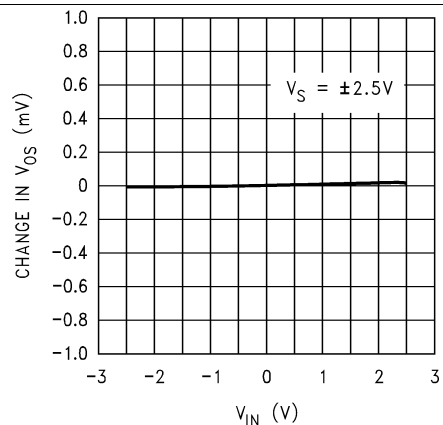


Figure 22.  $\Delta V_{OS}$  vs. CMR

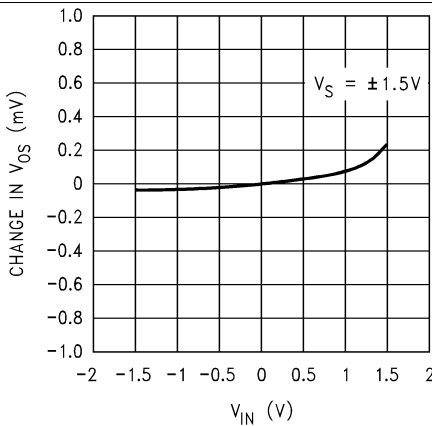


Figure 23.  $\Delta V_{OS}$  vs. CMR

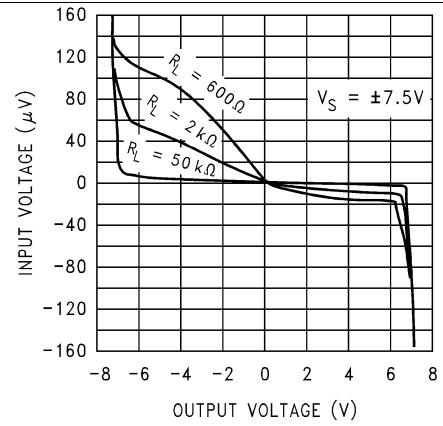


Figure 24. Input Voltage vs. Output Voltage

Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

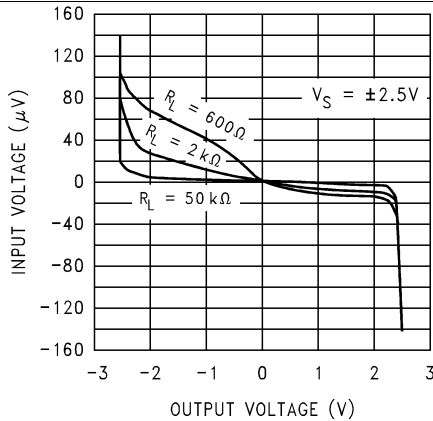


Figure 25. Input Voltage vs. Output Voltage

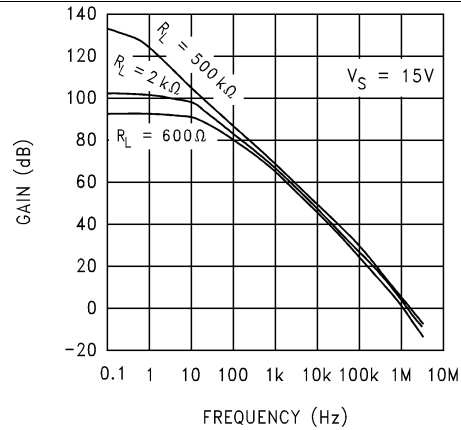


Figure 26. Open-Loop Frequency Response

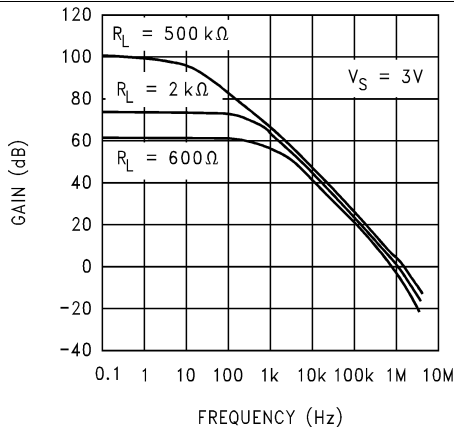


Figure 27. Open-Loop Frequency Response

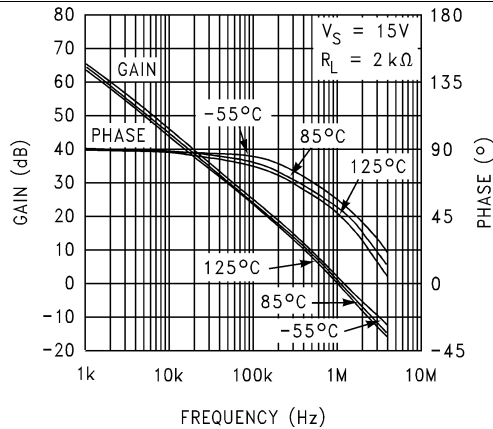


Figure 28. Open-Loop Frequency Response vs. Temperature

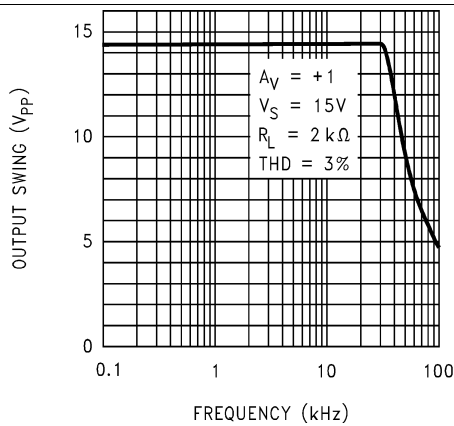


Figure 29. Maximum Output Swing vs. Frequency

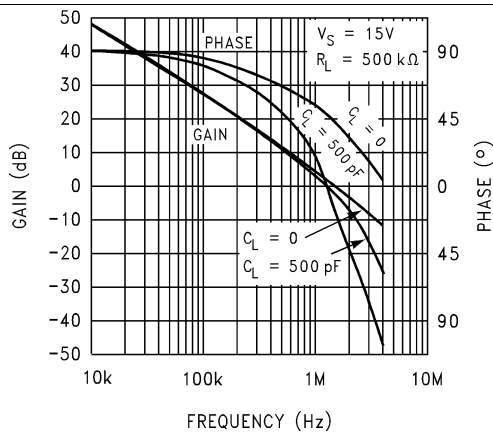


Figure 30. Gain and Phase vs. Capacitive Load

Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

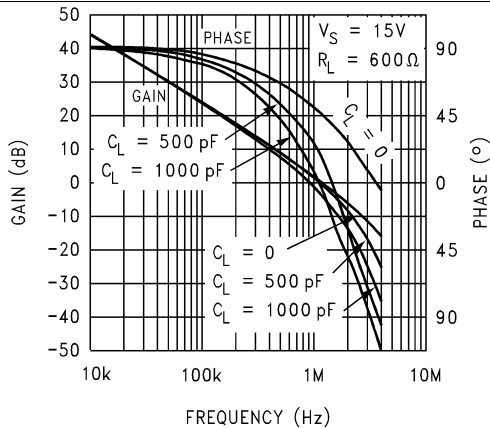


Figure 31. Gain and Phase vs. Capacitive Load

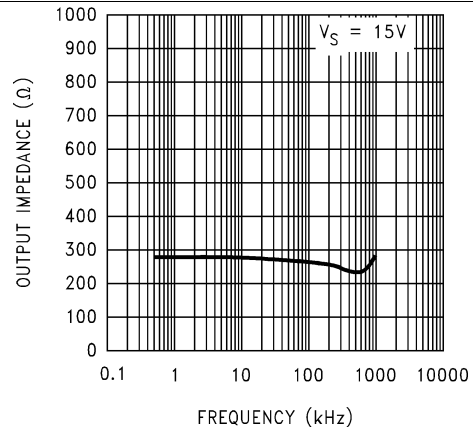


Figure 32. Open-Loop Output Impedance vs. Frequency

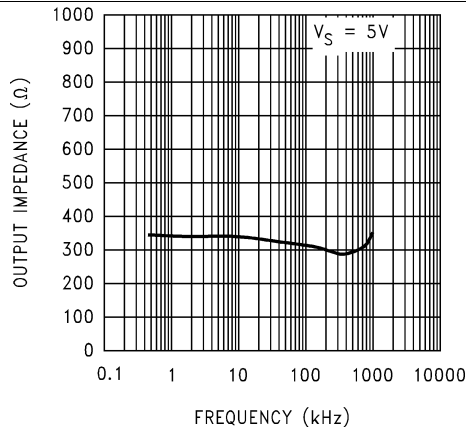


Figure 33. Open-Loop Output Impedance vs. Frequency

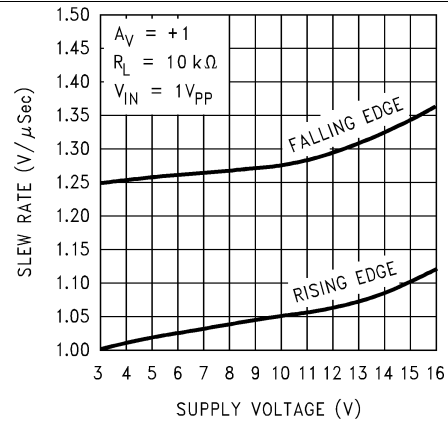


Figure 34. Slew Rate vs. Supply Voltage

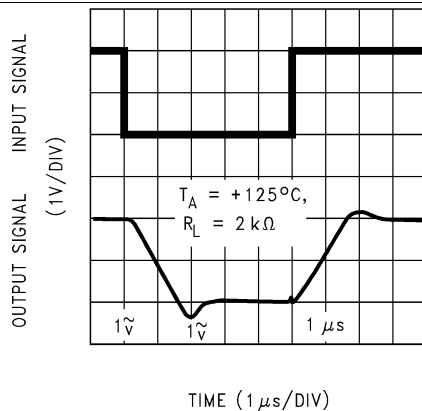


Figure 35. Noninverting Large Signal Pulse Response

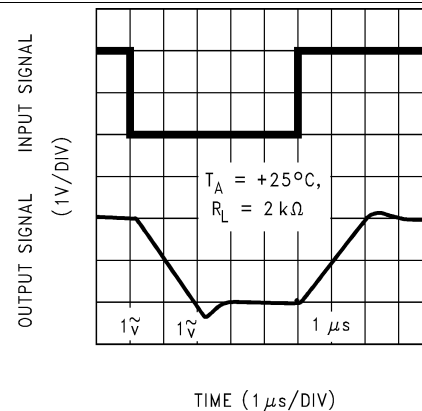


Figure 36. Noninverting Large Signal Pulse Response

Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

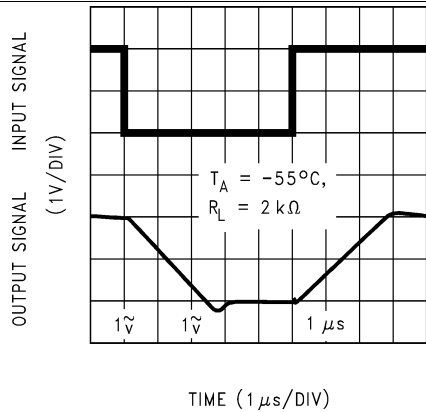


Figure 37. Noninverting Large Signal Pulse Response

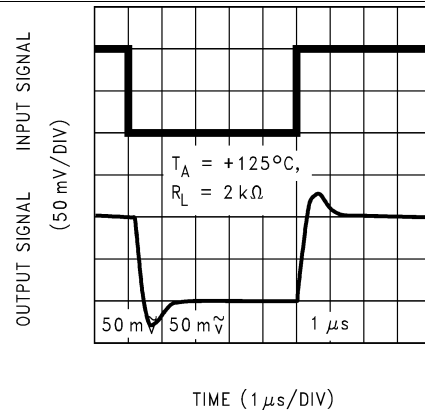


Figure 38. Noninverting Small Signal Pulse Response

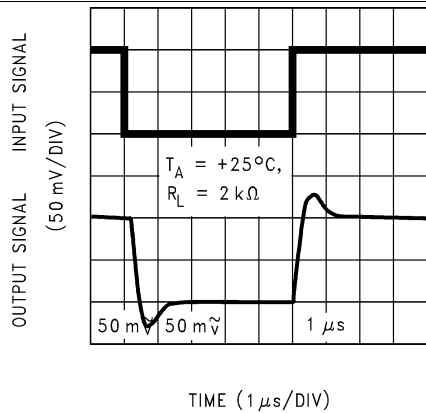


Figure 39. Noninverting Small Signal Pulse Response

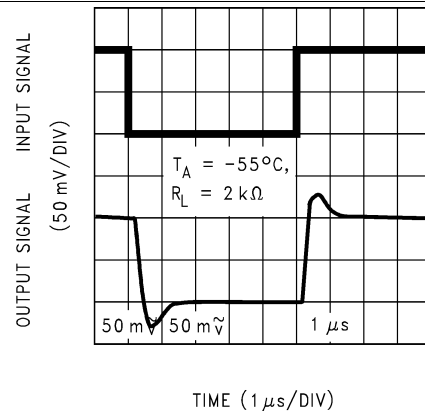


Figure 40. Noninverting Small Signal Pulse Response

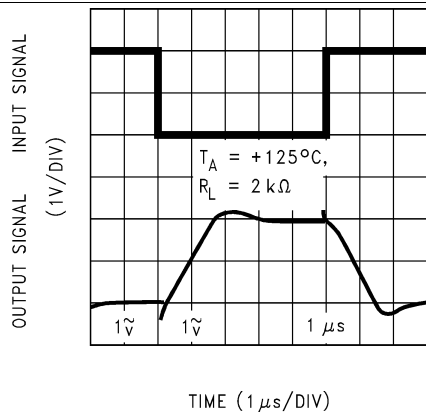


Figure 41. Inverting Large Signal Pulse Response

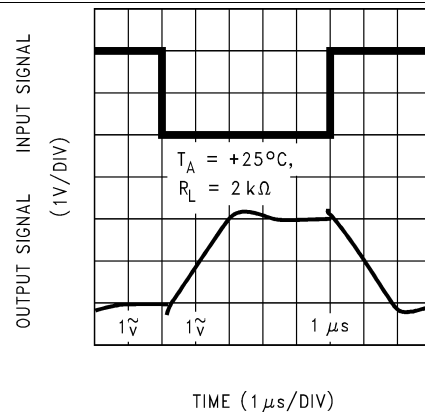


Figure 42. Inverting Large Signal Pulse Response

Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

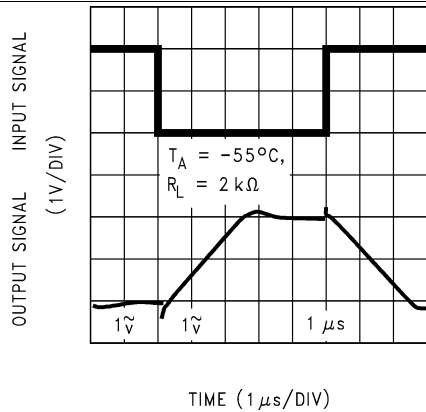


Figure 43. Inverting Large Signal Pulse Response

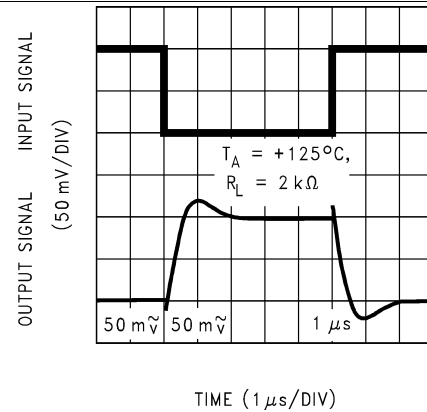


Figure 44. Inverting Small Signal Pulse Response

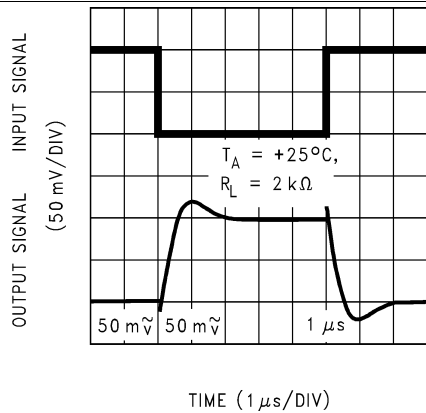


Figure 45. Inverting Small Signal Pulse Response

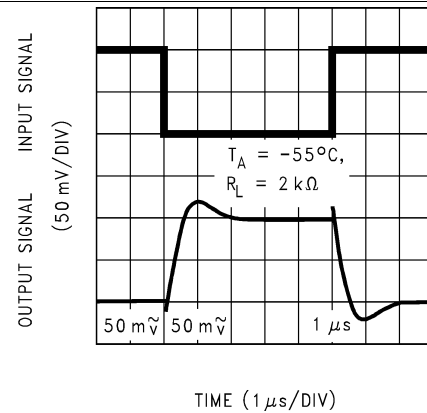


Figure 46. Inverting Small Signal Pulse Response

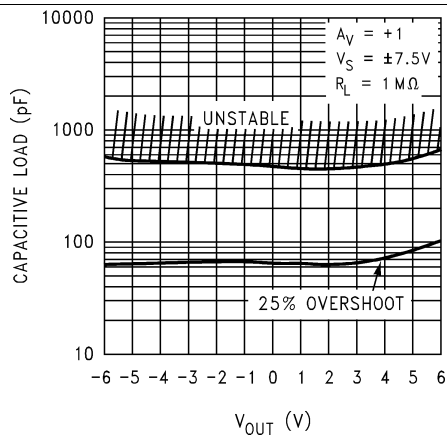


Figure 47. Stability vs. Capacitive Load

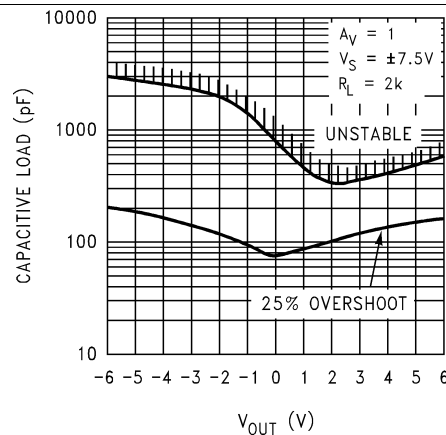


Figure 48. Stability vs. Capacitive Load

Typical Characteristics (continued)

$V_S = 15\text{ V}$ , Single Supply,  $T_A = 25^\circ\text{C}$  unless otherwise specified

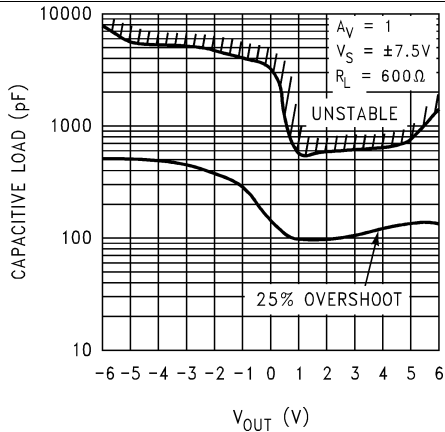


Figure 49. Stability vs. Capacitive Load

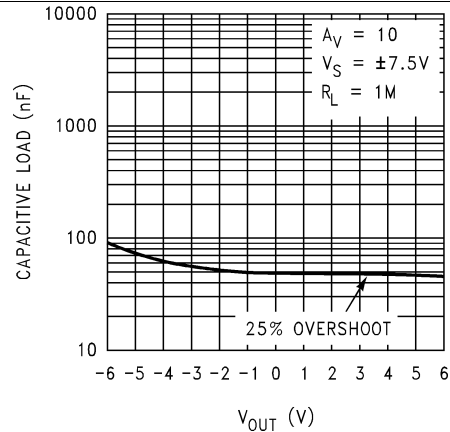


Figure 50. Stability vs. Capacitive Load

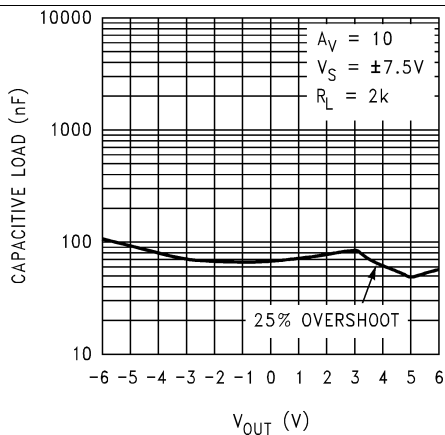


Figure 51. Stability vs. Capacitive Load

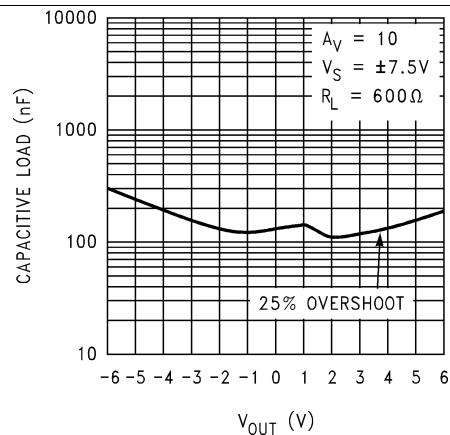


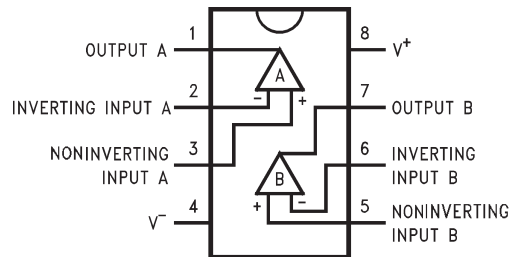
Figure 52. Stability vs. Capacitive Load

## 7 Detailed Description

### 7.1 Overview

The LMC6482-MIL is a dual CMOS operational amplifier that supports both rail-to-rail inputs and outputs. It may be operated in both dual supply mode and single supply mode.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

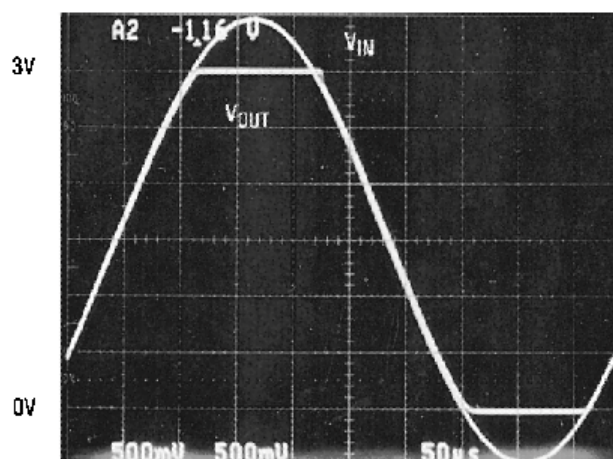
#### 7.3.1 Amplifier Topology

The LMC6482-MIL incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common-mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, crossover distortion, and open-loop gain variation.

The LMC6482-MILs input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

#### 7.3.2 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6482-MIL does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 53 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.



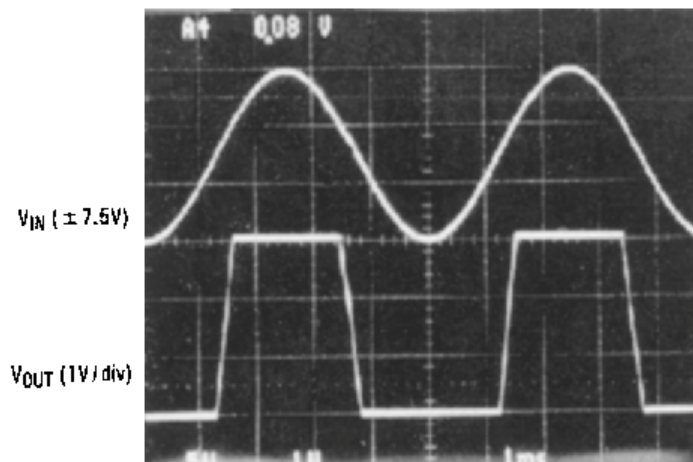
An input voltage signal exceeds the LMC6482-MIL power supply voltages with no output phase inversion.

**Figure 53. Input Voltage**

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 54, can cause excessive current to flow in or out of the input pins possibly affecting reliability.



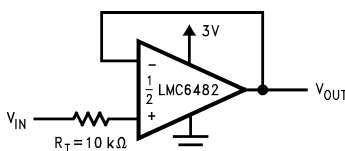
## Feature Description (continued)



A  $\pm 7.5\text{-V}$  input signal greatly exceeds the 3-V supply in [Figure 55](#) causing no phase inversion due to  $R_I$ .

**Figure 54. Input Signal**

Applications that exceed this rating must externally limit the maximum input current to  $\pm 5\text{ mA}$  with an input resistor ( $R_I$ ) as shown in [Figure 55](#).



$R_I$  input current protection for voltages exceeding the supply voltages.

**Figure 55.  $R_I$  Input Current Protection for Voltages Exceeding the Supply Voltages**

### 7.3.3 Rail-to-Rail Output

The approximated output resistance of the LMC6482-MIL is 180- $\Omega$  sourcing and 13-0 $\Omega$  sinking at  $V_S = 3\text{ V}$  and 110- $\Omega$  sourcing and 80- $\Omega$  sinking at  $V_S = 5\text{ V}$ . Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

## 7.4 Device Functional Modes

The LMC6482-MIL may be used in applications where each amplifier channel is used independently, or in applications in which the channels are cascaded. See [Typical Applications](#) for more information.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

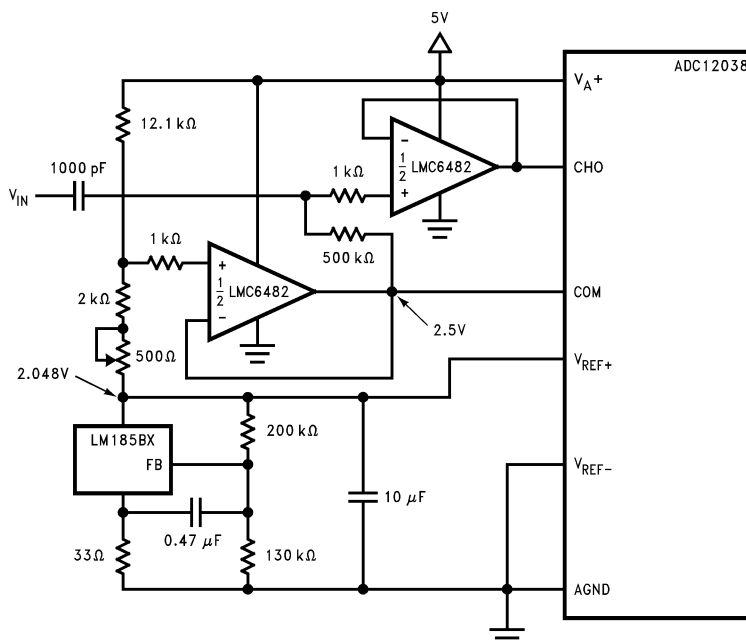
#### 8.1.1 Upgrading Applications

The LMC6484 quads and LMC6482-MIL duals have industry-standard pin outs to retrofit existing applications. System performance can be greatly increased by the features of the LMC6482-MIL. The key benefit of designing in the LMC6482-MIL is increased linear signal range. Most op-amps have limited input common-mode ranges. Signals that exceed this range generate a nonlinear output response that persists long after the input signal returns to the common-mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common-mode ranges resulting in output phase inversion or severe distortion.

#### 8.1.2 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482-MIL (Figure 56). Capable of using the full supply range, the LMC6482-MIL does not require input signals to be scaled down to meet limited common-mode voltage ranges. The LMC4282 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to  $\pm 0.325$  LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.



Operating from the same supply voltage, the LMC6482-MIL buffers the ADC12038 maintaining excellent accuracy.

**Figure 56. Buffering the ADC12038 With the LMC6482-MIL**

## Application Information (continued)

### 8.1.3 Instrumentation Circuits

The LMC6482-MIL has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482-MIL can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482-MIL an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with  $R_G$  to set the differential gain of the 3-op-amp instrumentation circuit in Figure 57. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

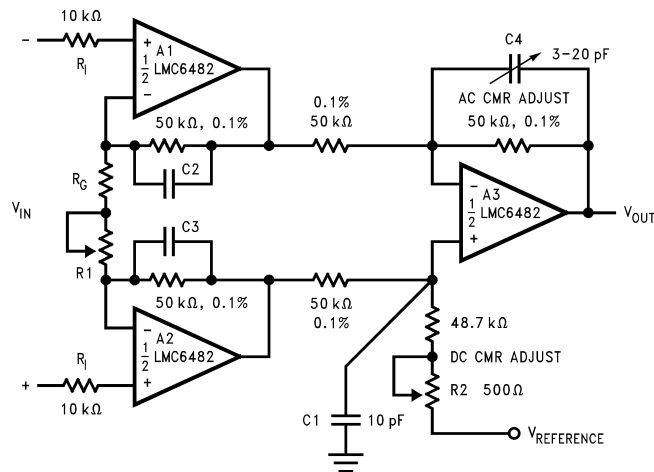


Figure 57. Low Power 3-Op-Amp Instrumentation Amplifier

A 2-op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 58. Low sensitivity trimming is made for offset voltage, CMRR, and gain. Low cost and low power consumption are the main advantages of this 2-op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a 3-op-amp instrumentation amplifier.

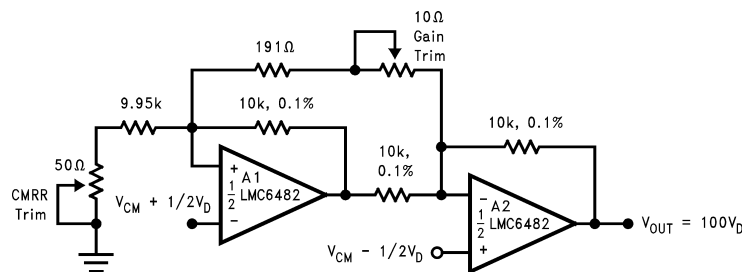


Figure 58. Low-Power Two-Op-Amp Instrumentation Amplifier

### 8.1.4 Spice Macromodel

A spice macromodel is available for the LMC6482-MIL. This model includes accurate simulation of the following:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

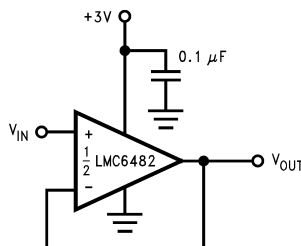
## Application Information (continued)

Many more characteristics are listed on the macromodel disk.

Contact your local TI sales office to obtain an operational amplifier spice model library disk.

## 8.2 Typical Applications

### 8.2.1 3-V Single Supply Buffer Circuit



**Figure 59. 3-V Single Supply Buffer Circuit**

#### 8.2.1.1 Design Requirements

For best performance, ensure that the input voltage swing is between  $V_+$  and  $V_-$ .

Ensure that the input does not exceed the common-mode input range.

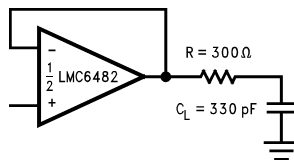
To reduce the risk of destabilizing the output, use resistive isolation on the output when driving capacitive loads (see the [Detailed Design Procedure](#) section).

When large feedback resistors are used, it may be necessary to compensate for parasitic capacitance on the input. See the [Detailed Design Procedure](#) section.

#### 8.2.1.2 Detailed Design Procedure

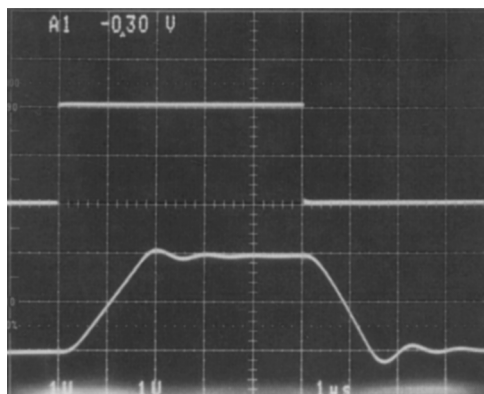
##### 8.2.1.2.1 Capacitive Load Compensation

Capacitive load compensation can be accomplished using resistive isolation as shown in [Figure 60](#). This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.



**Figure 60. Resistive Isolation of a 330-pF Capacitive Load**

**Typical Applications (continued)**

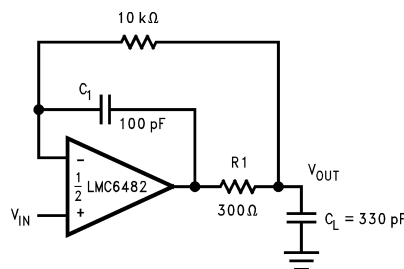


**Figure 61. Pulse Response of the LMC6482-MIL Circuit in Figure 60**

**8.2.1.2.1.1 Capacitive Load Tolerance**

The LMC6482-MIL can typically directly drive a 100-pF load with  $V_S = 15\text{ V}$  at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the output impedance of the op-amp and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Improved frequency response is achieved by indirectly driving capacitive loads, as shown in Figure 62.

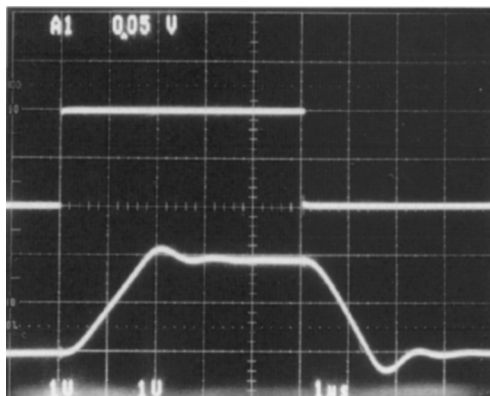


Compensated to handle a 330pF capacitive load.

**Figure 62. LMC6482-MIL Noninverting Amplifier**

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high-frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response is shown in Figure 63.

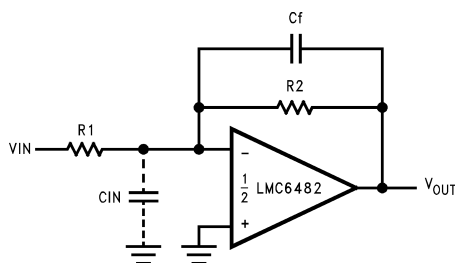
## Typical Applications (continued)



**Figure 63. Pulse Response of LMC6482-MIL Circuit in Figure 62**

### 8.2.1.2.1.2 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultralow input current, like the LMC6482-MIL. Large feedback resistors can react with small values of input capacitance due to transducers, photo diodes, and circuits board parasitics to reduce phase margins.



**Figure 64. Canceling the Effect of Input Capacitance**

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 64),  $C_f$ , is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

which typically provides significant overcompensation.

Printed-circuit-board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for  $C_f$  may be different. The values of  $C_f$  should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

### 8.2.1.2.1.3 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 65 and Figure 66. Large value resistances and potentiometers are used to reduce power consumption while providing typically  $\pm 2.5$  mV of adjustment range, referred to the input, for both configurations with  $V_S = \pm 5$  V.

Typical Applications (continued)

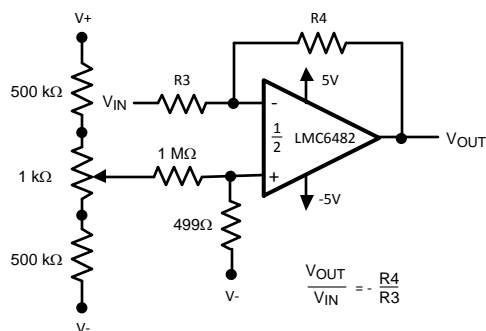


Figure 65. Inverting Configuration Offset Voltage Adjustment

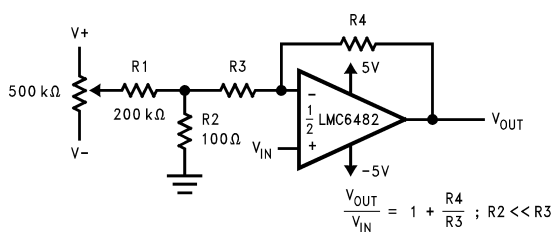
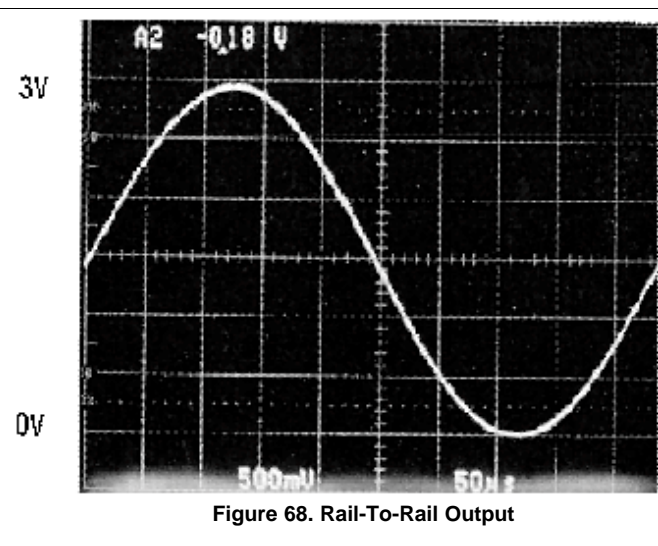
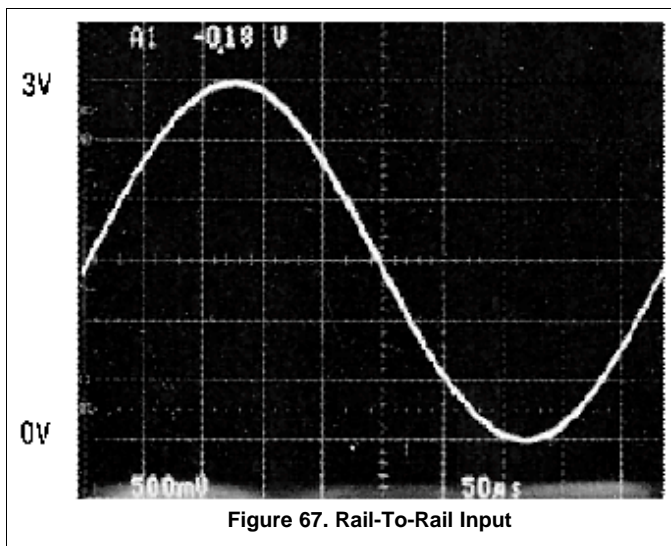


Figure 66. Noninverting Configuration Offset Voltage Adjustment

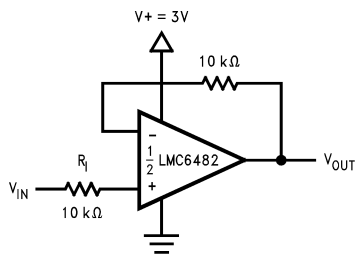
8.2.1.3 Application Curves



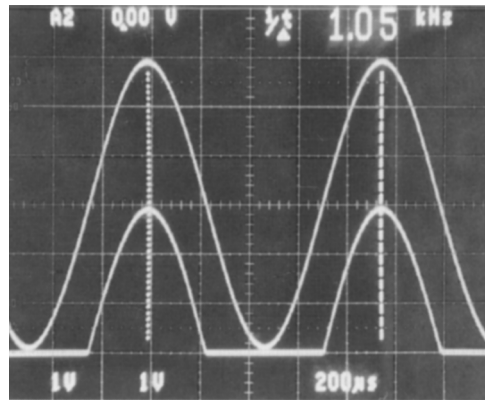
8.2.2 Typical Single-Supply Applications

The circuit in Figure 69 uses a single supply to half-wave rectify a sinusoid centered about ground. R<sub>1</sub> limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full-wave rectification is provided by the circuit in Figure 71.

**Typical Applications (continued)**



**Figure 69. Half-Wave Rectifier With Input Current Protection ( $R_I$ )**



**Figure 70. Half-Wave Rectifier Waveform**



Typical Applications (continued)

In Figure 75 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of  $C_H$  and diode leakage current. The ultralow input current of the LMC6482-MIL has a negligible effect on droop.

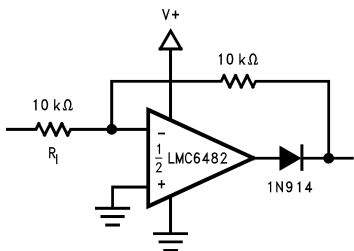


Figure 71. Full-Wave Rectifier With Input Current Protection ( $R_1$ )

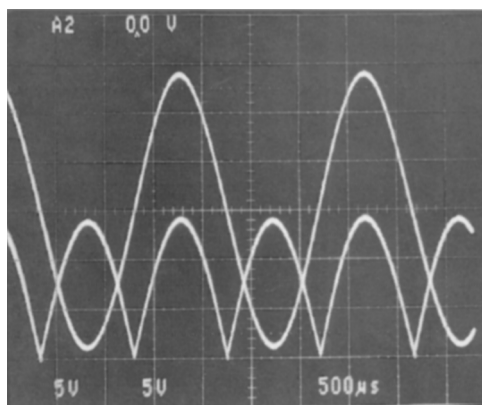


Figure 72. Full-Wave Rectifier Waveform

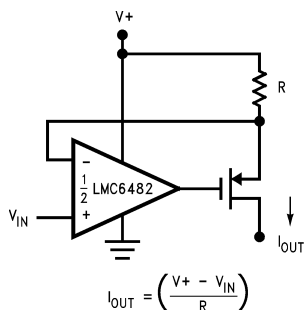


Figure 73. Large Compliance Range Current Source

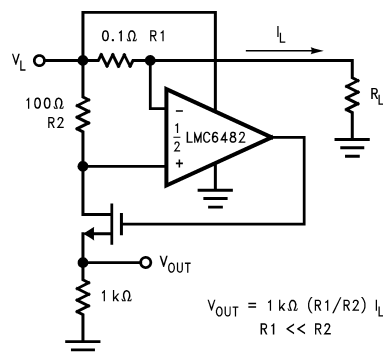


Figure 74. Positive Supply Current Sense

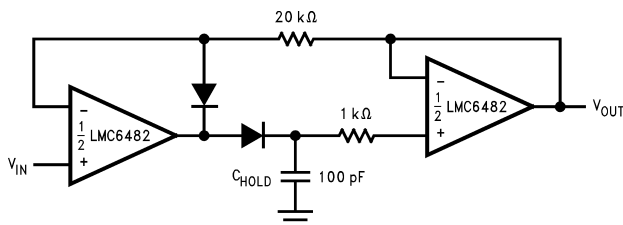
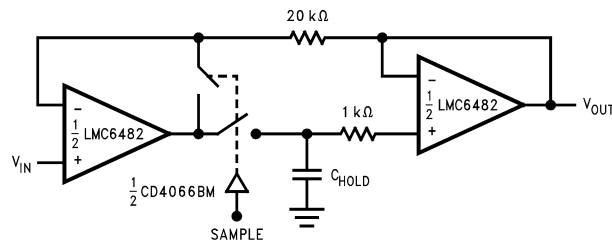


Figure 75. Low-Voltage Peak Detector With Rail-To-Rail Peak Capture Range

## Typical Applications (continued)

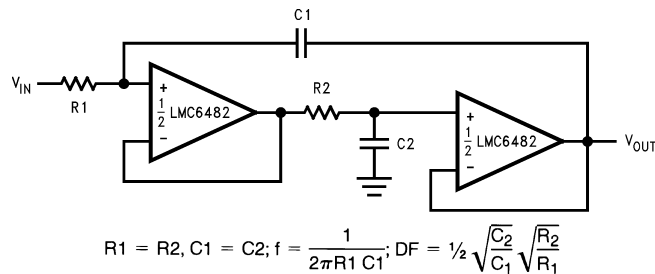
The high CMRR (82 dB) of the LMC6482-MIL allows excellent accuracy throughout the rail-to-rail dynamic capture range of the circuit.



**Figure 76. Rail-To-Rail Sample and Hold**

The low-pass filter circuit in [Figure 77](#) can be used as an anti-aliasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6482-MIL ultralow input current. The ultralow input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.



**Figure 77. Rail-To-Rail Single Supply Low Pass Filter**

## 9 Power Supply Recommendations

The LMC6482-MIL can be operated over a supply range of 3 V to 15 V. To achieve noise immunity as appropriate to the application, it is important to use good PCB layout practices for power supply rails and planes, as well as using bypass capacitors connected between the power supply pins and ground.

## 10 Layout

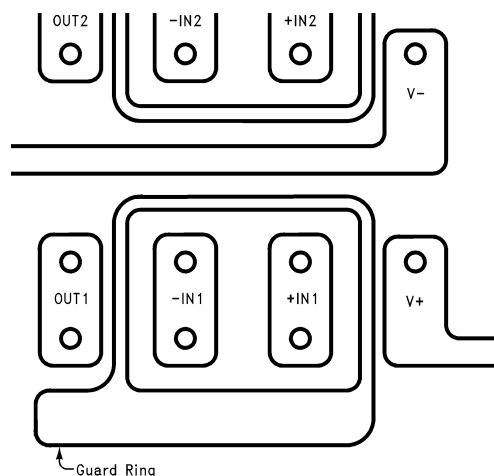
### 10.1 Layout Guidelines

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultralow input current of the LMC6482-MIL, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PCB, even through it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482s inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth connected to the inputs of the op-amp, as in [Figure 78](#). To have a significant effect, guard rings should be placed on both the top and bottom of the PCB. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of  $10^{12} \Omega$ , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input. This would cause a 250 times degradation from the actual performance of the LMC6482-MIL. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of  $10^{11} \Omega$  would cause only 0.05 pA of leakage current. See [Figure 79](#) through [Figure 81](#) for typical connections of guard rings for standard op-amp configurations.

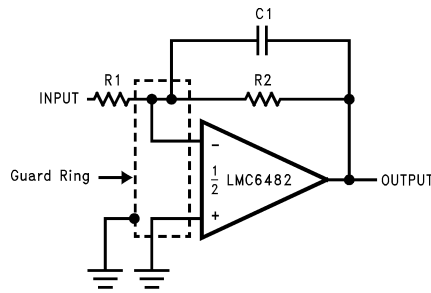
The designer should be aware that when it is inappropriate to lay out a PCB for the sake of just a few circuits, another technique is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the PCB at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 82](#).

### 10.2 Layout Example

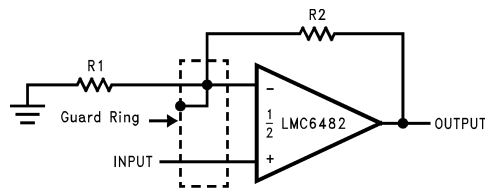


**Figure 78. Example of Guard Ring in PCB Layout Typical Connections of Guard Rings**

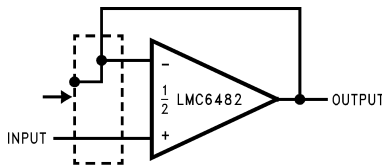
**Layout Example (continued)**



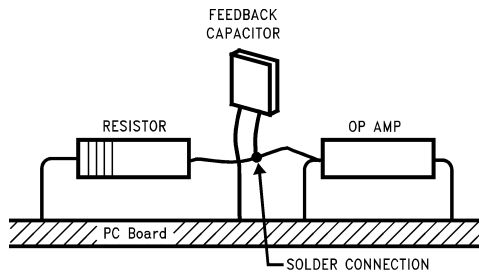
**Figure 79. Inverting Amplifier Typical Connections of Guard Rings**



**Figure 80. Noninverting Amplifier Typical Connections of Guard Rings**



**Figure 81. Follower Typical Connections of Guard Rings**



(Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB.)

**Figure 82. Air Wiring**

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6482AI MDA	ACTIVE	DIESALE	Y	0	324	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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