



ON Semiconductor®

FCB20N60-F085

N-Channel MOSFET

600V, 20A, 198mΩ

Features

- Typ $r_{DS(on)}$ = 173mΩ at V_{GS} = 10V, I_D = 20A
- Typ $Q_{g(tot)}$ = 72nC at V_{GS} = 10V, I_D = 20A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

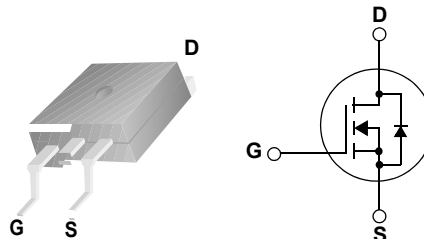
Description

SuperFET™ is ON Semiconductor's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on-resistance and

lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.

Consequently, SuperFET is suitable for various automotive DC/DC power conversion.



Applications

- Automotive On Board Charger
- Automotive DC/DC converter for HEV

MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	600	V
V_{GS}	Gate to Source Voltage	±30	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	$T_C = 25^\circ\text{C}$	A
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	480	mJ
P_D	Power Dissipation	341	W
	Derate above 25°C	2.3	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.44	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	43	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCB20N60	FCB20N60-F085	TO-263AB	330mm	24mm	800 units

Notes:

1: Current is limited by bondwire configuration.

2: Starting $T_J = 25^\circ\text{C}$, $L = 15\text{mH}$, $I_{AS} = 8\text{A}$, $V_{DD} = 100\text{V}$ during inductor charging and $V_{DD} = 0\text{V}$ during time in avalanche

3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	600	-	-	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 600\text{V}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0\text{V}$, $T_J = 150^\circ\text{C}(\text{Note 4})$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 30\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	3.0	4.0	5.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 20\text{A}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 10\text{V}$, $T_J = 150^\circ\text{C}(\text{Note 4})$	-	173	198	$\text{m}\Omega$
			-	471	570	$\text{m}\Omega$

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	2710	3080	pF
C _{oss}	Output Capacitance			-	1350	1665	pF
C _{rss}	Reverse Transfer Capacitance			-	86	150	pF
R _g	Gate Resistance	f = 1MHz		-	1	-	Ω
Q _{g(ToT)}	Total Gate Charge at 10V	V _{GS} = 0 to 10V	V _{DD} = 300V I _D = 20A	-	72	102	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 to 2V		-	5	8.6	nC
Q _{gs}	Gate to Source Gate Charge			-	15	-	nC
Q _{gd}	Gate to Drain “Miller” Charge			-	31	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 300\text{V}$, $I_D = 20\text{A}$, $V_{GS} = 10\text{V}$, $R_G = 25\Omega$	-	-	166	ns
$t_{d(on)}$	Turn-On Delay Time		-	44	-	ns
t_r	Rise Time		-	60	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	208	-	ns
t_f	Fall Time		-	43	-	ns
t_{off}	Turn-Off Time		-	-	400	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 20\text{A}$, $V_{GS} = 0\text{V}$	-	-	1.4	V
T_{rr}	Reverse Recovery Time	$I_F = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	486	632	ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 480\text{V}$	-	10	13	μC

Notes:

4: The maximum value is specified by design at $T_J = 150^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

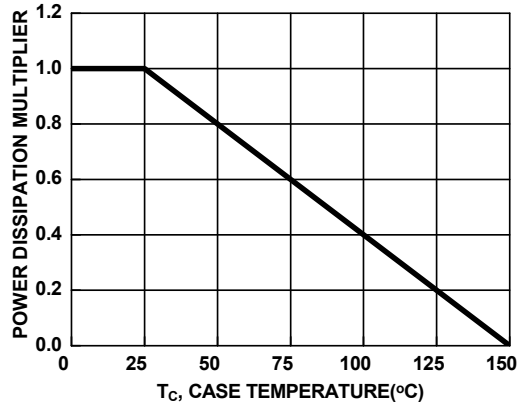


Figure 1. Normalized Power Dissipation vs Case Temperature

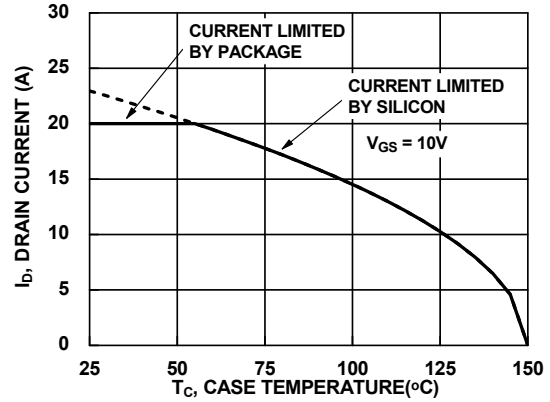


Figure 2. Maximum Continuous Drain Current vs Case Temperature

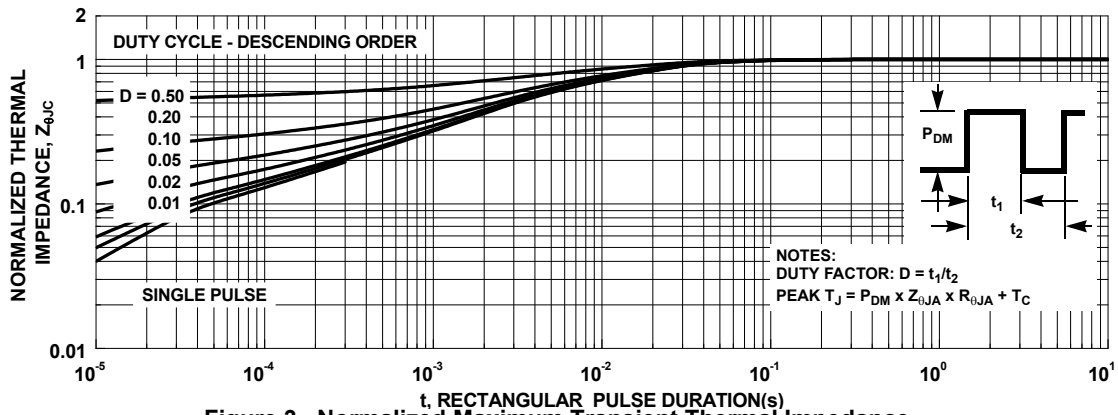


Figure 3. Normalized Maximum Transient Thermal Impedance

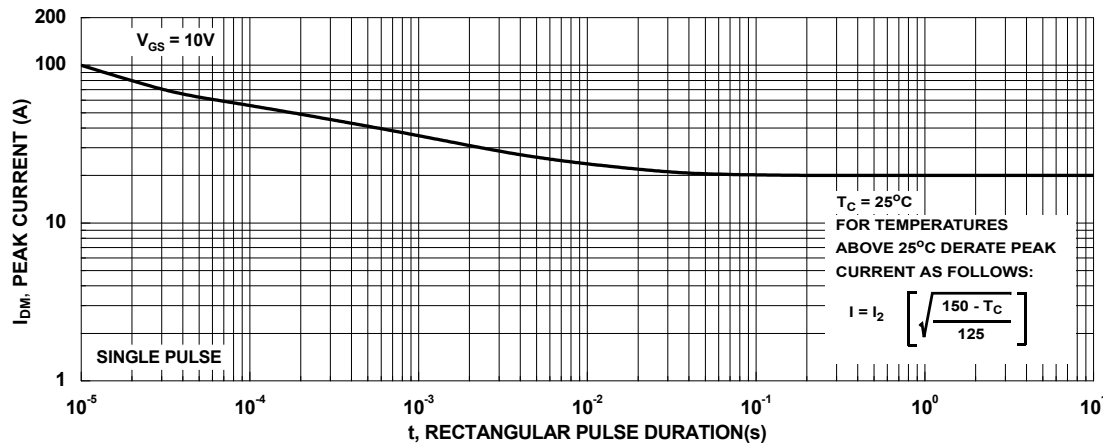


Figure 4. Peak Current Capability

Typical Characteristics

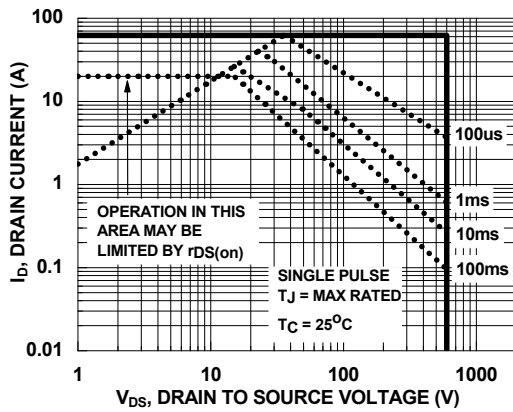


Figure 5. Forward Bias Safe Operating Area

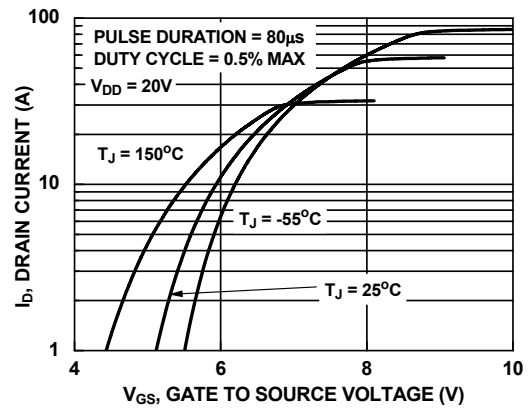


Figure 6. Transfer Characteristics

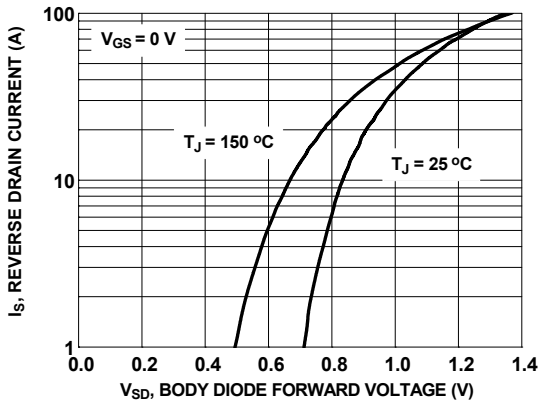


Figure 7. Forward Diode Characteristics

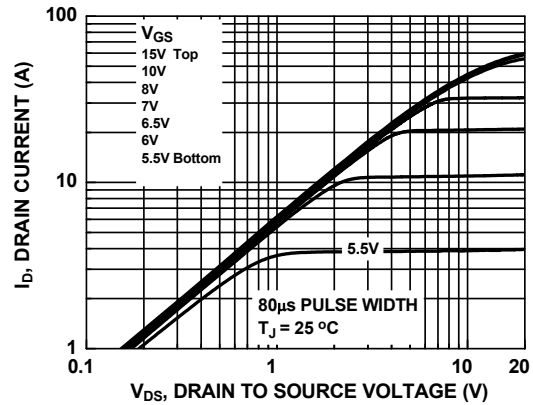


Figure 8. Saturation Characteristics

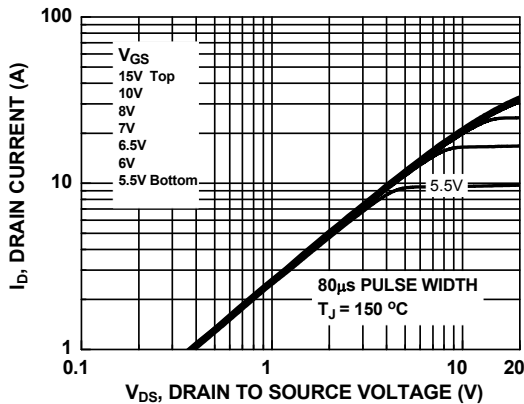


Figure 9. Saturation Characteristics

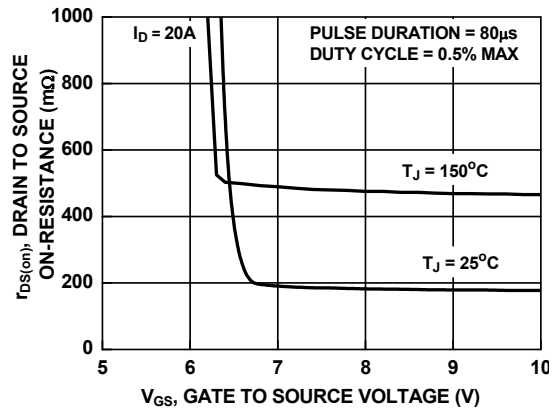


Figure 10. Rdson vs Gate Voltage

Typical Characteristics

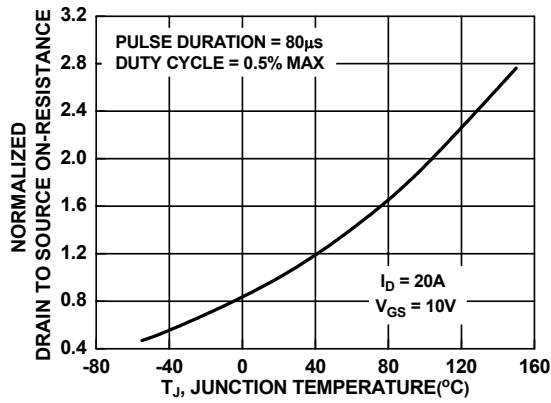


Figure 11. Normalized $R_{DS(on)}$ vs Junction Temperature

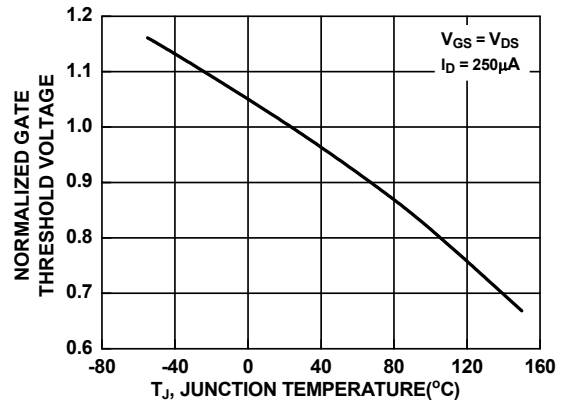


Figure 12. Normalized Gate Threshold Voltage vs Temperature

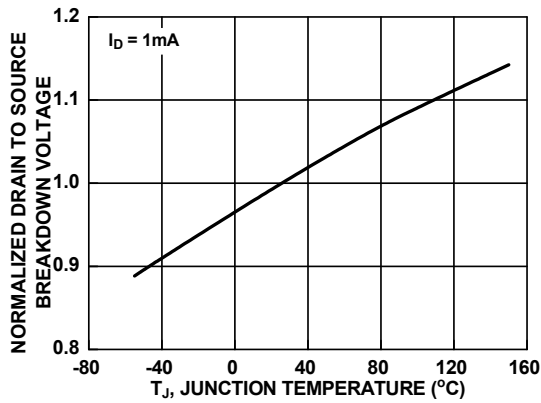


Figure 13. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

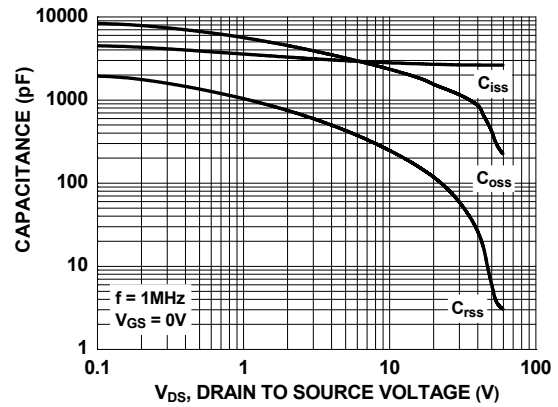


Figure 14. Capacitance vs Drain to Source Voltage

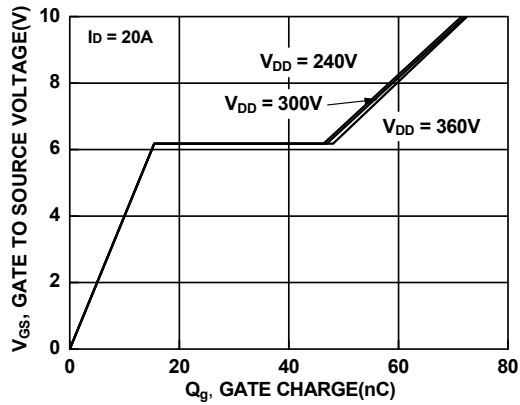


Figure 15. Gate Charge vs Gate to Source Voltage

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