

MC10ELT22, MC100ELT22

5.0 V Dual TTL to Differential PECL Translator

The MC10ELT/100ELT22 is a dual TTL to differential PECL translator. Because PECL (Positive ECL) levels are used only +5 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the ELT22 makes it ideal for applications which require the translation of a clock and a data signal.

Features

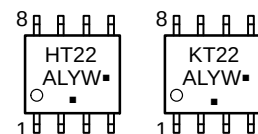
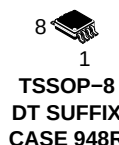
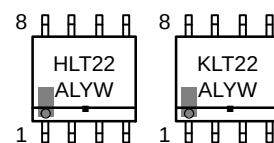
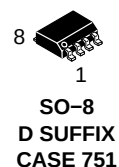
- 1.2 ns Typical Propagation Delay
- < 300 ps Typical Output to Output Skew
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- Operating Range: $V_{CC} = 4.75\text{ V}$ to 5.25 V with $GND = 0\text{ V}$
- No Internal Input Pulldown Resistors
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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MARKING DIAGRAMS*



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional information, see Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC10ELT22, MC100ELT22

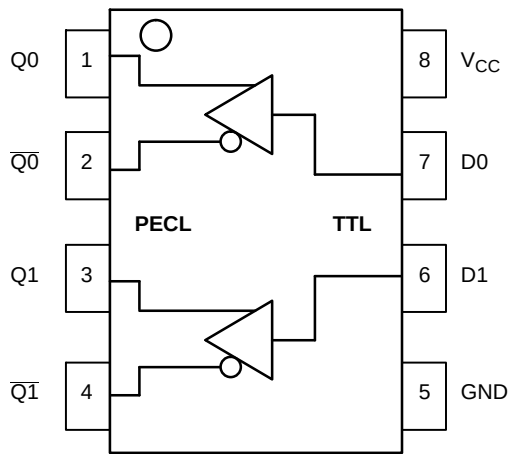


Table 1. PIN DESCRIPTION

Pin	Function
$Q_n, \overline{Q_n}$	PECL Differential Outputs*
D_n	TTL Inputs
V_{CC}	Positive Supply
GND	Ground

*Output state undetermined when inputs are open.

Figure 1. Logic Diagram and Pinout Assignment

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		51
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MC10ELT22, MC100ELT22

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Positive Power Supply	GND = 0 V		7	V
V _{IN}	Input Voltage	GND = 0 V		$GND + 0.025 \leq V_I \leq V_{CC} - 0.025$	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 SOIC	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 TSSOP	41 to 44 ± 5%	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. 10ELT SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; GND = 0.0 V (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{CC}	Power Supply Current			22			22			22	mA
V _{OH}	Output HIGH Voltage (Note 3)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V _{OL}	Output LOW Voltage (Note 3)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
- Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.

Table 5. 100ELT SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; GND = 0.0 V (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{CC}	Power Supply Current			22			22			22	mA
V _{OH}	Output HIGH Voltage (Note 5)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V _{OL}	Output LOW Voltage (Note 5)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
- Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.

MC10ELT22, MC100ELT22

Table 6. TTL INPUT DC CHARACTERISTICS $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$; $T_A = -40^\circ\text{C to } 85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	$V_{IN} = 2.7 \text{ V}$; $V_{IN} = (V_{CC} - 0.025) \text{ V}$			20	μA
I_{IHH}	Input HIGH Current	$V_{IN} = 7.0 \text{ V}$			100	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.5 \text{ V}$; $V_{IN} = (\text{GND} + 0.025) \text{ V}$			-0.6	mA
V_{IK}	Input Clamp Diode Voltage	$I_{IN} = -18 \text{ mA}$			-1.2	V
V_{IH}	Input HIGH Voltage		2.0		$V_{CC} - 0.025 \text{ V}$	V
V_{IL}	Input LOW Voltage		$\text{GND} + 0.025 \text{ V}$		0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

Table 7. AC CHARACTERISTICS $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$; $\text{GND} = 0.0 \text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Input Frequency					500					MHz
t_{PLH}	Propagation Delay (Note 6) 1.5 V to 50%	0.6		1.2	0.9	1.2	1.5	0.6		1.35	ns
t_{PHL}	Propagation Delay (Note 6) 1.5 V to 50%	0.4		1.0	0.5	0.8	1.1	0.7		1.30	ns
t_{skew}	Within-Device Skew (Note 7) Device-to-Device Skew (Note 8)		50 300	100 600		50 300	100 600		50 350	100 750	ps
t_{JITTER}	CLOCK Random Jitter (RMS)					0.5					ps
t_r/t_f	Output Rise/Fall Time (20–80%)	0.4		1.6	0.4		1.6	0.4		1.6	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Specifications for standard TTL input signal.

7. Skew is measured between outputs under identical transitions and conditions on any one device.

8. Device-to-Device Skew for identical transitions at identical V_{CC} levels.

MC10ELT22, MC100ELT22

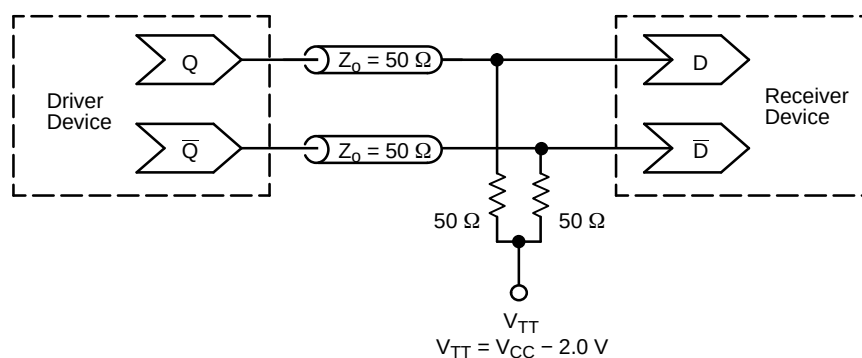


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10ELT22DG	SO-8 (Pb-Free)	98 Units / Rail
MC10ELT22DR2G	SO-8 (Pb-Free)	2500 Tape & Reel
MC10ELT22DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10ELT22DTR2G	TSSOP-8 (Pb-Free)	2500 Tape & Reel
MC100ELT22DG	SO-8 (Pb-Free)	98 Units / Rail
MC100ELT22DR2G	SO-8 (Pb-Free)	2500 Tape & Reel
MC100ELT22DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT22DTR2G	TSSOP-8 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

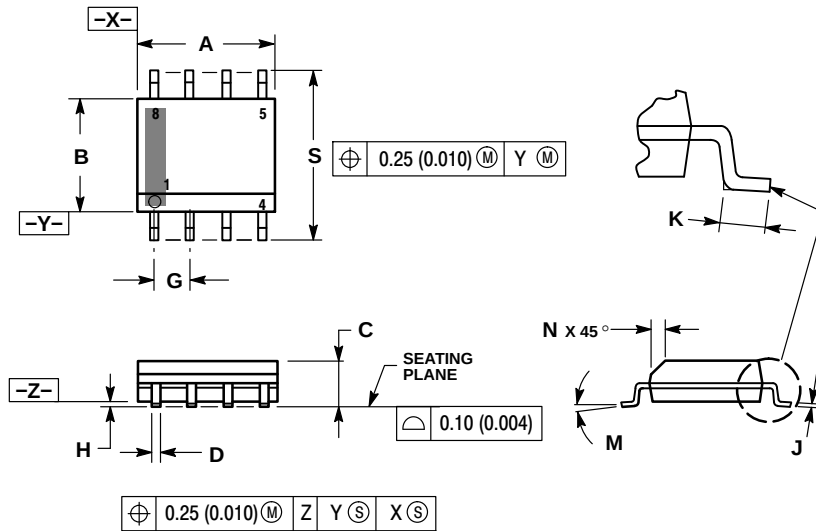
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC10ELT22, MC100ELT22

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

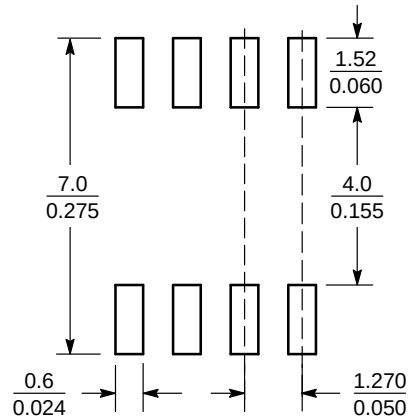


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



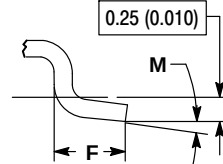
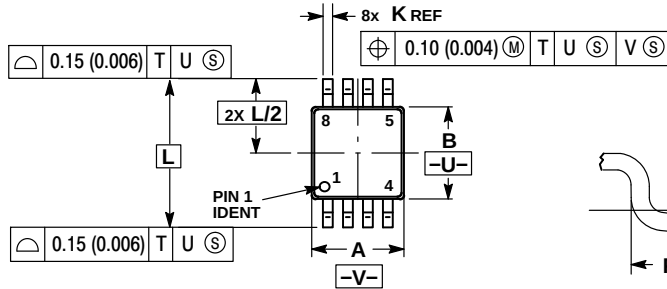
SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

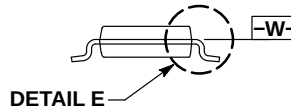
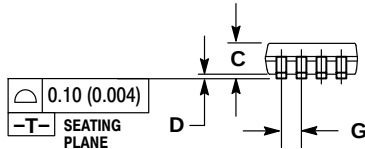
MC10ELT22, MC100ELT22

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
CASE 948R-02
ISSUE A



DETAIL E



DETAIL E

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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