UCC24630 Synchronous Rectifier Controller With Ultra-Low-Standby Current

1 Features

- Secondary-Side SR Controller Optimized for 5-V to 24-V Flyback Systems
- Operating Frequency Up to 200 kHz
- Volt-Second Balance SR On-Time Control
- Minimize Effect of MOSFET Device and Layout Inductance
- CCM Operation Compatibility
- Compatible with PSR and SSR Control
- Auto Low-Power Detect and 110-µA Standby Mode Current
- Wide VDD Range from 3.6 V to 28 V
- Rail-to-Rail Gate Driver with 13-V Clamp
- Open and Short Pin Fault Protection

2 Applications

- 5-V to 24-V Output Flyback and Forward Converters
- USB-PD Adapters and Chargers with Type-C Connector
- Chargers for Smart Phones and Tablets
- Notebook and Ultrabook Adapters
- High Efficiency Auxiliary Power in Server, Desktop and Appliance Applications
- Industrial and Medical SMPS

3 Description

The UCC24630 SR controller is a high-performance controller and driver for N-channel MOSFET power devices used for secondary-side synchronous rectification.

The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also reduces primary-side losses as well, due to compounding of efficiency gains.

Utilizing a volt-second balancing control method, the UCC24630 is ideal for flyback power supplies over a wide-output voltage range since the device is not connected directly to the MOSFET drain. The SR drive turn-off threshold is not dependent on the MOSFET $R_{DS(on)}$ which allows optimizing for maximum conduction time. Also secondary current ringing due to device and layout inductance does not affect the SR turn-off threshold.

The UCC24630 controller offers a programmable false-trigger filter, a frequency detector to automatically switch to standby mode during low power conditions and pin fault protections. The UCC24630 is compatible with DCM, TM and CCM operation.

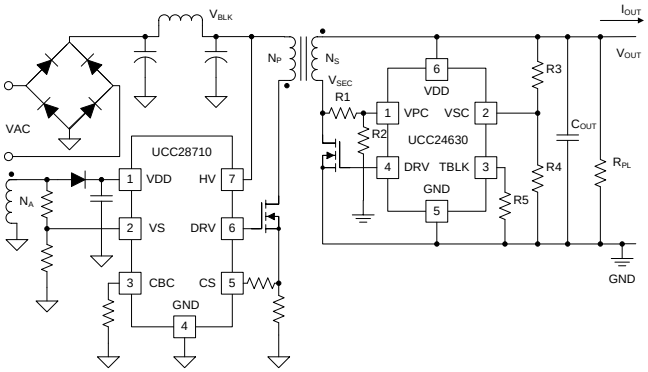
The wide VDD operating range, wide programming range of the VPC voltage and blanking time, allows use in a variety of flyback converter designs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC24630	SOT23 (6)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Gate-Drive Timing vs VDS Sensing SR Driver

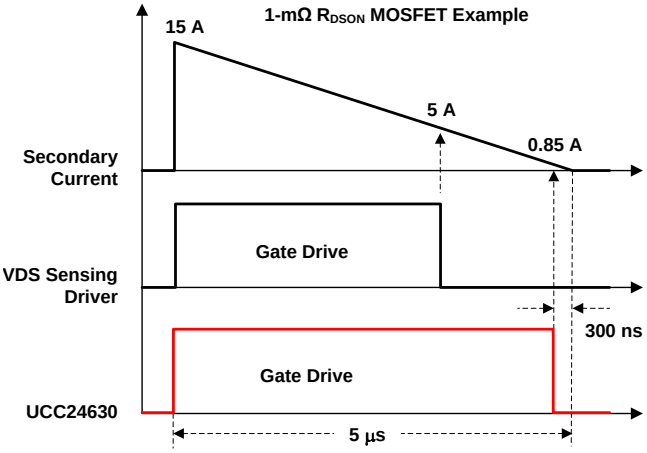


Table of Contents

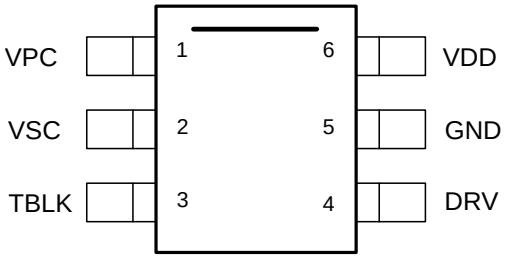
4 Revision History

Changes from Original (March 2015) to Revision A **Page**

- Changed Applications section typo. ... 1

5 Pin Configuration and Functions

DBV Package
6-Pin SOT23
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
DRV	4	O	**DRiVe** is an output used to drive the gate of an external synchronous rectifier N-channel MOSFET switching transistor, with source pin connected to GND.
GND	5	G	The **GrouND** pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
TBLK	3	–	**Time BLanK** pin is used to select the blanking time of the VPC rising edge. A programmable range from 200 ns to 1 µs is available to prevent false detection of the primary on-time due to ringing during DCM operation.
VDD	6	P	**VDD** is the bias supply input pin to the controller. A carefully placed bypass capacitor to GND is required on this pin.
VPC	1	I	The **Voltage during Primary Conduction** pin is connected to a resistor divider from the SR MOSFET drain. This pin determines a sample of the primary-side MOSFET volt seconds during the primary on-time. This voltage programs a voltage controlled current source for the internal VPC ramp charging current.
VSC	2	I	The **Voltage during Secondary Conduction** pin is connected to a resistor divider from the power-supply output. This pin determines a sample of the secondary-side output voltage used to determine SR MOSFET conduction time. This voltage programs a voltage controlled current source for the internal VSC ramp charging current.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{VDD}	Bias supply voltage, VDD	–0.3	30	V
I_{DRV}	Continuous gate current sink, DRV		50	mA
I_{DRV}	Continuous gate current source, DRV		–50	mA
I_{VPC}	Peak VPC pin current		–1.2	mA
V_{DRV}	Gate drive voltage at DRV	–0.3	Self limiting	V
V_{VPC}, V_{VSC}	Voltage range, VPC, VSC	–0.3	4.5	V
T_J	Operating junction temperature range	–55	150	°C
T_L	Lead temperature 0.6 mm from case for 10 seconds		260	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VDD}	Bias supply operating voltage	3.75	28	V
C_{VDD}	VDD bypass capacitor	0.47		µF
T_J	Operating junction temperature	-40	125	°C
V_{VPC}, V_{VSC}	Operating Range	–0.3	2.3	V

6.4 Thermal Information

THERMAL METRIC (1)		UCC24630 DBV (6 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	44	
ψ_{JT}	Junction-to-top characterization parameter	5.1	
ψ_{JB}	Junction-to-board characterization parameter	13.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating free-air temperature range, VDD = 12V, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state, F_{SW} = 0 kHz		0.9	1.2	mA
I_{STBY}	Supply current, standby	I_{DRV} = 0, standby mode		110	160	µA
UNDER-VOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	3.9	4	4.3	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	3.3	3.6	3.7	V
DRV						
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 100 mA		1	2	Ω
V_{DRVST}	DRV pull down in start-up	V_{DD}= 0 to 2 V, I_{DRV}= 10 µA			0.95	V
V_{DRCL}	DRV clamp voltage	V_{VDD} = 30 V	11	13	15	V
V_{PMOS}	Disable PMOS high-side drive	V_{DD} voltage to disable rail-to-rail drive, V_{DD} rising	9.3	10	10.5	V
$V_{PMOS-HYS}$	PMOS enable hysteresis	V_{DD} voltage hysteresis to enable rail to rail drive, V_{DD} falling	0.75	1	1.25	V
V_{DRHI}	DRV pull-up high voltage	V_{VDD} = 5 V, I_{DRV} = 15 mA	4.6	4.75	5	V
VSC INPUT						
V_{VSCEN}	SR enable voltage	V_{VSC} > V_{VSCEN}, V_{VSC} rising	250	300	340	mV
$V_{VSC-HYS}$	SR enable hysteresis	V_{VSC} falling		50		mV
V_{VSCDIS}	SR disable voltage		220		280	mV
I_{VSC}	Input bias current	V_{VSC} = 2 V	–0.25	0	0.4	µA
VPC INPUT						
V_{VPCEN}	SR enable voltage	V_{VPCEN} < V_{VPC}	345	400	450	mV
V_{VPCDIS}	VPC threshold to disable SR	V_{VPC} > V_{VPCDIS}	2.6	2.85	3.1	V
V_{VPC-TH}	Threshold of V_{VPC} rising edge	V_{VPC} = 0.95 V, V_{VPC-TH} = 0.85 x V_{VPC} previous cycle	0.76	0.808	0.86	V
$V_{VPC-TH-CLP}$	Clamp threshold of V_{VPC} rising edge	V_{VPC} = 2 V	0.9	1	1.1	V
I_{VPC}	Input bias current	V_{VPC} = 2 V	–0.25	0	0.4	µA
CURRENT EMULATOR						
$Ratio_{VPC\_VSC}$	K_{VPC}/K_{VSC}	V_{VPC} = 1.25 V, t_{VPC} = 1 µs, V_{VSC} = 1.25 V	3.97	4.17	4.35	
		V_{VPC} = 1.25 V, t_{VPC} = 5 µs, V_{VSC} = 1.25 V	3.95	4.17	4.37	
		V_{VPC} = 2 V, t_{VPC} = 1 µs, V_{VSC} = 1.25 V	3.85	4.09	4.26	
		V_{VPC} = 1.25 V, t_{VPC} = 1 µs, V_{VSC} = 0.45 V	3.85	4.07	4.28	
CCM DEAD TIME						
$K_{CCM-FAULT}$	If t_{SW} (N+1) > t_{SW} (N) x $K_{CCM-FAULT}$, disable SR		140%	150%	165%	
$n_{CCM-FLT}$	Number of cycles to exit CCM fault if t_{SW} (N+1) < t_{SW} (N) x $K_{CCM-FAULT}$			4		

Electrical Characteristics (continued)

Over operating free-air temperature range, VDD = 12V, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
STANDBY OPERATION						
n_{ENTO}	Number of switching cycles to enter standby operation during t_{ENTO}			64		
n_{EN}	Number of switching cycles to exit standby operation during t_{EN} (1)			32		
OVER TEMPERATURE PROTECTION						
$T_{(STOP)}$	Thermal shutdown temperature	Internal junction temperature		165		°C

(1) The device exits standby operation as soon as n_{EN} occurs within t_{EN}.

6.6 Timing Requirements

Over operating free-air temperature range, VDD = 12 V, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DRV						
t_R	DRV high-side rise time	V_{VDD} = 12 V, C_L = 3.3 nF, V_{DRV} = 2 V to 8 V		27	54	ns
		V_{VDD} = 5 V, C_L = 3.3 nF, V_{DRV} = 1 V to 4 V		50	100	ns
t_F	DRV low-side fall time	V_{VDD} = 12 V, C_L = 3.3 nF, V_{DRV} = 8 V to 2 V		20	54	ns
		V_{VDD} = 5 V, C_L = 3.3 nF, V_{DRV} = 4 V to 1 V		15	50	ns
t_{DRVON}	Propagation delay to DRV High	V_{VPC} = 1 V to –0.05 V falling to DRV high, V_{VDD} = 12 V, V_{DRV} = 0 V to 2 V		80	160	ns
t_{DRVOFF}	Propagation delay to DRV Low	Test mode		65	95	ns
VPC Input						
$t_{VPC-SPL}$	VPC sampling time window		81	100	125	ns
$t_{VPC-BLK}$	Minimum VPC pulse for SR DRV operation	R_{TBLK} = 5 kΩ	169	203	239	ns
		R_{TBLK} = 50 kΩ	0.87	1.04	1.2	µs
SR On Control						
$t_{SRONMIN}$	SR minimum on time after VPC falling.		300	350	425	ns
t_{OFF}	SR off blanking time from DRV falling.		2.35	2.5	2.65	us
CCM Dead Time						
t_{CCMDT}	SR turn-off dead time in CCM cycle limit	F_{SW} = 100 kHz, R_{TBLK} = 50 kΩ (1 µs $t_{VPC-BLK}$ setting)	500	600	700	ns
Standby Operation						
t_{ENTO}	Time to disable SR operation, enter standby	Time to disable DRV	11.5	12.8	14.1	ms
t_{EN}	Time to enable SR operation, exit standby operation	Time to enable DRV (1)	2.3	2.56	2.82	ms

(1) The device exits standby operation as soon as n_{EN} occurs within t_{EN}.

6.7 Typical Characteristics

V_{VDD} = 12 V, T_J = 25°C, unless otherwise noted.

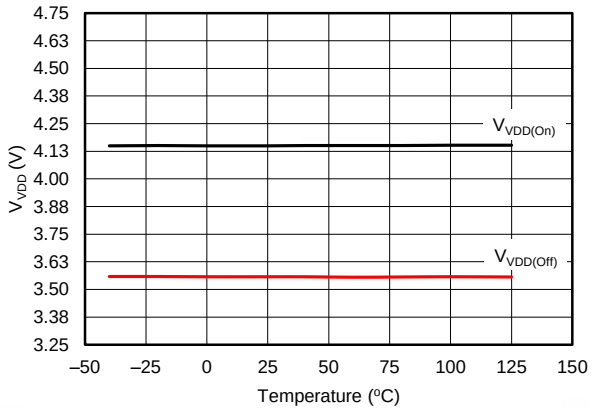


Figure 1. VDD Turn-On and Turn-Off Threshold vs Temperature

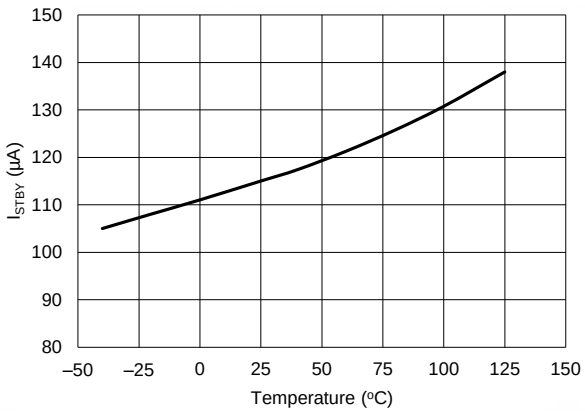


Figure 2. Standby Current vs Temperature

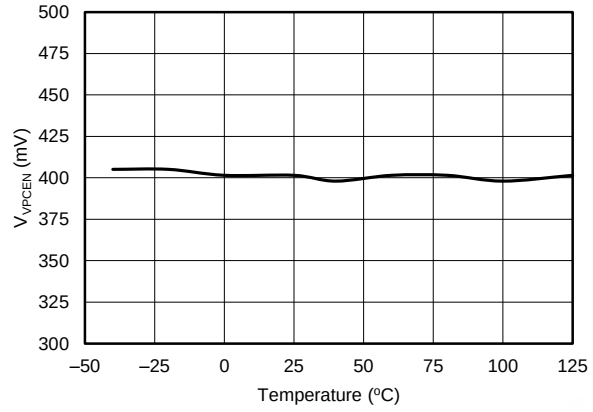


Figure 3. VPC Enable Threshold vs Temperature

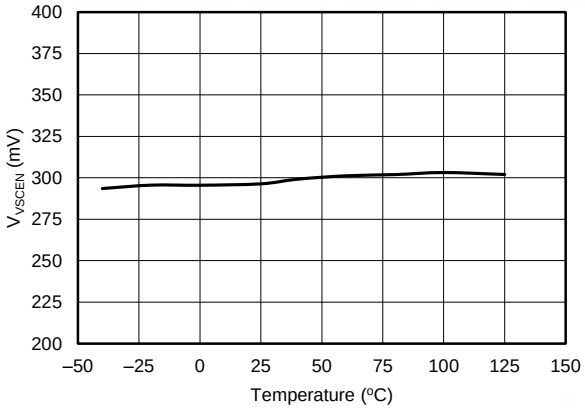
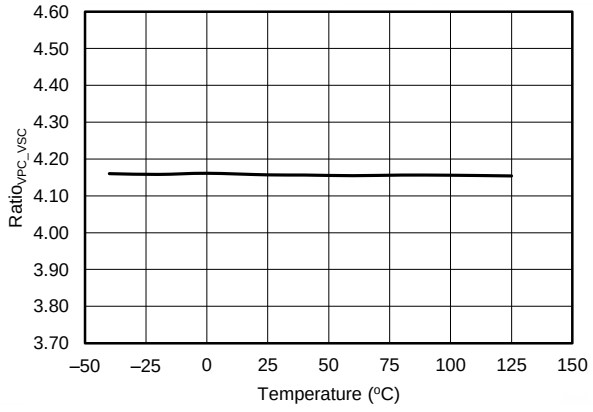
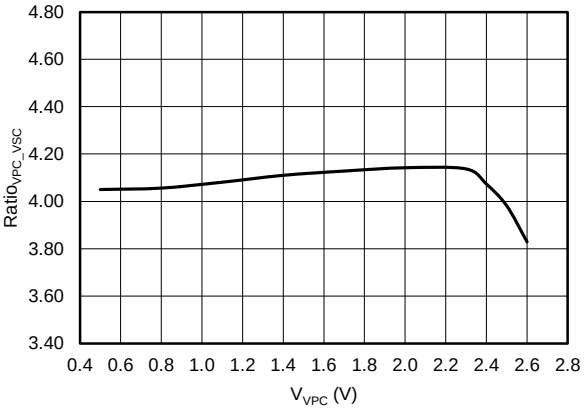


Figure 4. VSC Enable Threshold vs Temperature



V_{VPC} = 1.25 V t_{VPC} = 1 µs V_{VSC} = 1.25 V

Figure 5. VPC-to-VSC Ramp Gain Ratio vs Temperature

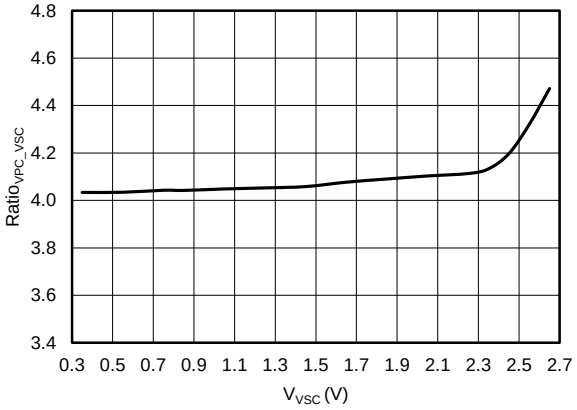


V_{VSC} = 1.25 V $t_{VPC} \times V_{VPC}$ = 3 V-µs

Figure 6. VPC-to-VSC Ramp-Gain Ratio vs VPC Voltage

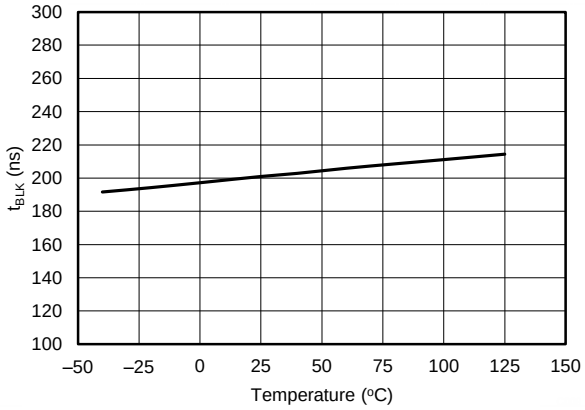
Typical Characteristics (continued)

V_{VDD} = 12 V, T_J = 25°C, unless otherwise noted.



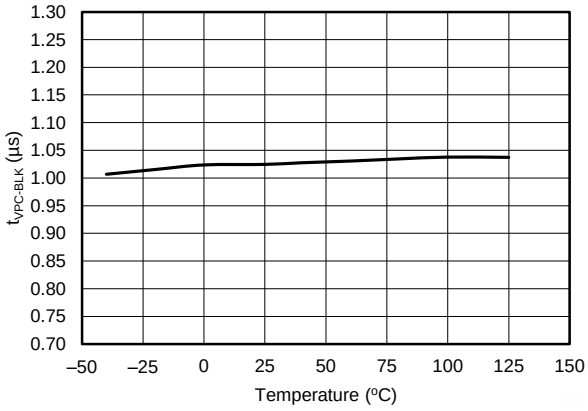
V_{VPC} = 12 V t_{VPC} = 2 µs

Figure 7. VPC-to-VSC Ramp-Gain Ratio vs VSC Voltage



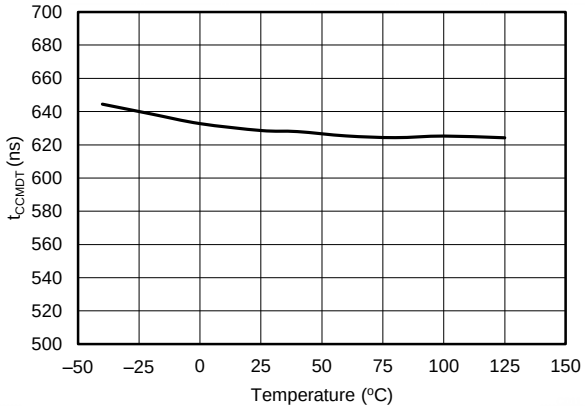
R_{TBLK} = 5 kΩ

Figure 8. VPC Blanking Time vs Temperature (minimum setting)



R_{TBLK} = 50 kΩ

Figure 9. VPC Blanking Time vs Temperature (maximum setting)



Fsw = 100 kHz R_{TBLK} = 50 k

Figure 10. CCM Dead Time vs Temperature

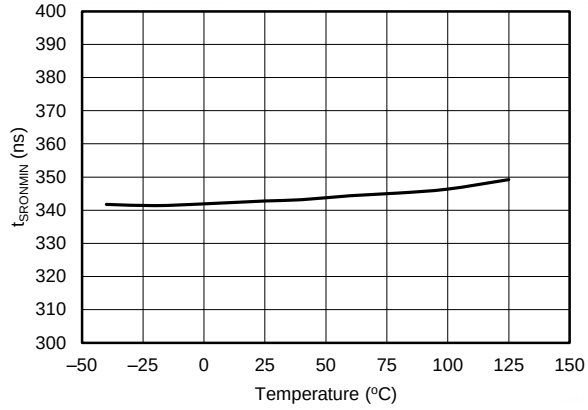


Figure 11. DRV Minimum On Time vs Temperature

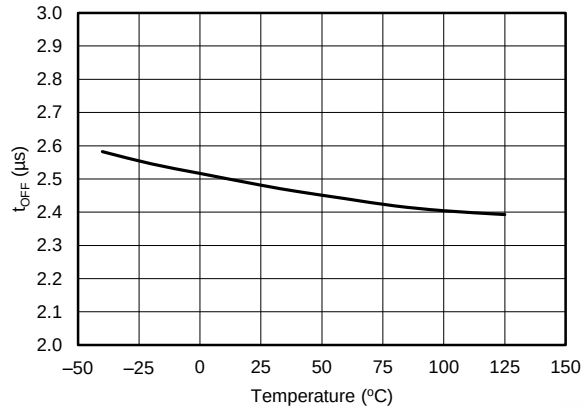


Figure 12. DRV Minimum Off Time vs Temperature

7 Detailed Description

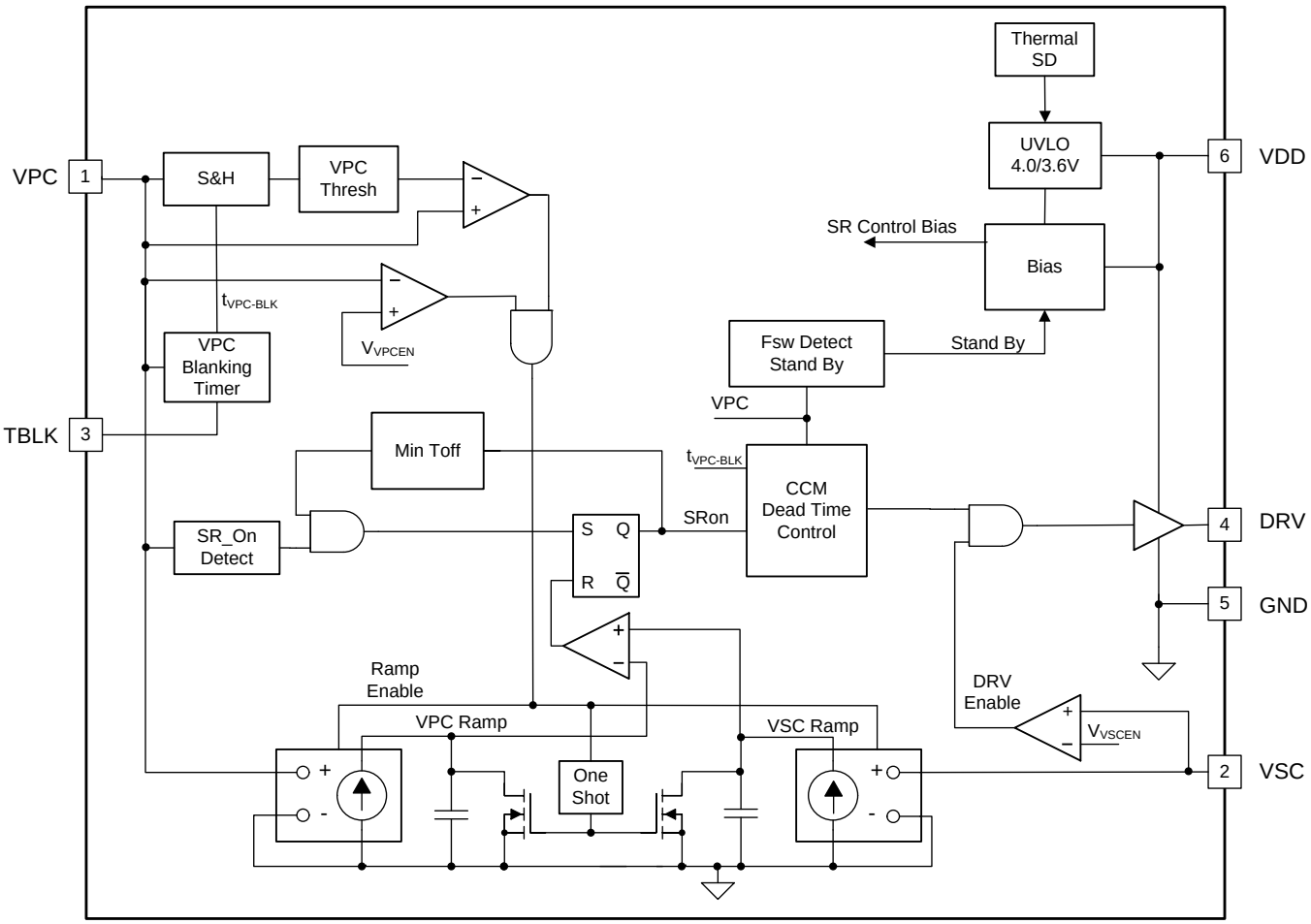
7.1 Overview

The UCC24630 SR controller is targeted for flyback converters operating in DCM, TM, and CCM modes of operation. The control method to determine SR on time is based on the volt-second balance principle of primary and secondary conduction volt-second product. In converters operating in DCM and TM, the secondary current always returns to zero in each cycle. In CCM operation, volt-second balance occurs in steady state operation. The inductor charge voltage and time product is equal to the discharge voltage and time product. The device uses internal current ramp emulators to predict the proper SR on time based on voltage and time information on the VPC and VSC pins.

In CCM converters during the transition from DCM operation into CCM, volt-second balance does not occur for a number of cycles. In this case CCM operation compatibility is achieved by limiting the maximum SR MOSFET on time with a CCM dead time function based on the previous switching period. There is fault protection to disable the SR in the event the operating periods become unstable during extreme operating transients.

To achieve very low standby power in the converter, the UCC24630 has a standby mode of operation that disables the SR MOSFET drive and reduces the device bias current to I_{STBY}. The device monitors the average switching frequency of the converter to enter and exit the standby mode of operation, and is compatible with converters operating in burst mode or constant frequency in light-load mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start Up and UVLO

The UCC24630 features a wide operating VDD range and low UVLO thresholds. The start up of the device is dependent on voltage levels on three pins: VDD, VPC and VSC. The VDD pin can be directly connected to the power supply output on converters from 5-V to 24-V nominal outputs. The start UVLO threshold is $V_{VDD(on)}$, 4.0 V typical, and stop threshold is $V_{VDD(off)}$, 3.6 V typical. The DRV output is not enabled unless the voltage on the VPC pin is greater than V_{VPCEN} for a time longer than $t_{VPC-BLK}$ and the voltage on the VSC pin is greater than V_{VSCEN}. Once the VDD, VSC and VPC voltage and time thresholds are met, there is an internal initialization time and a four-cycle-initialization start sequence before the DRV output is enabled.

Refer to Figure 13 for a startup sequence that illustrates the timing sequence and configurable DRV output based on VDD level. In most converter designs, the conditions for the VPC and VSC voltage to enable the device are met before the VDD start-voltage threshold, this is reflected in the timing diagram. When VDD exceeds $V_{VDD(on)}$ UVLO threshold the device starts the initialization sequence of 150 µs to 250 µs illustrated as $t_{INITIALIZE}$. After the device initialization, there is a logic initialization of 20 µs at which time V_{TBLK} is enabled (high). After the device is enabled, the CCM dead-time block requires four cycles to initialize the dead-time control before the DRV output is enabled. At VDD < V_{PMOS} the driver high-side PMOS device is enabled and the DRV peak will be close to VDD. When VDD exceeds V_{PMOS} the PMOS device is disabled and the driver is operating as a high-side NMOS only and DRV is approximately 1.2 V to 1.5 V lower than VDD. As VDD continues to increase, the DRV output is limited to V_{DRCL} regardless of VDD up to the recommended maximum rating.

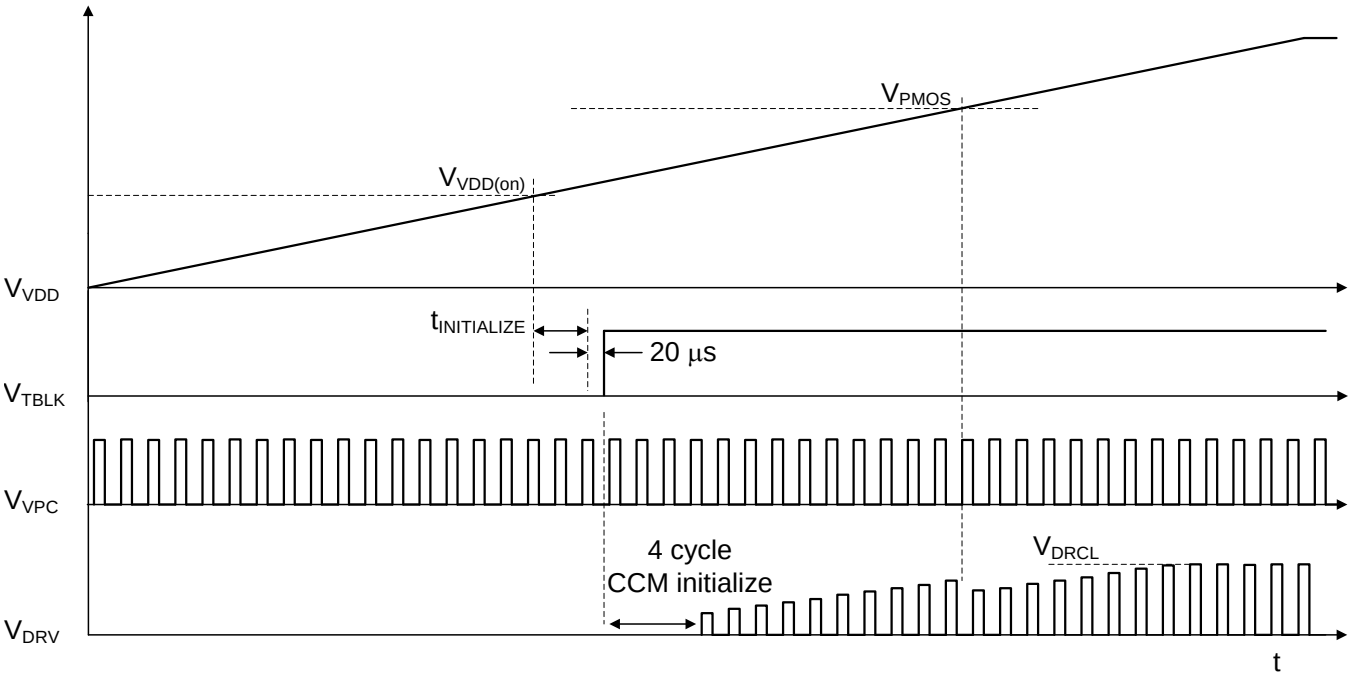


Figure 13. Start-Up Operation

Feature Description (continued)

7.3.2 Volt-Sec SR Driver On-Time Control

Refer to the timing diagrams in Figure 14 and Figure 15 for functional details of the UCC24630 volt-sec on-time control.

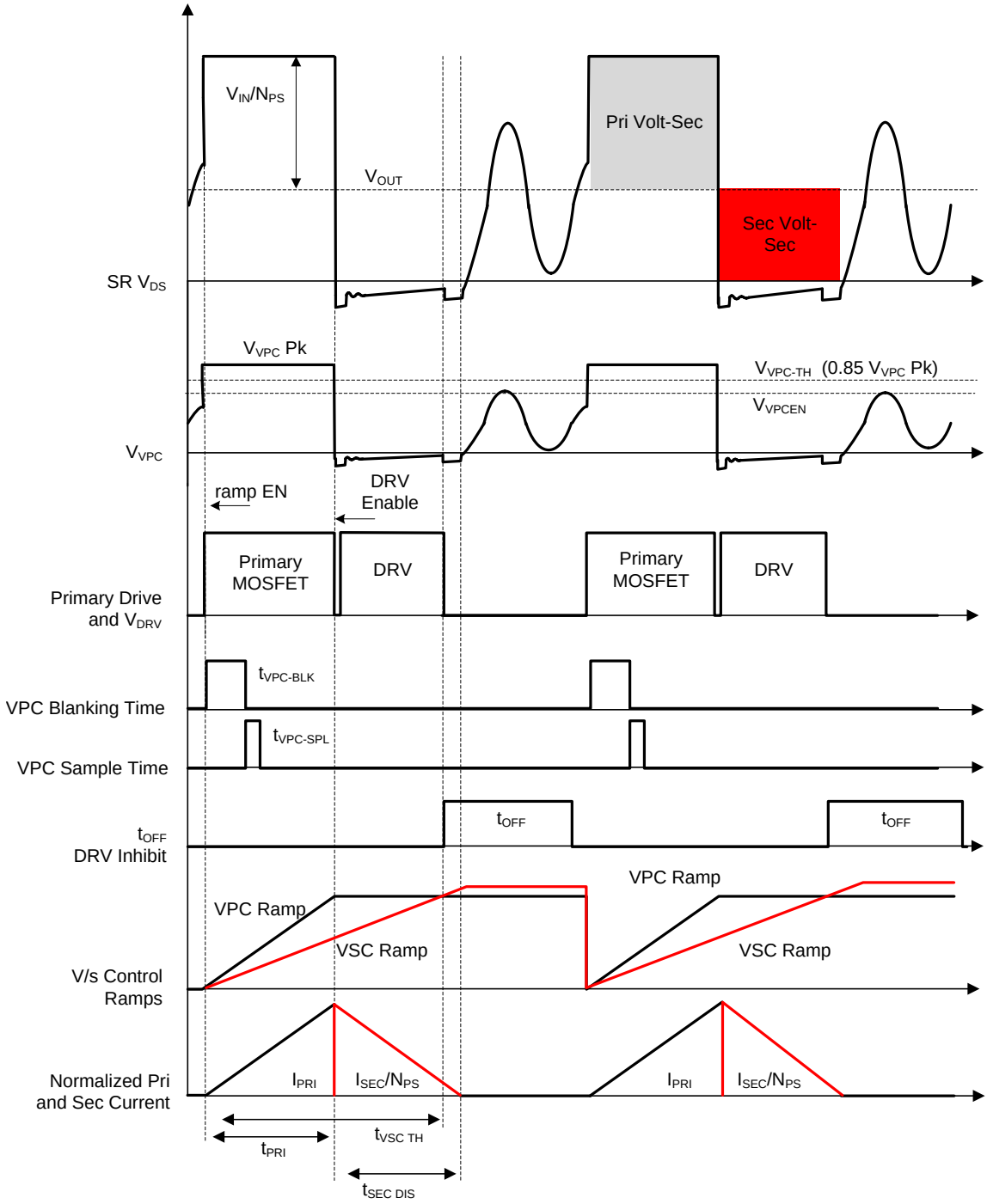


Figure 14. Operation in DCM

Feature Description (continued)

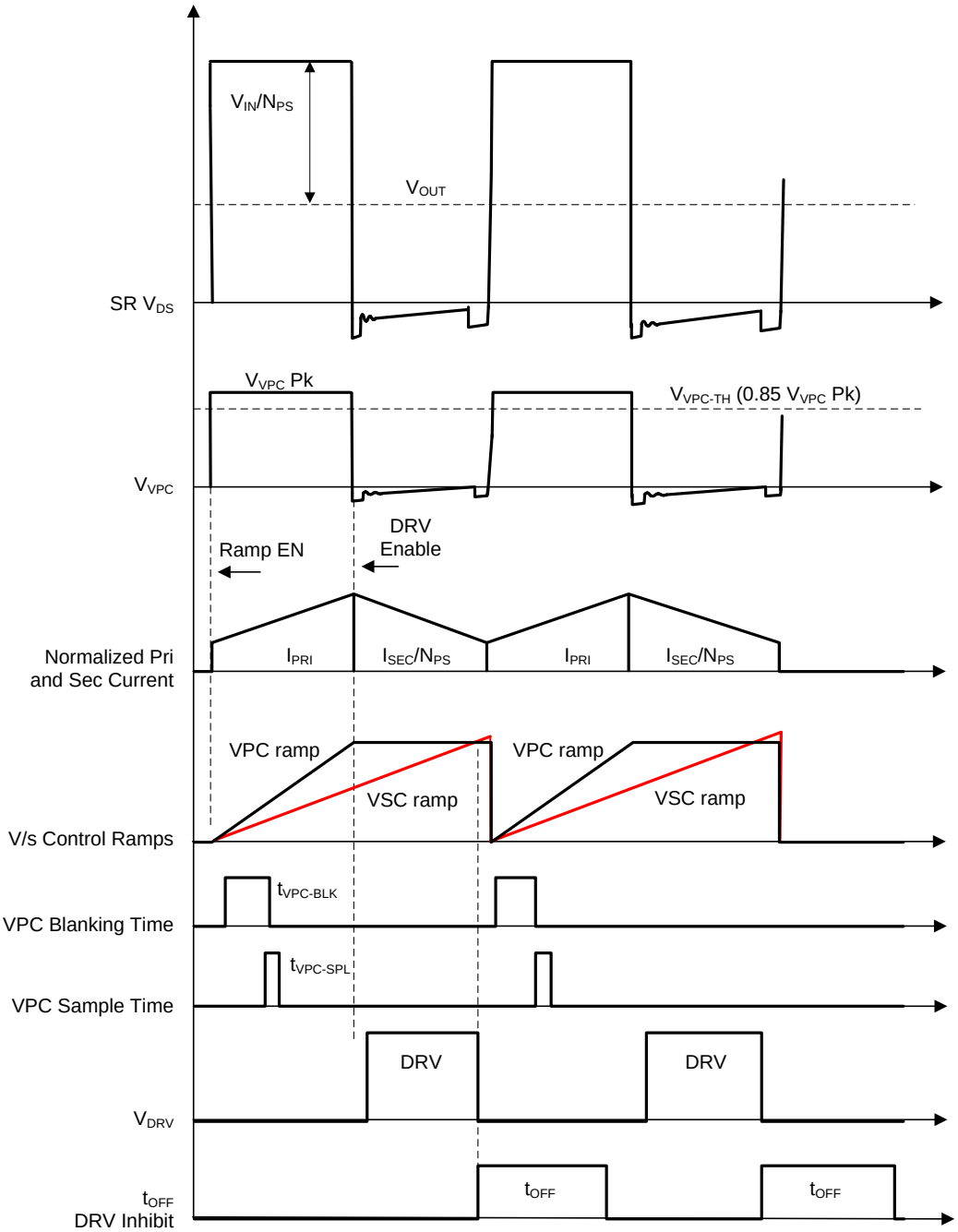


Figure 15. Operation in CCM

Feature Description (continued)

The UCC24630 uses the VPC and VSC pins to sense the SR MOSFET V_{DS} voltage and converter V_{OUT} voltage through resistor dividers. The information of V_{IN}/N_{PS}, t_{PRI}, and V_{OUT} can be obtained from the information on VPC and VSC pins. The SR MOSFET turn on is determined when the SR MOSFET body diode starts conducting and the VPC pin voltage falls to near zero; the SR MOSFET turn off is determined by the current emulator control ramps. The SR timing determined by the volt-sec balance function is the dominant mode of operation with all flyback converters, including CCM.

The UCC24630 volt-sec control generates the internal VPC ramp and VSC ramp to emulate the transformer Volt-Sec balancing as shown in Figure 14 and Figure 15.

The secondary current discharge time, $t_{SEC-DIS}$ can be determined indirectly. The primary volt-sec ramp and secondary volt-sec ramp both start when VPC rises above V_{VPC-EN} and V_{VPC-TH}. The charge currents for the VPC and VSC ramps are determined by the voltage on the VPC and VSC pins respectively.

When VPC is higher than V_{VPC-EN} and V_{VPC-TH} for $t > t_{VPC-BLK}$, the VPC pulse is qualified as a primary conduction pulse and the SR can be enabled on the VPC falling edge. The VPC ramp continues to rise until the VPC falling edge based on the real time voltage on the VPC pin and holds the peak for the cycle. The DRV output is turned on during the VPC falling edge near zero volts, and DRV is turned off when the VSC rising ramp crosses the VPC ramp held level.

Both VPC and VSC ramps are reset to zero on each VPC rising edge above the V_{VPC-EN} and V_{VPC-TH} thresholds.

To discriminate primary on-time pulses from DCM ringing, there are voltage and time criteria that must be satisfied on the VPC pin to enable the DRV output. $t_{VPC-BLK}$ can be adjusted through the resistor on TBLK pin.

At the rising edge of VPC when the voltage exceeds V_{VPC-EN} and V_{VPC-TH} the blanking time $t_{VPC-BLK}$ is initiated. At the end of $t_{VPC-BLK}$, the VPC voltage is sampled during $t_{VPC-SPL}$ window, which is 100 ns nominal. Also at the end of $t_{VPC-BLK}$, the DRV output can be enabled.

The VPC voltage sampled during $t_{VPC-SPL}$ determines the VPC dynamic threshold V_{VPC-TH} which is normally 85% of the sampled VPC voltage. The dynamic threshold provides the ability to reject the DCM ringing and detect the primary on-time. Noise immunity during the turn-on event of DRV at the falling edge of the VPC pin is enhanced by a minimum DRV on time of $t_{SRONMIN}$, which is 350 ns nominal.

During the falling edge of DRV, the t_{OFF} timer is initiated which inhibits turn on of the SR until t_{OFF} expires. This eliminates false turn on of DRV if the DCM ringing is close to ground.

Feature Description (continued)

The UCC24630 is designed to operate in a variety of flyback converter applications over a wide operating range. The internal volt-sec control ramps do have a dynamic range limit based on volt-sec on the VPC pin. As shown in Figure 16, a Volt-sec product exceeding 7 V-µs on the VPC pin will result in saturation of the VPC volt-sec control ramp. Operation beyond this point results in a DRV on-time less than expected. For example, if V_{VPC} = 0.5 V, t_{VPC} should be < 14 µs, or if V_{VPC} = 2.0 V, t_{VPC} should be < 3.5 µs, to operate within the dynamic range of the device. Assuming a converter operating in transition mode at low line and full load with a 50% duty cycle, the operating period is 28 µs which results in a frequency that is under 40 kHz. The UCC24630 low-frequency operating range extends to the standby mode threshold of 5 kHz; but each switching cycle V_{VPC} Volt-sec product should be less than 7 V-µs.

The device can support switching frequencies exceeding 200 kHz but the following timing limits need to be confirmed to be compatible with the power train. The minimum primary on time when the device is expected to be active needs to be compatible with the minimum VPC blanking time ($t_{VPC-BLK}$) setting of 203 ns plus the sampling window ($t_{VPC-SPL}$) of 100 ns. The minimum secondary current conduction time should be less than the minimum SR on time ($t_{SR(min)}$) of 350 ns. The minimum time from the SR drive turn off until the next SR drive turn on should be greater than the SR minimum off time (t_{OFF}) of 2.5 µs.

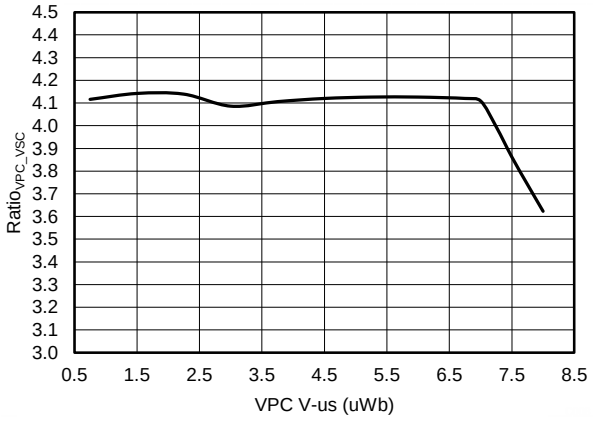


Figure 16. $Ratio_{VPC\_VSC}$ vs VPC V-µs

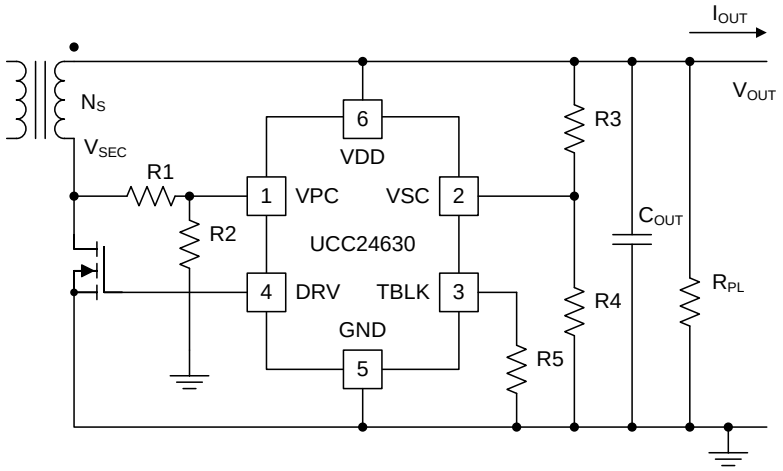


Figure 17. SR Controller Components

Feature Description (continued)

Determining the VPC and VSC divider resistors is based on the operating voltage ranges of the converter and $Ratio_{VPC\text{-}VSC}$ gain ratio. Referring to Figure 17, the following equation determines the VPC divider values.

For R2 a value of 10 kΩ is recommended for minimal impact on time delay, and low-resistor dissipation. A higher R2 value reduces resistor divider dissipation but may increase the DRV turn-on delay due to the time constant of ~2 pF pin capacitance and divider resistance. A lower R2 value can be used with the tradeoff of higher dissipation in the resistor divider. A factor of 10% over the VPC threshold, V_{VPCEN}, is shown in Equation 1 for design margin.

$$R1 = \frac{\left[\left(\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)}\right) - V_{VPCEN} \times 1.1\right] \times R2}{V_{VPCEN} \times 1.1} \quad (1)$$

where

- $V_{IN(min)}$ is the converter minimum primary bulk capacitor voltage.
- $V_{OUT(min)}$ is the minimum converter output voltage in normal operation.
- V_{VPCEN} is the VPC enable threshold, use the specified maximum value.
- N_{PS} is the transformer primary to secondary turns ratio.

The operating voltage range on the VPC pin should be within the range of 0.45 V < V_{VPC} < 2 V. Referring to Figure 6, if V_{VPC} is greater than 2.3 V the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is reduced; in this condition the DRV on time is less than expected. If V_{VPC} is greater than 2.6 V for 500 ns, a fault is generated and DRV is disabled for the cycle, refer to Pin Fault Protection . To ensure the maximum voltage is within range confirm with Equation 2.

$$V_{VPC(max)} = \frac{\left(\frac{V_{IN(max)}}{N_{PS}} + V_{OUT(max)}\right) \times R2}{R1 + R2} \quad (2)$$

where

- $V_{IN(max)}$ is the converter maximum primary bulk capacitor voltage.
- $V_{OUT(max)}$ is the maximum converter output voltage at OVP.
- N_{PS} is the transformer primary-to-secondary turns ratio.

The program voltage on the VSC pin is determined by the VPC divider ratio and the device's parameter $Ratio_{VPC\_VSC}$. The current emulator ramp gain is higher on the VPC pin by the multiple $Ratio_{VPC\_VSC}$, so the VSC resistor divider ratio is reduced by the same $Ratio_{VPC\_VSC}$ accordingly. Determine the VSC divider resistors using equation 3 below. To minimize resistor divider dissipation, a recommended range for R4 is 25 kΩ to 50 kΩ. Higher R4 values results in increasing offset due to VSC input current, I_{VSC}. Lower R4 values increases the resistor divider dissipation. To ensure DRV turn off slightly before the secondary current reaches zero, 10% margin is shown for initial values. Use a nominal value of 4.15 for $Ratio_{VPC\_VSC}$.

$$R3 = \left[\left(\frac{\frac{R1 + R2}{R2}}{Ratio_{VPC\_VSC} \times 1.1}\right) - 1\right] \times R4 \quad (3)$$

where

- $Ratio_{VPC\_VSC}$ is the device parameter VPC and VSC gain ratio, use a value of 4.15.

Feature Description (continued)

The operating voltage on the VSC pin should be within the range of 0.3 V < V_{VSC} < 2 V. Referring to Figure 7, if V_{VSC} is greater than 2.3 V, the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is increased; in this condition the DRV on time is more than expected. To ensure the VSC voltage is within range confirm with Equation 4 and Equation 5.

$$\frac{R4}{R3+R4} \times V_{OUT(min)} \geq 0.3V \quad (4)$$

$$\frac{R4}{R3+R4} \times V_{OUT(max)} \leq 2.0\,V \quad (5)$$

where

- $V_{OUT(min)}$ is the minimum converter output operating voltage of the SR controller.
- $V_{OUT(max)}$ is the maximum converter output operating voltage of the voltage at OVP.

Discrimination of ringing during DCM operation from valid primary on-time is achieved by a dynamic VPC rising threshold and programmable blanking time. The dynamic threshold V_{VPC-TH} is 85% typical ratio of the previous VPC pin peak voltage. Referring to Figure 14, the VPC pin voltage is sampled after the VPC voltage is greater than V_{VPCEN} and V_{VPC-TH} for t > $t_{VPC-BLK}$. The function of the dynamic threshold V_{VPC-TH} is to reject the ringing in DCM operation from the primary conduction pulses. The dynamic threshold has an active range from the minimum V_{VPCEN} voltage to a maximum of 1 V clamp. The blanking time is programmable from 200 ns to 1 µs in order to accommodate a variety of converter designs.

Refer to Figure 18 for guidance on selecting the blanking time. The blanking time should be selected as long as reasonable and still accommodate the minimum primary on-time at light-load condition and high-line voltage. In the high-line minimum load condition, select a blanking time that meets the following criteria (Equation 6) to accommodate tolerance of the blanking time and the $t_{VPC-SPL}$ sampling time window.

$$t_{VPC-BLK} = (t_{PRI} \times 0.85) - 120\ ns \quad (6)$$

For rejection of DCM ringing, the blanking time should be longer than the time that the ring is above the V_{VPC-TH} dynamic threshold, which is 85% of the minimum SR VDS peak voltage. Determine these criteria at low line and maximum load condition. It is recommended that the transformer turns ratio be selected such that the secondary reflected voltage is < 85% of $V_{IN(min)}$ bulk capacitor voltage at the highest load when DCM operation occurs at the low line input condition.

To determine the resistor value for $t_{VPC-BLK}$ use Equation 7 to select from a range of 200 ns to 1 µs.

$$R5 = \frac{t_{VPC-BLK} - 100\ ns}{18\ pF} \quad (7)$$

where

- $t_{VPC-BLK}$ is the target blanking time.

Additional discrimination for proper SR timing control is provided by the t_{OFF} function. Refer to Figure 14 and Figure 15 for the timing details. After the DRV turn off, the DRV is inhibited from turning on again until the t_{OFF} timer expires. This protects against SR false turn on from SR V_{DS} DCM ringing below ground.

Feature Description (continued)

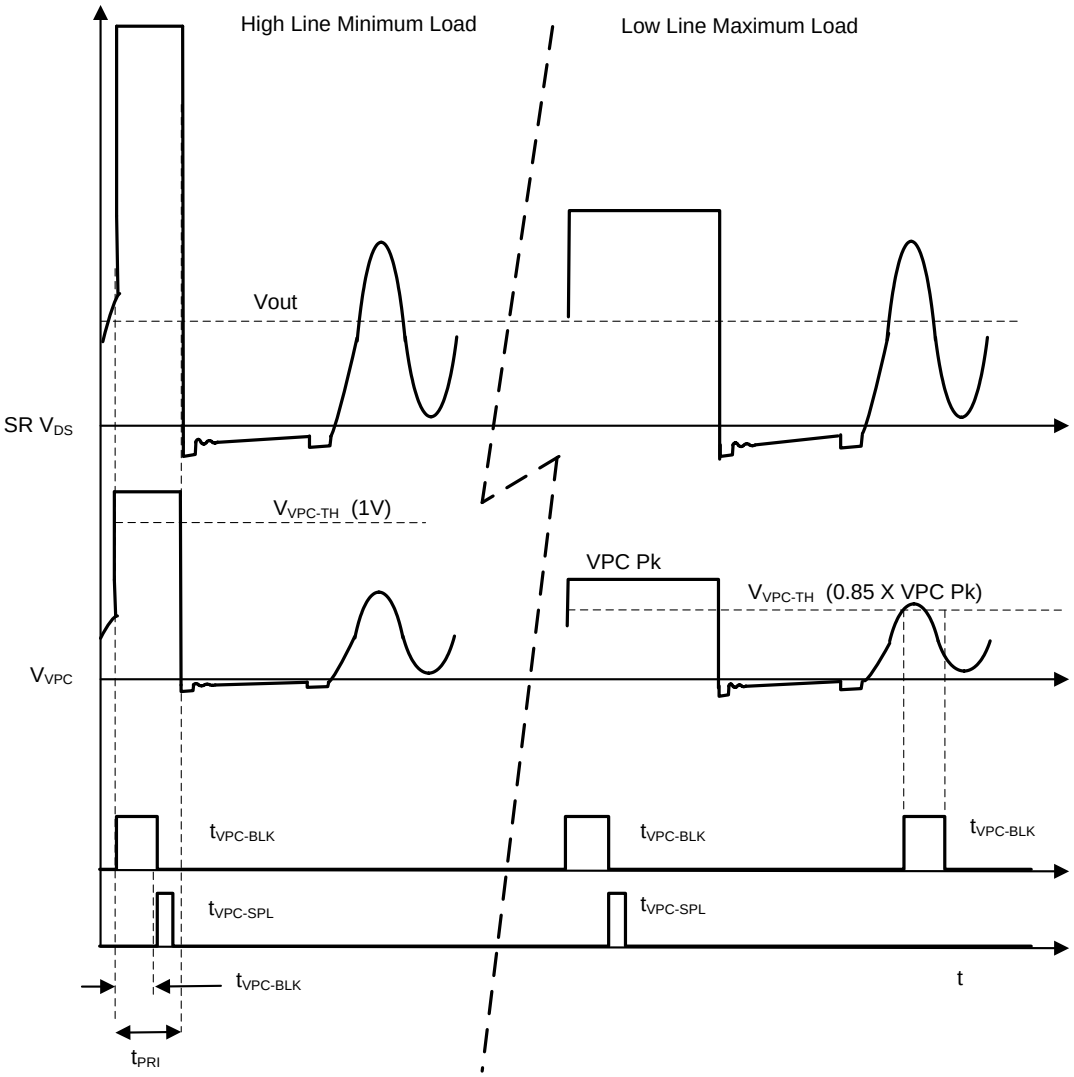


Figure 18. VPC Blanking Time Criteria

Feature Description (continued)

7.3.3 CCM Dead Time

Operation of CCM converters during transition from DCM to CCM results in a number of switching cycles where volt-sec balance is not achieved. To accommodate CCM operation the UCC24630 SR controller incorporates CCM dead-time protection to ensure turn off of the SR MOSFET before the next primary MOSFET turn on. The function provides a limit of the total period of the primary on time plus SR on time to the previous cycle minus the dead time, 600 ns typical. This is accomplished by limiting the SR on time of the active cycle, t (N+1), to the previous recorded cycle, t (N), minus t_{CCMDT}. As can be seen in Figure 19, the CCM dead time limits the DRV on time even though the VSC volt-sec ramp threshold is not satisfied.

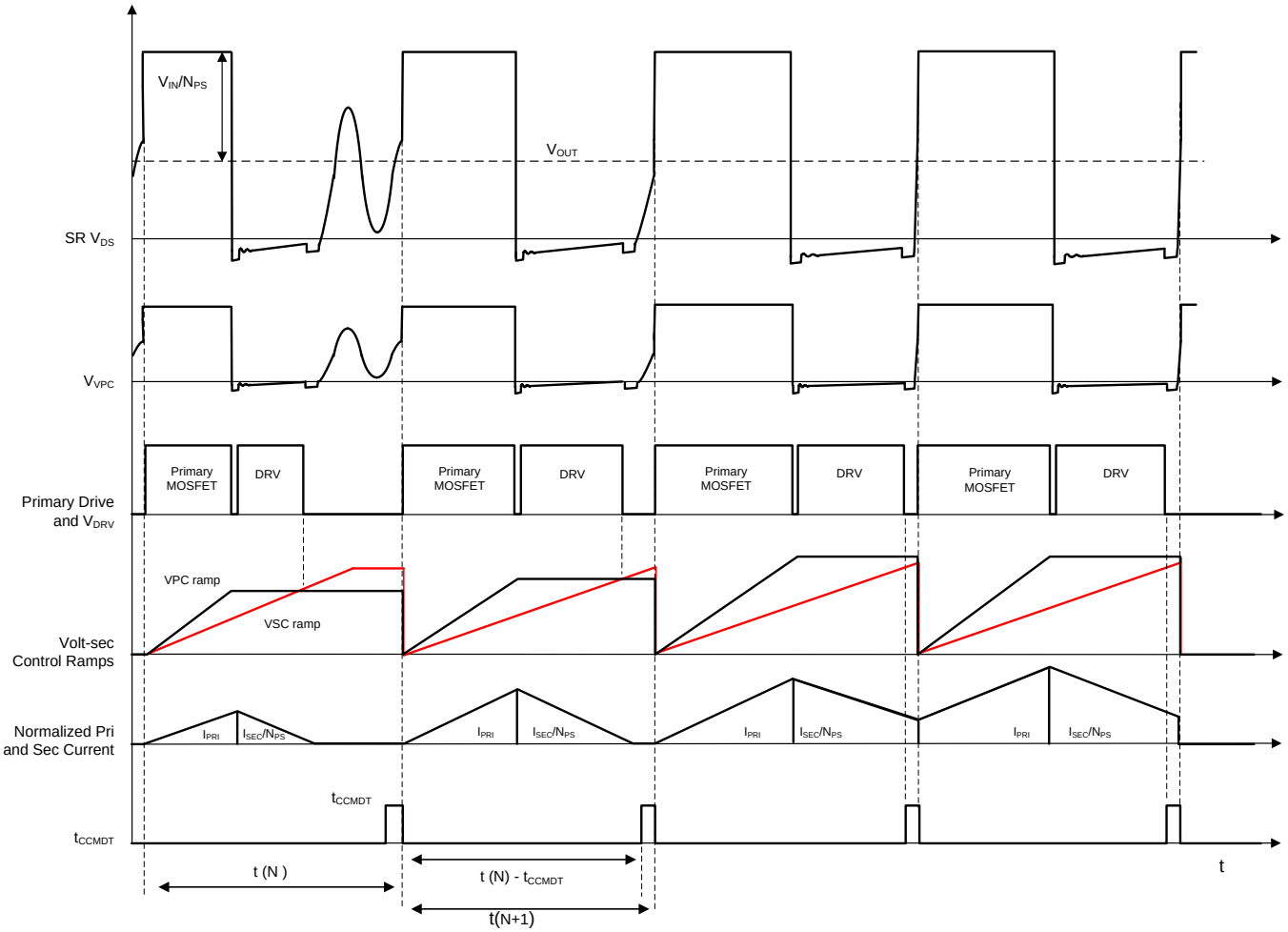


Figure 19. CCM Dead-Time Function

Feature Description (continued)

CCM cycle fault provides protection if the switching frequency is unstable during abnormal conditions. The CCM cycle fault triggers if the switching period exceeds the previous switching period by $K_{CCM-FAULT}$, 150% typical. The CCM cycle fault disables the DRV output for four consecutive cycles. During the four-cycle disable interval if another CCM cycle fault occurs the fault is retriggered for another four cycles, DRV will not be enabled until four consecutive cycles occur that do not generate a CCM cycle fault. Refer to Figure 20 and Figure 21 for CCM cycle fault behavior.

The N+1 cycle with the longer period sets up the next following cycle to have a longer allowable maximum SR on time based on t(N) – t_{CCMDT}; if CCM operation occurs in this case the maximum allowable SR on time could conflict with the primary turn on if the converter switching period returns to the previous time. The DRV output is disabled to prevent this potential timing conflict with the primary switch.

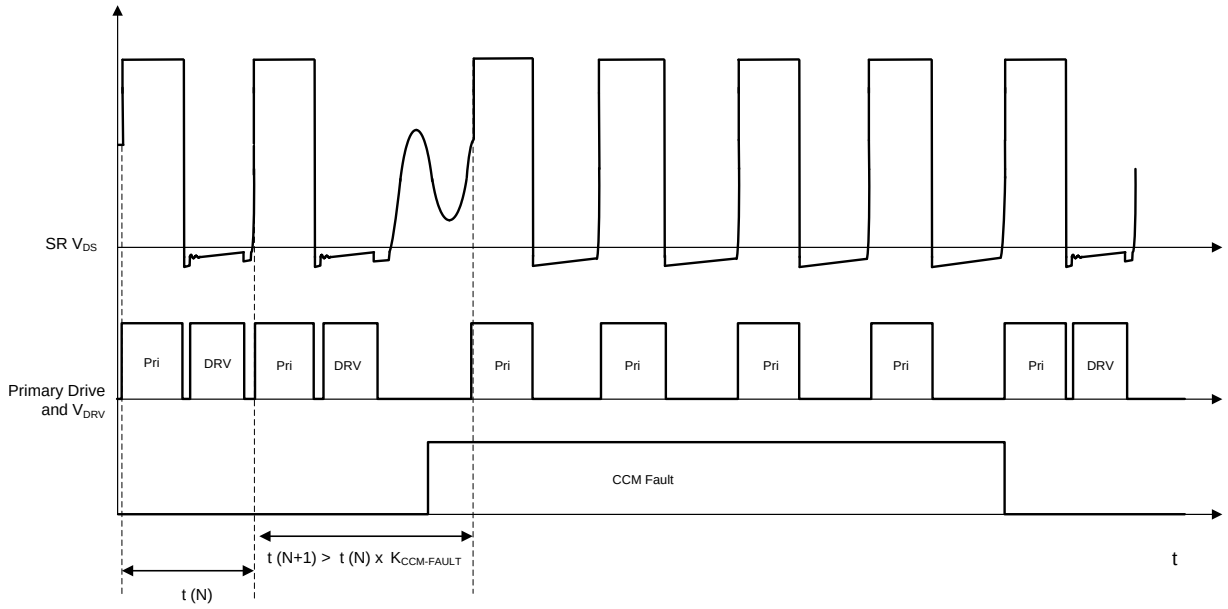


Figure 20. CCM Cycle-Fault Behavior, CCM Operation

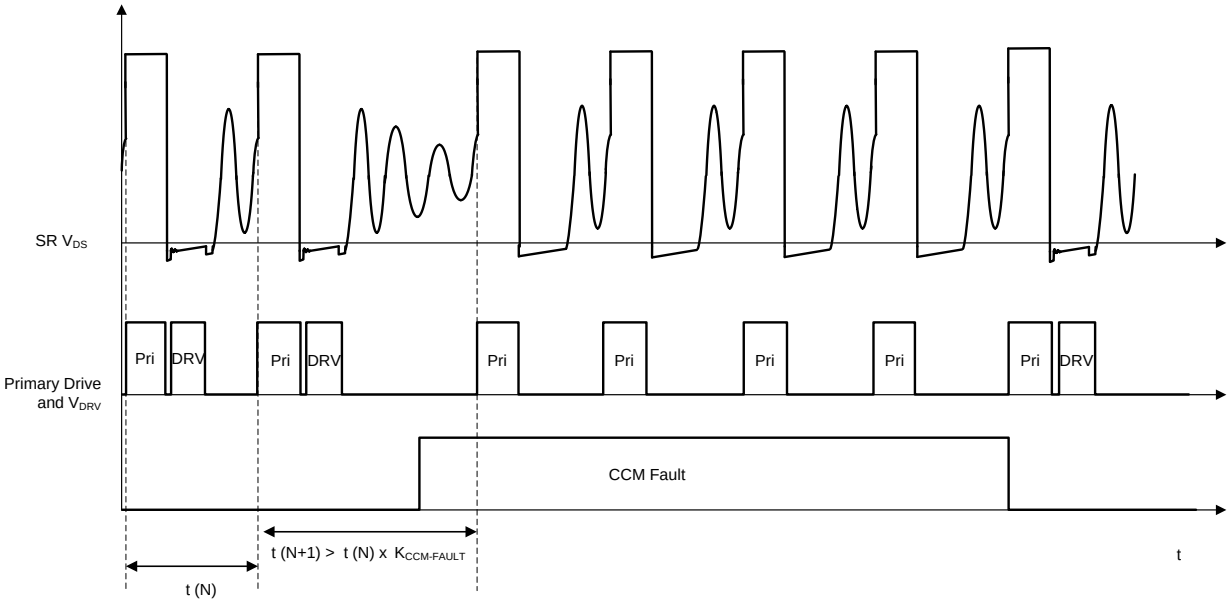


Figure 21. CCM Cycle-Fault Behavior, DCM Operation

Feature Description (continued)

7.3.4 Standby Operation

To minimize power consumption at very light load and standby conditions, the UCC24630 disables the SR DRV output and enters a low current operating state. The criteria for operating in standby mode or normal operation are determined by the average frequency detected on the VPC pin. The frequency detection is compatible with burst mode operation or continuous low frequency FM operation. At start up the device is in normal operation to enable DRV to the SR MOSFET. If < 64 cycles occur in t_{ENTO},12.8 ms typical, the device disables the DRV output and enters low-current operating mode with bias current of I_{STBY}. In standby mode the criteria to enter normal operating mode is when > 32 cycles occur within t_{EN}, 2.56 ms typical. The device enters normal operation as soon as the 32 cycles occur to reduce the response time exiting standby operation. The average frequency of entering standby mode is 5 kHz typical, and the average frequency of exiting standby mode is 12.5 kHz typical. Refer to Figure 22 for an illustration of standby mode timing.

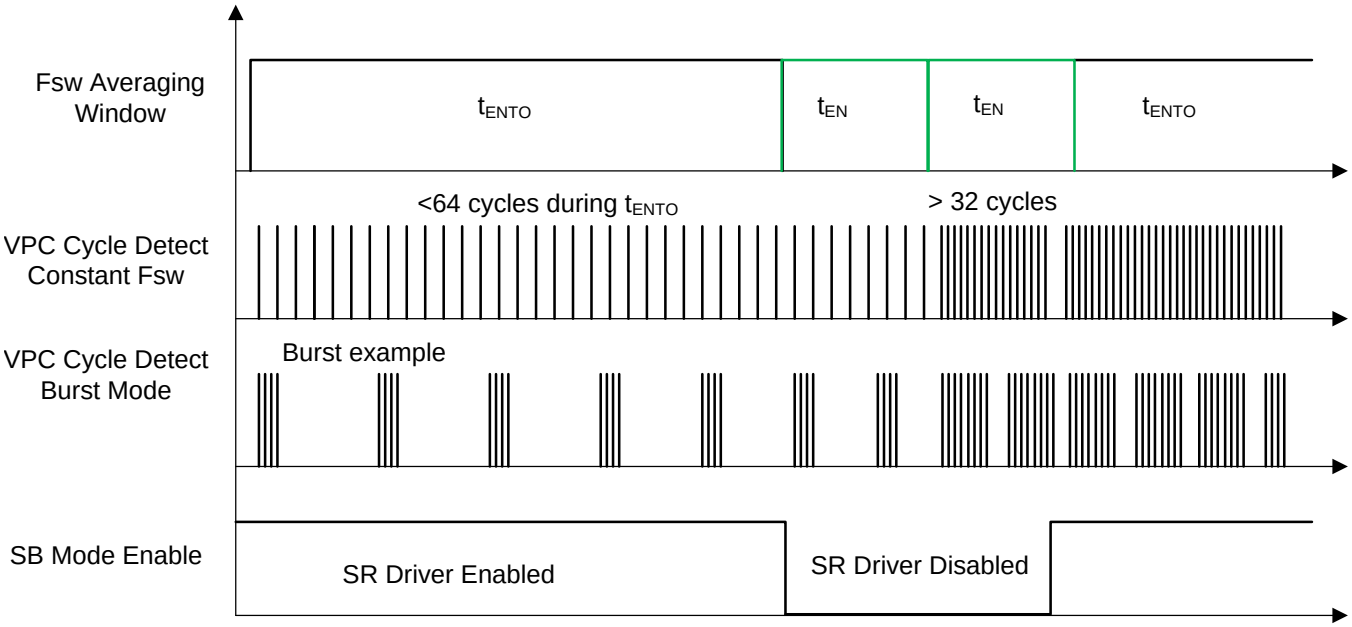


Figure 22. Standby Mode Operation

Feature Description (continued)

7.3.5 Pin Fault Protection

The UCC24630 controller includes fault protection in the event of open pin, shorted pin to ground and abnormal out of range operation.

7.3.5.1 VPC Pin Overvoltage

In the event that there is an abnormal high level on the VPC pin for a period beyond expected transformer leakage spike duration, the DRV output is disabled on a cycle-to-cycle basis. If the voltage on the VPC pin exceeds V_{VPCDIS}, 2.6 V minimum, for 500 ns the SR is not enabled until the next valid cycle.

7.3.5.2 VPC Pin Open

In the event of an open circuit VPC pin, the device defaults to a no VPC input signal condition which results in disabling DRV operation.

7.3.5.3 VSC Pin Open

In the event of an open circuit VSC pin, the device defaults to a zero VSC input signal condition which results in disabling DRV operation.

7.3.5.4 TBLK Pin Open

In the event of an open circuit TBLK pin, the device disables DRV operation.

7.3.5.5 VPC and VSC Short to Ground

Since the VPC and VSC enable thresholds must be satisfied for DRV operation, DRV is inherently disabled.

7.3.5.6 TBLK Pin Short to Ground

A shorted TBLK pin results in a minimum setting for $t_{VPC-BLK}$ blanking time.

7.4 Device Functional Modes

According to VDD voltage, VSC voltage, and VPC voltage and frequency the device can operate in different modes.

7.4.1 Start-Up

During start-up when VDD is less than $V_{VDD(on)}$ the device is disabled. When VDD exceeds the $V_{VDD(on)}$ UVLO threshold the I_{DD} goes to I_{RUN} and the device begins the start sequence detailed in Section 8.3.1 .

7.4.2 Normal Operation

When VDD exceeds $V_{VDD(on)}$, the VPC voltage exceeds V_{VPC-EN} and V_{VPC-TH}, and the VSC voltage exceeds V_{VSCEN} the DRV output is active. If the switching frequency is above the standby criteria of > 5 kHz the device is in normal operation determining the DRV time based on volt-sec control, or CCM dead time control. I_{DD} will be I_{RUN}.

1. The device operates in volt-sec control when the primary on-time plus the DRV on-time is less than the previous cycle minus t_{CCMDT}. This is the mode of operation the majority of the time.
2. The device operates in CCM dead-time control when the primary on-time plus DRV on time would be greater, as determine by the volt-sec control ramps, than the previous cycle minus t_{CCMDT}. This occurs only in CCM converters, during the transition of DCM into CCM operation

7.4.3 Standby Operation

If the number of VPC pulses is less than n_{ENTO}, 64, during t_{ENTO} the device enters standby mode. DRV operation stops and most device functions are shut down. I_{DD} is I_{STBY} during standby operation. To exit standby mode the number of VPC pulses must exceed n_{EN}, 32, during t_{EN}. I_{DD} returns to I_{RUN} and the DRV output starts after 4 VPC cycles.

7.4.4 Conditions to Stop Operation

The following conditions can disable DRV operation, I_{DD} is I_{RUN} during these conditions.

1. VPC overvoltage: When $V_{VPC} > V_{VPCDIS}$ for >500 ns the DRV output is disabled for the cycle.
2. CCM Fault: If the current cycle period is greater than the previous cycle times K_{CCM_FAULT}, the DRV output is disabled for 4 cycles. The 4-cycle count can be reset, and extended if another CCM fault occurs during the 4-cycle DRV disable counter.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC24630 is a high performance controller driver for N-channel MOSFET power devices used for secondary-side synchronous rectification. The UCC24630 is designed to operate as a companion device to a primary-side controller to help achieve efficient synchronous rectification in switching power supplies. The controller features a high-speed driver and provides appropriately timed logic circuitry that seamlessly generates an efficient synchronous rectification system. With its current emulator architecture, the UCC24630 has enough versatility to be applied in DCM, TM and CCM modes. The UCC24630 SR on-time adjustability allows optimizing for PSR and SSR applications. Additional features such as pin fault protection, dynamic VPC threshold sensing, and voltage sense blanking time and make the UCC24630 a robust synchronous controller. CCM dead-time protection shuts off the DRV signal in the event of an unstable switching frequency.

8.2 Typical Application

8.2.1 AC-to-DC Adapter, 19.5 V, 65 W

This design example describes the design of a 65-W off-line flyback converter providing 19.5 V at 3.33-A maximum load and operating from a universal AC input. The design uses the LM5023 AC-to-DC quasi-resonant primary-side controller in a DCM type flyback converter and achieves over 92% full-load efficiency with the use of the secondary side UCC24630 synchronous rectifier controller.

- The design requirements are detailed in Section 9.2.2
- The design procedure for selecting the component circuitry for use with the UCC24630 is detailed in Calculation of Component Values.
- Test results shown in section 9.2.4 highlight the unique advantages of using the UCC24630.

Typical Application (continued)

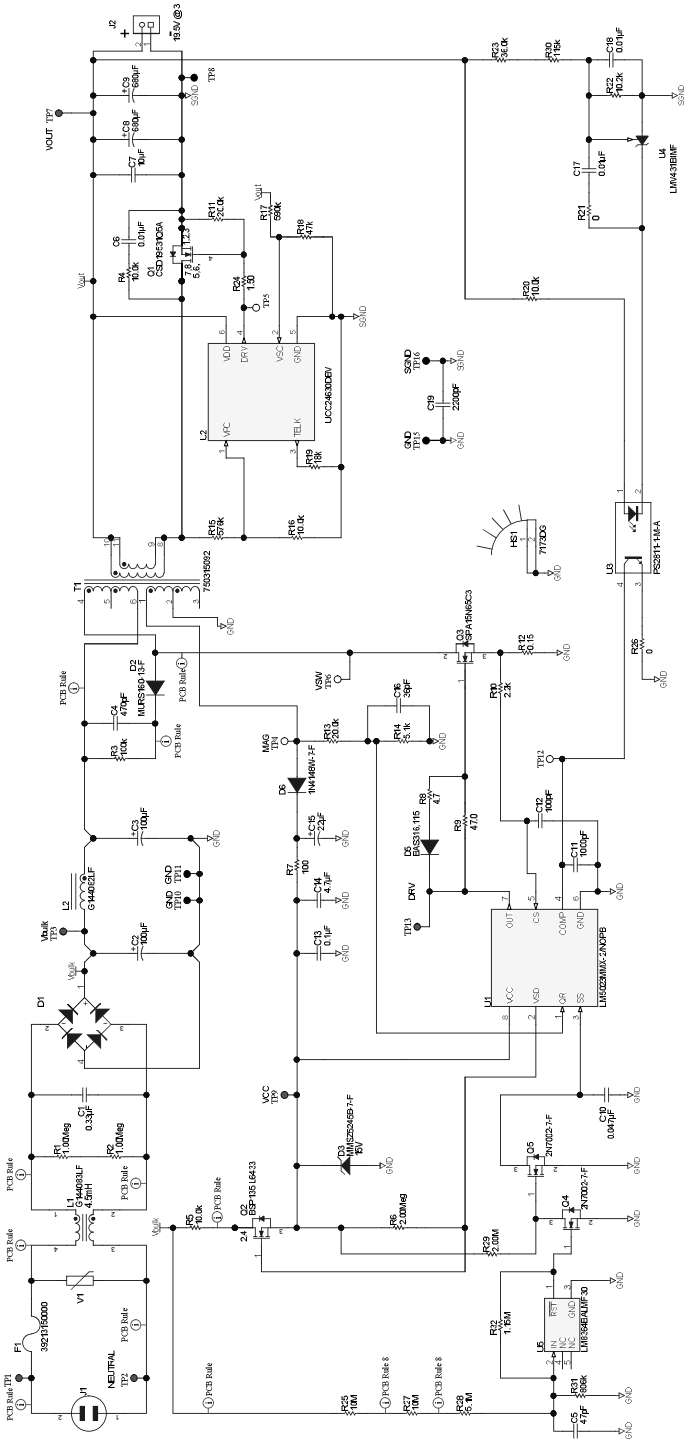


Figure 23. AC-to-DC Adapter 19 V, 65 W

Typical Application (continued)

8.2.2 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Performance Specifications AC-to-DC Adapter 19 V, 65 W

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Input Characteristics						
V_{ACIN}	Input voltage		90	115/230	265	V
f_{LINE}	Frequency		47	50/60	64	Hz
$V_{AC(uvlo)}$	Brownout voltage	$I_{OUT} = I_{OUT(nom)}$		80		VRMS
$V_{AC(run)}$	Brownout recovery voltage			90		VRMS
I_{IN}	Input current	$V_{ACIN} = V_{ACIN(min)}$, $I_{OUT} = I_{OUT(nom)}$		1.65		A
Output Characteristics						
V_{OUT}	Output voltage	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$, $I_{OUT} = 0$ to $I_{OUT(nom)}$	18.5	19.5	20.5	V
$I_{OUT(nom)}$	Nominal output current	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$		3.33		A
$I_{OUT(min)}$	Minimum output current	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$		0		A
ΔV_{OUT}	Output voltage ripple	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$, $I_{OUT} = 0$ to $I_{OUT(nom)}$		500		mV
P_{OUT}	Output power	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$		65		
System Characteristics						
η_{avg}	Average efficiency	$V_{ACIN} = V_{ACIN(nom)}$, I_{OUT} = 25%, 50%, 75%, 100% of $I_{OUT(nom)}$	89%	90%		
$\eta_{10\%}$	10% Load efficiency	$V_{ACIN} = V_{ACIN(nom)}$, I_{OUT} = 10% of $I_{OUT(nom)}$	79%	82%		
P_{NL}	No load power	$V_{ACIN} = V_{ACIN(nom)}$, $I_{OUT} = 0$		60	120	mW

8.2.3 Calculation of Component Values

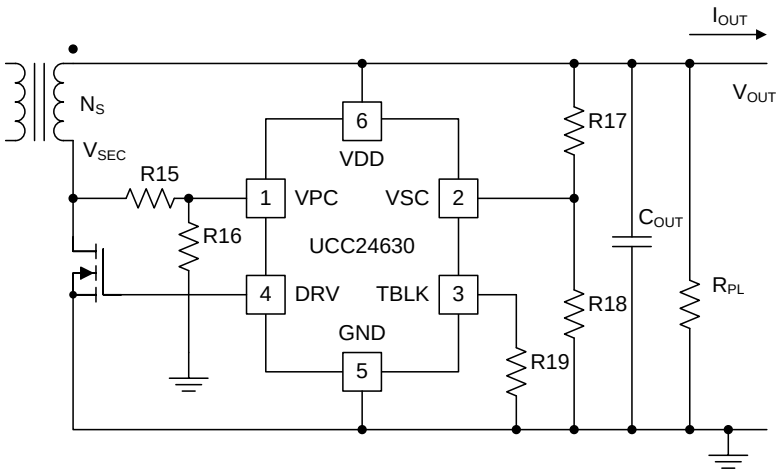


Figure 24. UCC24630 Circuit Design

For ease of understanding, Figure 24 is a modified version of Figure 17 where the component reference designators are the same as the schematic drawing of Figure 23.

8.2.3.1 VPC Input

For minimal power dissipation:

$$R16 = 10\,k\Omega$$

$$R15 = \frac{\left[\left(\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)}\right) - V_{VPC\_EN} \times 1.1\right] \times R16}{V_{VPC\_EN}}$$

$$V_{OUT(min)} = 18\,V$$

$$N_{PS} = 5.5$$

$$V_{IN(min)} = 60\,V$$

$$R15 = 574\ k\Omega \quad (8)$$

With **R15 = 576 kΩ**

$$V_{VPC(max)} = \frac{\left(\frac{V_{IN(max)}}{N_{PS}} + V_{OUT(max)}\right) \times R16}{R15 + R16}$$

$$V_{VPC(max)} = 1.50\,V \quad (9)$$

$$V_{VPC(min)} = \frac{\left(\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)}\right) \times R16}{R15 + R16}$$

$$V_{VPC(min)} = 0.49\,V \quad (10)$$

Therefore, V_{VPC} is within the recommended range of 0.45 V to 2 V.

8.2.3.2 VSC Input

The value of R18 is recommended to be with the range of 25 kΩ to 50 kΩ.

$$R18 = 47\ k\Omega$$

$$R17 = \left[\left(\frac{\frac{R15 + R16}{R16}}{Ratio_{VPC\_VSC} \times 1.1} \right) - 1 \right] \times R18$$

$$R17 = 554\ k\Omega \quad (11)$$

With R17 = 590 kΩ the operating range of the VSC pin is:

$$V_{VSC(min)} = \left[\left(\frac{R18}{R17 + R18} \right) \right] \times V_{OUT(min)}$$

$$V_{VSC(min)} = 1.32\,V \quad (12)$$

$$V_{VSC(max)} = \left[\left(\frac{R18}{R17 + R18} \right) \right] \times V_{OUT(max)}$$

$$V_{VSC(max)} = 1.55\,V \quad (13)$$

Therefore, V_{VSC} is within the recommended range of 0.3 V to 2 V.

8.2.3.3 TBLK Input

The blanking time is set with resistor R19.

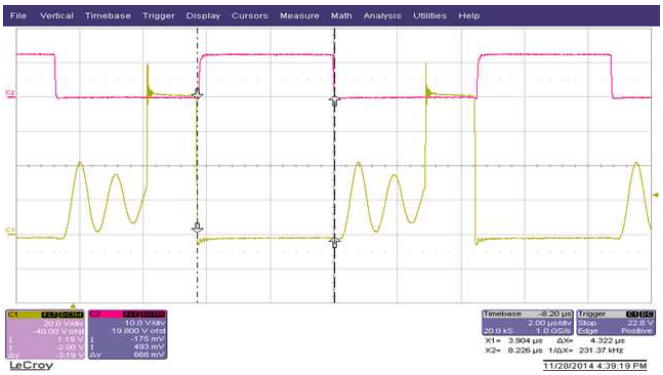
Select the blanking time to meet the following criteria based on minimum primary on-time at high line.

$t_{VPC\text{-}BLK} = (t_{PRI} \times 0.85) - 120$ ns

$$R19 = \frac{t_{VPC-BLK} - 100\ ns}{18\ pF} \quad (14)$$

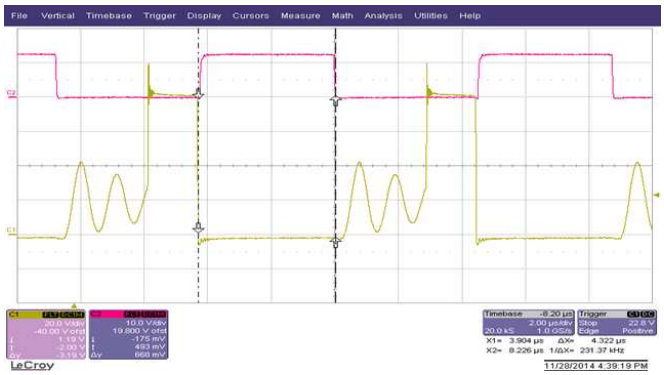
A value of **R19 = 18 kΩ** results in a blanking time of approximately 420 ns.

8.2.4 Application Curves



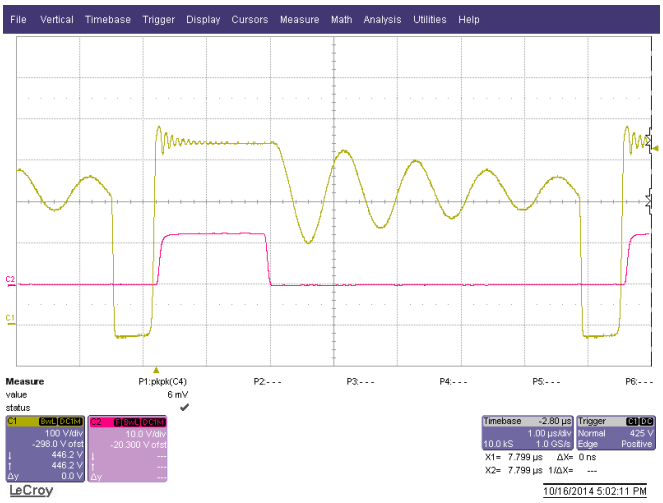
C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of synchronous rectifier Q1

Figure 25. DRV Timing at 230 V_{AC}, 65 W



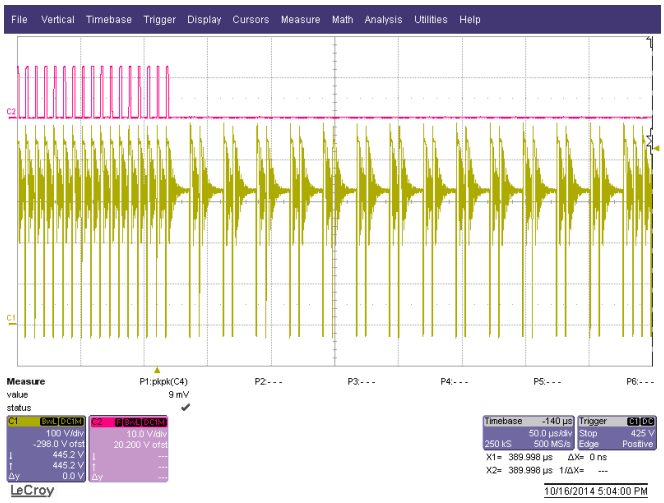
C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of synchronous rectifier Q1

Figure 26. DRV Timing at 115 V_{AC}, 65 W



C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of primary-side MOSFET Q3

Figure 27. DRV Timing at 230 V_{AC}, 12 W



C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of primary-side MOSFET Q3

Figure 28. Light-Load Behavior (230 V_{AC}, 8 W)

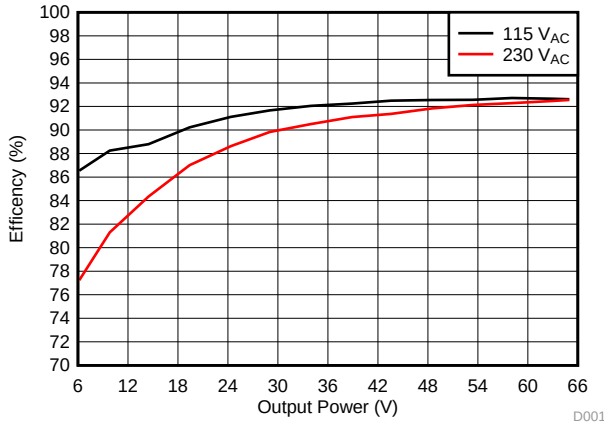


Figure 29. Efficiency vs Output Power

8.3 Do's and Don'ts

- Do operate the device within the recommended operating maximum parameters. Consider output overvoltage conditions when determining stress.
- Do consider the guideline for setting the blanking time resistor value illustrated in Figure 18.
- Do not use the UCC24630 with converters that operate in constant skip cycle mode at high-power levels. The skip cycle behavior results in numerous CCM faults and missing DRV pulses.
- Do not use the UCC24630 in CCM designs that are operating in CCM while the flyback controller is operating in variable frequency, FM, modulation. The CCM dead-time function is compatible with CCM operation during fixed-frequency, PWM operation.
- Do not use the UCC24630 in hysteretic control CCM flyback converters. Constant skip-cycle operation at high-power levels results in numerous CCM cycle faults resulting in efficiency loss.
- Do not use the UCC24630 in LLC converters.

9 Power Supply Recommendations

The UCC24630 is recommended as a synchronous rectifier controller in a wide variety of flyback power supplies. It is compatible with Discontinuous Conduction Mode (DCM) and Transition Mode (TM) controllers in fixed frequency or variable frequency applications. It is compatible with Continuous Conduction Mode (CCM) controllers in fixed frequency applications.

It is suitable as a synchronous rectifier for flyback power supplies with an input of 85 V_{AC} to 265 V_{AC} and an output from 5 V to 24 V. It can also be used in other flyback applications with different input and/or output voltages. But be sure all voltages and currents are within the recommended operating conditions and absolute ratings of the device.

It is compatible with flyback converters operating at the transition mode limit, at low line, with switching frequencies as low as 40 kHz. It may also be used in switching speeds up to 200 kHz.

The VDD operating range allows direct connection to converter outputs from 5 V to 24 V. Since the driver and control share the same VDD and ground, it is recommended to place a good quality ceramic capacitor as close as possible to VDD and GND pins. To reduce VDD noise and eliminate high-frequency ripple current injected from the converter output, it is recommended to place a small resistance of 2.2 Ω to 10 Ω between the converter output and VDD. The device can tolerate VDD rise times from 100 µs to very long rise times typical of constant current chargers. The start-up sequence will always be as shown in Figure 13. VDD can be connected to an external bias to extend the device's operating range below 3.5 V or above 24-V converter outputs.

10 Layout

10.1 Layout Guidelines

In general, try to keep all high current loops as short as possible. Keep all high current/high frequency traces away from other traces in the design. If necessary, high-frequency/high-current traces should be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up. Always consider appropriate clearances between the high-voltage connections and any low-voltage nets.

10.1.1 VDD Pin

The VDD pin must be decoupled to GND with good quality, low ESR, low ESL ceramic bypass capacitors with short traces to the VDD and GND pins. The value of the required capacitance on VDD is determined as shown in Section 7.3 . To eliminate high-frequency ripple current in the SR control circuit, it is recommended to place a small value resistance of 2.2 Ω to 10 Ω between VDD and the converter output voltage.

10.1.2 VPC Pin

The trace between the resistor divider and the VPC pin should be as short as possible to reduce/eliminate possible noise coupling. The lower resistor of the resistor divider network connected to the VPC pin should be returned to GND with short traces. Avoid adding any significant external capacitance to the VPC pin so that there is no delay of signal. If filtering is necessary a recommended maximum capacitance is 10 pF with a lower resistor divider network value of 10 kΩ. Avoid high dV/dt traces close to the VPC pin and connection trace such as the SR MOSFET drain and DRV output.

10.1.3 VSC Pin

The trace between the resistor divider and the VSC pin should be as short as possible to reduce/eliminate possible noise coupling. The lower resistor of the resistor divider network connected to the VSC pin should be returned to GND with short traces. Avoid adding any external capacitance to the VPC pin so that there is no delay of signal. If filtering is necessary a recommended maximum capacitance is 47 pF with a lower resistor divider network value of 50 kΩ. Avoid high dV/dt traces close to the VSC pin and connection trace such as the SR MOSFET drain and DRV output.

10.1.4 GND Pin

The GND pin is the power and signal ground connection for the controller. The effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Place all decoupling capacitors as close as possible to the device pins with short traces. The device ground and power ground should meet at the output bulk capacitor's return. Try to ensure that high frequency/high current from the power stage does not go through the signal ground.

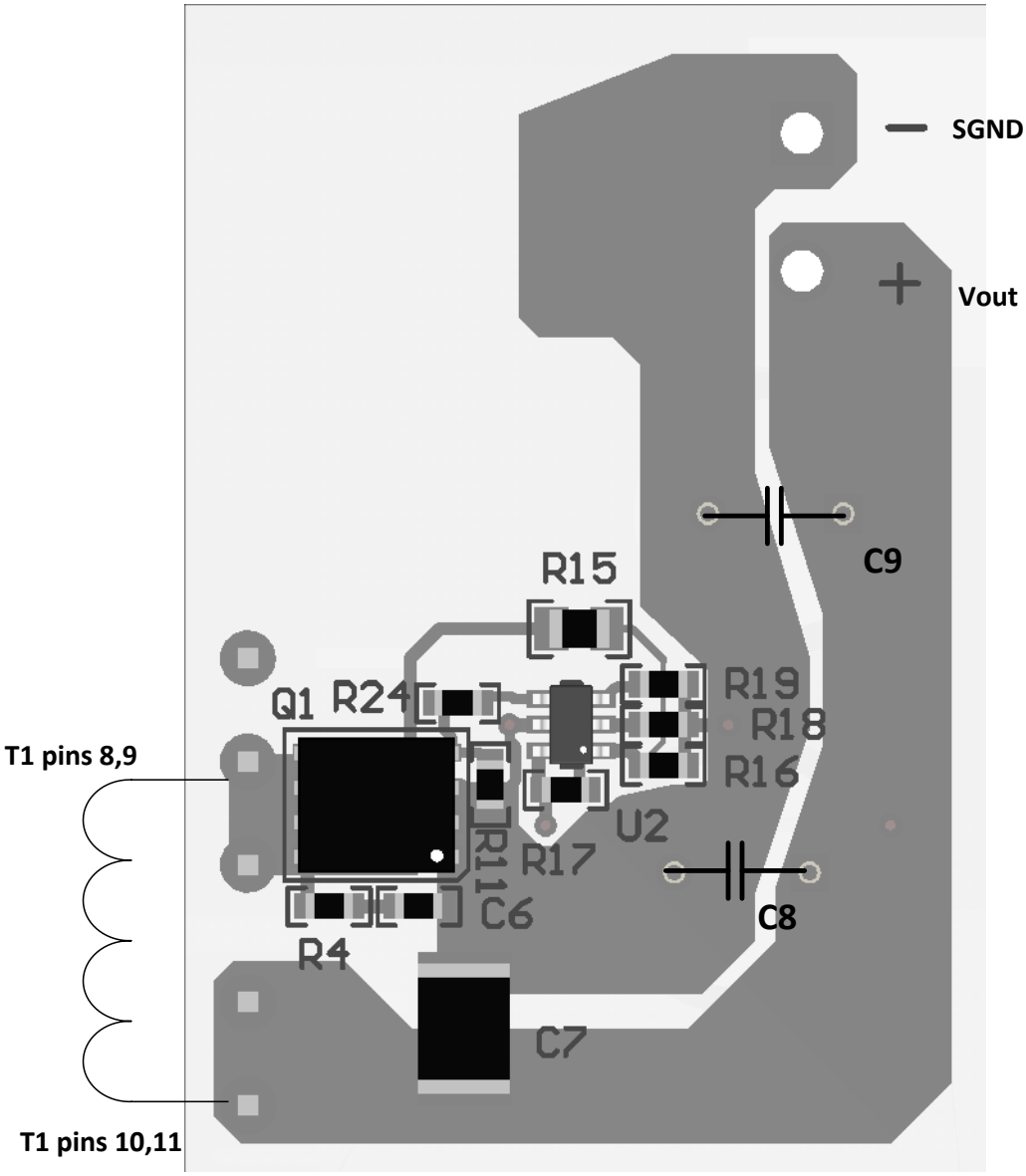
10.1.5 TBLK Pin

The programming resistor is placed on TBLK to GND, with short traces. The value may have to be adjusted based on the time delay required. Avoid high dV/dt traces close to the TBLK pin and connection trace such as the SR MOSFET drain and DRV output.

10.1.6 DRV Pin

The track connected to DRV carries high dv/dt signals. Minimize noise pickup by routing the trace to this pin as far away as possible from tracks connected to the device signal inputs, VPC, VSC, and TBLK.

10.2 Layout Example



11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 Definition of Terms

- $V_{IN(min)}$ = 60 V: converter minimum primary bulk capacitor voltage
- $V_{IN(max)}$ = 370 V: converter maximum primary bulk capacitor voltage
- $V_{OUT(min)}$ = 18 V: minimum converter output operating voltage of the UCC24630
- $V_{OUT(max)}$ = 21 V: maximum converter output operating voltage of the UCC24630
- V_{VPC_EN} = 0.45 V: synchronous rectifier enable voltage
- $V_{VPC(max)}$ = 2.0 V: maximum operating level of VPC
- N_{PS} = 5.5: transformer primary to secondary turns ratio
- $Ratio_{VPC\_VSC}$ = 4.15 : Current emulator gain K_{VPC}/K_{VSC}
- t_{VPC_BLK}: Minimum VPC pulse for synchronous rectifier operation

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC24630DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U630	Samples
UCC24630DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U630	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

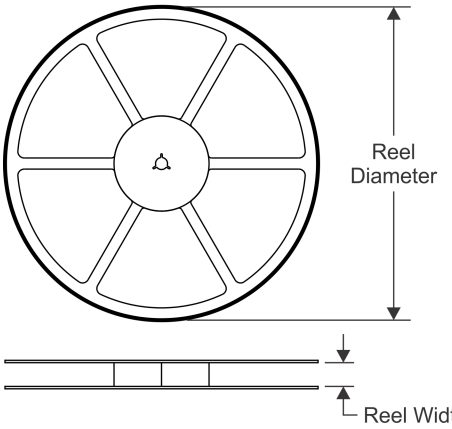
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

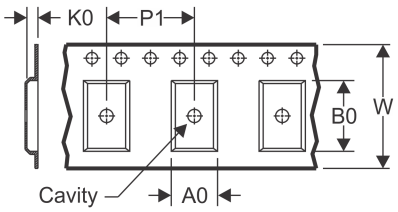
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

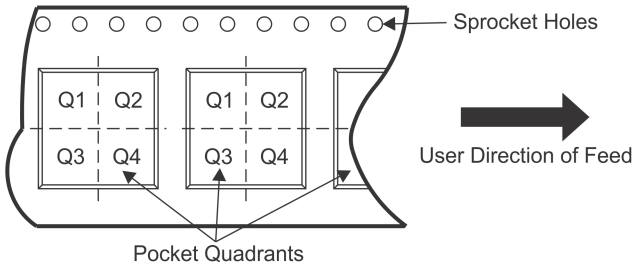


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

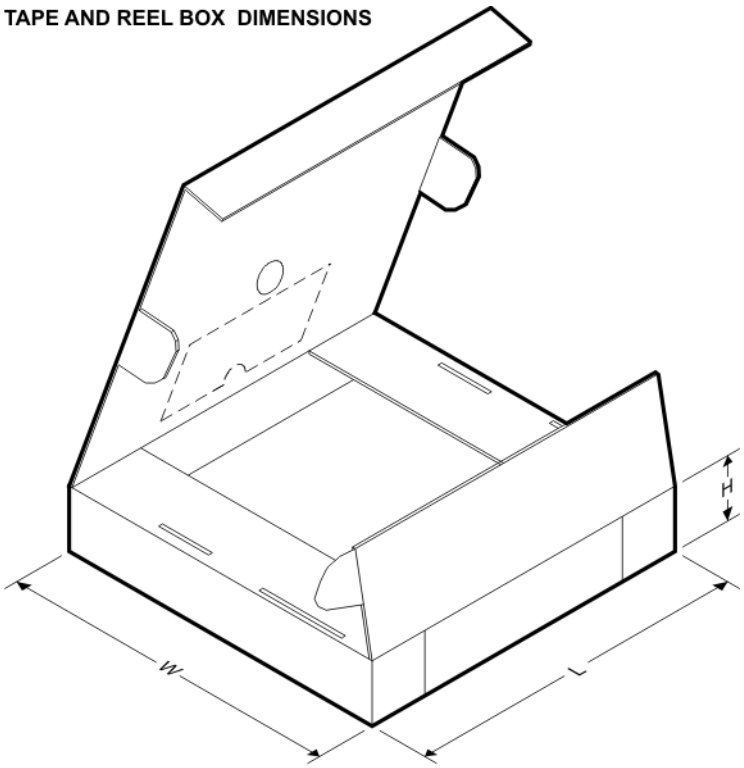
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC24630DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC24630DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

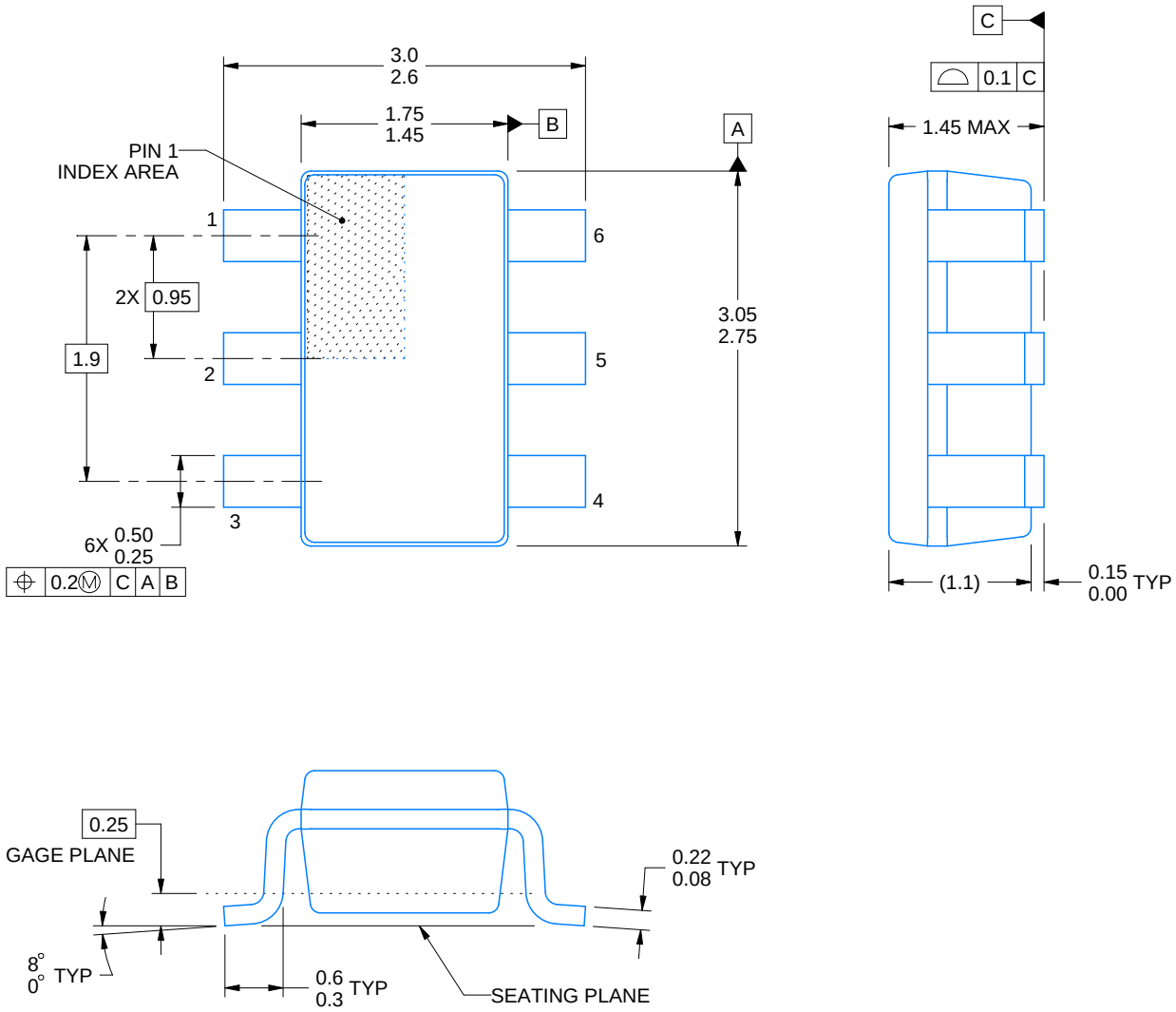
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC24630DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC24630DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

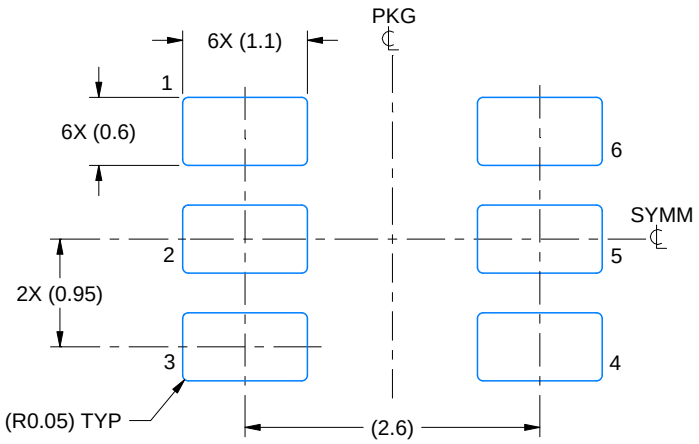
SMALL OUTLINE TRANSISTOR



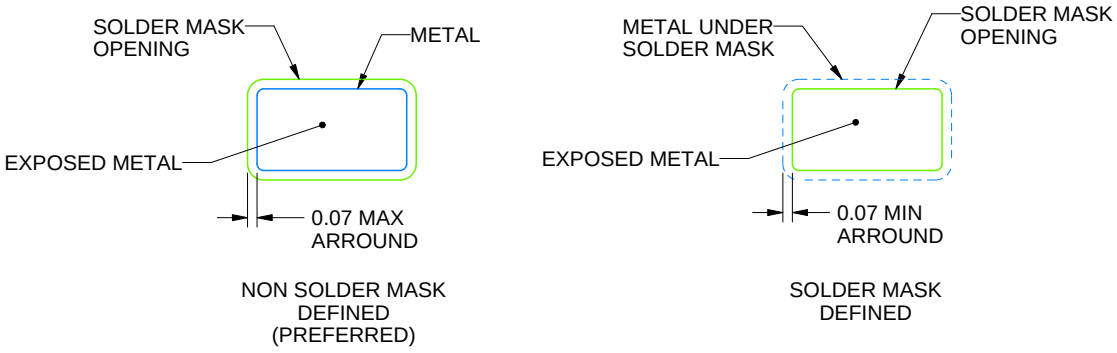
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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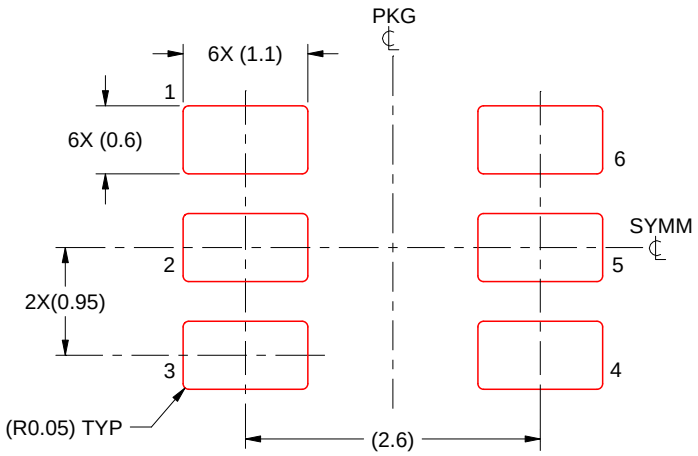
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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